**Technical
Information**

MOTOROLA *G24 JAVA HMI*

DISPLAY INTEGRATION GUIDE

MOTOROLA

REVISION HISTORY

Revision	Date	Purpose
A	March 15, 2008	Initial release

G24 KJAVA HMI
Display Integration Guide

CONTENTS

CHAPTER 4 - SOFTWARE SPECIFICATIONS

CHAPTER 1 - INTRODUCTION

1.1   PURPOSE

This guide provides Hardware and Software details required for the G24-J HMI display integration.

The descriptions given in this guide are based on a Reference Display Board.

To obtain a Reference Display Board, please contact M2M Customer Care: M2MCare@motorola.com

The main objectives of this guide are:

• General understanding of operating the reference design board
• Give tools for designing a customer's board with a G24-J HMI
• Knowledge of the Java interface for the FPGA & display configuration.

1.2   INTENDED AUDIENCE

This guide is intended for Motorola Wireless Modules customers designing a device that requires Display and/or keypad capability.

1.3   DISCLAIMER

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1.4   ABBREVIATIONS, ACRONYMS AND DEFINITIONS

Abbreviation	Full Name
EVB	**EV**aluation **B**oard
Flex	G24 configuration file, allows product **flex**ibility
G24-J	**G**24 **J**ava
GPIO	**G**eneral **P**urpose **I**nput **O**utput
HMI	**H**uman **M**achine **I**nterface. G24 with display and keypad support
JAD	**J**ava **A**pplication **D**escriptor
JAR	**J**ava **A**rchive
Kjava	**K**ilobyte Java
KMgr pin	**K**JAVA **M**ana**ger** GPIO pin
M2M	**M**achine to **M**achine
MIDlet	An application that conforms to the MIDP standard.
MIDP	**M**obile **I**nformation **D**evice **P**rofile
NVM	**N**on **V**olatile **M**emory
OEM	**O**riginal **E**quipment **M**anufacturer
UART	**U**niversal **A**synchronous **R**eceiver/**T**ransmitter
UM	**U**ser **M**IDlet
URL	**U**niform **R**esource **L**ocator

1.5   TRADEMARKS

MOTOROLA and the Stylized M Logo are registered in the U.S. Patent and Trademark Office. All other product or service names are the property of their respective owners.

1.6   APPLICABLE DOCUMENTATION

[1] Motorola G24 KJAVA User Guide, at G24-J MOTODEV Web Page

[2] MOTO2MOTO API Javadoc, available in 'MOTO2MOTO Wireless Toolkit Powered by Sun Java(TM) Technology' and 'MOTODEV SDK for Java(TM) ME'

1.7 PROBLEM REPORTING INSTRUCTIONS

Problems or corrections to this guide should be reported to M2M Customer Care by mail: M2MCare@motorola.com

1.8 HOW THIS GUIDE IS ORGANIZED

This guide contains the following chapters:

- **Chapter 1** - Introduction
- **Chapter 2** - Overview
- **Chapter 3** - Hardware Specifications
- **Chapter 4** - Software Specifications

CHAPTER 2 - OVERVIEW

2.1   INTRODUCTION

The HMI unit is a model of G24-J that can be integrated with a display through a FPGA interface. The display and keypad will be available only for Java applications (MIDlets). The display will be controlled by standard KJava libraries.

The following paragraphs give two alternatives for display integration.

2.2   DISPLAY CONNECTED WITHOUT PROM (PLATFORM FLASH)

The configuration file (FPGA's firmware) will be loaded from the G24-J's NVM to the FPGA upon each power up (see Figure 1).
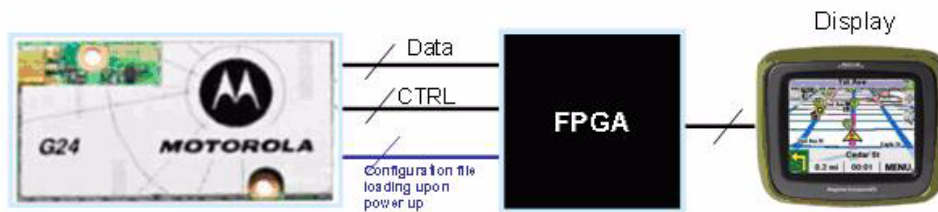

Figure 1. G24-J Loads the FPGA Configuration File

2.3   DISPLAY CONNECTED WITH PROM

The configuration file (FPGA's firmware) will be loaded from an external memory (PROM) to the FPGA upon each power up (see Figure 2).
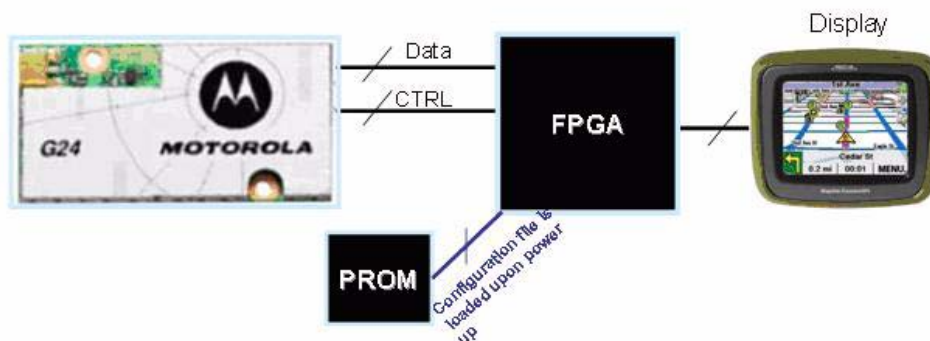

Figure 2. PROM Loads the FPGA Configuration FILE

CHAPTER 3 - HARDWARE SPECIFICATIONS

3.1   GENERAL

The Hardware specifications are detailed by a demonstration of a Reference Display Board designed at Motorola as a display integration model for the G24-J HMI customers.

3.2   G24-J DISPLAY BOARD LAYOUT

Figure 3 and Figure 4 below shows the reference display board layout. This layout will help you understand the reference display board, as well as help you design your application over the G24-J HMI.
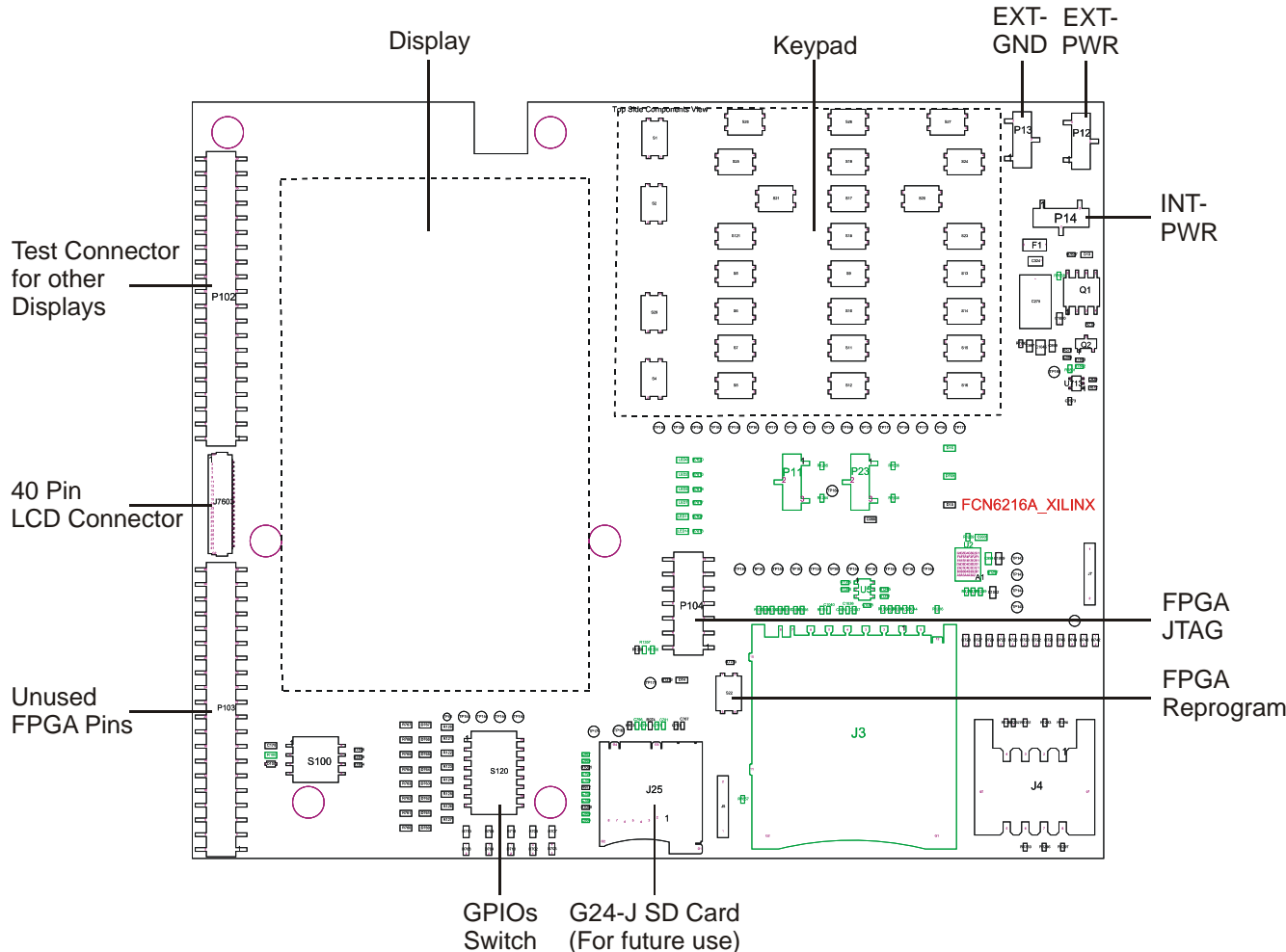

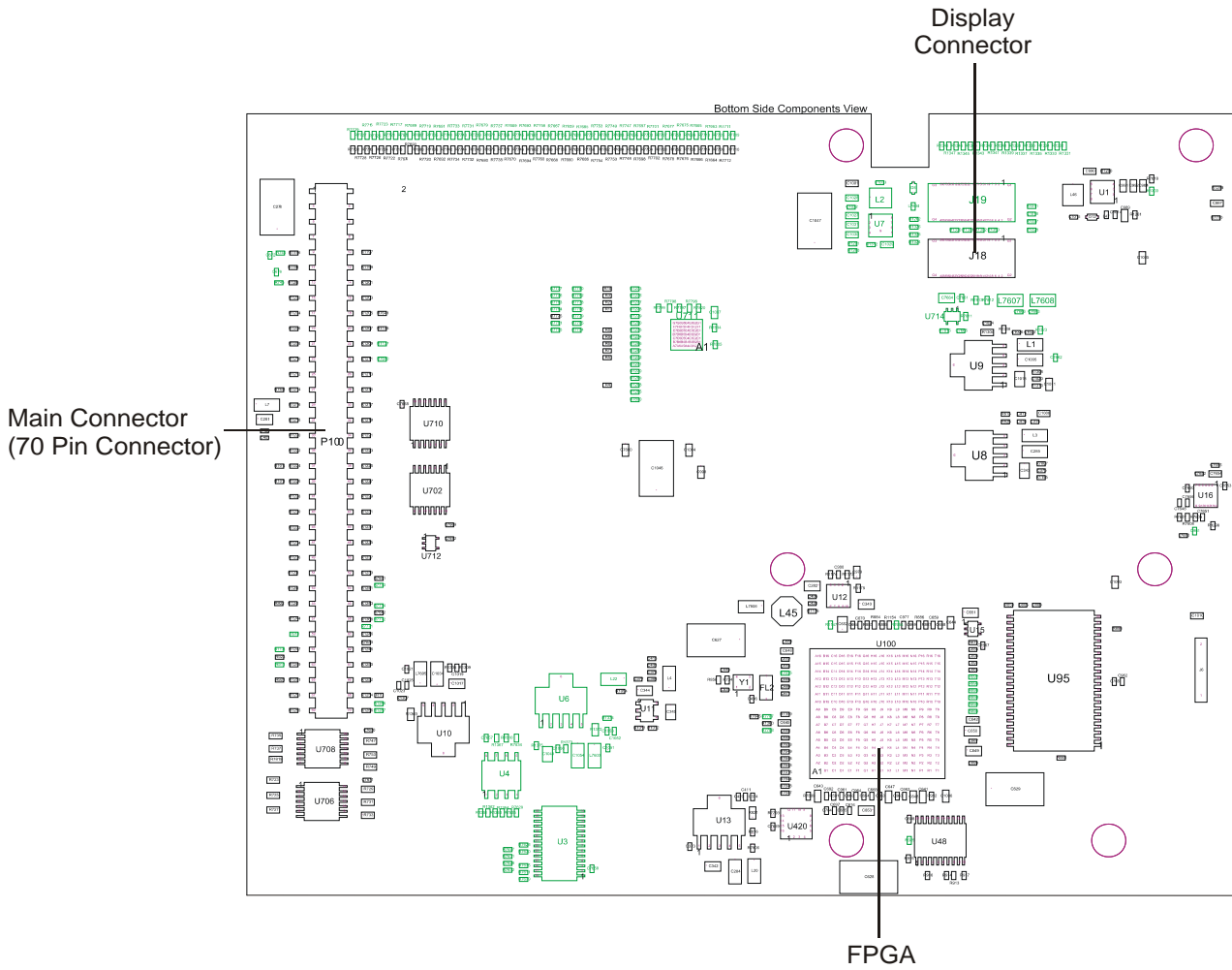Figure 3. G24-J Display Board Layout - Top View

Figure 4. G24-J Display Board Layout - Bottom View

3.3   G24-J DISPLAY BOARD WITH G24-J HMI LAYOUT

Figure 5 shows the location of the main components on the Display Board, with a G24-J HMI installed.
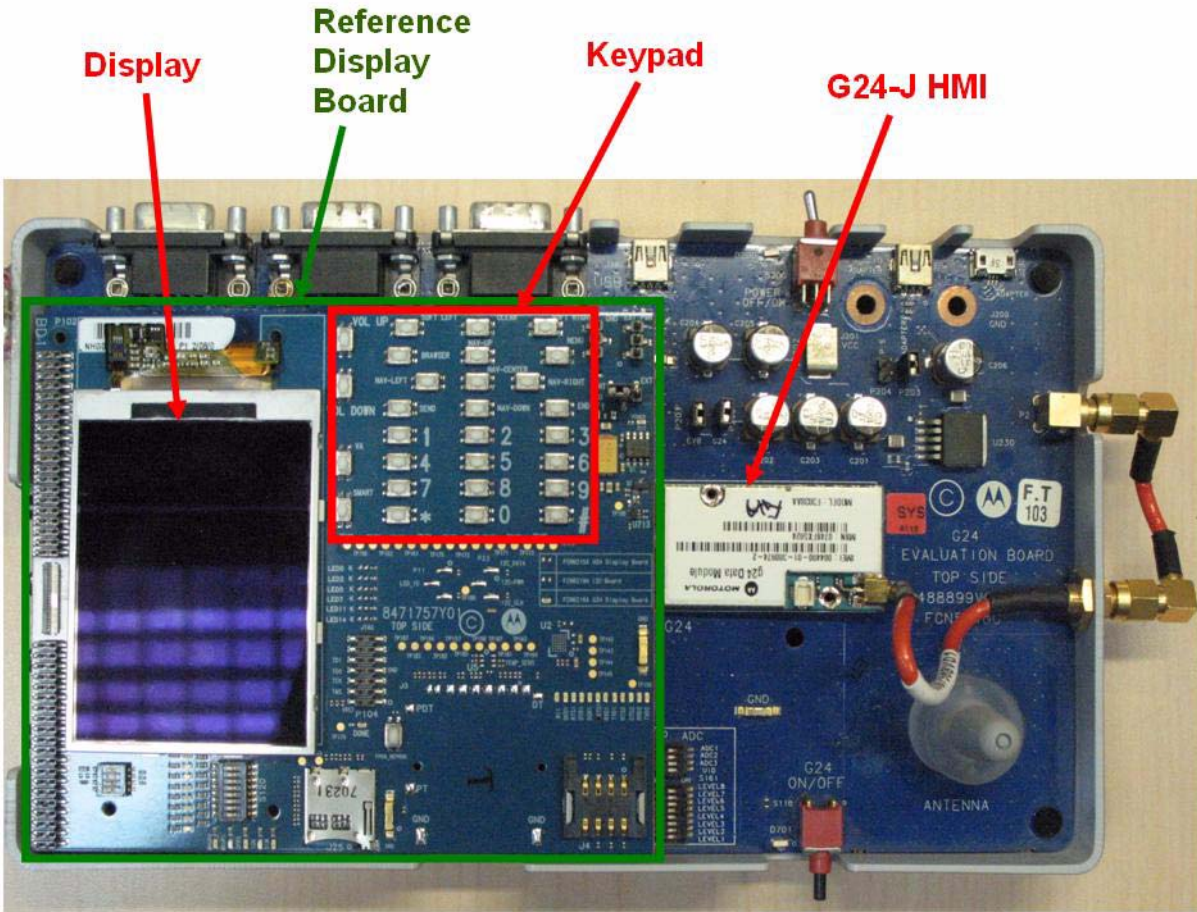

Figure 5. G24-J Display Board with G24-J HMI - Layout

Note
- The Display Board receive its power via the main connector.
- The display can only work with a G24-J HMI module connected.
- The Display Board is plugged onto the 70 pin connector (P100) on the EVB.

3.4   BOARD CONFIGURATION

In order to operate and configure the Display Board, the following guidelines should be considered:

3.4.1   Power

The Display Board receives power in one of two ways:

1. INT_PWR (Normal operation).

    • Place a jumper between left and middle pins of **P14**.

2. EXT_PWR.
    To use this option:

    • Place a jumper between right and middle pins of **P14**.
    • Connect **P12** to VCC.
    • Connect **P13** to GND.

Note

• Operation voltage is 4V to 4.8V.
• Make sure that all dip switches on the Display Board are set to H/OFF (left side).

3.4.2   FPGA Programming

The FPGA does not have a NVM for holding the configuration file when its power is off. So it must be programmed upon every power up. The FPGA may be programmed using the following two ways:

• Via UM (G24-J User MIDlet) - set **S100 switch 3** to "OFF"
• Via on-board PROM - set **S100 switch 3** to "ON"

3.4.2.1   FPGA Programming Via UM

The configuration file is saved in the G24-J's NVM. The G24-J programs the FPGA upon power up.

Connecting the GPIOs for FPGA Programming

Four of the G24-J GPIOs are used for programming the FPGA (see Table 1). Once programming is done, three of the GPIOs below may be re-routed by the FPGA. Once re-routed, these lines will be available for the GPIO API, see column "Available for GPIO API" in Table 1.

FPGA also outputs a line "DONE" to indicate a successful programming of the configuration file. This line is not processed by the G24-J. The user may connect this FPGA line.

Table 1: Pins Required for FPGA Programming

70 Pin Conn. Pin No.	Original Usage	FPGA Programming Usage		Pin Direction	Available for GPIO API
		Name	**Description**		
26	GPIO11	**FPGA_PROG_B**	Reset FPGA and start configuration.	Out	No
23	GPIO12	**FPGA_INIT_B**	A problem occurred, start image loading from the beginning.	In	Yes

Table 1: Pins Required for FPGA Programming *(Continued)*

70 Pin Conn. Pin No.	Original Usage	FPGA Programming Usage		Pin Direction	Available for GPIO API
		Name	**Description**		
13	GPIO13	**FPGA_CCLK**	Clock.	Out	Yes
19	GPIO14	**PROM_D0**	Configuration data.	Out	Yes

> **Note**
>
> For more details regarding programming the FPGA through the G24-J UM, refer to CHAPTER 4 - SOFTWARE SPECIFICATIONS.

3.4.2.2   FPGA Programming Via On-Board PROM

Using this configuration, the PROM holds the configuration file, and programs the FPGA upon power up. Below, there's a description of how to use Xilinx iMPACT application in order to program the PROM through the JTAG on the display's Reference Board.

> **Note**
>
> In order to reprogram the FPGA from the PROM when the G24-J is already powered up - press and release **S22**. Of course, this function is only valid for on board PROM configuration.

PROM Programming Procedure

The FPGA and the PROM are both connected to a JTAG chain (see Figure 6):
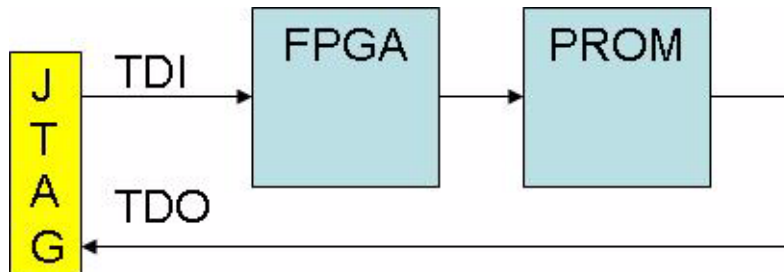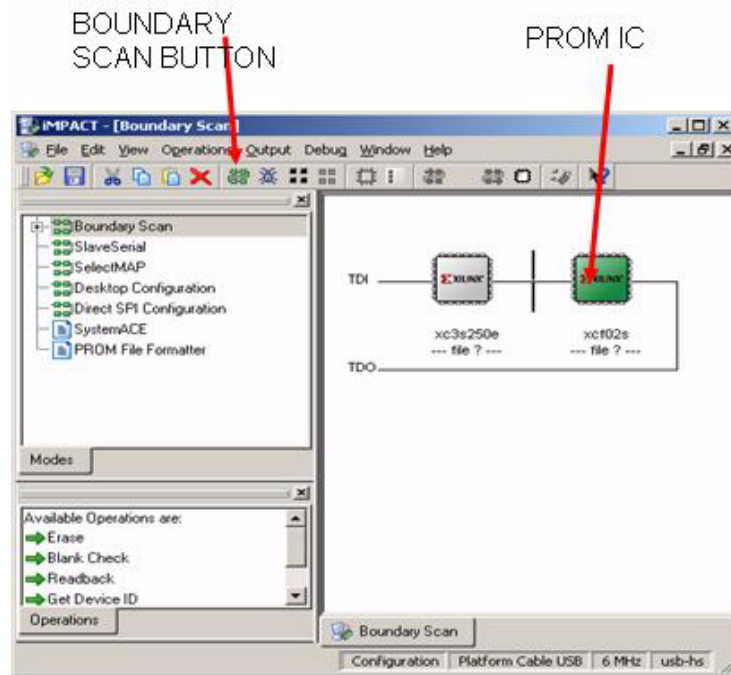

Figure 6. JTAG Chain

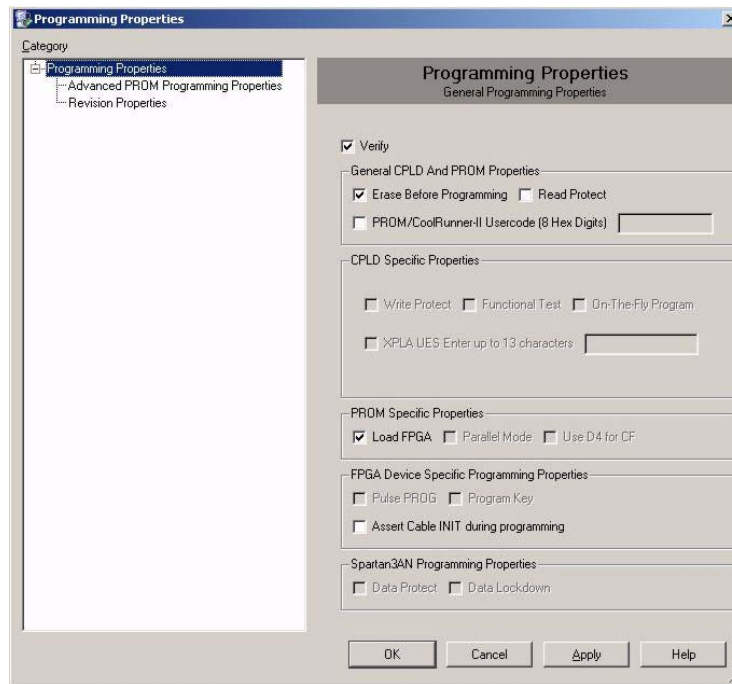Use the Xilinx iMPACT tool and follow these steps (with the help of the screens):

1. Connect to the JTAG chain using the 'Boundary Scan' button.
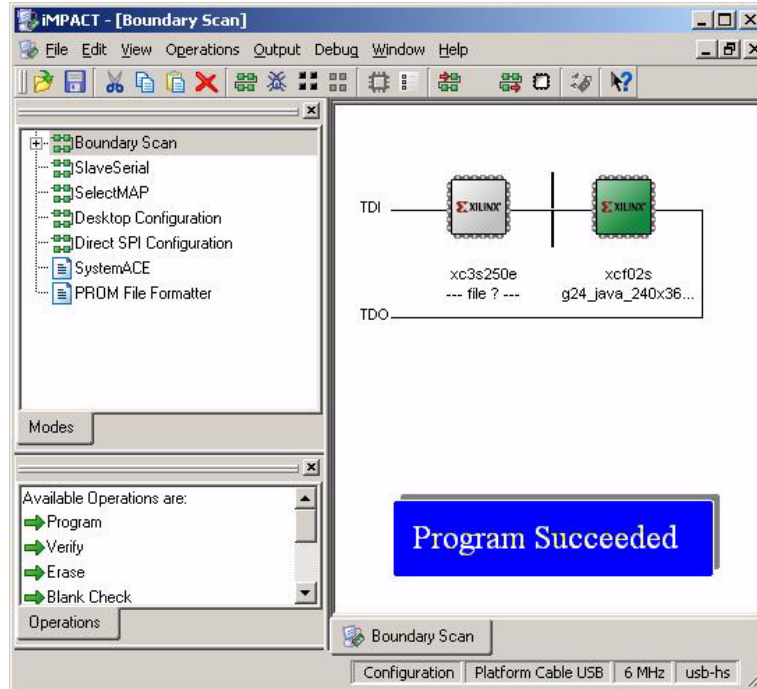
2. Double click the PROM IC.

3. Select file you want to program.
4. Right click on the PROM IC.

5. Select Load FPGA and press OK.

6. Verify that the Program Succeeded message appears and Done LED is ON.

3.5   CONNECTORS

3.5.1   P103

Xilinx unused (spare) GPIOs: most FPGA IOs that are not in used are routed to this connector; these IOs can be used by the customer for their application and needs.

GPIO Pin Number on FPGA	Pin Number on P103	Pin Number on P103	GPIO Pin Number on FPGA
E6	1	2	GND
K13	3	4	N16
E9	5	6	G2
D5	7	8	B1
B16	9	10	C1
M16	11	12	D1
H16	13	14	D16
D11	15	16	D10
H15	17	18	E10
A3	19	20	A10
B10	21	22	D9
C12	23	24	A7

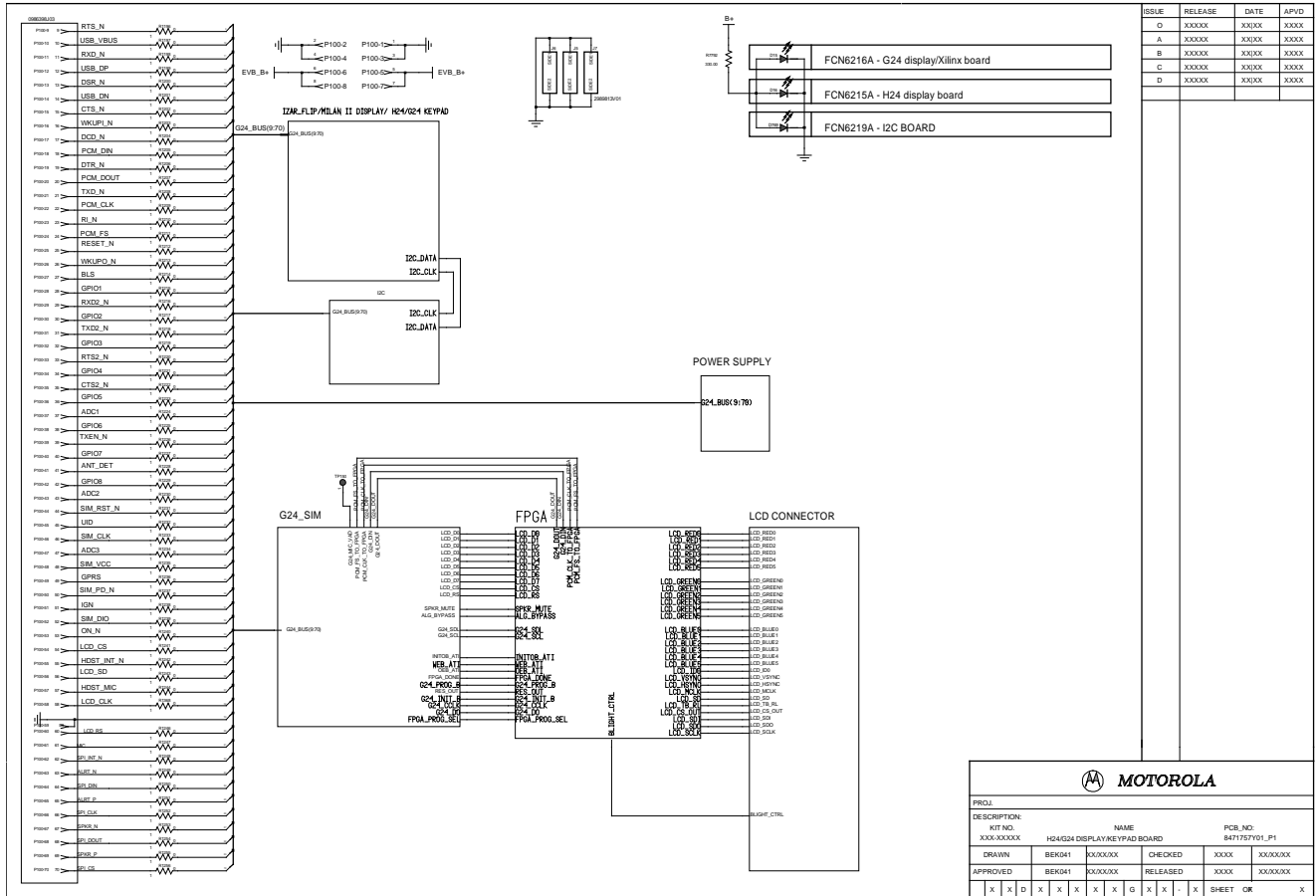| GPIO Pin Number on FPGA	Pin Number on P103	Pin Number on P103	GPIO Pin Number on FPGA
J14	25	26	P16
F14	27	28	E11
J11	29	30	C13
M13	31	32	R15
C11	33	34	R16
L15	35	36	J12
J16	37	38	3V
GND	39	40	2.5V

3.5.2 P102

Test connector for other Displays connection.

Description	Pin Number on P102	Pin Number on P102	Description
LCD_ID0	1	2	LCD_SDO
LCD_RED5	3	4	LCD_SDI
LCD_RED4	5	6	GND
LCD_RED3	7	8	LCD_VSYNC
LCD_RED2	9	10	GND
LCD_RED1	11	12	LCD_HSYNC
LCD_RED0	13	14	GND
LCD_GREEN5	15	16	LCD_MCLK
LCD_GREEN4	17	18	GND
LCD_GREEN3	19	20	LCD_SD
LCD_GREEN2	21	22	LCD_TB_RL
LCD_GREEN1	23	24	LCD_CS_OUT
LCD_GREEN0	25	26	2_775V
LCD_BLUE0	27	28	2_775V
LCD_BLUE1	29	30	LCD_SCLK
LCD_BLUE2	31	32	LED_ANODA
LCD_BLUE3	33	34	LED_PWM
LCD_BLUE4	35	36	B+
LCD_BLUE5	37	38	LED_CATODA
GND	39	40	GND

3.6   SCHEMATICS

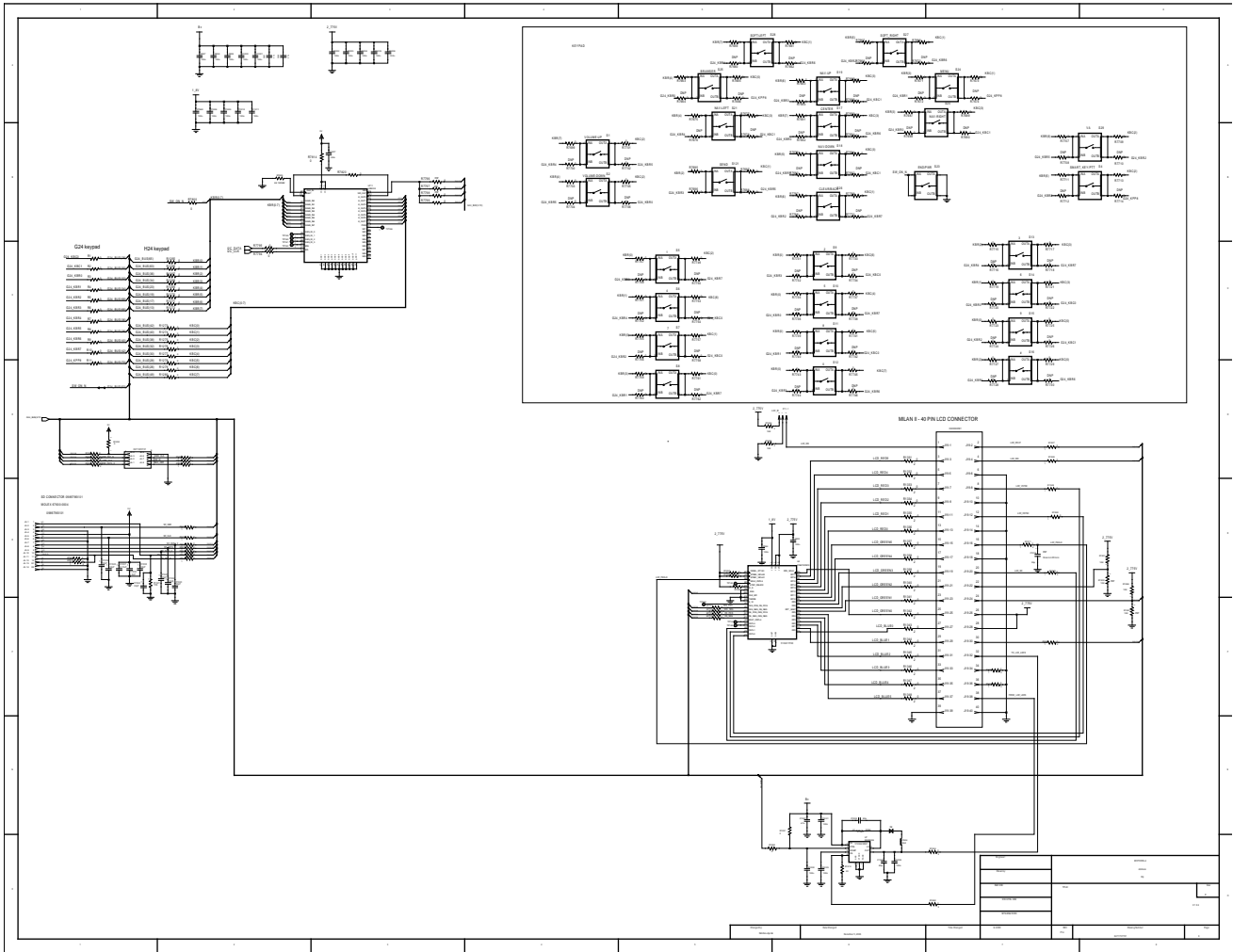The following are the Display Board schematic diagrams.

G24 interface

WEB_ATI
OEB_ATI
RES_OUT
G24_SCL
G24_SDL
G24_CCLK
G24_DO
G24_PROG_B
LCD_D0
LCD_D1
LCD_D2
LCD_D3
LCD_D4
LCD_D5
LCD_D6
LCD_D7
LCD_RS
LCD_CS

FPGA_DONE
SPKR_MUTE
G24_INIT_B
INITOB_ATI
FPGA_PROG_SEL

G24_DOUT
G24_DIN
BLIGHT_CTRL

LCD interface

LCD_RED0	LCD_TB_RL
LCD_RED1	LCD_BLUE3
LCD_RED2	LCD_BLUE4
LCD_RED3	LCD_BLUE5
LCD_RED4	LCD_VSYNC
LCD_RED5	LCD_HSYNC
LCD_GREEN0	LCD_MCLK
LCD_GREEN1	LCD_SD
LCD_GREEN2	LCD_CS_OUT
LCD_GREEN3	LCD_SDI
LCD_GREEN4	LCD_SDO
LCD_GREEN5	LCD_SCLK
LCD_BLUE0	LCD_ID0
LCD_BLUE1	
LCD_BLUE2	

2Mbit PROM

PRON_CCLK
PROM_INIT_B
FPGR_DONE
FPGA_TMS
FPGA_TCK
FPGA_TDO

U420
FPGA_PROM_SEL
G24_PROG_B
G24_DO
G24_CCLK
G24_INIT_B
PROM_PROG_B
PROM_DO
PRON_CCLK
PROM_INIT_B

FPGA_PROG_B
FPGA_DO
FPGA_CCLK
FPGA_INIT_B

FPGA_REPROGRAM
S22
INA OUTA
INB OUTB

PCM_INTERFACE

PCM_CLK_TO_FPGA
PCM_FS_TO_FPGA

XILINX UNUSED PINS

FM_DOUT
BT_DIN
FM_DIN
BT_DOUT
B+_CUTOFF
AUX_ALRT_OEM
LBS
FM_FPGA_RESET
FM_EXT_RESET
EXT_MIC_DET
EXT_SPKR_PB
CTRL_5_12V_SW
ROTARY_B
ROTARY_A
PCM_CLK
PCM_FS
FM_PCM_SEL

BLUE_EN
PH_DET
PS_EN0
PS_EN1
PS_EN2
PS_EN3
IN_CALL_IND
MUTE_SPK1
MUTE_SPK2
FM_15
FM_17
FM_26
MP3_SEL
SPK_DET_EN
ALG_BYPASS
ROW0
ROW4
COL1

4Mbit SRAM

SR_CE
SR_OE
ADD[0:18]
ADD(0)
ADD(1)
ADD(2)
ADD(3)
ADD(4)
ADD(5)
ADD(6)
ADD(7)
ADD(8)
ADD(9)
ADD(10)
ADD(11)
ADD(12)
ADD(13)
ADD(14)
ADD(15)
ADD(16)
ADD(17)
ADD(18)

DATA[0:7]
DATA(0)
DATA(1)
DATA(2)
DATA(3)
DATA(4)
DATA(5)
DATA(6)
DATA(7)

JTAG STANDARD CONNECTOR
JTAG_VREF
FPGA_TMS
FPGA_TCK
PROM_TDO
FPGA_TDI

FPGA INTERFACE
FPGA chip on page #2

1. DRAWING GENERATED BY COMPUTER.

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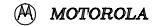
PROJ.
DESCRIPTION:
KIT NO.   NAME   PCB_NO:
                 FPGA   8471757Y01

| DRAWN | XXX | 5/06/07 | | XXXX | XX/XXXX |
| APPROVED | XXX | 5/06/07 | | XXXX | XXXXXXX |

SHEET OF   12

MINI SDcard

FPGA
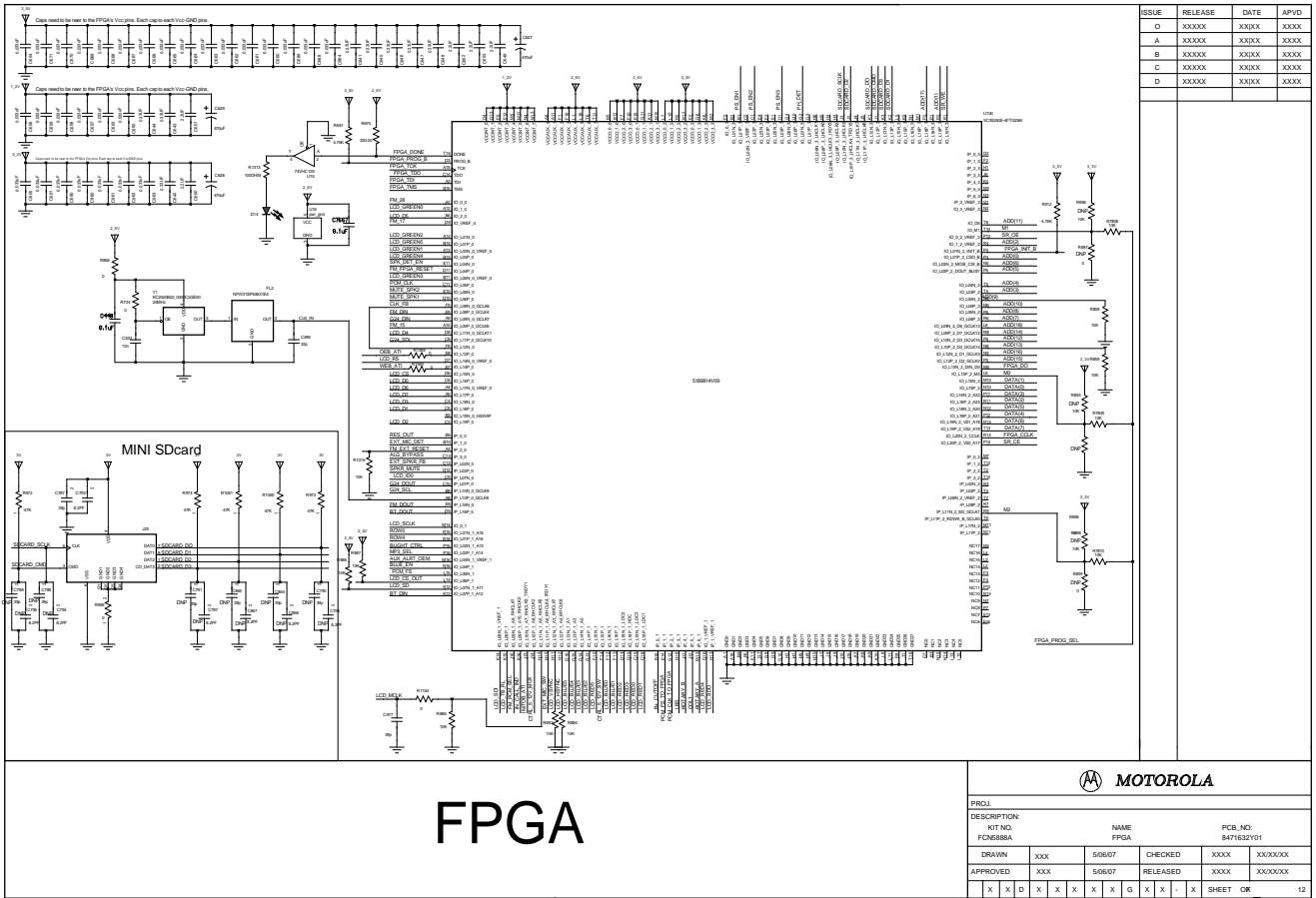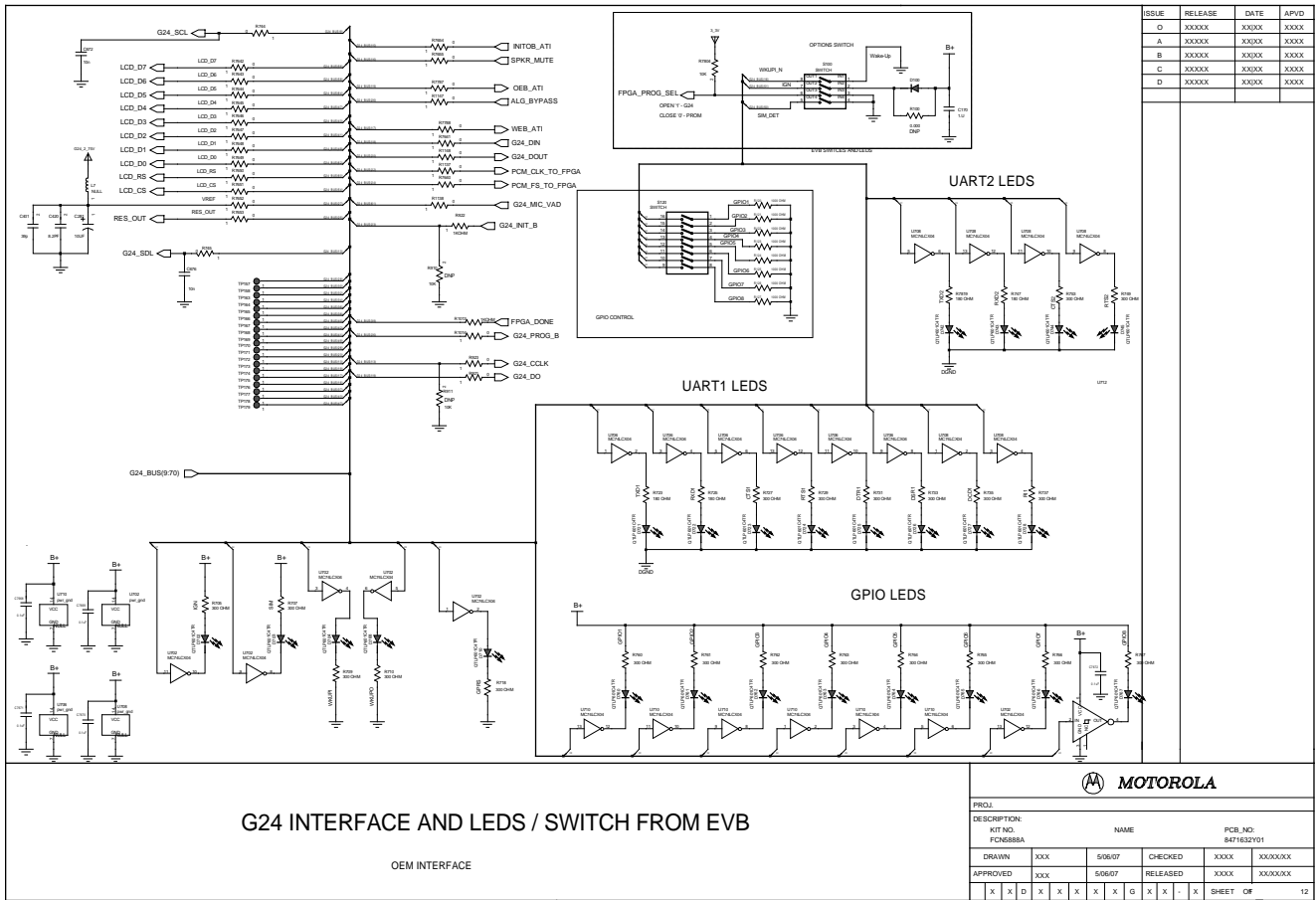
G24 INTERFACE AND LEDS / SWITCH FROM EVB

OEM INTERFACE

40 PIN LCD CONNECTOR AND 40 PIN TEST CONNECTOR

J7203:FOR QVGA, TM.2.0   P/N 72R7150xF01
J18:FOR 480X640 VGA2.8   P/N 7271163C01
P102 IS A 40 PIN CONNECTOR FOR REWORK ANY DISPLAY

LCDS CONNECTORS

Ⓜ MOTOROLA
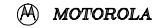
PROJ.	H24/G24 DISPLAY BOARD			
DESCRIPTION:				
KIT NO.		NAME		PCB_NO: 8471757Y01
DRAWN	XXX	5/06/07	CHECKED	XXXX	XX/XX/XX
APPROVED	XXX	5/06/07	RELEASED	XXXX	XX/XX/XX
X X D X X X X G X X - X			SHEET OF		12

POWER SUPPLY

3.7   GPIO AVAILABILITY IN G24-J HMI

Four GPIOs are available for the GPIO API (package com.motorola.oem.hapi):

- GPIO **15**
- GPIO **12**, GPIO **13**, GPIO **14** - Available after FPGA programming is done (see "Connecting the GPIOs for FPGA Program-ming")

For further details about GPIO API, refer to [1].

4.1   GENERAL

The display & keypad operations are managed by standard Java ME GUI libraries (javax.microedition.lcdui). Motorola proprietary Java interface is provided for FPGA & display configuration.

Note   For detailed package usage information refer to Javadoc (com.motorola.oem.osc package). See reference [2].

4.2   MOTOROLA PROPRIETARY JAVA INTERFACE FOR FPGA & DISPLAY CONFIGURATION

The DisplayConfig class configures and controls the main display FPGA settings. It is part of package com.motorola.oem.osc. It allows the following operations:

- FPGA programming (Available when **S100 switch 3** is set to "OFF", see "FPGA Programming" on page 10)
- G24-J Output Resolution
- FPGA & Display's manufacturer's commands

4.2.1   FPGA Programming Via UM

The configuration file is a resource in the UM jar file.

DisplayConfig.loadFpgaConfigFile loads the configuration file to the G24-J NVM. Then it is automatically loaded to the FPGA, upon each power up.

4.2.2   Resolution

DisplayConfig.setDeviceOutputResolution sets the G24-J output resolution.

Available resolutions are:

- 320x240 (Recommended)
- 220x176
- 160x128

All resolutions are available in portrait and landscape.

Default resolution of the G24-J: 320x240.

Note   The resolution selection should be coordinated with the FPGA supplier.

4.2.3   FPGA & Display Manufacturer Commands

DisplayConfig.sendFpgaCommand allows sending control commands to the FPGA or display.

Note — The available commands are manufacturer dependent and will be detailed by the FPGA and/or display manufacturer.

Possible commands are:

- Set rescaler algorithm:
    - Pixel duplication.
    - Linear interpolation.
    - Cubic interpolation.
    - Boosted cubic interpolation.
- Enable/Disable rotation (180 degrees)
- Power on/off

Example:

import com.motorola.oem.osc.DisplayConfig;

...

// Set rescaler algorithm to 'Boosted cubic interpolation'

DisplayConfig.sendFpgaCommand((byte)0x44);

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