74HC138; 74HCT138

3-to-8 line decoder/demultiplexer; inverting
Rev. 03 — 23 December 2005 Proc

Product data sheet

1. **General description**

The 74HC138; 74HCT138 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL).

The 74HC138; 74HCT138 decoder accepts three binary weighted address inputs (A0, A1 and A3) and when enabled, provides 8 mutually exclusive active LOW outputs ($\overline{Y}0$ to $\overline{Y}7$).

The 74HC138; 74HCT138 features three enable inputs: two active LOW (E1 and E2) and one active HIGH (E3). Every output will be HIGH unless E1 and E2 are LOW and E3 is HIGH.

This multiple enable function allows easy parallel expansion of the 74HC138; 74HCT138 to a 1-of-32 (5 lines to 32 lines) decoder with just four 74HC138; 74HCT138 ICs and one inverter.

The 74HC138; 74HCT138 can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Not used enable inputs must be permanently tied to their appropriate active HIGH- or LOW-state.

The 74HC138; 74HCT138 is identical to the 74HC238; 74HCT238 but has inverting outputs.

2. **Features**

- Demultiplexing capability
- Multiple input enable for easy expansion
- Complies with JEDEC standard no. 7A
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- ESD protection:
 - ◆ HBM EIA/JESD22-A114-C exceeds 2000 V
 - MM EIA/JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C



Quick reference data

Table 1: Quick reference data $GND = 0 \ V; \ T_{amb} = 25 \ ^{\circ}C; \ t_r = t_f = 6 \ ns.$

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
74HC138	3					
t _{PHL} ,	propagation delay	$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$				
t _{PLH}	An to \overline{Y} n		-	12	-	ns
	E3 to \overline{Y} n		-	14	-	ns
	Ēn to ₹n		-	14	-	ns
C _i	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance	$V_I = GND$ to V_{CC}	[1] -	67	-	pF
74HCT13	38					
t _{PHL} ,	propagation delay	$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$				
t _{PLH}	An to \overline{Y} n		-	17	-	ns
	E3 to \overline{Y} n		-	19	-	ns
	Ēn to ₹n		-	19	-	ns
C _i	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance	$V_I = GND$ to $(V_{CC} - 1.5 V)$	[1] -	67	-	pF

^[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

Ordering information

Table 2: **Ordering information**

Product data sheet

Type number	Package			
	Temperature range	Name	Description	Version
74HC138	·			
74HC138N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
74HC138D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC138DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC138PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC138BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body $2.5\times3.5\times0.85$ mm	SOT763-1
74HC_HCT138_3			© Koninklijke Philips Electronics N.V	. 2005. All rights reserved.

Rev. 03 — 23 December 2005

2 of 23

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$

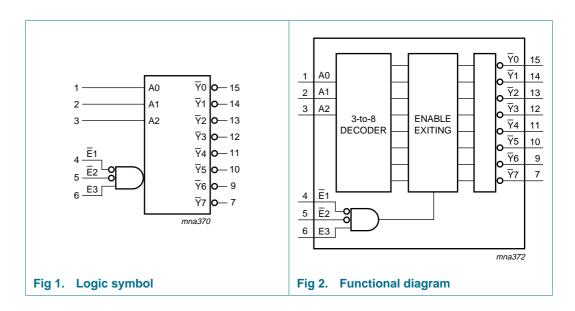
 f_i = input frequency in MHz;

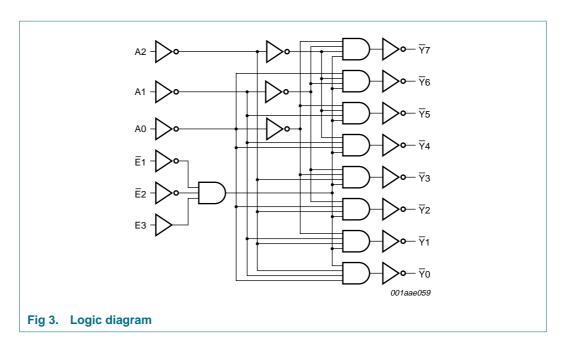


Ordering information ...continued Table 2:

Type number	Package			
	Temperature range	Name	Description	Version
74HCT138				
74HCT138N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
74 HCT138D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT138DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT138PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT138BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body $2.5\times3.5\times0.85$ mm	SOT763-1

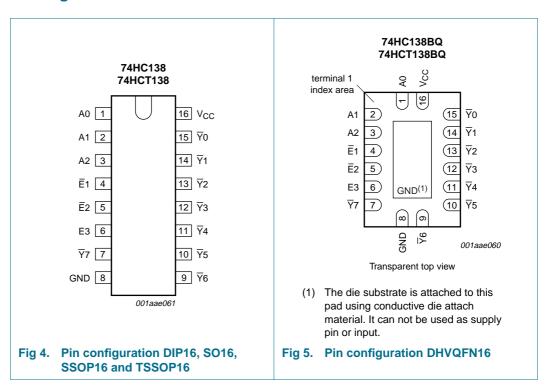
5. Functional diagram





6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3: Pin description

Table 5.	i ili description	
Symbol	Pin	Description
A0	1	address input 0
A1	2	address input 1
A2	3	address input 2
E1	4	enable input 1 (active LOW)
E2	5	enable input 2 (active LOW)
E3	6	enable input 3 (active HIGH)
Y 7	7	output 7 (active LOW)
GND	8	ground (0 V)
Y 6	9	output 6 (active LOW)
Y 5	10	output 5 (active LOW)
\overline{Y} 4	11	output 4 (active LOW)
 Y 3	12	output 3 (active LOW)
<u>¥</u> 2	13	output 2 (active LOW)
<u>\overline{Y}</u> 1	14	output 1 (active LOW)
 Y 0	15	output 0 (active LOW)
V_{CC}	16	positive supply voltage

7. Functional description

Table 4: Function table [1]

Idolo			tubio_										
Cont	rol		Input	t		Out	put						
Ē1	E2	E3	A2	A1	A0	Y 7	∀ 6	Y 5	Y 4	Y 3	₹2	<u>¥</u> 1	₹0
Н	Χ	Χ	X	Χ	Χ	Н	Н	Н	Н	Н	Н	Н	Н
Χ	Н	Х											
Χ	Χ	L											
L	L	Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	L
			L	L	Н	Н	Н	Н	Н	Н	Н	L	Н
			L	Н	L	Н	Н	Н	Н	Н	L	Н	Н
			L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н
			Н	L	L	Н	Н	Н	L	Н	Н	Н	Н
			Н	L	Н	Н	Н	L	Н	Н	Н	Н	Н
			Н	Н	L	Н	L	Н	Н	Н	Н	Н	Н
			Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н

^[1] H = HIGH voltage level;

L = LOW voltage level;

X = don't care.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7	V
I _{IK}	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$		-	±20	mA
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or} $ $V_O > V_{CC} + 0.5 \text{ V} $		-	±20	mA
Io	output current	$V_{O} = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$		-	±25	mΑ
I _{CC}	quiescent supply current			-	50	mΑ
I_{GND}	ground current			-	-50	mΑ
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation					
	DIP16 package		<u>[1]</u>	-	750	mW
	SO16 package		[2]	-	500	mW
	SSOP16 package		[3]	-	500	mW
	TSSOP16 package		[3]	-	500	mW
	DHVQFN16 package		<u>[4]</u>	-	500	mW

^[1] For DIP16 package: Ptot derates linearly with 12 mW/K above 70 °C.

9. Recommended operating conditions

Table 6: Recommended operating conditions

supply voltage					
,					
		2.0	5.0	6.0	V
input voltage		0	-	V_{CC}	V
output voltage		0	-	V_{CC}	V
ambient temperature		-40	+25	+125	°C
input rise and fall time	$V_{CC} = 2.0 \text{ V}$	-	-	1000	ns
	V _{CC} = 4.5 V	-	6.0	500	ns
	V _{CC} = 6.0 V	-	-	400	ns
supply voltage		4.5	5.0	5.5	V
input voltage		0	-	V_{CC}	V
output voltage		0	-	V_{CC}	V
ambient temperature		-40	+25	+125	°C
input rise and fall time	$V_{CC} = 4.5 \text{ V}$	-	6.0	500	ns
· i	output voltage ambient temperature input rise and fall time supply voltage input voltage output voltage ambient temperature	output voltage ambient temperature input rise and fall time $ \frac{V_{CC} = 2.0 \text{ V}}{V_{CC} = 4.5 \text{ V}} $ $ \frac{V_{CC} = 6.0 \text{ V}}{V_{CC} = 6.0 \text{ V}} $ supply voltage input voltage output voltage ambient temperature	coutput voltage 0 ambient temperature -40 input rise and fall time $V_{CC} = 2.0 \text{ V}$ - $V_{CC} = 4.5 \text{ V}$ - $V_{CC} = 6.0 \text{ V}$ - supply voltage 4.5 input voltage 0 output voltage 0 ambient temperature -40	coutput voltage 0 - ambient temperature -40 +25 input rise and fall time $V_{CC} = 2.0 \text{ V}$ - -6.0 V $V_{CC} = 4.5 \text{ V}$ - -6.0 V supply voltage 0 -	coutput voltage 0 - V_{CC} ambient temperature -40 +25 +125 input rise and fall time $V_{CC} = 2.0 \text{ V}$ - 0.00 V - 0.00 J

74HC_HCT138_3

^[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

^[3] For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

^[4] For DHVQFN16 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

10. Static characteristics

Table 7: Static characteristics 74HC138

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T _{amb} = 25	°C					
V _{IH}	HIGH-state input voltage	V _{CC} = 2.0 V	1.5	1.2	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	V
V _{IL}	LOW-state input voltage	V _{CC} = 2.0 V	-	0.8	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	V
V _{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_{O} = -20 \mu A; V_{CC} = 2.0 V$	1.9	2.0	-	V
		$I_{O} = -20 \mu A; V_{CC} = 4.5 V$	4.4	4.5	-	V
		$I_{O} = -20 \mu A; V_{CC} = 6.0 V$	5.9	6.0	-	V
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.98	4.32	-	V
		$I_{O} = -5.2 \text{ mA}; V_{CC} = 6 \text{ V}$	5.48	5.81	-	V
V _{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20 \mu A; V_{CC} = 2.0 \text{ V}$	-	0	0.1	V
		$I_O = 20 \mu A$; $V_{CC} = 4.5 V$	-	0	0.1	V
		$I_O = 20 \mu A$; $V_{CC} = 6.0 \text{ V}$	-	0	0.1	V
		$I_O = 4.0 \text{ mA}$; $V_{CC} = 4.5 \text{ V}$	-	0.15	0.26	V
		$I_O = 5.2 \text{ mA}; V_{CC} = 6 \text{ V}$	-	0.16	0.26	V
I _{LI}	input leakage current	$V_1 = V_{CC}$ or GND; $V_{CC} = 6 \text{ V}$	-	-	±0.1	μΑ
l _{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$			±0.5	μΑ
I _{CC}	quiescent supply current	$V_{CC} = 6.0 \text{ V}; I_O = 0 \text{ A};$ $V_1 = V_{CC} \text{ or GND}$	-	-	8.0	μΑ
Ci	input capacitance		-	3.5	-	pF
T _{amb} = -4	0 °C to +85 °C					
V _{IH}	HIGH-state input voltage	V _{CC} = 2.0 V	1.5	-	-	V
		V _{CC} = 4.5 V	3.15	-	-	V
		V _{CC} = 6.0 V	4.2	-	-	V
V _{IL}	LOW-state input voltage	V _{CC} = 2.0 V	-	-	0.5	V
		V _{CC} = 4.5 V	-	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.8	V
V _{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}				
	•	$I_O = -20 \mu A$; $V_{CC} = 2.0 \text{ V}$	1.9	-	-	V
		$I_O = -20 \mu A$; $V_{CC} = 4.5 V$	4.4	-	-	V
		$I_O = -20 \mu\text{A}; V_{CC} = 6.0 \text{V}$	5.9	-	-	V
		$I_O = -4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.84	-	-	V
		$I_{O} = -5.2 \text{ mA}; V_{CC} = 6 \text{ V}$	5.34	_	-	V

74HC_HCT138_3



At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20 \mu A; V_{CC} = 2.0 V$	-	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 4.5 V$	-	-	0.1	V
		$I_{O} = 20 \mu A; V_{CC} = 6.0 V$	-	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.33	V
		$I_O = 5.2 \text{ mA}; V_{CC} = 6 \text{ V}$	-	-	0.33	V
I _{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6 \text{ V}$	-	-	±1.0	μΑ
I _{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$			±5.0	μΑ
Icc	quiescent supply current	$V_{CC} = 6.0 \text{ V}; I_O = 0 \text{ A};$ $V_I = V_{CC} \text{ or GND}$	-	-	80	μΑ
$T_{amb} = -4$	0 °C to +125 °C					
V_{IH}	HIGH-state input voltage	V _{CC} = 2.0 V	1.5	-	-	V
		V _{CC} = 4.5 V	3.15	-	-	V
		V _{CC} = 6.0 V	4.2	-	-	V
V _{IL}	LOW-state input voltage	V _{CC} = 2.0 V	-	-	0.5	V
		V _{CC} = 4.5 V	-	-	1.35	V
		V _{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -20 \mu A; V_{CC} = 2.0 V$	1.9	-	-	V
		$I_O = -20 \mu A; V_{CC} = 4.5 V$	4.4	-	-	V
		$I_O = -20 \mu A; V_{CC} = 6.0 V$	5.9	-	-	V
		$I_O = -4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.7	-	-	V
		$I_{O} = -5.2 \text{ mA}; V_{CC} = 6 \text{ V}$	5.2	-	-	V
V_{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20 \mu A; V_{CC} = 2.0 V$	-	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 4.5 V$	-	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 6.0 \text{ V}$	-	-	0.1	V
		$I_{O} = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.4	V
		$I_O = 5.2 \text{ mA}; V_{CC} = 6 \text{ V}$	-	-	0.4	V
I _{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6 \text{ V}$	-	-	±1.0	μΑ
l _{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$			±10.0	μΑ
I _{CC}	quiescent supply current	$V_{CC} = 6.0 \text{ V}; I_{O} = 0 \text{ A};$ $V_{I} = V_{CC} \text{ or GND}$	-	-	160	μΑ



At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Γ _{amb} = 25	°C					
/ _{IH}	HIGH-state input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	1.6	-	V
/ _{IL}	LOW-state input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	1.2	8.0	V
/ _{OH}	HIGH-state output voltage	$V_I = V_{IH} \text{ or } V_{IL}$				
		$I_{O} = -20 \mu A$; $V_{CC} = 4.5 \text{ V}$	4.4	4.5	-	V
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.98	4.32	-	V
/ _{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20 \mu A; V_{CC} = 4.5 V$	-	0.0	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.15	0.26	V
LI	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.1	μΑ
OZ	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 5.5$ V; $V_O = V_{CC}$ or GND; $I_O = 0$ A	-	-	±0.5	μΑ
СС	quiescent supply current	$V_{CC} = 6.0 \text{ V}; I_{O} = 0 \text{ A};$ $V_{I} = V_{CC} \text{ or GND}$	-	-	8.0	μΑ
Δl _{CC}	additional quiescent supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$; other inputs at V_{CC} or GND; $V_{CC} = 4.5 \text{ V}$ to 5.5 V; $I_O = 0 \text{ A}$				
	pin An		-	150	540	μΑ
	pin En		-	125	450	μΑ
	pin E3		-	100	360	μΑ
C _i	input capacitance		-	3.5	-	pF
Γ _{amb} = −4	0 °C to +85 °C					
/ _{IH}	HIGH-state input voltage	V _{CC} = 4.5 to 5.5 V	2.0	-	-	V
/ _{IL}	LOW-state input voltage	V _{CC} = 4.5 to 5.5 V	-	-	0.8	V
/он	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_{O} = -20 \mu A$; $V_{CC} = 4.5 \text{ V}$	4.4	-	-	V
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.84	-	-	V
/ _{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20 \mu A; V_{CC} = 4.5 V$	-	-	0.1	V
		$I_{O} = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.33	V
LI	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±1.0	μΑ
OZ	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 5.5$ V; $V_O = V_{CC}$ or GND; $I_O = 0$ A	-	-	±5.0	μΑ
CC	quiescent supply current	$V_{CC} = 5.5 \text{ V}; I_O = 0 \text{ A};$ $V_I = V_{CC} \text{ or GND}$	-	-	80	μΑ
7l ^{CC}	additional quiescent supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$; other inputs at V_{CC} or GND; $V_{CC} = 4.5 \text{ V}$ to 5.5 V; $I_O = 0 \text{ A}$				
	pin An		-	-	675	μΑ
	pin En		-	-	562.5	μΑ
	pin E3		-	-	450	μΑ

74HC_HCT138_3





At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$T_{amb} = -4$	0 °C to +125 °C					
V _{IH}	HIGH-state input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V _{IL}	LOW-state input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	8.0	V
V _{OH}	HIGH-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_{O} = -20 \mu A; V_{CC} = 4.5 V$	4.4	-	-	V
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.7	-	-	V
V _{OL}	LOW-state output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20 \mu A; V_{CC} = 4.5 \text{ V}$	-	-	0.1	V
		$I_{O} = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.4	V
ILI	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	1.0	μΑ
l _{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 5.5$ V; $V_O = V_{CC}$ or GND; $I_O = 0$ A	-	-	±10.0	μΑ
I _{CC}	quiescent supply current	$V_{CC} = 5.5 \text{ V; } I_{O} = 0 \text{ A;}$ $V_{I} = V_{CC} \text{ or GND}$	-	-	160	μΑ
Δl _{CC}	additional quiescent supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$; other inputs at V_{CC} or GND; $V_{CC} = 4.5 \text{ V}$ to 5.5 V; $I_O = 0 \text{ A}$				
	pin An		-	-	735	μΑ
	pin En		-	-	612.5	μΑ
	pin E3		-	-	490	μΑ

11. Dynamic characteristics

Table 9: Dynamic characteristics 74HC138

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified. For test circuit see Figure 8.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T _{amb} = 2	5 °C					
t _{PHL} ,	propagation delay					
t _{PLH}	An to ₹n	see Figure 6				
		V _{CC} = 2.0 V	-	41	150	ns
		V _{CC} = 4.5 V	-	15	30	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	12	-	ns
		V _{CC} = 6.0 V	-	12	26	ns
	E3 to \overline{Y} n	see Figure 6				
		V _{CC} = 2.0 V	-	47	150	ns
		V _{CC} = 4.5 V	-	17	30	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	14	-	ns
		V _{CC} = 6.0 V	-	14	26	ns
	Ēn to ₹n	see Figure 7				
		V _{CC} = 2.0 V	-	47	150	ns
		V _{CC} = 4.5 V	-	17	30	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	14	-	ns
		V _{CC} = 6.0 V	-	14	26	ns
t _{THL} ,	output transition	see Figure 6 and 7				
TLH	time	V _{CC} = 2.0 V	-	19	75	ns
		V _{CC} = 4.5 V	-	7	15	ns
		V _{CC} = 6.0 V	-	6	13	ns
C _{PD}	power dissipation capacitance	$V_I = GND \text{ to } V_{CC}$	<u>[1]</u> -	67	-	pF
T _{amb} = -	40 °C to +85 °C					
:PHL,	propagation delay					
PLH	An to \overline{Y} n	see Figure 6				
		V _{CC} = 2.0 V	-	-	190	ns
		V _{CC} = 4.5 V	-	-	38	ns
		V _{CC} = 6.0 V	-	-	33	ns
	E3 to \overline{Y} n	see Figure 6				
		V _{CC} = 2.0 V	-	-	190	ns
		V _{CC} = 4.5 V	-	-	38	ns
		V _{CC} = 6.0 V	-	-	33	ns
	Ēn to ₹n	see Figure 7				
		V _{CC} = 2.0 V	-	-	190	ns
		V _{CC} = 4.5 V	-	-	38	ns
		V _{CC} = 6.0 V			33	ns

74HC_HCT138_3

 Table 9:
 Dynamic characteristics 74HC138 ...continued

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified. For test circuit see Figure 8.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
THL,	output transition	see Figure 6 and 7				
^t TLH	time	V _{CC} = 2.0 V	-	-	95	ns
		V _{CC} = 4.5 V	-	-	19	ns
		V _{CC} = 6.0 V	-	-	16	ns
Γ _{amb} = -	40 °C to +125 °C					
PHL,	propagation delay					
PLH	An to \overline{Y} n	see Figure 6				
		$V_{CC} = 2.0 \text{ V}$	-	-	225	ns
		$V_{CC} = 4.5 \text{ V}$	-	-	45	ns
_		V _{CC} = 6.0 V	-	-	38	ns
	E3 to \overline{Y} n	see Figure 6				
		V _{CC} = 2.0 V	-	-	225	ns
		V _{CC} = 4.5 V	-	-	45	ns
		V _{CC} = 6.0 V	-	-	38	ns
	En to ₹n	see Figure 7				
		V _{CC} = 2.0 V	-	-	225	ns
		V _{CC} = 4.5 V	-	-	45	ns
		V _{CC} = 6.0 V	-	-	38	ns
THL,	output transition	see Figure 6 and 7				
TLH	time	V _{CC} = 2.0 V	-	-	110	ns
		V _{CC} = 4.5 V	-	-	22	ns
		V _{CC} = 6.0 V	-	-	19	ns

^[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

 $P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}{}^2 \times f_o) \text{ where:}$

 f_i = input frequency in MHz;

 f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

Table 10: Dynamic characteristics 74HCT138

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified. For test circuit see Figure 8.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T _{amb} = 2	5 °C					
t _{PHL} ,	propagation delay					
t _{PLH}	An to \overline{Y} n	see Figure 6				
		V _{CC} = 4.5 V	-	20	35	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	17	-	ns
	E3 to \overline{Y} n	see Figure 6				
		V _{CC} = 4.5 V	-	18	40	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	19	-	ns
	Ēn to ₹n	see Figure 7				
		V _{CC} = 4.5 V	-	19	40	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	19	-	ns
t _{THL} ,	output transition time	see Figure 6 and 7				
t _{TLH}		V _{CC} = 4.5 V	-	7	15	ns
C_{PD}	power dissipation capacitance	$V_I = GND \text{ to } (V_{CC} - 1.5 \text{ V})$ [1]] -	67	-	pF
T _{amb} = -	40 °C to +85 °C					
t _{PHL} ,	propagation delay					
t _{PLH}	An to \overline{Y} n	see Figure 6				
		V _{CC} = 4.5 V	-	-	44	ns
	E3 to \overline{Y} n	see Figure 6				
		$V_{CC} = 4.5 \text{ V}$	-	-	50	ns
	$\overline{E}n$ to $\overline{Y}n$	see Figure 7				
		$V_{CC} = 4.5 \text{ V}$	-	-	50	ns
t _{THL} ,	output transition time	see Figure 6 and 7				
t _{TLH}		$V_{CC} = 4.5 \text{ V}$	-	-	19	ns
T _{amb} = -	40 °C to +125 °C					
t _{PHL} ,	propagation delay					
t _{PLH}	An to \overline{Y} n	see Figure 6				
		V _{CC} = 4.5 V	-	-	53	ns
	E3 to \overline{Y} n	see Figure 6				
		V _{CC} = 4.5 V	-	-	60	ns
	Ēn to ₹n	see Figure 7				
		V _{CC} = 4.5 V	-	-	60	ns
t _{THL} ,	output transition time	see Figure 6 and 7				
t _{TLH}		V _{CC} = 4.5 V	-	-	22	ns

^[1] $\;\;C_{PD}$ is used to determine the dynamic power dissipation (P_D in $\mu W).$

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

 f_i = input frequency in MHz;

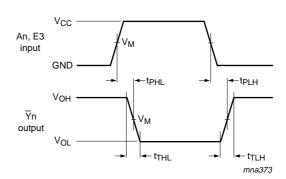
 f_o = output frequency in MHz;

C_L = output load capacitance in pF;

74HC_HCT138_3

$$\begin{split} &V_{CC} = \text{supply voltage in V;} \\ &N = \text{number of inputs switching;} \\ &\Sigma(C_L \times V_{CC}{}^2 \times f_o) = \text{sum of the outputs.} \end{split}$$

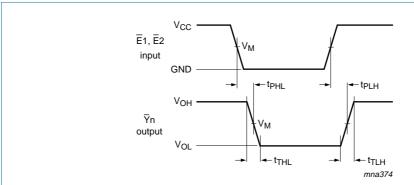
12. Waveforms



Measurement points are given in Table 11.

 V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 6. Propagation delay input (An) and enable input (E3) to output $(\overline{Y}n)$ and transition time output $(\overline{Y}n)$



Measurement points are given in Table 11.

 V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 7. Propagation delay enable input $(\overline{P}n)$ to output $(\overline{Y}n)$ and transition time output $(\overline{Y}n)$

Table 11: Measurement points

Туре	Input	Output
	V _M	V _M
74HC138	0.5V _{CC}	0.5V _{CC}
74HCT138	1.3 V	1.3 V

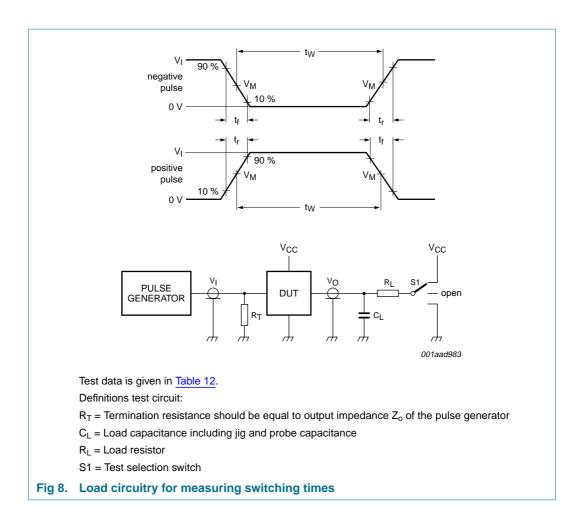


Table 12: Test data

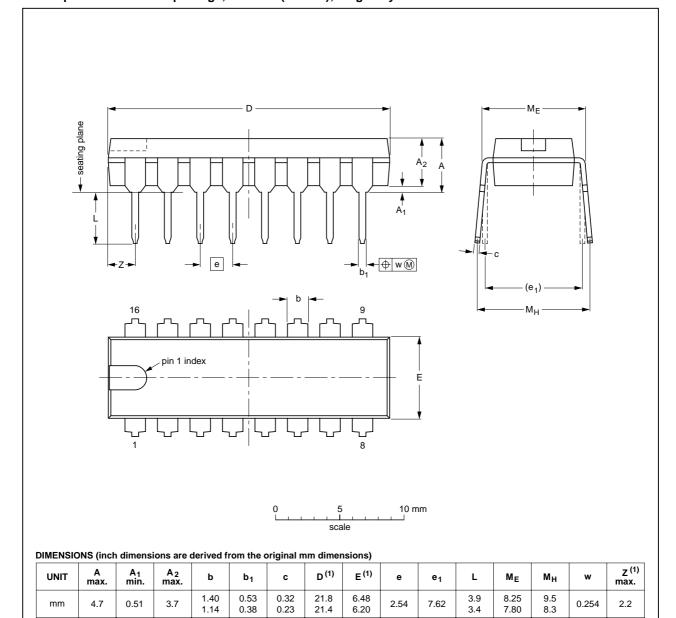
Туре	Input		Load		S1 position			
	VI	t _r , t _f	C _L	R _L	t _{PHL} , t _{PLH}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}	
74HC138	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}	
74HCT138	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}	



13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil); long body

SOT38-1



inches

0.19

0.02

0.15

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

0.055

0.021

0.013

OUTLINE		EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT38-1	050G09	MO-001	SC-503-16		99-12-27 03-02-13

0.86

0.26

Fig 9. Package outline SOT38-1 (DIP16)

74HC_HCT138_3

© Koninklijke Philips Electronics N.V. 2005. All rights reserved.

0.37

0.01

0.087

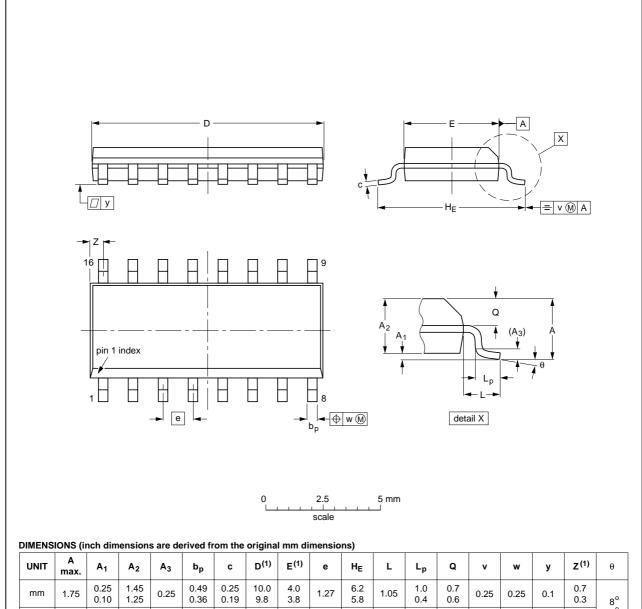
0.15

0.13

0.3

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075		0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	0°

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

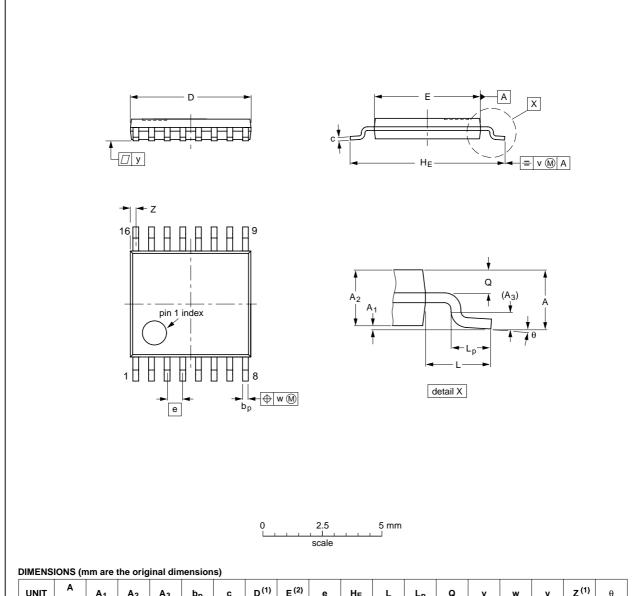
	REFER	EUROPEAN	ISSUE DATE	
IEC	JEDEC	JEITA	PROJECTION	1330E DATE
076E07	MS-012			99-12-27 03-02-19
	-	IEC JEDEC	IEC JEDEC JEITA	IEC JEDEC JEITA PROJECTION

Fig 10. Package outline SOT109-1 (SO16)

74HC_HCT138_3

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



 						-,												
UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Q	v	w	у	z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

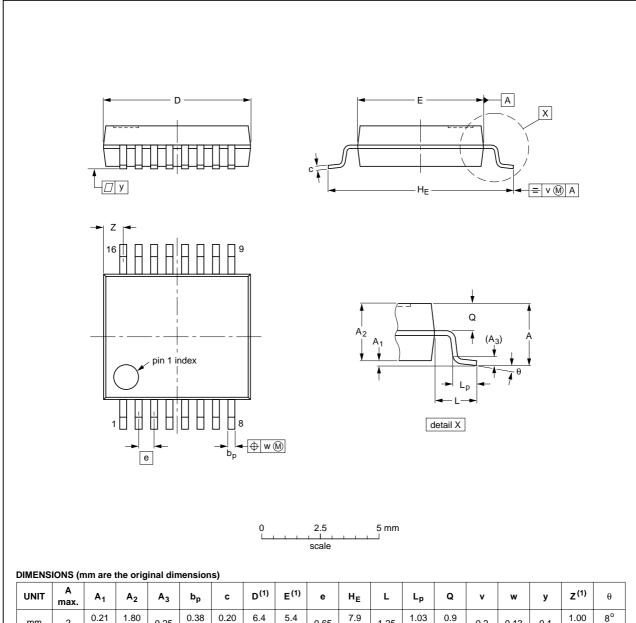
OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT403-1		MO-153				99-12-27 03-02-18	

Fig 11. Package outline SOT403-1 (TSSOP16)

74HC_HCT138_3

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



ι	JNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
	mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE		EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT338-1		MO-150			99-12-27 03-02-19

Fig 12. Package outline SOT338-1 (SSOP16)

74HC_HCT138_3

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm SOT763-1

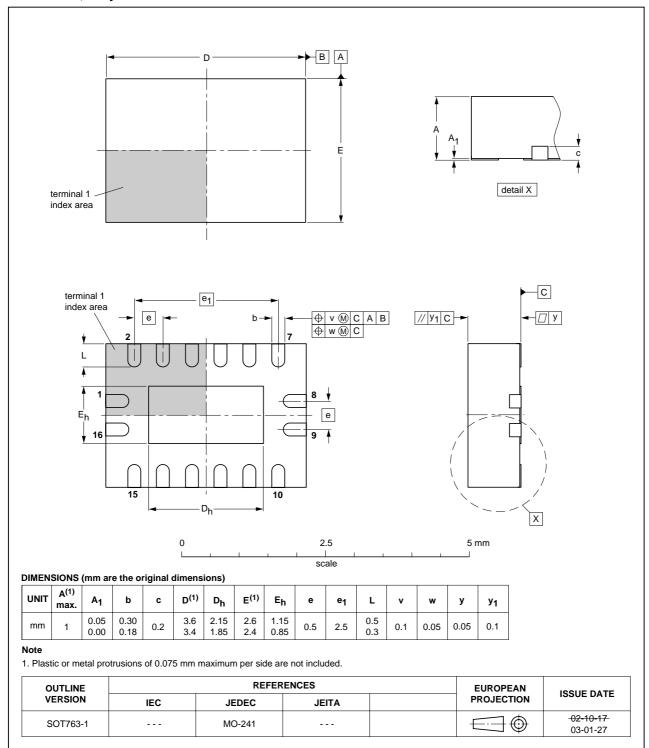


Fig 13. Package outline SOT763-1 (DHVQFN16)

74HC_HCT138_3



14. Abbreviations

Table 13: Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model

15. Revision history

Table 14: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes		
74HC_HCT138_3	20051223	Product data sheet	-	-	74HC_HCT138_CNV_2		
Modifications:	 The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. 						
		'Ordering information' dded DHVQFN packa	· 	ng information"	and Section 13 "Package		
	Section 10	"Static characteristic	s": Added from the	e family specifica	ation		
74HC_HCT138_CNV_2	19970827	Product specification	-	-	-		



Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

- [1] Please consult the most recently issued data sheet before initiating or completing a design.
- [2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
- [3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

17. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

18. Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors

customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

19. Trademarks

Notice — All referenced brands, product names, service names and trademarks are the property of their respective owners.

20. Contact information

For additional information, please visit: http://www.semiconductors.philips.com
For sales office addresses, send an email to: sales.addresses@www.semiconductors.philips.com

74HC138; 74HCT138

Philips Semiconductors

3-to-8 line decoder/demultiplexer; inverting

21. Contents

1	General description
2	Features
3	Quick reference data
4	Ordering information
5	Functional diagram 3
6	Pinning information 4
6.1	Pinning 4
6.2	Pin description 5
7	Functional description 5
8	Limiting values 6
9	Recommended operating conditions 6
10	Static characteristics 7
11	Dynamic characteristics
12	Waveforms
13	Package outline 16
14	Abbreviations
15	Revision history
16	Data sheet status
17	Definitions
18	Disclaimers 22
19	Trademarks
20	Contact information 22



All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Date of release: 23 December 2005 Document number: 74HC_HCT138_3

