



February 20, 2003  
Version 1.1

# PCI 9030/C6000 AN

Texas Instruments TMS320C6000 HPI bus to PCI 9030  
Application Note

## Features

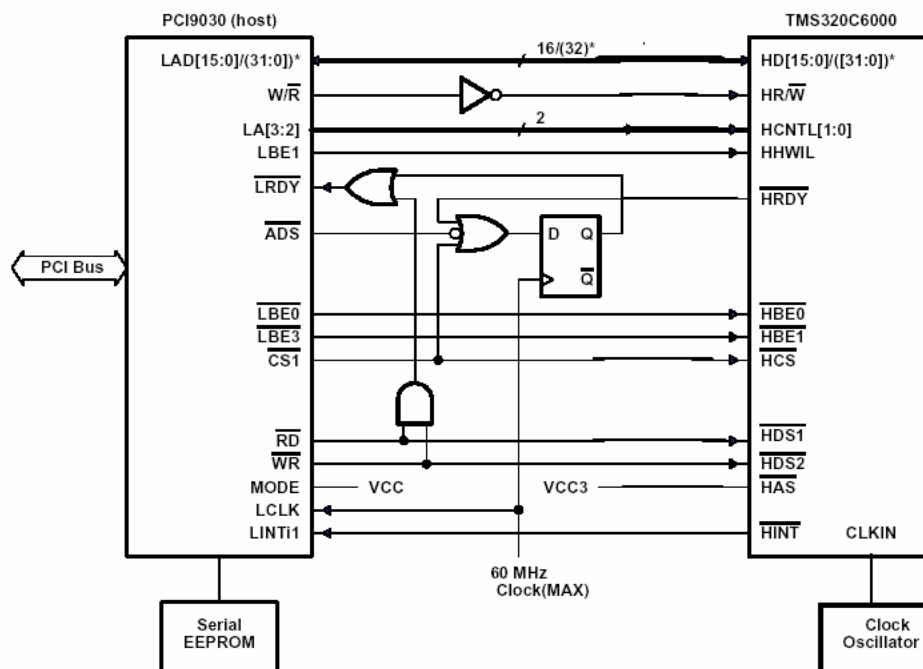
- Application Note for designing a PCI adapter board based on the connection of the PLX PCI 9030 to the Texas Instruments TMS320C6000 DSP.
- Superior PCI performance based on the PLX PCI 9030:
- 32-bit, 33MHz PCI bus, 8/16/32-bit 60MHz Local bus
- PCI Local Bus Specification v2.2 compliant Target
- 3.3/5v tolerant Universal PCI Adapter designs
- CompactPCI Hot Swap Ready

## General Description

This application note describes how to interface the Texas Instruments TMS320C6000 family HPI bus to the PCI bus using the PLX PCI 9030 SMARTarget™ I/O accelerator.

The PCI 9030 is a PCI Bus Target and a Local Bus Master. PCI Target operations originate on the PCI Bus, go through PCI 9030, and finally access the Local Bus. The PCI 9030 can allow a PCI master to perform house-keeping duties in DSP-based systems, allowing the DSPs to achieve higher signal processing rates.

The PCI 9030 with the one of the TMS320C6000 family DSPs can be used in Voice over IP (VoIP), high-speed image processing, and DSP resource card applications



# **TMS320C6000 HPI to PCI Bus**

## ***Using the PLX PCI9030***

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### **ABSTRACT**

This application report describes an interface between the Texas Instruments TMS320C6000™ DSP host port and the PLX Technology PCI9030, the PCI interface chip. PCI 9030 is PCI Local Bus Specification v2.2-compliant 32-bit, 33Mhz Bus Target Interface Device enabling PCI Burst Transfer up to 132MB/s, and industry's first CompactPCI Hot Swap Ready Device.

This application report includes a diagram showing connections between the two devices, PAL equations, and verification that timing requirements are met for each device (using tables and timing diagrams).

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## 1 Host Port Interface to the PCI Bus

The PCI9030 provides a compact high-performance PCI bus target (slave) interface for adapter boards. The PCI9030 is designed to connect a wide variety of local bus designs to the PCI bus. The PCI9030 can be programmed to connect directly to the multiplexed or nonmultiplexed 8-bit, 16-bit, or 32-bit local bus.

The PCI9030 contains two independent FIFOs to speed match the 32-bit wide, 33-MHz PCI bus to a local bus, which may be narrower or slower. Up to five local address spaces and up to four independent chip selects are supported.

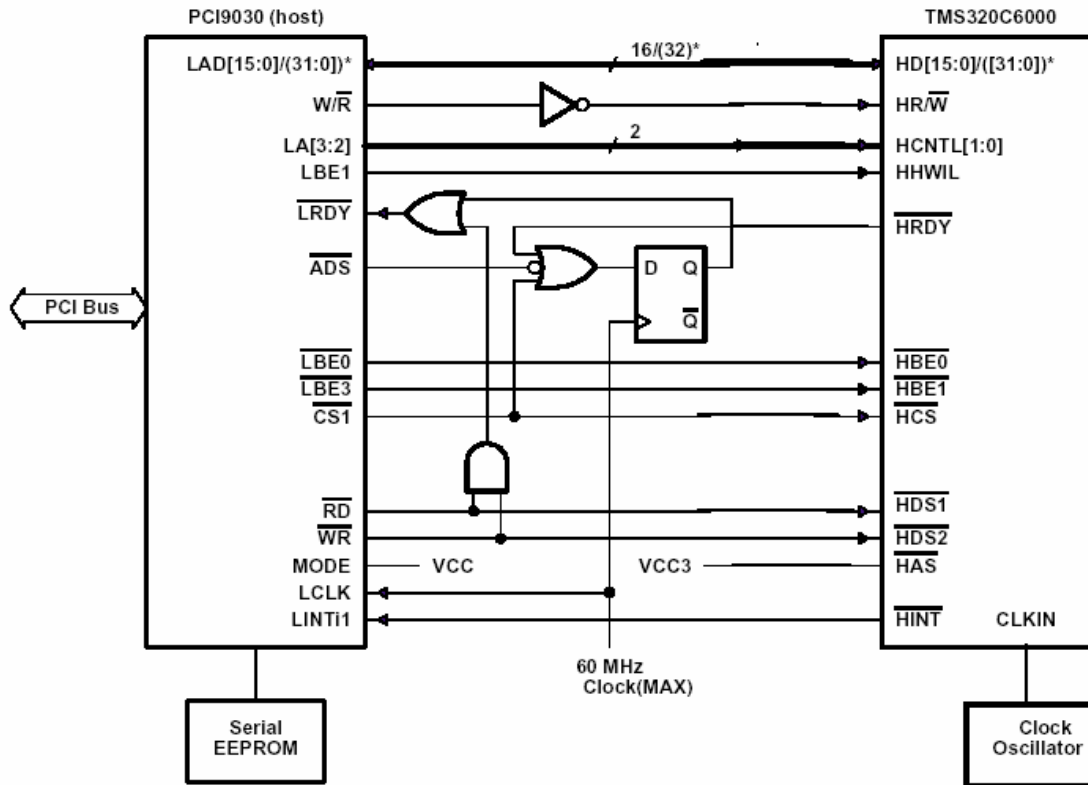
## 2 PCI9030 Interface

Voltage conversion is not required between PCI9030 and TMS320C6000 DSP because both the PCI 9030 and the C6000 DSP are 3.3-V I/O devices. This is a simpler connection than PCI 9030's predecessors (PCI 9050/52) because such devices require 5V to operate.

The PCI9030 has no direct master capability on the PCI bus. The internal registers are accessible from the host CPU on the PCI bus or from the serial EEPROM.

Figure 1 is a diagram and Table 1 is a list of the PCI9030-to-HPI connections. The PCI9030 local bus is programmed to be multiplexed (MODE pin is tied to VCC).

The configuration shown does not support the PCI9030 burst mode.



**Figure 1. PCI-to HPI Interface Block Diagram**

**Table 1. PCI9050-to-HPI Pin Connections**

HPI Pin	PCI9050 Pin	Function
HCNTL[1:0]	LA[3:2]	Address bits of PCI9050 are used as control signals
HHWIL	LBE1	LBE1 identifies the first or second half-word of transfer. This Signal is absent on the TMS320C64x 32-bit HPI.
HR/W	Inverted W/R	Indicates a read or write access. Because the C6000 HPI port has a read-write (HR/W) line with the opposite polarity of the PCI9050 read-write pin (W/R), an inverter is used to connect these two lines.
HD[15:0]/[31:0]	LAD[15:0]/[31:0]	16 LSBs of data. 21-bit word for C64x 32-bit HPI.
HDS1	RD	HDS1 is connected to the RD.
HDS2	WR	HDS2 is connected to the WR.
HAS	Vcc	Address latch enable is not used in this interface.
HCS	CS1	HCS can be connected to any of the PCI9050 CS output lines.

**Table 1. PCI9030-to-HPI Pin Connections (Continued)**

HPI Pin	PCI9030 Pin	Function
$\overline{\text{HBE0}}$	$\overline{\text{LBE0}}$	HPI uses this value on writes only. This signal is absent on the C6211/C6711 and C64x.
$\overline{\text{HBE1}}$	$\overline{\text{LBE3}}$	HPI uses this value on writes only. This signal is absent on the C6211/C6711 and C64x.
$\overline{\text{HRDY}}$	$\overline{\text{LRDY}}$	Asynchronous $\overline{\text{HPI}}$ ready output ( $\overline{\text{HRDY}}$ ) is synchronized and connected to $\overline{\text{LRDY}}$ .
$\overline{\text{HINT}}$	$\overline{\text{XINTx}}$	Any external interrupt can be chosen.

### 3 Configuration

During power up, the PCI  $\overline{\text{RST}}$  signal resets the default values of the PCI9030 internal registers. In return, the PCI9030 outputs the local reset signal ( $\overline{\text{LRESET}}$ ) and checks for the existence of the serial EEPROM. If a serial EEPROM is installed and the first 16-bit word is not FFFFh, the PCI9030 loads the internal registers for the serial EEPROM. Otherwise, default values are used. The PCI9030 configuration registers can be written only by the optional serial EEPROM or the PCI host processor.

Five local address spaces (local spaces 0–3 and expansion ROM) are accessible from the PCI bus. In this example, local space 1 is used. A set of four registers defines each space, defining the local bus characteristics:

- PCI base address
- Local range
- Local base address (remap)
- Local bus region descriptor

Local bus address space 1 region descriptor register (LAS1BRD) must be set to:

- Disable burst (LAS1BRD[0] = 0)
- Enable READY input (LAS1BRD[1] = 1)
- Disable BTERM input (LAS1BRD[2] = 0)
- Enable 16-bit bus width (LAS1BRD[23:22] = 01) or enable 32-bit bus width for TMS320C64x™ 32-bit HPI (LAS1BRD[23:22] = 10)
- Little-endian (LAS1BRD[24] = 0)
- The PCI9030 provides a write-cycle hold parameter that should be used to extend the cycle for one clock after the write strobe is deasserted (LAS1BRD[31:30] = 01 to extend a write cycle for one clock). This is done to meet the data hold-time requirement for the C6000 DSP.

The wait states for READ strobe should be cleared to 0.

## 4 PCI9030-to-HPI Timing Verification

To verify proper operation, two functions have been examined:

1. a PCI9030 write to the HPI (Table 2, Figure 2, and Figure 3)
2. a PCI9030 read from the HPI (Table 3, Figure 4, and Figure 5)

In each instance, timing requirements were compared for each of the devices.

Note that the write cycle is extended for one clock (by setting LAS1BRD[31:30] = 01) after the write strobe is deasserted (to meet data hold-time requirement of the HPI).

The estimated maximum transfer speed between the 16-bit HPI and the PCI bus is 20 Mbytes/s for reads, and 16 Mbytes/s for writes.

The tables and timing diagrams show that the timing parameters for both devices are met in the interface of the PCI9030 and the HPI. The PCI9030 local bus in this example operates at 40 MHz based on historical test data. However the best performance can be achieved at 60MHz. The TMS320C6201 DSP operates at 100-200Mhz(C6211 or C6701 devices can operate at 167Mhz, and C64X devices can operate at frequencies up to 600 MHz).

**Table 2. Timing Requirements for PCI9030 Write to TMS320C6000 HPI**

HPI Symbol	PCI9030 Symbol <sup>†</sup>	Parameter	C6x01 HPI Min (ns)	C6x11 HPI Min (ns)	C64x HPI Min (ns)	PCI9030 Min (ns)
tw(HSTBL)	2Tcyc-td(RD) <sub>max</sub> +td(RD) <sub>min</sub>	Pulse width of HDS low	10	24	24	30
tsu(SEL-HSTBL)	Tcyc-td(LBE)+td(WR)	Setup time, select signals <u>valid</u> before HDS	4	5	5	14
th(HSTBL-SEL)	2Tcyc-td(RD)+ td(LBE)	Hold time, select signals <u>valid</u> after HDS low	2	4	2	27
tsu(HDV-HSTBH)	2Tcyc-td(LAD)+td(WR)	Setup time, host <u>data</u> valid before HDS high (WRITE SETUP TIME)	3	5	5	38
th(HSTBH-HDV)	Tcyc-td(WR)+ td(LAD)	Hold time, host <u>data</u> valid after HDS high	2	3	2	17

<sup>†</sup> Tcyc denotes one clock cycle time of PCI9030 local bus. At 40-MHz operating frequency, Tcyc = 25 ns.

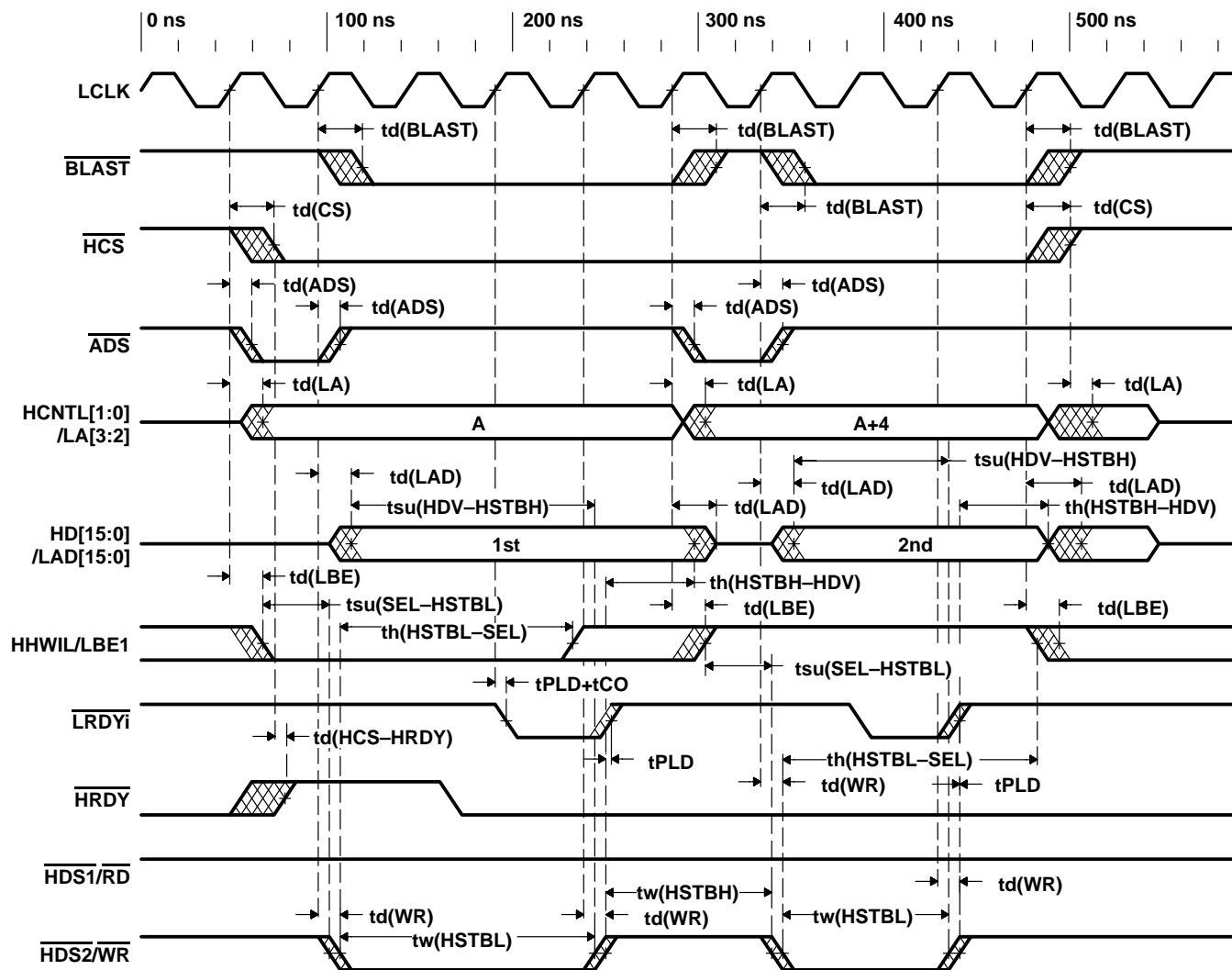


Figure 2. PCI9030 Write to TMS320C6000 DSP Using the HPI (16-Bit)

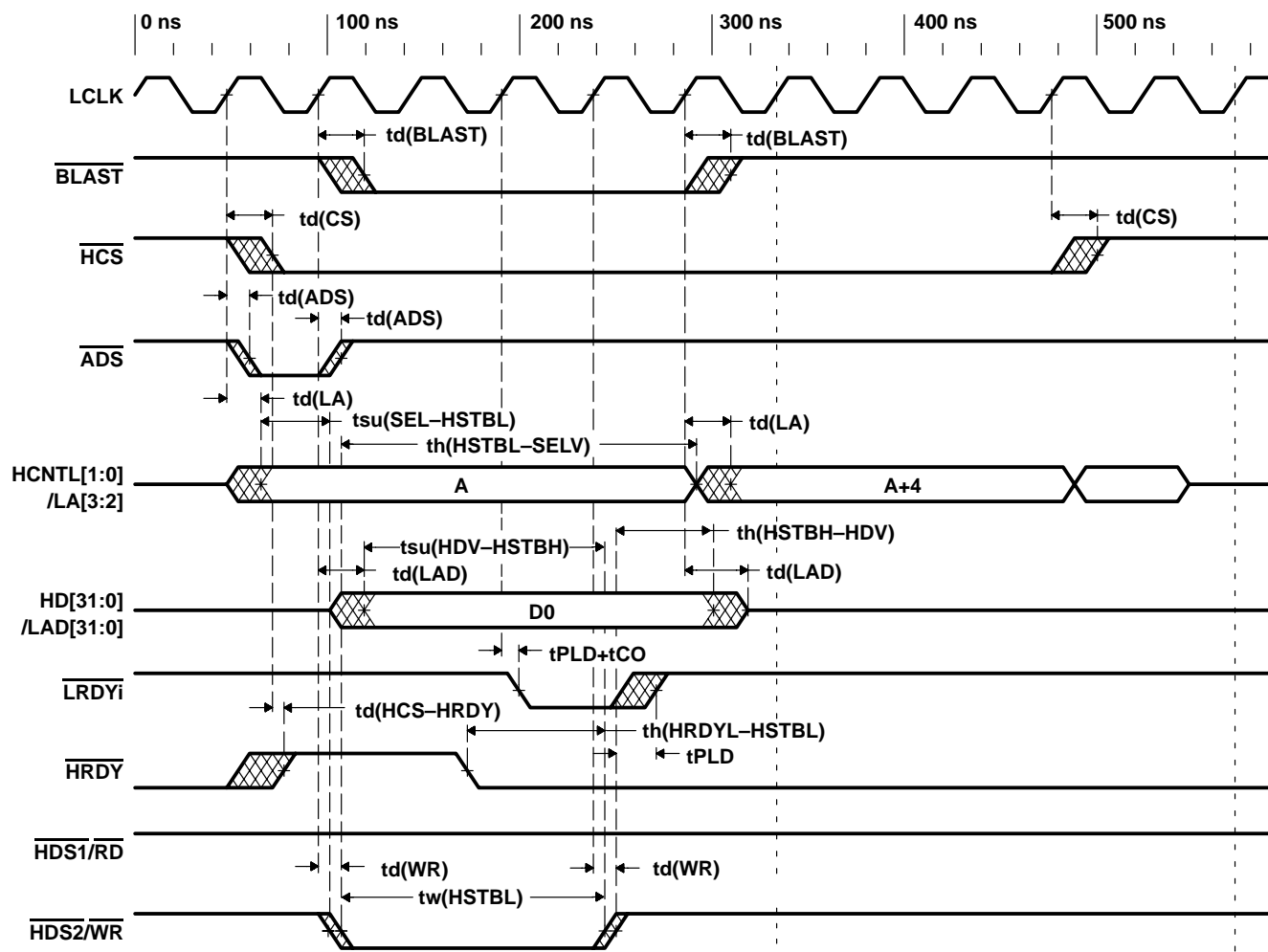


Figure 3. PCI9030 Write to TMS320C64x DSP Using the HPI (32-Bit)



**Table 3. Timing Requirements for PCI9030 Read From TMS320C6000 HPI**

HPI Symbol†	PCI9030 Symbol	Parameter	C6201 HPI Min (ns)	C6211 HPI Min (ns)	C64x HPI Min (ns)	PCI9030 Min (ns)
2Tcyc–td(RD)–td(HSTBL–HDV)	Tsu	(READ SETUP TIME) Input setup LAD[15:0]/[31:0] – LCLK	11	8	11	5
td(RD)+th(HSTBH–HDV)	Th	Input hold from LCLK – LAD[15:0]/[31:0]	9	10	9	1
Tcyc–tCO–tPLD	Tsu	LRDYi valid to LCLK high–READY setup time	15	15	15	7
Td(RD)+tPLD	Th	LCLK high to LRDYi invalid–READY hold time	12	12	12	1

† Tcyc denotes one clock cycle time of PCI9030 local bus. At 40-MHz operating frequency, Tcyc = 25 ns.

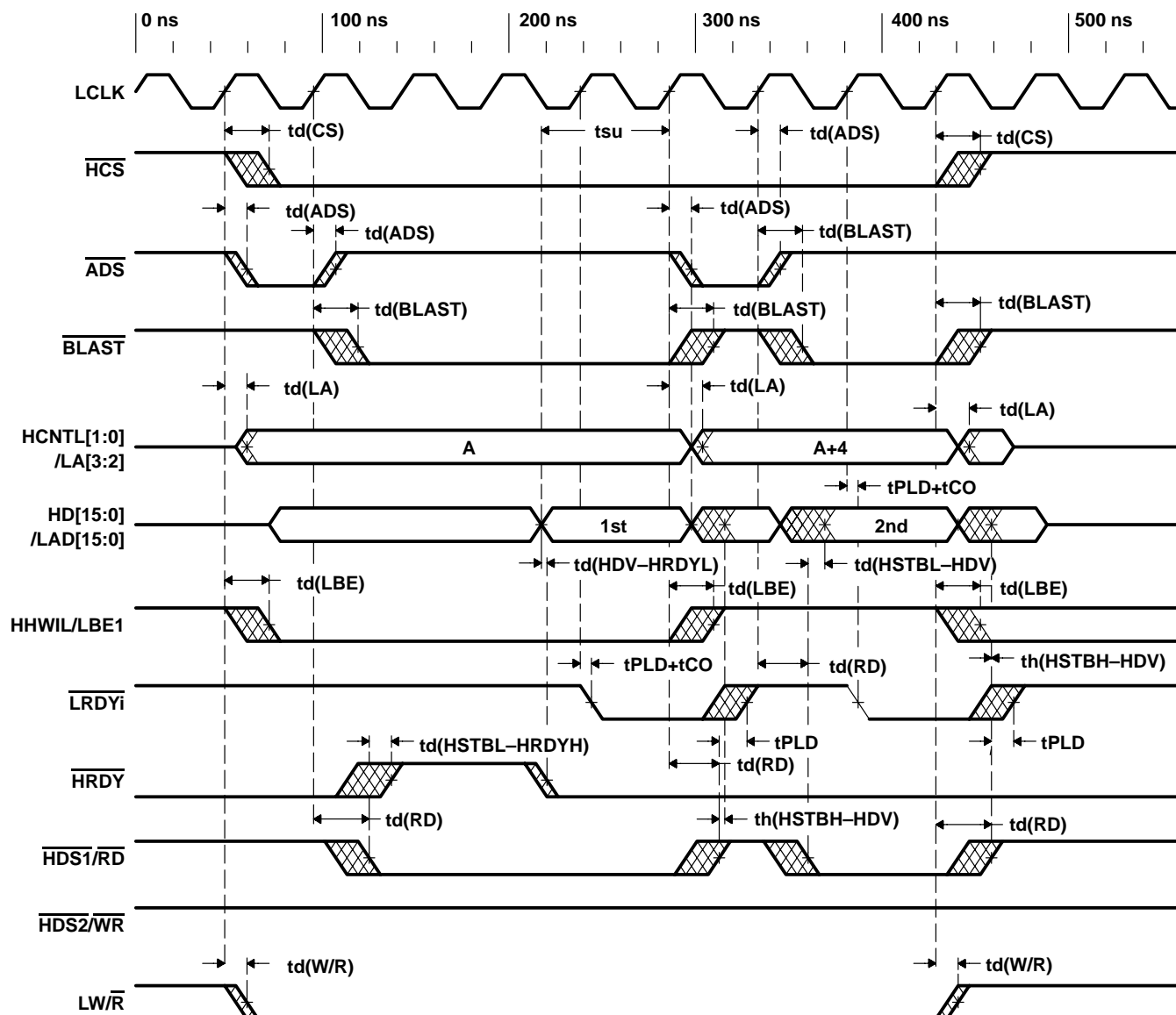


Figure 4. PCI9030 Read From TMS320C6000 DSP Internal Memory Using the HPI (16-Bit)

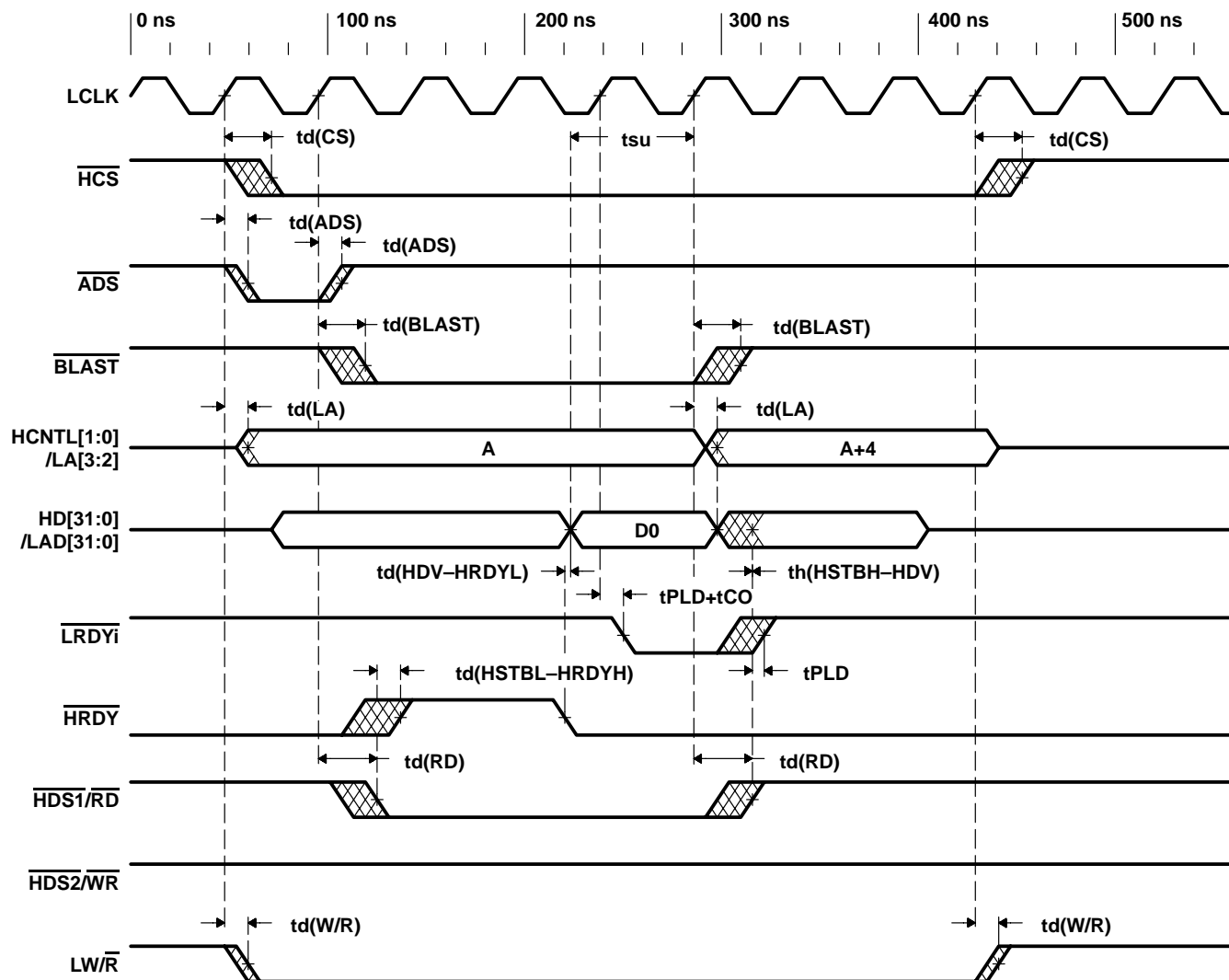


Figure 5. PCI9030 Read From TMS320C64x DSP Internal Memory Using the HPI (32-Bit)

## 5 References

1. *TMS320C6000 Peripherals Reference Guide*, (SPRU190).
2. See the Texas Instruments web site at [www.ti.com](http://www.ti.com) for the TMS320C62x™, C64x, and TMS320C67x™ DSP generation devices that have HPI and their respective device-specific data sheets.
3. *TMS320C6201 Fixed-Point Digital Signal Processor* (SPRS051).
4. *TMS320C6211, TMS320C6211B Fixed-Point Digital Signal Processor* (SPRS073).
5. *TMS320C6414 Fixed-Point Digital Signal Processor* (SPRS134).
6. *TMS320C6415 Fixed-Point Digital Signal Processor* (SPRS146).
7. *TMS320C6416 Fixed-Point Digital Signal Processor* (SPRS164).
8. *TMS320C6701 Floating-Point Digital Signal Processor* (SPRS067).
9. *TMS320C6711, TMS320C6711B Floating-Point Digital Signal Processors* (SPRS088).
10. *PLX PCI9030 Datasheet*, PLX Technology, Inc.

## Appendix A TMS320C6000 Timing Requirements

The timing requirements in Table A–1 are provided for quick reference only. For detailed descriptions, notes, and restrictions, see the C62x™, C64x, and/or C67x™ DSP generation device-specific data sheets.

**Table A–1. Timing Requirements for TMS320C6000 HPI**

Characteristic	Symbol	C6201 HPI (ns) <sup>†</sup>		C6211 HPI (ns) <sup>†</sup>		C64x HPI (ns) <sup>†</sup>	
		Min	Max	Min	Max	Min	Max
Pulse width of $\overline{\text{HSTROBE}}$ high between consecutive accesses	tw(HSTBH)	2 Tcyc		4 Tcyc		4 Tcyc	
Hold time, $\overline{\text{HSTROBE}}$ low after HRDY low	th(HRDY–HSTBL)	1		2		2	
Pulse width of strobe low	tw(HSTBL)	2 Tcyc		4 Tcyc		4 Tcyc	
Delay time, $\overline{\text{HCS}}$ to $\overline{\text{HRDY}}$	td(HCS–HRDY)	1	9	1	15	1	7
Setup time, select signals valid before $\overline{\text{HSTROBE}}$ low	tsu(SEL–HSTBL)	4		5		5	
Hold time, select signals valid after $\overline{\text{HSTROBE}}$ low	th(HSTBL–SEL)	2		4		2	
Setup time, select signals valid before $\overline{\text{HAS}}$ low	tsu(SEL–HASL)	4		5		5	
Hold time, select signals valid after $\overline{\text{HDS}}$ low	th(HASL–SEL)	2		3		2	
Setup time, host data valid before $\overline{\text{HSTROBE}}$ high	tsu(HDV–HSTBH)	3		5		5	
Hold time, host data valid after strobe $\overline{\text{HSTROBE}}$ high (write)	th(HSTBH–HDV)	2		3		2	
Hold time, host data valid after $\overline{\text{HSTROBE}}$ high (HPI read)	th(HSTBH–HDV)	2		3		2	
Hold time, host data low impedance after $\overline{\text{HSTROBE}}$ low	th(HSTBL–HDLZ)	4		2		2	
Delay time, $\overline{\text{HSTROBE}}$ high to host data not driven	td(HSTBH–HDHZ)	3	12	3	15		12
Delay time, $\overline{\text{HSTROBE}}$ low to HRDY high	td(HSTBL–HRDYH)	3	12	3	15	3	12
Delay time, host data valid to HRDY low	td(HDV–HRDYL)	Tcyc – 3	Tcyc + 3	2Tcyc – 4	2Tcyc + 4	2Tcyc – 6	
Delay time, host data valid after $\overline{\text{HSTROBE}}$ low	td(HSTBL–HDV)	2	12	3	15		12
Delay time, $\overline{\text{HSTROBE}}$ high to HRDY high	td(HSTBH–HRDYH)	3	12	3	15	3	12

<sup>†</sup> Tcyc = (1/ DSP clock frequency) [ns]

## Appendix B PCI9030 Timing Requirements

The timing requirements in Table B–1 are provided for quick reference only. For detailed descriptions, notes, and restrictions, see *PLX PCI9030 Datasheet*.

**Table B–1. Timing Requirements for PCI9030**

Characteristic	Symbol	Min (ns)	Max (ns)
Local bus address strobe	td(ADS)	5	10
Local bus burst last signal	td(BLAST)	5	10
Local bus address	td(LA)	5	10
Local bus data	td(LAD)	5	10
Local bus byte enables	td(LBE)	5	10
Local bus write control signal	td(WR)	5	10
Local bus read control signal	td(RD)	7	10
Local bus W/R_ control signal	td(W/R)	5	10
Local bus input setup time	Tsu		7
Local bus input hold time	Th	1	

## Appendix C PAL Equations

Page 1

Synario 3.10 - Device Utilization Chart  
9030.bls

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Module : 'pci9030'

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Input files:

ABEL PLA file : pci9030.tt3  
Device library : P22V10C.dev

Output files:

Report file : pci9030.rep  
Programmer load file : pci9030.jed

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Synario 3.10 - Device Utilization Chart

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9030.bls

P22V10C Programmed Logic:

```
-----  
LRDY      = ( N_9.Q  
              #   RDn & WRn );  
N_9.D     = ( CS1  
              #   !ADSn  
              #   HRDY ); " ISTYPE 'INVERT'  
N_9.C     = ( CLKIN );  
RnW       = ( !WnR );
```

Synario 3.10 - Device Utilization Chart

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9030.bls

P22V10C Chip Diagram:

P22V10C									
C									
L									
L									
C	R	K				R	R		
S	D	I				n	D		
1	n	N				W	Y		
/-----									
/	4	3	2	1	28	27	26		
ADSn	5						25		
HRDY	6						24		
WnR	7						23		
	8						22		
WRn	9						21		
	10						20		
	11						19		
	12	13	14	15	16	17	18		

N

—

9

SIGNATURE: N/A



Synario 3.10 - Device Utilization Chart

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9030.bls

P22V10C Resource Allocations:

Device	Resource	Design	
Resources	Available	Requirement	Unused
=====	=====	=====	=====
Input Pins:			
Input:	12	7	5 ( 41 %)
Output Pins:			
In/Out:	10	3	7 ( 70 %)
Output:	-	-	-
Buried Nodes:			
Input Reg:	-	-	-
Pin Reg:	10	1	9 ( 90 %)
Buried Reg:	-	-	-

Synario 3.10 - Device Utilization Chart

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9030.bls

P22V10C Product Terms Distribution:

Signal Name	Pin Assigned	Terms Used	Terms Max	Terms Unused
=====	=====	=====	=====	=====
LRDY	26	2	10	8
N_9.D	17	3	8	5
RnW	27	1	8	7

==== List of Inputs/Feedbacks ====

Signal Name	Pin	Pin Type
=====	=====	=====
CLKIN	2	CLK/IN
RDn	3	INPUT
CS1	4	INPUT
ADSn	5	INPUT
HRDY	6	INPUT
WnR	7	INPUT
WRn	9	INPUT

Synario 3.10 - Device Utilization Chart

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9030.bls

P22V10C Unused Resources:

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Pin Number	Pin Type	Product Terms	Flip-flop Type
=====	=====	=====	=====
10	INPUT	-	-
11	INPUT	-	-
12	INPUT	-	-
13	INPUT	-	-
16	INPUT	-	-
18	BIDIR	NORMAL 10	D
19	BIDIR	NORMAL 12	D
20	BIDIR	NORMAL 14	D
21	BIDIR	NORMAL 16	D
23	BIDIR	NORMAL 16	D
24	BIDIR	NORMAL 14	D
25	BIDIR	NORMAL 12	D

Synario 3.10 - Device Utilization Chart

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9030.bls

P22V10C Fuse Map:

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	0	10	20	30	40
44:	-----	-----	-----	-----	----
88:	-----	-----	-X-----	-----	----
440:	-----	-----	-----	-----	----
484:	-----	-----	-----	-----	-X----
528:	---X-----	-----	---X-----	-----	----
5368:	-----	-----	-----	-----	----
5412:	-----X-	-----	-----	-----	----
5456:	-----	---X-----	-----	-----	----
5500:	-----	-----X--	-----	-----	----
	0	10			
5808:	----XXXXXX	XXXXXXXXXX			