

CD4067B, CD4097B Types

CMOS Analog Multiplexers/Demultiplexers

High-Voltage Types (20-Volt Rating)

CD4067B – Single 16-Channel
Multiplexer/Demultiplexer

CD4097B – Differential 8-Channel
Multiplexer/Demultiplexer

■ CD4067B and CD4097B CMOS analog multiplexers/demultiplexers* are digitally controlled analog switches having low ON impedance, low OFF leakage current, and internal address decoding. In addition, the ON resistance is relatively constant over the full input-signal range.

The CD4067B is a 16-channel multiplexer with four binary control inputs, A, B, C, D, and an inhibit input, arranged so that any combination of the inputs selects one switch.

The CD4097B is a differential 8-channel multiplexer having three binary control inputs A, B, C, and an inhibit input. The inputs permit selection of one of eight pairs of switches.

A logic "1" present at the inhibit input turns all channels off.

The CD4067B and CD4097B types are supplied in 24-lead hermetic dual-in-line ceramic packages (F3A suffix), 24-lead dual-in-line plastic packages (E suffix), 24-lead small-outline packages (M, M96, and NSR suffixes), and 24-lead thin shrink small-outline packages (P and PWR suffixes).

*When these devices are used as demultiplexers, the channel in/out terminals are the outputs and the common out/in terminals are the inputs.

Recommended Operating Conditions at $T_A = 25^\circ\text{C}$ (Unless Otherwise Specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges. Values shown apply to all types except as noted.

Characteristic	Min.	Max.	Units
Supply-Voltage Range (T_A = Full Package-Temp. Range)	3	18	V
Multiplexer Switch Input Current Capability	—	25	mA
Output Load Resistance	100	—	Ω

NOTE:

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into terminal 1 on the CD4067; terminals 1 and 17 on the CD4097.

Features:

- Low ON resistance: $125\ \Omega$ (typ.) over 15 V_{p-p} signal-input range for $V_{DD}-V_{SS}=15\ \text{V}$
- High OFF resistance: channel leakage of $\pm 10\ \text{pA}$ (typ.) @ $V_{DD}-V_{SS}=10\ \text{V}$
- Matched switch characteristics: $R_{ON}=5\ \Omega$ (typ.) for $V_{DD}-V_{SS}=15\ \text{V}$
- Very low quiescent power dissipation under all digital-control input and supply conditions: $0.2\ \mu\text{W}$ (typ.) @ $V_{DD}-V_{SS}=10\ \text{V}$
- Binary address decoding on chip
- 5-V, 10-V, and 15-V parametric ratings
- 100% tested for quiescent current at 20 V
- Standardized symmetrical output characteristics
- Maximum input current of $1\ \mu\text{A}$ at 18 V over full package temperature range; $100\ \text{nA}$ at 18 V and 25°C
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Analog and digital multiplexing and demultiplexing
- A/D and D/A conversion
- Signal gating

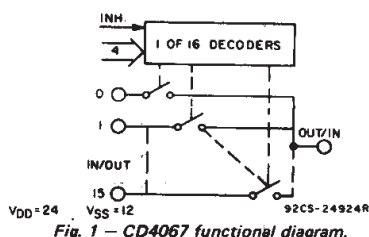
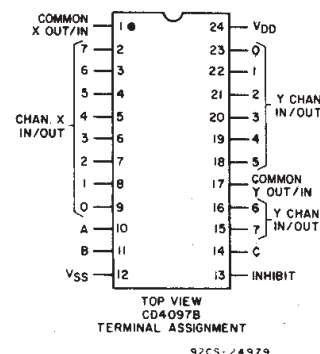
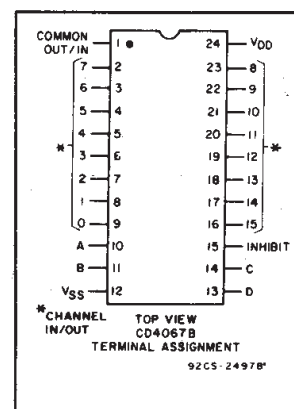


Fig. 1—CD4067 functional diagram.

CD4067 TRUTH TABLE

A	B	C	D	Inh	Selected Channel
0	0	0	0	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

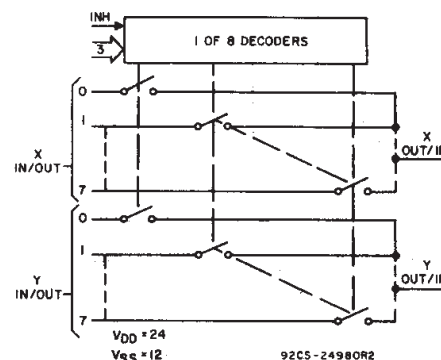



Fig. 2—CD4097 functional diagram.

CD4097 TRUTH TABLE

A	B	C	Inh	Selected Channel
0	0	0	1	None
0	0	0	0	0X, 0Y
1	0	0	0	1X, 1Y
0	1	0	0	2X, 2Y
1	1	0	0	3X, 3Y
0	0	1	0	4X, 4Y
1	0	1	0	5X, 5Y
0	1	1	0	6X, 6Y
1	1	1	0	7X, 7Y

CD4067B, CD4097B Types

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							Units	
	V _{is} (V)	V _{SS} (V)	V _{DD} (V)	-55	-40	+85	+125	+25				
								Min.	Typ.	Max.		
SIGNAL INPUTS (V _{is}) AND OUTPUTS (V _{Os})												
Quiescent Device Current, I _{DD} Max.			5	5	5	150	150	—	0.04	5	μA	
			10	10	10	300	300	—	0.04	10		
			15	20	20	600	600	—	0.04	20		
			20	100	100	3000	3000	—	0.08	100		
ON-state Resistance V _{SS} ≤ V _{is} ≤ V _{DD} r _{on} Max.		0	5	800	850	1200	1300	—	470	1050	Ω	
		0	10	310	330	520	550	—	180	400		
		0	15	200	210	300	320	—	125	240		
Change in on-state Resistance (Between Any Two Channels) Δr _{on}		0	5	—	—	—	—	—	15	—	Ω	
		0	10	—	—	—	—	—	10	—		
		0	15	—	—	—	—	—	5	—		
OFF Channel Leakage Current: Any Channel OFF Max. or All Channels OFF (Common OUT/IN) Max.		0	18	±100*		±1000*		—	±0.1	±100*	nA	
Capacitance: Input, C _{is}		-5	5	—	—	—	—	—	5	—	pF	
Output, C _{os}				—	—	—	—	—	55	—		
CD4067				—	—	—	—	—	35	—		
CD4097				—	—	—	—	—	—	—		
Feed-through, C _{ios}				—	—	—	—	—	0.2	—		
Propagation Delay Time (Signal Input to Output)		R _L = 200 KΩ C _L = 50 pF t _r , t _f = 20 ns	5	—	—	—	—	—	30	60	ns	
			10	—	—	—	—	—	15	30		
			15	—	—	—	—	—	10	20		
CONTROL (ADDRESS or INHIBIT) V _C												
Input Low Voltage, V _{IL} Max.	=V _{DD} thru 1 KΩ	R _L = 1 KΩ to V _{SS} I _{IS} ≤ 2 μA on all OFF Channels	5	1.5			—		—		1.5	V
			10	3			—		—		3	
			15	4			—		—		4	
Input High Voltage, V _{IH} Min.			5	3.5			3.5		—		—	
			10	7			7		—		—	
			15	11			11		—		—	

* Determined by minimum feasible leakage measurement for automatic testing.

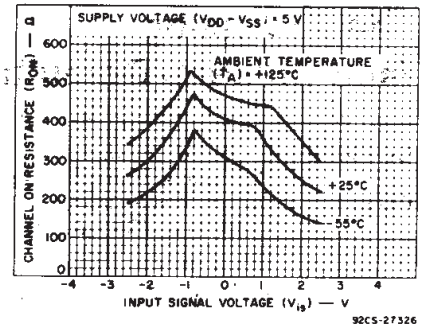


Fig. 3—Typical ON resistance vs. input signal voltage (all types).

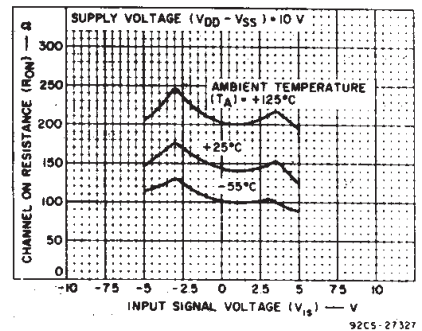


Fig. 4—Typical ON resistance vs. input signal voltage (all types).

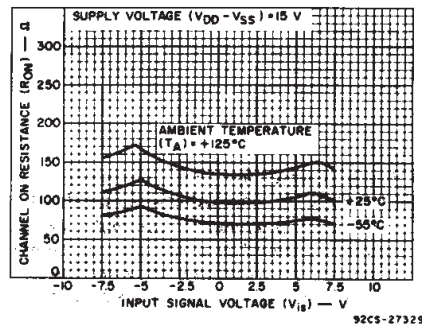


Fig. 5—Typical ON resistance vs. input signal voltage (all types).

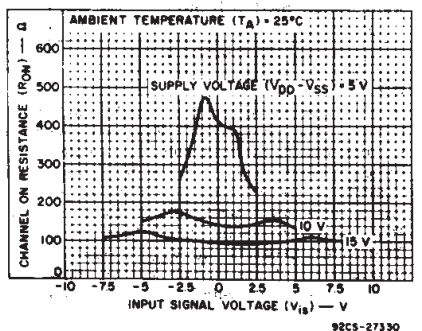


Fig. 6—Typical ON resistance vs. input signal voltage (all types).

CD4067B, CD4097B Types

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							Units		
	V _{IS} (V)	V _{SS} (V)	V _{DD} (V)	-55	-40	+85	+125	+25					
								Min.	Typ.	Max.			
Input Current, I _{IN} Max.	V _{IN} = 0, 18 V		18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA		
Propagation Delay Time: Address or Inhibit-to-Signal OUT (Channel turning ON)	R _L = 10 KΩ, C _L = 50 pF, t _r , t _f = 20 ns			—	—	—	—	—	325	650	ns		
												0	5
												0	10
												0	15
Address or Inhibit-to-Signal OUT (Channel turning OFF)	R _L = 300 Ω, C _L = 50 pF, t _r , t _f = 20 ns			—	—	—	—	—	220	440	ns		
												0	5
												0	10
												0	15
Input Capacitance, C _{IN}	Any Address or Inhibit Input			—	—	—	—	—	5	7.5	pF		

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to $V_{DD} + 0.5\text{V}$

DC INPUT CURRENT, ANY ONE INPUT $\pm 10\text{mA}$

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearly at $12\text{mW}/^\circ\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch (1.59 \pm 0.79mm) from case for 10s max $+265^\circ\text{C}$

TEST CIRCUITS

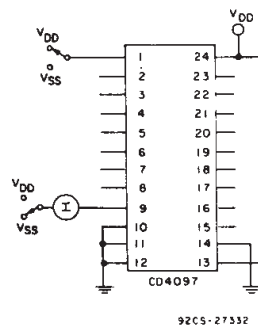
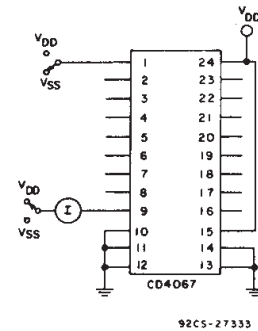


Fig. 7—OFF channel leakage current—any channel OFF.

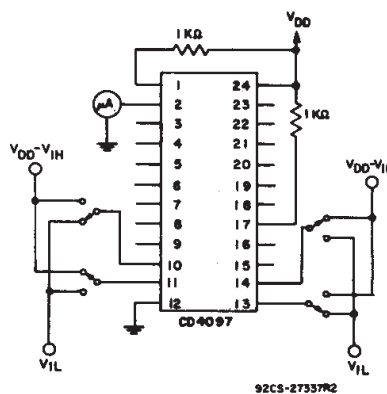
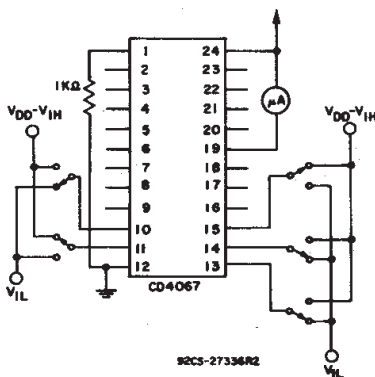


Fig. 8—Input voltage—measure $< 2\ \mu\text{A}$ on all OFF channels (e.g., channel 12).

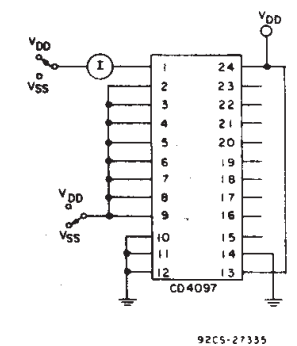
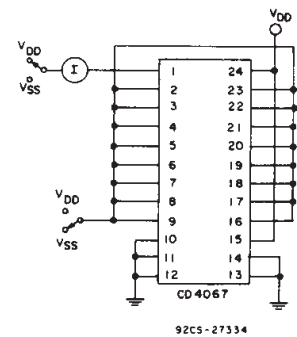


Fig. 9—OFF channel leakage current—all channels OFF.

CD4067B, CD4097B Types

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARAC- TERISTIC	TEST CONDITIONS			TYPICAL VALUES	UNITS
	V _{is} (V)	V _{DD} (V)	R _L (KΩ)		
Cutoff (-3-dB) Frequency Channel ON (Sine Wave Input)	5 [•]	10	1		
	$20 \log \frac{V_{os}}{V_{is}} = -3 \text{ dB}$		V _{os} at Common OUT/IN	CD4067	14
				CD4097	20
	V _{os} at Any Channel				60
Total Harmonic Distortion, THD	2 [•]	5	10		0.3
	3 [•]	10			0.2
	5 [•]	15			0.12
	f _{is} = 1 kHz sine wave				
-40-dB Feedthrough Frequency (All Channels OFF)	5 [•]	10	1		
	$20 \log \frac{V_{os}}{V_{is}} = -40 \text{ dB}$		V _{os} at Common OUT/IN	CD4067	20
				CD4097	12
	V _{os} at Any Channel				8
Signal Cross- talk (Fre- quency at -40 dB)	5 [•]	10	1		
	$20 \log \frac{V_{os}}{V_{is}} = -40 \text{ dB}$		Between Any 2 Channels [▲]		1
			Between Sections CD4097 Only	Measured on Common	10
				Measured on Any Channel	18
Address-or- Inhibit-to- Signal Crosstalk	—	10	10*		
	V _{SS} =0, t _r , t _f =20 ns, V _C =V _{DD} -V _{SS} (Square Wave)				75
					mV (Peak)

• Peak-to-peak voltage symmetrical about $\frac{V_{DD}-V_{SS}}{2}$.

▲ Worst case.

* Both ends of channel.

TEST CIRCUITS (Cont'd)

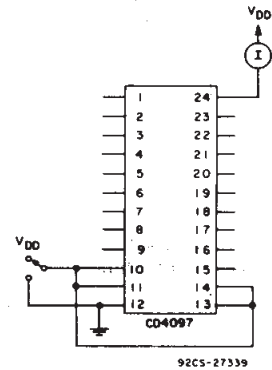
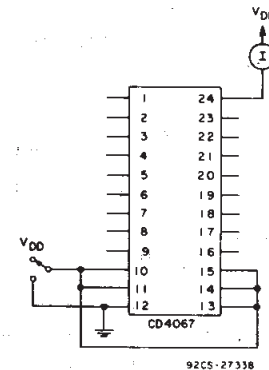


Fig. 10—Quiescent device current.

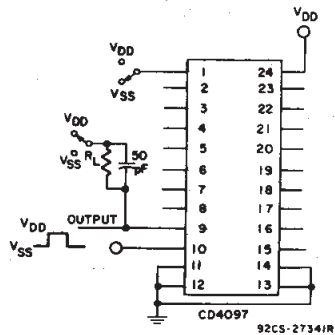
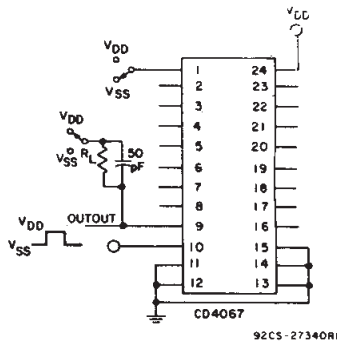


Fig. 11—Turn-on and turn-off propagation delay—address select input to signal output (e.g. measured on channel 0).

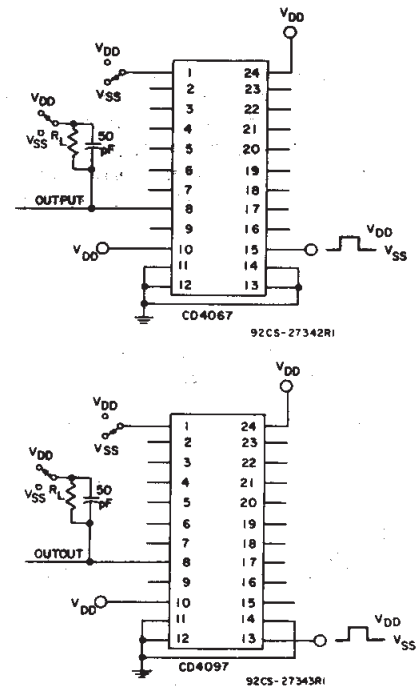


Fig. 12—Turn-on and turn-off propagation delay—inhibit input to signal output (e.g. measured on channel 1).

CD4067B, CD4097B Types

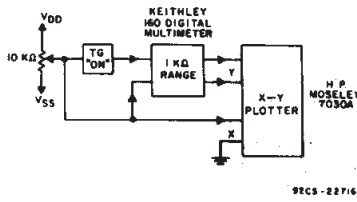


Fig. 13- Channel ON resistance measurement circuit.

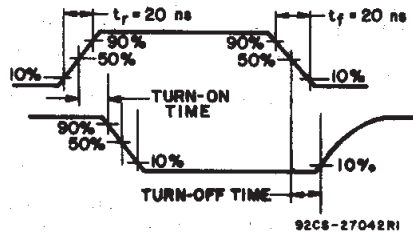


Fig. 14- Propagation delay waveform channel being turned ON ($R_L = 10\text{ K}\Omega$, $C_L = 50\text{ pF}$).

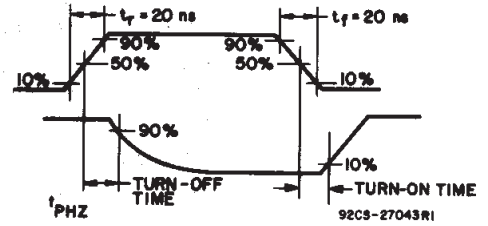


Fig. 15- Propagation delay waveform, channel being turned OFF ($R_L = 300\Omega$, $C_L = 50\text{ pF}$).

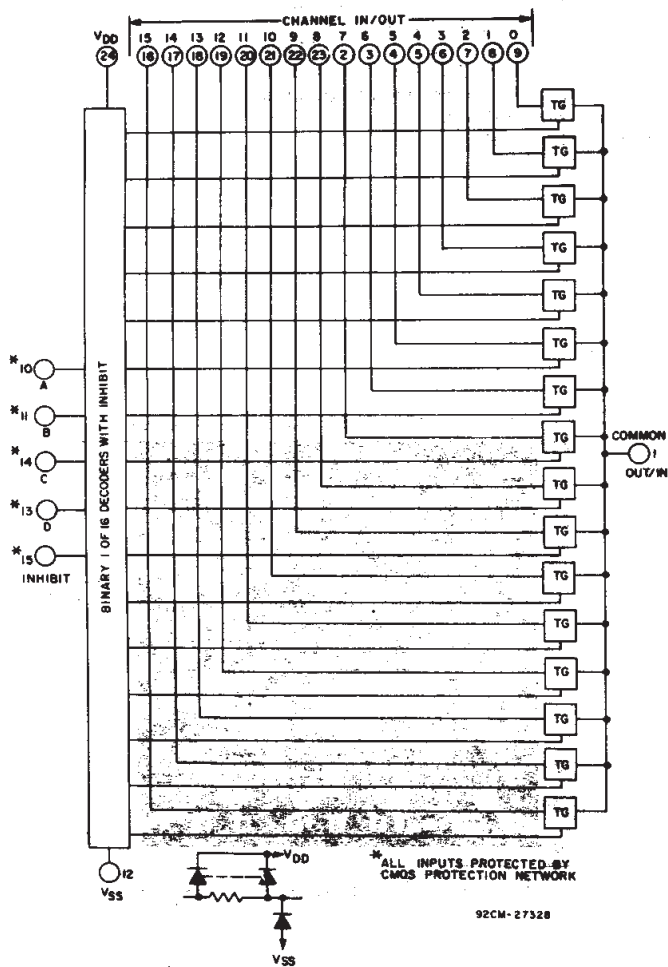


Fig. 16- CD4067 logic diagram.

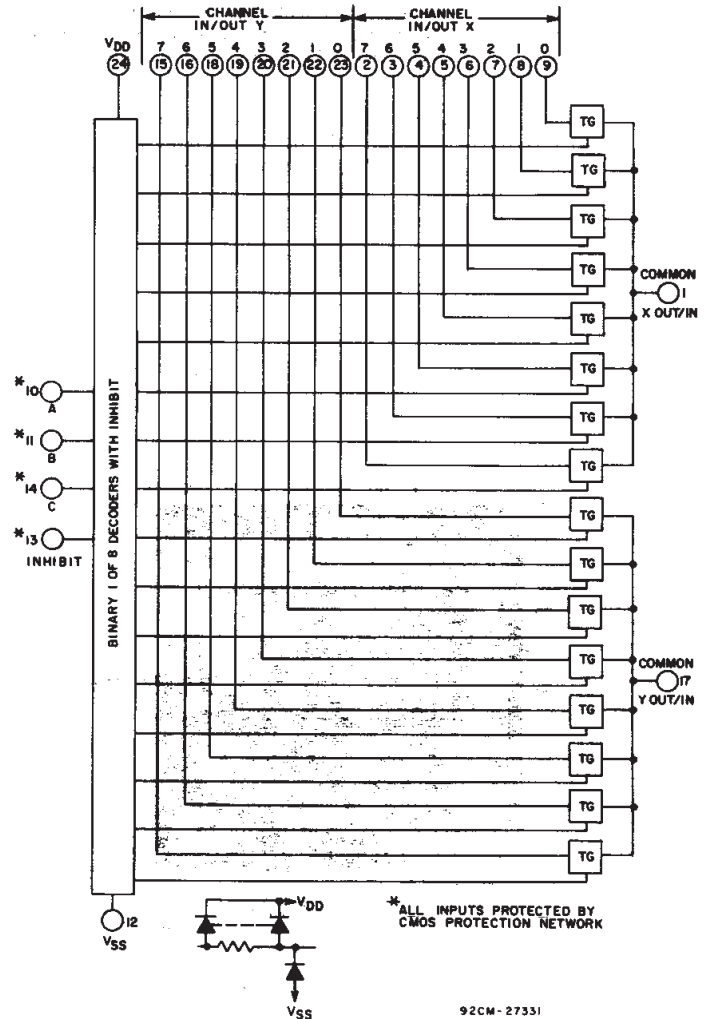


Fig. 17- CD4097 logic diagram.

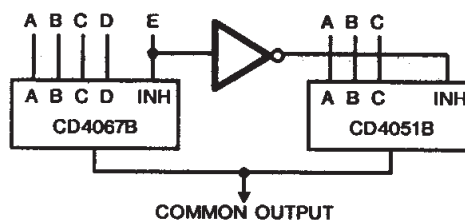


Fig. 18-24-to-1 MUX Addressing

CD4067B, CD4097B Types

SPECIAL CONSIDERATIONS

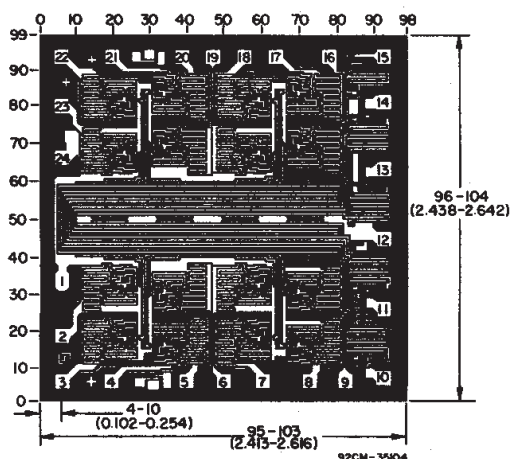
In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L =effective external load). This provision avoids permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4067B or CD4097B.

When switching from one address to another, some of the ON periods of the channels of the multiplexers will overlap momentarily, which may be objectionable in certain applications. Also when a channel is turned on or off by an address input, there is a momentary conductive path from the channel to V_{SS} , which will dump some charge from any capacitor connected to the input or output of the channel. The inhibit input turning on a channel will similarly dump some charge to V_{SS} .

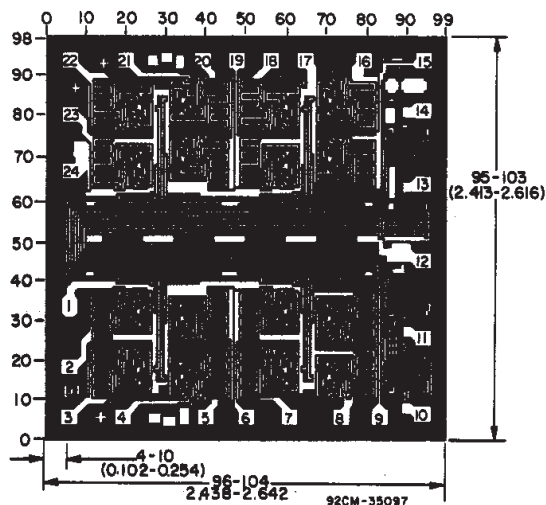
The amount of charge dumped is mostly a function of the signal level above V_{SS} . Typically, at $V_{DD}-V_{SS}=10$ V, a 100-pF

capacitor connected to the input or output of the channel will lose 3-4% of its voltage at the moment the channel turns on or off. This loss of voltage is essentially independent of the address or inhibit signal transition time, if the transition time is less than 1-2 μ s. When the inhibit signal turns a channel off, there is no charge dumping to V_{SS} . Rather, there is a slight rise in the channel voltage level (65 mV typ.) due to capacitive coupling from inhibit input to channel input or output. Address inputs also couple some voltage steps onto the channel signal levels.

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into terminal 1 on the CD4067B, terminals 1 and 17 on the CD4097B.



Dimensions and pad layout for CD4067BH.



Dimensions and pad layout for CD4097BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD4067BE	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4067BEE4	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4067BF	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type
CD4067BF3A	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type
CD4067BM	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4067BM96	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4067BM96E4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4067BM96G4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4067BME4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4067BMG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4067BPW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4067BPWE4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4067BPWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4097BE	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4097BEE4	ACTIVE	PDIP	N	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4097BF	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type
CD4097BM	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4097BM96	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4097BM96E4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4097BM96G4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4097BME4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4097BMG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4097BPW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4097BPWE4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4097BPWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4097BPWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD4097BPWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4097BPWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4067BM96	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CD4097BM96	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CD4097BPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

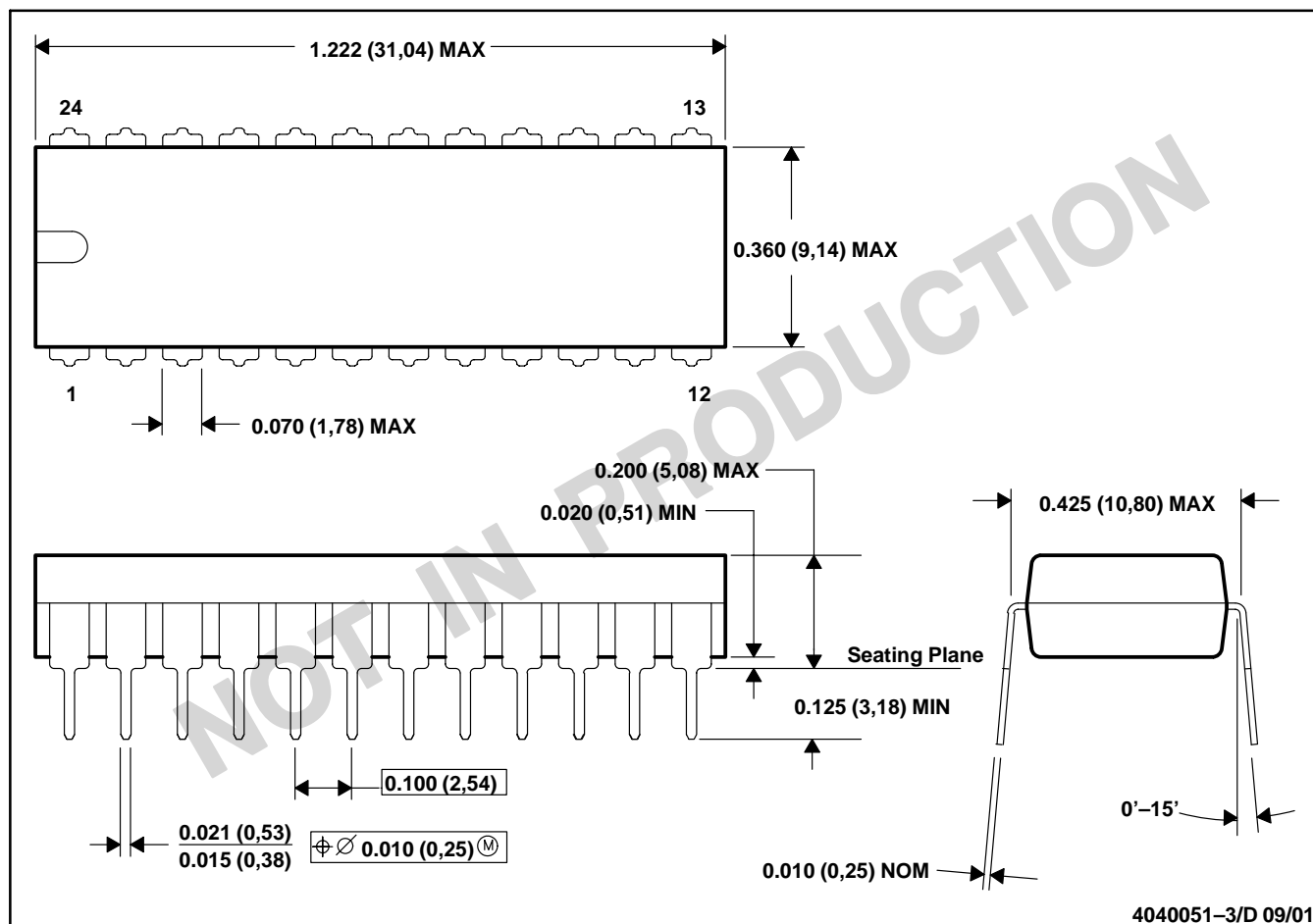


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4067BM96	SOIC	DW	24	2000	346.0	346.0	41.0
CD4097BM96	SOIC	DW	24	2000	346.0	346.0	41.0
CD4097BPWR	TSSOP	PW	24	2000	346.0	346.0	33.0

N (R-PDIP-T24)

PLASTIC DUAL-IN-LINE

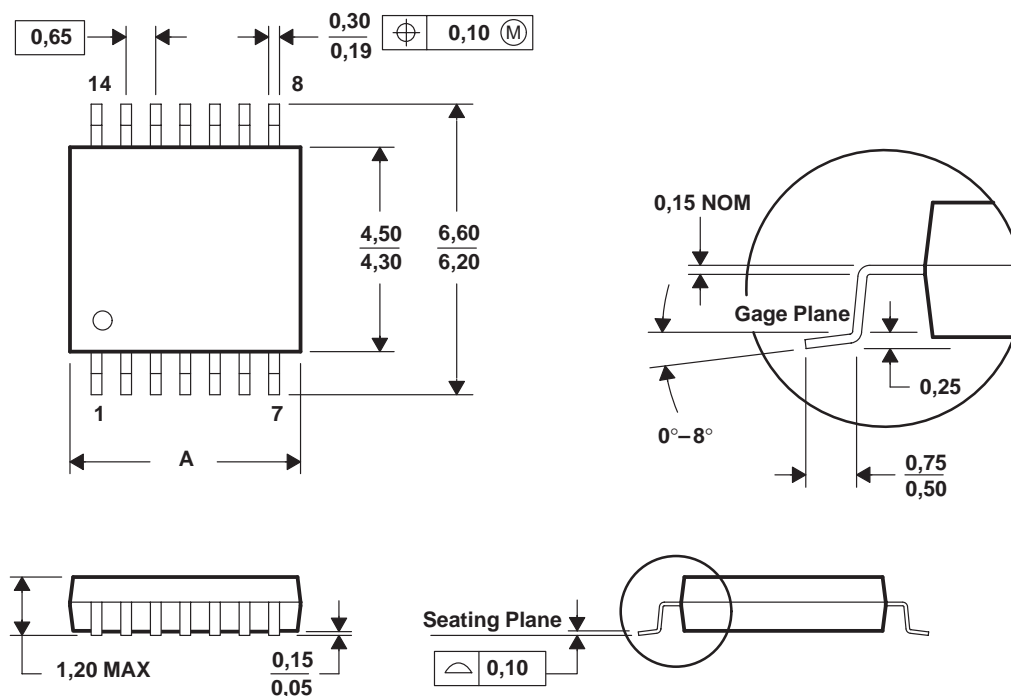


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-010

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

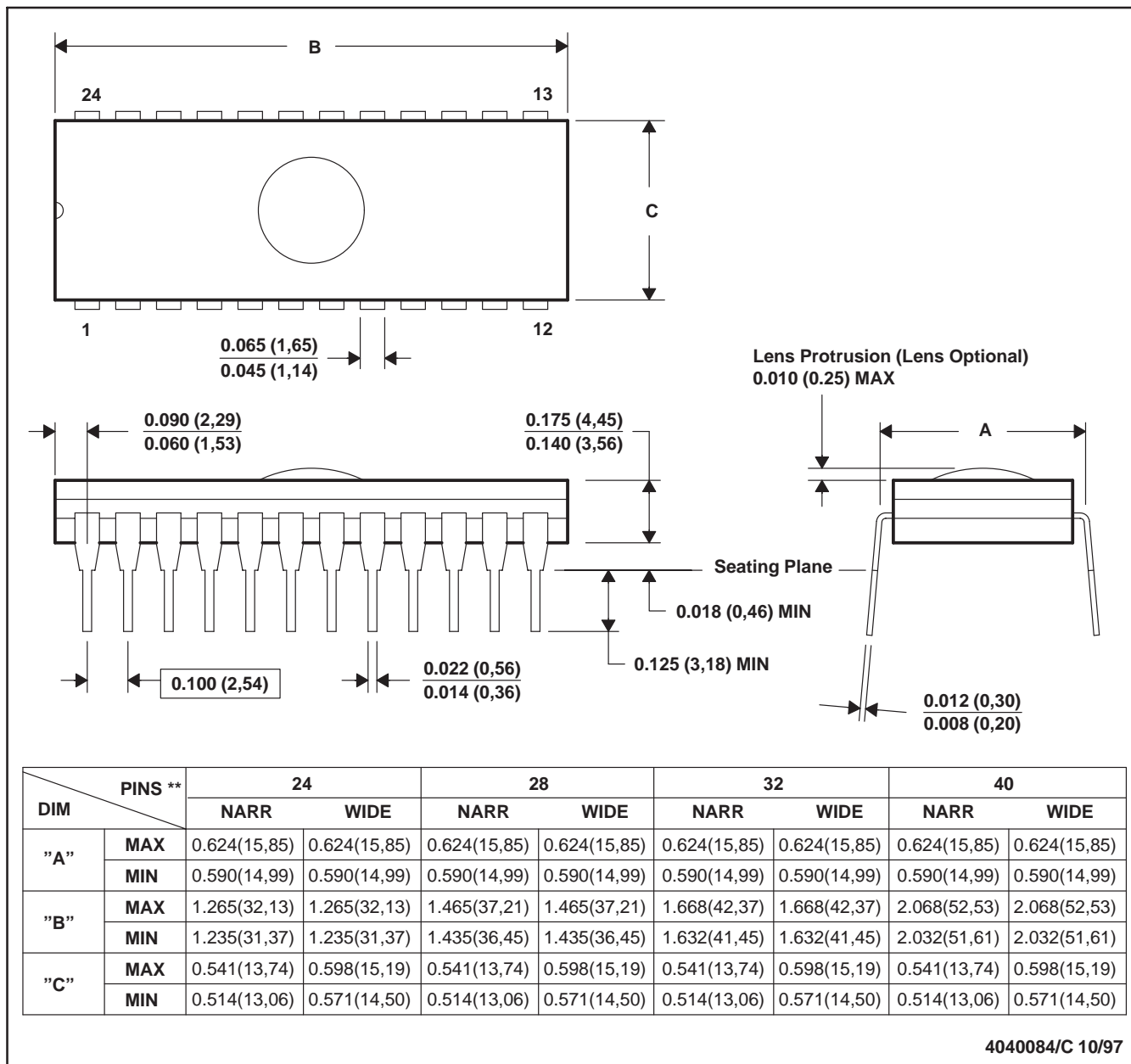
14 PINS SHOWN



PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

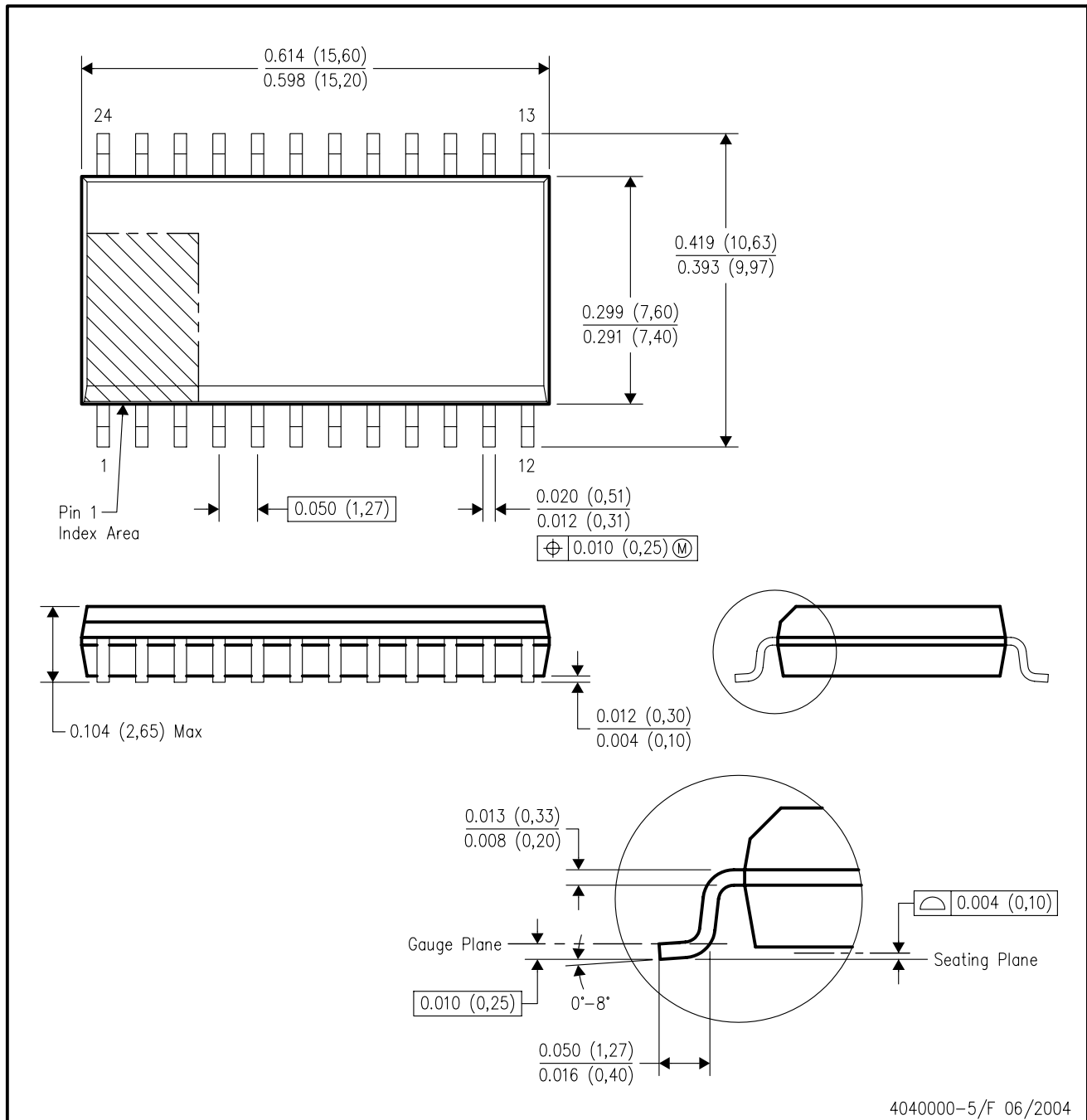
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

J (R-GDIP-T)****CERAMIC DUAL-IN-LINE PACKAGE****24 PINS SHOWN**

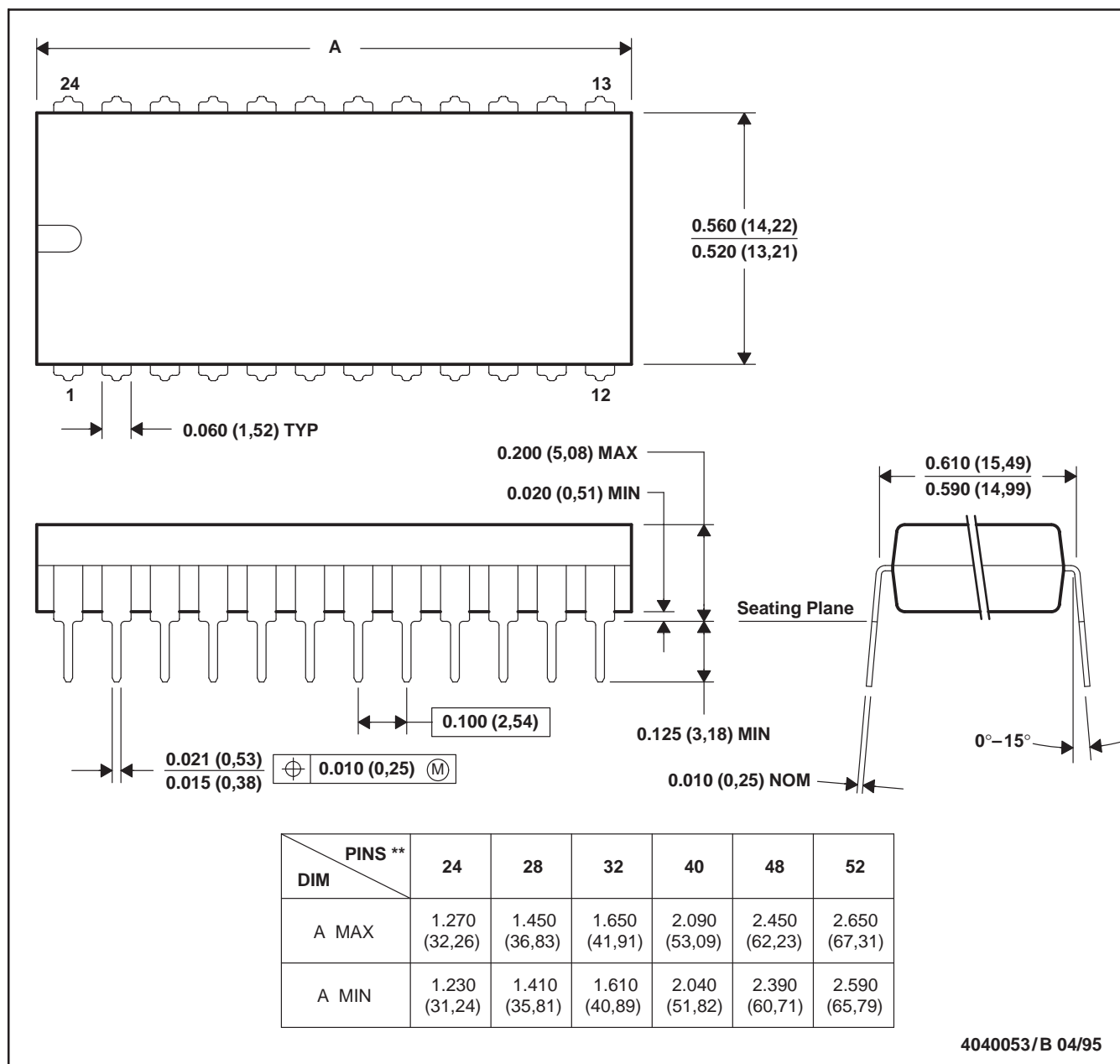
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).
 D. This package can be hermetically sealed with a ceramic lid using glass frit.
 E. Index point is provided on cap for terminal identification.

DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

N (R-PDIP-T)****PLASTIC DUAL-IN-LINE PACKAGE****24 PIN SHOWN**

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-011
 D. Falls within JEDEC MS-015 (32 pin only)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2009, Texas Instruments Incorporated