1 Register Description

1.1 COMMON BANK

1.1.1 WHO_AM_I

REG Name	WHO_AM_I: Device Identifier							
REG Address	Bank COMMON - 0x20 (Hex) - 32 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-10110001							
Content	WHOAMI							

Description

Device Identifier register. This number uniquely identifies the device type.

Parameters

- **WHOAMI**: Device Identifier 0xB1 (Hex)

1.1.2 BANK_SELECT

REG Name	BANK_SELECT: Bank Selector							
REG Address	Bank COMMON - 0x21 (Hex) - 33 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-0000				RW-0000			
Content	RFU				BANK_SEL			

Description

User Bank selection register. It is used to have at any time 32 locations available for read and write operations, although more than 32 registers are available. The locations from 0x20 up to 0x3F (Common Bank) are always available, while locations from 0x00 to to 0x1F can be selected using the BANK_SEL parameter.

Parameters

- **BANK_SEL**: These four bits allow addressing 16 different pages of register other than the common bank. Page size is of 32 byte. Default bank is the user (0h) bank. Valid Combinations are:

0000 -> Bank 0 (User bank)
0001 -> Bank 1 (Interrupt bank)
Banks beyond Bank 1 are reserved.

1.1.3 SYSTEM_STATUS

REG Name	**SYSTEM_STATUS: System Status**							
REG Address	Bank COMMON - 0x22 (Hex) - 34 (Dec)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Type - Def. Value	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
Content	RFU						DR_ERROR	DATA_READY

Description

This is the System Status register. It reports two fundamental flags necessary to properly manage the communication with the MAX21000. Ideally, every new data-reading operation from the MAX21000 should only take place when at least a new DATA_READY event has occurred. Failure to have a data reading every DATA_READY may result in either reading twice the same data or missing the data. That is particularly true when the FIFO is disabled.
The DR_ERR flag indicates the occurence of either one of the events described above.
If the FIFO is used, multiple data can be read safely, according to the FIFO_COUNT (0x3C) register, even though many DATA_READY have been generated.
The way the DATA_READY flag is reset can be configured using register DR_CFG (0x13).
Bits[7:3] are reserved.

Parameters

- **DR_ERROR**: This bit goes high when a new data is generated before or during data reading
- **DATA_READY**: DATA_READY flag: it goes high when a new set of gyroscope data is available

1.1.4 GYRO_X_H

REG Name	**GYRO_X_H: Gyro Data, X-axis, MSB**							
REG Address	Bank COMMON - 0x23 (Hex) - 35 (Dec)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Type - Def. Value	R-00000000							
Content	GYRO_X_MSB							

Description

This register stores the most recent gyroscope measurement, specifically the MSB of the X-axis.
Gyroscope measurements are written to these registers at the Output Data Rate as defined in Register SENSE_CFG2.
The user is responsible for ensuring a set of single byte reads correspond to a single sampling instant by checking the Data Ready bit, optionally configured as interrupt source..
Each 16-bit gyroscope measurement has a full scale defined in SENSE_CFG0.

Parameters

- **GYRO_X_MSB**: Gyroscope X output (MSBs). These bits become LSBs if Endian bit = 1.

1.1.5 GYRO_X_L

REG Name	**GYRO_X_L: Gyro Data, X-axis, LSB**							
REG Address	Bank COMMON - 0x24 (Hex) - 36 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	GYRO_X_LSB							

Description

LSB of the X-axis. See GYRO_X_H for additional details.

Parameters

- **GYRO_X_LSB**: Gyroscope X output (LSBs). These bits become MSBs if Endian = 1.

1.1.6 GYRO_Y_H

REG Name	**GYRO_Y_H: Gyro Data, Y-axis, MSB**							
REG Address	Bank COMMON - 0x25 (Hex) - 37 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	GYRO_Y_MSB							

Description

MSB of the Y-axis. See GYRO_X_H for additional details.

Parameters

- **GYRO_Y_MSB**: Gyroscope Y output (MSBs). These bits become LSBs if Endian bit = 1.

1.1.7 GYRO_Y_L

REG Name	**GYRO_Y_L: Gyro Data, Y-axis, LSB**							
REG Address	Bank COMMON - 0x26 (Hex) - 38 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	GYRO_Y_LSB							

Description

LSB of the Y-axis. See GYRO_X_H for additional details.

Parameters

- **GYRO_Y_LSB**: Gyroscope Y output (LSBs). These bits become MSBs if Endian bit = 1.

1.1.8 GYRO_Z_H

REG Name	**GYRO_Z_H: Gyro Data, Z-axis, MSB**							
REG Address	Bank COMMON - 0x27 (Hex) - 39 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	GYRO_Z_MSB							

Description

MSB of the Z-axis. See GYRO_X_H for additional details.

Parameters

- **GYRO_Z_MSB**: Gyroscope Z output (MSBs). These bits become LSBs if Endian bit = 1.

1.1.9 GYRO_Z_L

REG Name	**GYRO_Z_L: Gyro Data, Z-axis, LSB**							
REG Address	Bank COMMON - 0x28 (Hex) - 40 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	GYRO_Z_LSB							

Description

LSB of the Z-axis. See GYRO_X_H for additional details.

Parameters

- **GYRO_Z_LSB**: Gyroscope Z output (LSBs).These bits become MSBs if Endian bit = 1.

1.1.10 TEMP_H

REG Name	**TEMP_H: Temperature Sensor, MSB**							
REG Address	Bank COMMON - 0x29 (Hex) - 41 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	TEMP_MSB							

Description

MSB of the temperature sensor. The temperature data is provided as an absolute value expressed in Celsius degrees. The sensitivity is 256 LSB/deg, which means that the TEMP_H registers changes whenever the temperature varies by 1 degree.
Temperature data cannot be read through the FIFO, it must be read using data registers.

Parameters

- **TEMP_MSB**: Temperature sensor output (MSBs). These bits become LSBs if Endian bit = 1.

1.1.11 TEMP_L

REG Name	**TEMP_L: Temperature Sensor, LSB**							
REG Address	Bank COMMON - 0x2A (Hex) - 42 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	TEMP_LSB							

Description

LSB of the temperature sensor. The temperature data is provided as an absolute value expressed in Celsius degrees. The sensitivity is 256 LSB/deg, which means that the TEMP_L registers changes 256 times whenever the temperature varies by 1 degree.
Temperature data cannot be read through the FIFO, it must be read using data registers.

Parameters

- **TEMP_LSB**: Temperature sensor output (LSBs).These bits become MSBs if Endian bit = 1.

1.1.12 HP_RST

REG Name	HP_RST: High Pass filter reset							
REG Address	Bank COMMON - 0x3B (Hex) - 59 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	HP_RESET							

Description

High Pass filter reset register.

Parameters

- **HP_RESET**: Reading this address causes the HP filter to be reset.

1.1.13 FIFO_COUNT

REG Name	FIFO_COUNT: Number of samples available in the FIFO							
REG Address	Bank COMMON - 0x3C (Hex) - 60 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	FIFO_CNT							

Description

FIFO Count Register. This register should be read whenever the FIFO is enabled to make sure that the data read from the FIFO are only valid data. In fact, attention must be paid to the The completed procedure to read data from the FIFO is described in the Programming Examples section.

Parameters

- **FIFO_CNT**: The content of this register is the number of samples available, LSB of number of FIFO words filled (from 0 to 256)

1.1.14 FIFO_STATUS

REG Name	FIFO_STATUS: Status of the FIFO						
REG Address	Bank COMMON - 0x3D (Hex) - 61 (Dec)						
	Bit7	Bit 6:5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-0	R-00	R-0	R-0	R-0	R-0	R-0
Content	FIFO_CNT	RFU	FIFO_WR_FULL	FIFO_ RD_EMPTY	FIFO_TH	FIFO_FULL	FIFO_EMPTY

Description

FIFO status register. This register gathers all the bits defining the status of the FIFO.
Bits [6:5] are unused.

Parameters

- **FIFO_CNT** : the MSB of FIFO words filled (from 0 to 256)
- **FIFO_WR_FULL** : At least one data was written (and lost) whilst the FIFO was full
- **FIFO_ RD_EMPTY** : At least one read has occurred whilst the FIFO was empty
- **FIFO_TH** : The FIFO contains data above the threshold
- **FIFO_FULL** : The FIFO is full
- **FIFO_EMPTY** : The FIFO is empty

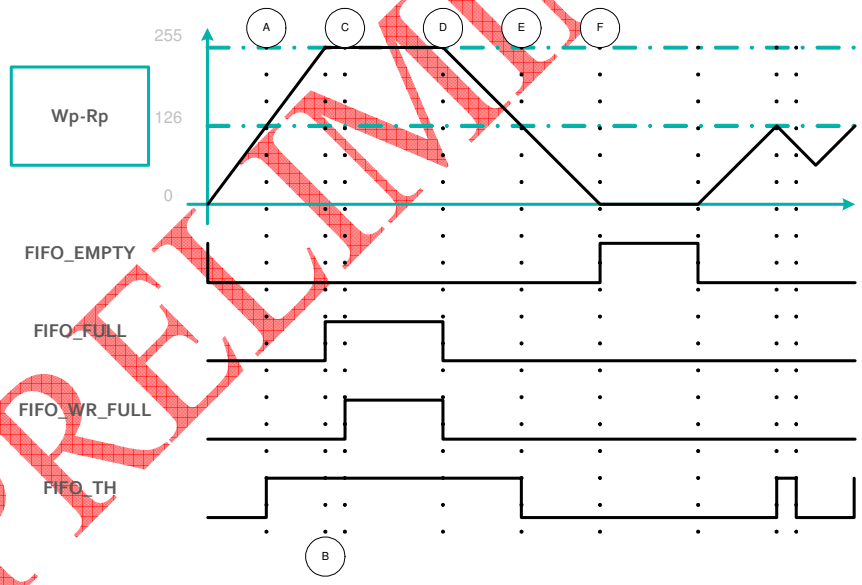

Figure 1: FIFO Flags

A) The difference between the Write Pointer and the Read Pointer reaches the programmed threshold
B) FIFO is full, next write operation will cause data to be lost
C) At least one data has been lost
D) Read access clears FIFO_FULL and FIFO_WR_FULL flags
E) Wp-Rp < programmed threshold
F) FIFO is empty: all the available new data have been read

1.1.15 FIFO_DATA

REG Name	FIFO_DATA: Gyroscope data available through the FIFO							
REG Address	Bank COMMON - 0x3E (Hex) - 62 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	FIFO_DAT							

Description

This register is used to read and write data from the FIFO buffer.

The contents of the sensor data registers are written into the FIFO buffer when their corresponding FIFO enable flags are set to 1 in FIFO_EN .

If the FIFO buffer has overflowed, the status bit **FIFO_WR_FULL** is automatically set to 1. This bit is located in the FIFO_STATUS (0x3D) register. When the FIFO buffer has overflowed, the oldest data will be lost and new data will be written to the FIFO if the override bit is set in the FIFO_CFG (0x18) register .

If the FIFO buffer is empty, reading this register will return the last byte that was previously read from the FIFO until new data is available. The user should check FIFO_COUNT (0x3C) to ensure that the FIFO buffer is not read when empty.

Parameters

- **FIFO_DAT**: When FIFO is enabled reading this address with burst reading all the data stored in the FIFO are readable.
  Burst reading allows FIFO address to increment and the FIFO memory to be scrolled

1.1.16 PAR_RST

REG Name	**PAR_RST: Parity Reset register**							
REG Address	Bank COMMON - 0x3F (Hex) - 63 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	PARITY_RST							

Description

Parity Reset Register.

Parameters

- **PARITY_RST**: Reading this register clears the parity error flag (ITF_OTP[1]).

1.2 USER BANK #0 (Bank_sel = 0000)

1.2.1 POWER_CFG

REG Name	**POWER_CFG: Power Configuration**							
REG Address	Bank 0 - 0x00 (Hex) - 0 (Dec)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Type - Def. Value	RW-00		RW-000			RW-1	RW-1	RW-1
Content	FS		PW			EN_Z_RATE	EN_Y_RATE	EN_X_RATE

Description

Full Scale, Power Mode and axes configuration register.

Parameters

- **FS**: Full scale configuration bits:

Table 1: Full Scale configuration

OIS_FS	FS	full scale
0	00	2000 dps (default)
0	01	1000 dps
0	10	500 dps
0	11	250 dps
1	00	250 dps (default when OIS=1)
1	01	125 dps
1	10	62.5 dps
1	11	31.25 dps

- **PWR_MODE**: configuration of the power mode of the:

Table 2: Power Mode Configuration

PWR_MODE(bit field)	DSYNC (pin)	Power Mode
000	X	Power Down
001	X	Normal
010	X	Standby
011	X	ECO
100	0	Standby
100	1	ECO
101	0	Power Down
101	1	ECO
110	0	Standby
110	1	Normal
111	0	Power Down
111	1	Normal

- **EN_Z_RATE**: Z direction enable bit . '1' means enabled.
- **EN_Y_RATE**: Y direction enable bit . '1' means enabled.
- **EN_X_RATE**: X direction enable bit . '1' means enabled.

1.2.2 SENSE_CFG1

REG Name	SENSE_CFG1: Sensing chain configuration register #1							
REG Address	Bank 0 - 0x01 (Hex) - 1 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00		RW-1010				RW-0	RW-0
Content	SELF_TEST		BW				RFU	OIS_FS

Description

Low Pass filter, OIS and Self Test configuration register.

Parameters

- **SELF_TEST** : Bit 6 is used to activate the self-test mode. When activated, an offset is generated on the digital output whose amount depends on the full scale selected. Bit 7 can be used to invert the sign of the self-test output. The output of this parameter is affected by a strong spread, in the order of +/- 50%. This test allows detecting both electrical and mechanical issues. The table below summarizes the expected values.

Table 3: Self-Test Output

Axis	FS= 2000	FS= 1000	FS=500	FS=250
X[dps]	450	225	110	55
Y[dps]	-450	-225	-110	-55
Z[dps]	450	225	110	55

- **SNS_LPF_BND**: Output bandwidth selection bits

Table 4: Bandwidth configuration

BW	bandwidth
0	2Hz
1	4Hz
2	6Hz
3	8Hz
4	10Hz
5	14Hz
6	22Hz
7	32Hz
8	50Hz
9	75Hz
10	100Hz (default)
11	150Hz
12	200Hz
13	250Hz
14	300Hz
15	400Hz

- **OIS_FS**: Full scale for OIS applications

0: normal full scale (from 250 to 2000 dps)
1: OIS full scale (from 31.25 to 250 dps)

1.2.3 SENSE_CFG2

REG Name	**SENSE_CFG2: Sensing chain configuration register #2**							
REG Address	Bank 0 - 0x02 (Hex) - 2 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00010011							
Content	ODR							

Description

Output Data Rate configuration register. This register selects the preferred Output Data Rate (ODR) according to the description that follows.

When it ECO mode, the two least significant bits are used to configure the ODR.

Parameters

- **SNS_ODR**

ODR = 10kHz/(n+1) for n=0..99 (100Hz<=ODR<=10kHz)
ODR = 10kHz/(100+5*(n-99)) for n=100..179 (20Hz<=ODR<100Hz)
ODR = 10kHz / (500+20*(n-179)) for n=180..255 (4.95Hz<=ODR<20Hz)

In ECO mode:
ODR[1:0] = 00 ODR = 200Hz
ODR[1:0] = 01 ODR = 100Hz
ODR[1:0] = 10 ODR = 50Hz
ODR[1:0] = 11 ODR = 25Hz

1.2.4 SENSE_CFG3

REG Name	SENSE_CFG3: Sensing chain configuration register #3							
REG Address	Bank 0 - 0x03 (Hex) - 3 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00		RW-00		RW-0000			
Content	RFU		SRC_CFG		HP_CUT			

Description

High Pass filter configuration register.
This register comprises 2 fields. The 4 LSBs can be used to select the cut-off frequency of the high-pass filter.
Bit [5:4] are used to activate/de-activate the high pass filter and to optionally force the ODR at the highest rate, disregarding the ODR settings .

Bits [7:6] are reserved.

Parameters

- **SRC_CFG**: Output data can be chosen as follow:

00 -> data at ODR without hi-pass filtering
01 -> data at ODR with hi-pass filtering
10 -> data at 10k without hi-pass filtering
11 -> data at 10k with hi-pass filtering

- **SNS_HPF_CO**: Configuration for the HP filter cutoff frequency:

Table 5: High Pass Filter configuration

HP_CUT	bandwidth
0	0.1Hz (default)
1	0.2Hz
2	0.3Hz
3	0.5Hz
4	0.7Hz
5	1.0Hz
6	1.7Hz
7	3.0Hz
8	4.5Hz
9	7.0Hz
10	11Hz
11	17Hz
12	26Hz
13	40Hz
14	64Hz
15	100Hz

1.2.5 DR_CFG

REG Name	DR_CFG: Data Ready Configuration							
REG Address	Bank 0 - 0x13 (Hex) - 19 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00		RW-00		R-00		RW-0	RW-1
Content	RFU		DR_RST_MODE		RFU		COARSE_TEMP	TEMP_EN

Description

Data Ready configuration register.
Bits [7:6] and [3:2] are reserved.

Parameters

- **DR_RST_MODE**: These bits control the way the DATA_READY is reset and the way the data are updated. 3 available modes:

00 : ALL - DATA_READY is cleared when all the active channels are read.
Data Set is updated only when all the data are read

01 : ANY - DATA_READY is cleared when at least one half active channel is read.
Data Set is not guaranteed because data can be updated immediately

10: STATUS - DATA_READY is cleared when status register is read.
Data Set is maintained until status register is read.

- **COARSE_TEMP** : '0' is fine, '1' is for coarse. If "fine", temperature data is updated only when both bytes are read. If "coarse", reading MSB enables the data update.
- **TEMP_EN** **:** Enable (1) or Disable (0) the temperature sensor

1.2.6 IO_CFG

REG Name	**IO_CFG: Input/output Configuration**							
REG Address	Bank 0 - 0x14 (Hex) - 20 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
Content	DSYNC_PD_EN	DSYNC_PU_EN	INT1_PD_EN	INT1_PU_EN	INT2_PD_EN	INT2_PU_EN	SCL_PU_DIS	SDA_PU_DIS

Description

I/O configuration Register. This register controls the pull-up and pull-down resistors of the pins DSYNC, INT1 and INT2.
Bit [1: 0] are reserved.

Parameters

- **DSYNC_PD_EN**: When 1, the internal pull down of the pad is connected
- **DSYNC_PU_EN**: When 1, the internal pull up of the pad is connected
- **INT1_PD_EN**: When 1, the internal pull down of the pad is connected
- **INT1_PU_EN**: When 1, the internal pull up of the pad is connected
- **INT2_PD_EN**: When 1, the internal pull down of the pad is connected
- **INT2_PU_EN**: When 1, the internal pull up of the pad is connected
- **SCL_PU_DIS**: When 0, the internal pull up of the SCL pad is connected
- **SDA_PU_DIS**: When 0, the internal pull up of the SDA pad is connected

1.2.7 I2C_CFG

REG Name	**I2C_CFG: I2C Configuration**							
REG Address	Bank 0 - 0x15 (Hex) - 21 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-0	RW-000			RW-01		RW-0	RW-0
Content	RFU	I2C_SETTING			DRIVE		RFU	I2C_OFF

Description

I2C configuration register.
Bit 7 and 1 are reserved.

Parameters

- **I2C_SETTING**:
  000 -> I2C Fast Mode without anti-spike filter
  001 -> I2C Fast Mode standard configuration
  010 -> I2C High Speed standard configuration
  011 -> I2C High Speed without anti-spike filter
  100 -> I2C Fast Mode without filters and delays
  101 -> SPI interface recommended
  110 -> Reserved for future use
  111 -> Reserved for future use
- **DRIVE_1, DRIVE_0** Change the current of the pad according to the following table:

Table 6: I/O Current Configuration

DRIVE		IOs Output Current [mA]
0	0	3
0	1	6
1	0	6
1	1	12

- **I2C_OFF**: This bit is used for turn off the I2C interface. By default I2C is active. Setting to 1 this bit I2C is turned off. It may be used when connecting several SPI devices in parallel.

1.2.8 ITF_OTP

REG Name	ITF_OTP: Interface and OTP control							
REG Address	Bank 0 - 0x16 (Hex) - 22 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-0	R-0	RW-0	RW-00		RW-0	R-0	RW-0
Content	RFU	PARITY_ERROR	SPI_3_WIRE	IF_PARITY		ENDIAN	MEMORY_RUNNING	RESTART

Description

Interface and OTP configuration register

Parameters

- **PARITY_ERROR**: Error in SPI/I2C address
- **SPI_3_WIRE** : 3 or 4 wires SPI mode. When set SPI 3 wire is enabled
- **IF_PARITY** : Interface bit 6 configuration bits:
  00 -> bit 6 of the register address is used for auto increment mode (default)
  01 -> bit 6 of the register address represents the even parity bit
  10 -> bit 6 of the register address represents the odd parity bit
- **ENDIAN**: Big little endian configuration bit.
  - 0 is for big endian (MS Byte, LS Byte),
  - 1 for little (LS Byte, MS Byte)

- **MEMORY_RUNNING**: Flag indicating that the OTP is being downloaded
- **RESTART** : Command to reload the OTP trimming values: set it to '1' to start. It automatically reverts to 0 immediately after write. Use memory_running flag to understand when OTP downloading is done.

Note: when IF_PARITY != 0, then the burst is auto-incremental by default.

Note: ENDIAN bit only affects the way data are stored into the registers, not the way data are saved into the FIFO.

1.2.9 FIFO_TH

REG Name	**FIFO_TH: FIFO threshold for the interrupt generation**							
REG Address	Bank 0 - 0x17 (Hex) - 23 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00000000							
Content	FIFO_SAMPLES							

Description

FIFO Threshold configuration register. This register defines the number of samples that should be used as threshold to set the FIFO_OVTHOLD bit

Parameters

- **FIFO_SAMPLES**: When the number of samples yet to be read stored in FIFO crosses this number, an interrupt is generated on FIFO_OVTHOLD

Note: This parameter specifies the number of Gyroscope output samples expressed in words (16-bit OR 2 bytes). It does not refer to one single axis but to the overall number of samples coming from entire set the selected axis.

1.2.10 FIFO_CFG

REG Name	**FIFO_CFG: FIFO configuration bits**						
REG Address	Bank 0 - 0x18 (Hex) - 24 (Dec)						
	Bit 7:6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
Content	FIFO_MODE	FIFO_INT_SEL	FIFO_OVERRUN	FIFO_STORE_TEMP	FIFO_STORE_Z	FIFO_STORE_Y	FIFO_STORE_X

Description

FIFO configuration register. This register determines which sensor measurements are loaded into the FIFO buffer and selects the desired FIFO behavior.
Data stored inside the sensor data registers will be loaded into the FIFO buffer if a sensor's respective FIFO_store bit is set to 1 in this register. The behavior of FIFO writes when the FIFO buffer is full can be configured with the FIFO_MODE bit. In order to read the data in the FIFO buffer, the FIFO_MODE must be set to a value >0.
When the FIFO_STORE_{X,Y,Z} bit is enabled in this register, data will be loaded into the FIFO buffer for the corresponding axis.
The sensors are written into the FIFO at the Output Data Rate defined in Register 0x02.
For further information regarding sensor data registers, please refer to Registers 0x23 to 0x28.

Parameters

- **FIFO_MODE**: These bits are used to configure the FIFO mode:

00 -> OFF
01 -> NORMAL
10 -> INTERRUPT
11 -> SNAPSHOT

- **FIFO_INT_SEL**: When an interrupt mode is selected, this bits define which kind of mask must be used:

0: use OR mask
1: use AND mask

- **FIFO_OVERRUN**: When set to TRUE, FIFO data are overwritten and oldest are lost. When FALSE, FIFO is a buffer that stops when full
- **FIFO_STORE_TEMP**: When set to TRUE, 16-bits temperature data is stored in FIFO
- **FIFO_STORE_Z**: When set to TRUE, 16-bits Z direction data is stored in FIFO
- **FIFO_STORE_Y**: When set to TRUE, 16-bits Y direction data is stored in FIFO
- **FIFO_STORE_X**: When set to TRUE, 16-bits X direction data is stored in FIFO

1.2.11 DSYNC_CFG

REG Name	**DSYNC_CFG: DSYNC Configuration**						
REG Address	Bank 0 - 0x1A (Hex) – 26 (Dec)						
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	2:1	0
Type - Def. Value	RW-0	RW-0	RW-0	RW-0	RW-0	R-00	RW-0
Content	DSQ_ENR	DSQ_ENF	DSW_EDG	DSW_LOW	DSM_ENB	RFU	DS_TEMP

Description

DSYNC configuration register. This register has to be used to configure the way the MAX21000 manages events occurring on the DSYNC pin. Multiple different actions can be taken simultaneously, like changing the power mode, mapping the DSYNC pin value onto the gyroscope LSB data and concurrently triggering the capture of new data.
When the DSYNC pin is configured as active on edge and a dynamic power mode is configured, only the active edge determines the transition. The opposite transition must be done wither in SW or by reversing the active edge.
Bit 0 is reserved.

Parameters

- **DSQ_ENR**: When 1, enable data queuing with DSYNC rising
- **DSQ_ENF**: When 1, enable data queuing with DSYNC falling
- **DSW_EDG**: When 1, DSYNC is an active on edge. When 0, DSYNC is an active on level
- **DSW_LOW**: When 1, DSYNC is an active low level control to wake up. When 0, DSYNC is an active high level to wake up. This bit affects both the edge and the level modes.
- **DSM_ENB**: When 1, the DSYNC signal is mapped onto the Gyro LSB
- **DS_TEMP:** **When 1, the DSYNC signal is mapped onto the temperature LSB.**

1.2.12 DSYNC_CNT

REG Name	**DSYNC_CNT: DSYNC Counter**
REG Address	Bank - 0x1B (Hex) – 27 (Dec)
	Bit 7:0
Type - Def. Value	RW-00000000
Content	DSYNC_COUNTER

Description

DSYNC counter configuration register. This register can be used to track the evolution of the rate signal from the gyroscope immediately after an external event captured on the DSYNC pin.

Parameters

- **DSYNC_COUNTER**: This register specifies the number of samples to be stored into the FIFO upon detecting a DSYNC active edge

1.3 USER BANK #1 (Bank_sel = 0001)

1.3.1 INT_REF_X

REG Name	**INT_REF_X: Interrupt Reference for X-axis, MSB**							
REG Address	Bank 1 - 0x00 (Hex) - 0 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00000000							
Content	INT_REF_X							

Description

Rate Interrupt Reference, X-axis.

Parameters

- **INT_REF_X**: These are the 8 MSB of the reference for interrupt of X direction. 8 LSB are assumed = 0x00. If INT_SINGLE_REF = '1', then the reference is { INT_REF_X, INT_REF_Y }, with **INT_REF_X** used as MSB and **INT_REF_Y** used as LSB.

1.3.2 INT_REF_Y

REG Name	**INT_REF_Y: Interrupt Reference for Y-axis, MSB**							
REG Address	Bank 1- 0x01 (Hex) - 1 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00000000							
Content	INT_REF_Y							

Description

Rate Interrupt Reference, Y-axis.

Parameters

- **INT_REF_Y**: These are the 8 MSB of the reference for interrupt of Y direction. 8 LSB are assumed = 0x00. If INT_SINGLE_REF = '1', then the reference is {INT_REF_X, INT_REF_Y}, with **INT_REF_X** as MSB and **INT_REF_Y** as LSB.

1.3.3 INT_REF_Z

REG Name	**INT_REF_Z: Interrupt Reference for Z-axis, MSB**							
REG Address	Bank 1- 0x02 (Hex) - 2 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00000000							
Content	INT_REF_Z							

Description

Rate Interrupt Reference, Z-axis.

Parameters

- **INT_REF_Z**: These are the 8 MSB of the reference for interrupt of Z direction. 8 LSB are assumed = 0x00. If INT_SINGLE_REF = '1' the reference is {INT_REF_X, INT_REF_Y}, with **INT_REF_X** used as MSB and **INT_REF_Y** used as LSB.

1.3.4 INT_DEB_X

REG Name	**INT_DEB_X: Interrupt Debounce on X-axis**							
REG Address	Bank 1- 0x03(Hex) - 3 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00000000							
Content	INT_DEB_X							

Description

Rate Interrupt debounce register on X-axis.
This register determines how long (measured in number of samples) the selected AND/OR rate interrupt configuration has to stay asserted before the corresponding interrupt source bit is set and the interrupt on either INT1 or INT2 is eventually generated.
When the selected AND/OR rate interrupt configuration de-asserts (goes to 0) the corresponding interrupt source bit de-asserts immediately, without debounce.

Parameters

- **INT_DEB_X**: This register allows to count the number of samples (@ODR) requested to generate the rate interrupt signal for the X direction.

1.3.5 INT_DEB_Y

REG Name	**INT_DEB_Y: Interrupt Debounce on Y-axis**							
REG Address	Bank - 0x04 (Hex) - 4 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00000000							
Content	INT_DEB_Y							

Description

Rate Interrupt debounce register on Y-axis.
This register determines how long (measured in number of samples) the selected AND/OR rate interrupt configuration has to stay asserted before the corresponding interrupt source bit is set and the interrupt on either INT1 or INT2 is eventually generated.
When the selected AND/OR rate interrupt configuration de-asserts (goes to 0) the corresponding interrupt source bit de-asserts immediately, without debounce

Parameters

- **INT_DEB_Y**: This register allows to count the number of samples (@ODR) requested to generate the interrupt signal for the Y direction.

1.3.6 INT_DEB_Z

REG Name	**INT_DEB_Z: Interrupt Debounce on Z-axis**							
REG Address	Bank 1- 0x05 (Hex) - 5 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00000000							
Content	INT_DEB_Z							

Description

Rate Interrupt debounce register on Z-axis.

This register determines how long (measured in number of samples) the selected AND/OR rate interrupt configuration has to stay asserted before the corresponding interrupt source bit is set and the interrupt on either INT1 or INT2 is eventually generated.

When the selected AND/OR rate interrupt configuration de-asserts (goes to 0) the corresponding interrupt source bit de-asserts immediately, without debounce

Parameters

- **INT_DEB_Z**: This register allows to count the number of sample s(@ODR) requested to generate the interrupt signal for the Z direction. If INT_SINGLE_DEB = '1' the debounce is {INT_DEB_X, INT_DEB_Y}, with INT_DEB_X used as MSB and INT_DEB_Y used as LSB.

1.3.7 INT_MSK_X

REG Name	INT_MSK_X: Interrupt Mask X-axis				
REG Address	Bank 1- 0x06 (Hex) - 6 (Dec)				
	Bit 7:4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-0000	R-0	R-0	R-0	R-0
Content	INT_MASK_X	X_HIGH_POS	X_LOW_POS	X_HIGH_NEG	X_LOW_NEG

Description

Rate Interrupt, X-axis configuration register.
This register comprises 2 fields. The 4 LSBs are read-only one-hot encoded bits which indicate whether the rate is positive or negative and whether it is above or below the rate threshold.
The 4 MSBs are writable bits which enable, when set to 1, the generation of interrupts based on configurable AND/OR combination of some of them.

Parameters

- **INT_MASK_X**: For each bit, enables ('1') or disables ('0') the interrupt generation for the threshold event detection on the X-axis.
  - Bit4: enable ('1')/ disable ('0') the event X_LOW_NEG.
  - Bit5: enable ('1')/ disable ('0') the event X_HIGH_NEG.
  - Bit6: enable ('1')/ disable ('0') the event X_LOW_POS.
  - Bit7: enable ('1')/ disable ('0') the event X_HIGH_POS.

For example, writing INT_MASK_X = 4'b0100 enables the condition with X_LOW_POS only active to generate an interrupt.

- **X_HIGH_POS:** Signal is positive, above threshold
- **X_LOW_POS:** Signal is positive, below threshold
- **X_HIGH_NEG:** Signal is negative, above threshold
- **X_LOW_NEG:** Signal is negative, below threshold

See also Interrupt Zones drawing.

1.3.8 INT_MSK_Y

REG Name	INT_MSK_Y: Interrupt Mask Y-axis				
REG Address	Bank 1- 0x07 (Hex) – 7 (Dec)				
	Bit 7:4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-0000	R-0	R-0	R-0	R-0
Content	INT_MASK_Y	Y_HIGH_POS	Y_LOW_POS	Y_HIGH_NEG	Y_LOW_NEG

Description

Rate Interrupt, Y-axis configuration register.

This register comprises 2 fields. The 4 LSBs are read-only one-hot encoded bits which indicate whether the rate is positive or negative and whether it is above or below the rate threshold.

The 4 MSBs are writable bits which enable, when set to 1, the generation of interrupts based on configurable AND/OR combination of some of them.

Parameters

- **INT_MASK_Y**: For each bit, enables ('1') or disables ('0') the interrupt generation for threshold event detection on the Y-axis.
  - Bit4: enable ('1')/ disable ('0') the event Y_LOW_NEG.
  - Bit5: enable ('1')/ disable ('0') the event Y_HIGH_NEG.
  - Bit6: enable ('1')/ disable ('0') the event Y_LOW_POS.
  - Bit7: enable ('1')/ disable ('0') the event Y_HIGH_POS.

For example, writing INT_MASK_Y = 4'b0100 enables the condition with Y_LOW_POS only to generate an interrupt.

Here is the meaning of the other bits:

- **Y_HIGH_POS:** Signal is positive, above the threshold
- **Y_LOW_POS:** Signal is positive, below threshold
- **Y_HIGH_NEG:** Signal is negative, above threshold
- **Y_LOW_NEG:** Signal is negative, below threshold

See also Interrupt Zones drawing.

1.3.9 INT_MSK_Z

REG Name	INT_MSK_Z: Interrupt Mask Z-axis				
REG Address	Bank 1- 0x08 (Hex) - 8 (Dec)				
	Bit 7:4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-0000	R-0	R-0	R-0	R-0
Content	INT_MASK_Z	Z_HIGH_POS	Z_LOW_POS	Z_HIGH_NEG	Z_LOW_NEG

Description

Rate Interrupt, Z-axis configuration register.
This register comprises 2 fields. The 4 LSBs are read-only one-hot encoded bits which indicate whether the rate is positive or negative and whether it is above or below the rate threshold.
The 4 MSBs are writable bits which enable, when set to 1, the generation of interrupts based on configurable AND/OR combination of some of them.

Parameters

- **INT_MASK_Z**: For each bit, enables ('1') or disables ('0') the interrupt generation for the threshold event detection on the Z-axis.
  - Bit4: enable ('1')/ disable ('0') the event Z_LOW_NEG.
  - Bit5: enable ('1')/ disable ('0') the event Z_HIGH_NEG.
  - Bit6: enable ('1')/ disable ('0') the event Z_LOW_POS.
  - Bit7: enable ('1')/ disable ('0') the event Z_HIGH_POS.

For example, writing INT_MASK_Z = 4'b0100 enables the condition with Z_LOW_POS only to generate an interrupt.

Here is the meaning of the other bits:

- **Z_HIGH_POS:** Signal is positive, above threshold
- **Z_LOW_POS:** Signal is positive, below threshold
- **Z_HIGH_NEG:** Signal is negative, above threshold
- **Z_LOW_NEG:** Signal is negative, below threshold

See also Interrupt Zones drawing.

1.3.10 INT_MSK_AO

REG Name	INT_MASK_AO: Interrupt AND and Interrupt OR masks							
REG Address	Bank 1- 0x09 (Hex) - 9 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-0	RW-0	RW-000			RW-000		
Content	RFU	INT_FREEZE	INT_MASK_XYZ_AND			INT_MASK_XYZ_OR		

Description

Interrupt AND/OR masks register.

Parameters

- **INT_FREEZE:**

0 -> disables interrupts on threshold freeze;
1 -> enables interrupts on threshold freeze.

When INT_FREEZE = '1' the {X,Y,Z}_{HIGH,LOW}_{NEG,POS} flags hold values until interrupt will be cleared. The INT_FREEZE bit does not affect the behavior of the Interrupt Status Registers at locations 0x0E and 0x0F.

- **INT_MASK_XYZ_AND**: When the bit is set to 1 it's indicates that the corresponding direction is used in AND, X mask in 0x20, Y mask in 0x10, Z mask in 0x08
- **INT_MASK_XYZ_OR**: When the bit is set to 1 it's indicates that the corresponding direction is used in OR, X mask in 0x04, Y mask in 0x02, Z mask in 0x01

1.3.11 INT_CFG1

REG Name	INT_CFG1: Interrupt 1 Configuration Register					
REG Address	Bank 1- 0xA (Hex) – 10 (Dec)					
	Bit 7:6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1:0
Type - Def. Value	RW-00	RW-0	RW-0	RW-0	RW-0	RW-00
Content	SNS_INTP_FSC	INT1_CLK_OUT	INT2_CLK_OUT	INT_SINGLE_DEB	INT_SINGLE_REF	SNS_INTP_CFG

Description

Interrupt 1 configuration register.

Parameters

- **SNS_INTP_FSC**: These two bits are used for set the Full scale used by rate interrupts:
  - 00 - 2000 dps (default)
  - 01 - 1000 dps
  - 10 - 500 dps
  - 11 - 250 dps
- **INT1_CLK_OUT**: INT1 pad drives out the internal clock (8.8MHz)
- **INT2_CLK_OUT**: INT2 pad drives out the internal clock (8.8MHz)
- **INT_SINGLE_DEB**: Single duration is used for all the direction.
  - int_deb_x used as MSB
  - int_deb_y used as LSB
- **INT_SINGLE_REF:** Single threshold is used for all the direction.
  - int_ref_x used as MSB
  - int_ref_y used as LSB
- **SNS_INTP_CFG:** Interrupt data can be chosen as follow:
  - 00 -> data at ODR without hi-pass filtering
  - 01 -> data at ODR with hi-pass filtering
  - 10 -> data at 10k without hi-pass filtering
  - 11 -> data at 10k with hi-pass filtering

1.3.12 INT_CFG2

REG Name	**INT_CFG2: Interrupt 2 Configuration Register**						
REG Address	Bank 1- 0xB (Hex) – 11 (Dec)						
	Bit 7:6	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 1**
Type - Def. Value	R-00	RW-1	RW-0	RW-0	RW-1	RW-0	RW-0
Content	RFU	INT1_ENABLE	INT1_ACT_LVL	INT1_MODE	INT2_ENABLE	INT2_ACT_LVL	INT2_MODE

Description

Interrupt 2 configuration register. This register determines how the interrupt lines INT1 and INT2 will behave in terms of :

- Being enabled/disabled
- Push-Pull vs Open-Drain configuration
- Active level

When the interrupt lines are disabled, they will stay at the selected un-active level regardless the settings in the INT1_MSK and INT2_MSK registers.

Parameters

- **INT1_ENABLE** :
  - 0 -> disable interrupt on INT1
  - 1 -> enable interrupt on INT1
- **INT1_ACT_LVL :**
  - 0 -> INT1 active High
  - 1 -> INT1 active low
- **INT1_ MODE :**
  - 0 -> push pull configuration
  - 1 -> open drain configuration
- **INT2_ENABLE** :
  - 0 -> disable interrupt on INT2
  - 1 -> enable interrupt on INT2
- **INT2_ ACT_LVL :**
  - 0 -> INT2 active High
  - 1 -> INT2 active low
- **INT2_ MODE :**
  - 0 -> push pull configuration
  - 1 -> open drain configuration

1.3.13 INT_TMO

REG Name	INT_TMO: Interrupt timeout and interrupt mode configuration		
REG Address	Bank 1- 0x0C (Hex) - 12 (Dec)		
	Bit 7:6	Bit 5:4	Bit 3:0
Type - Def. Value	RW-00	RW-00	RW-0000
Content	INT1_LATCH_MODE	INT2_LATCH_MODE	INT_TIMEOUT

Description

Interrupt Timeout and Interrupt Mode configuration register.
This register allows to configure the interrupt lines to operate as either un-latched, latched or timed.
As un-latched, they can be further configured in such a way that interrupt sources (INT1_STS and INT2_STS) can be cleared when they are read or cleared when they are written with a logic 1.
Clearing an interrupt source by writing a logic 1 allows clearing single bits rather than the entire register.

Parameters

- **INT1_LATCH_MODE**:
  - 00 -> interrupt is not latched
  - 01-> latched mode. Interrupt is maintained until cleared on Read
  - 10 -> latched mode. Interrupt is maintained until cleared on Write
  - 11 -> Timed (see INT_TIMEOUT)
- **INT2_LATCH_MODE**:
  - 00 -> interrupt is not latched
  - 01-> latched mode. Interrupt is maintained until cleared on Read
  - 10 -> latched mode. Interrupt is maintained until cleared on Write
  - 11 -> Timed (see INT_TIMEOUT)
- **INT_TIMEOUT**: Interrupt temporary period. This is shared between INT1 and INT2:
  - 0000 Temporary: 100us
  - 0001 Temporary: 200us
  - 0010 Temporary: 500us
  - 0011 Temporary: 1ms
  - 0100 Temporary: 2ms
  - 0101 Temporary: 5ms
  - 0110 Temporary: 10ms
  - 0111 Temporary: 20ms
  - 1000 Temporary: 50ms
  - 1001 Temporary: 100ms
  - 1010 Temporary: 200ms
  - 1011 Temporary: 500ms

1.3.14 INT_STS_UL

REG Name	INT_STS_UL: Interrupt sources, unlatched							
REG Address	Bank 1- 0x0D (Hex) - 13 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
Content	DATA_RDY	FIFO_EMPTY	FIFO_OVR	FIFO_TH	INT_AND	INT_OR	RESTART	DSYNC

Description

Interrupt sources, un-latched. These bits are the un-latched version of the interrupt status registers; as these signals are shared by the INT1 generator and the INT2 generator, there is a unique register shared.

This register is the actual source for the interrupt lines when the interrupts are configured as un-latched.

When the interrupt lines are configured as latched, be it both or just one of them, these bits can be used to keep monitoring the status of an interrupt source, previously identified by means of its latched version, to see how it changes after the event.

Parameters

- **DATA_RDY** : DATA_READY status bit (0x22[0])
- **FIFO_EMPTY** : FIFO empty status bit (0x3D[0])
- **FIFO_OVR** : FIFO overrun status bit (0x3D[4])
- **FIFO_TH** : FIFO threshold status bit (0x3D[2])
- **INT_AND** : rate interrupt OR status
- **INT_OR** : rate interrupt AND status
- **RESTART** : restart status (0x1C[0])
- **DSYNC** : DSYNC pin status, according to DSYNC_CFG

1.3.15 INT1_STS

REG Name	INT1_STS: Interrupt 1 Status register (latched)							
REG Address	Bank 1- 0x0E (Hex) - 14 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
Content	DATA_RDY	FIFO_EMPTY	FIFO_OVR	FIFO_TH	INT_AND	INT_OR	RESTART	DSYNC

Description

Interrupt 1, status register. These are the latched interrupt sources.
When INT1 is configured to operate as latched, it can be cleared, when asserted, in two ways:

- Clear-On-Read: by reading the entire INT1_STS register
- Clear-On-Write: by selectively writing with ‚1' the specific interrupt source bit in INT1_STS register, until they are all cleared. Many bits can be cleared at once by forming the appropriate mask.

When INT1 is configured to operate as either latched or timed, these registers are set to 0.

Parameters

- **DATA_RDY** : DATA_READY status bit
- **FIFO_EMPTY** : FIFO empty status bit (unlatched if INT1 configured to be timed)
- **FIFO_OVR** : FIFO overrun status bit
- **FIFO_TH** : FIFO threshold status bit
- **INT_AND** : rate interrupt OR status
- **INT_OR** : rate interrupt AND status
- **RESTART** : restart status
- **DSYNC** : DSYNC pin status, according to DSYNC_CFG

1.3.16 INT2_STS

REG Name	INT2_STS: Interrupt 2 Status register (latched)							
REG Address	Bank 1- 0x0F (Hex) - 15 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
Content	DATA_RDY	FIFO_EMPTY	FIFO_OVR	FIFO_TH	INT_AND	INT_OR	RESTART	DSYNC

Description

Interrupt 2, status register. These are the latched interrupt sources.
When INT2 is configured to operate as latched, it can be cleared, when asserted, in two ways:

- Clear-On-Read: by reading the entire INT2_STS register
- Clear-On-Write: by selectively writing with ‚1' the specific interrupt source bit in INT2_STS register, until they are all cleared. Many bits can be cleared at once by forming the appropriate mask.

When INT2 is configured to operate as either latched or timed, these registers are set to 0.

Parameters

- **DATA_RDY** : DATA_READY status bit
- **FIFO_EMPTY** : FIFO empty status bit (unlatched if INT2 configured to be timed)
- **FIFO_OVR** : FIFO overrun status bit
- **FIFO_TH** : FIFO threshold status bit
- **INT_AND** : rate interrupt OR status
- **INT_OR** : rate interrupt AND status
- **RESTART** : restart status
- **DSYNC** : DSYNC pin status, according to DSYNC_CFG

1.3.17 INT1_MSK

REG Name	INT1_MSK: Interrupt 1 Generation Mask							
REG Address	Bank 1- 0x10 (Hex) - 16 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-1	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
Content	DATA_RDY	FIFO_EMPTY	FIFO_OVR	FIFO_TH	INT_AND	INT_OR	RESTART	DSYNC

Description

Interrupt 1 generation, mask register. This register is meant to be used to enable selected interrupt sources in the INT1_STS (0x0E) register to activate the INT1 interrupt line. Interrupt sources are masked (prevented from generating an interrupt) as long as the corresponding bit in the mask register is 0.

Valid configurations are with None, One, Multiple or Every bit set to 1; having multiple possible interrupt sources will require the Interrupt Service routine to identify the correct one(s).

Parameters

- **DATA_RDY** : DATA_READY status bit
- **FIFO_EMPTY** : FIFO empty status bit (unlatched if INT1 configured to be timed)
- **FIFO_OVR** : FIFO overrun status bit
- **FIFO_TH** : FIFO threshold status bit
- **INT_AND** : rate interrupt OR status
- **INT_OR** : rate interrupt AND status
- **RESTART** : restart status
- **DSYNC** : DSYNC pin status, according to DSYNC_CFG

1.3.18 INT2_MSK

REG Name	**INT2_MSK: Interrupt 2 Generation Mask**							
REG Address	Bank 1- 0x11 (Hex) - 17 (Dec)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Type - Def. Value	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-1	RW-0
Content	DATA_RDY	FIFO_EMPTY	FIFO_OVR	FIFO_TH	INT_AND	INT_OR	RESTART	DSYNC

Description

Interrupt 2 generation, mask register. This register is meant to be used to enable selected interrupt sources in the INT2_STS (0x0F) register to activate the INT2 interrupt line. Interrupt sources are masked (prevented from generating an interrupt) as long as the corresponding bit in the mask register is 0.
Valid configurations are with None, One, Multiple or Every bit set to 1; having multiple possible interrupt sources will require the Interrupt Service routine to identify the correct one(s).

Parameters

- **DATA_RDY** : DATA_READY status bit
- **FIFO_EMPTY** : FIFO empty status bit (unlatched if INT2 configured to be timed)
- **FIFO_OVR** : FIFO overrun status bit
- **FIFO_TH** : FIFO threshold status bit
- **INT_AND** : rate interrupt OR status
- **INT_OR** : rate interrupt AND status
- **RESTART** : restart status
- **DSYNC** : DSYNC pin status, according to DSYNC_CFG

1.3.19 (OTP_STATUS)

REG Name	**OTP_STATUS: OTP status Register**	
REG Address	Bank 1- 0x19 (Hex) – 25 (Dec)	
	Bit 7:2	**Bit 1:0**
Type – Def. Value	R-000000	R-00
Content	OTP status	

Description

OTP status register. This register provides the OTP download status. If read the two LSB, it could get the code of different download status.

OTP_STATUS[1:0] = 00	OTP download OK, no error.
OTP_STATUS[1:0] = 01	OTP download OK, 1 bit corrected.
OTP_STATUS[1:0] = 10	OTP download OK, after n trays.
OTP_STATUS[1:0] = 11	OTP download completed with errors.

1.3.20 SERIAL_0

REG Name	**SERIAL_0: Serial Number byte 0**							
REG Address	Bank 1- 0x1A (Hex) – 26 (Dec)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Type – Def. Value	R	R	R	R	R	R	R	R
Content	SERIAL_0							

Description

Serial number, byte 0 register. SERIAL_X registers (with X going from 0 to 5) are 6 registers used to assign a unique identifier to every single MAX21000 sample to enable a complete track-ability of each of them, in terms of LOTs, Assembly history and Test equipment.

Parameters

- **Serial_0** : Serial number, byte 0

1.3.21 SERIAL_1

REG Name	**SERIAL_1: Serial Number byte 1**							
REG Address	Bank 1- 0x1B (Hex) – 27 (Dec)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Type – Def. Value	R	R	R	R	R	R	R	R
Content	SERIAL_1							

Description

Serial number, byte 1 register.

Parameters

- **SERIAL_1** : Serial number, byte 1

1.3.22 SERIAL_2

REG Name	**SERIAL_2: Serial Number byte 2**							
REG Address	Bank 1- 0x1C (Hex) – 28 (Dec)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Type – Def. Value	R	R	R	R	R	R	R	R
Content	SERIAL_2							

Description

Serial number, byte 2 register.

Parameters

- **SERIAL_2** : Serial number, byte 2

1.3.23 SERIAL_3

REG Name	**SERIAL_3: Serial Number byte 3**							
REG Address	Bank 1- 0x1D (Hex) – 29 (Dec)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Type – Def. Value	R	R	R	R	R	R	R	R
Content	SERIAL_3							

Description

Serial number, byte 3 register. SERIAL_X registers (with X going from 0 to 5) are 6 registers used to assign a unique identifier to every single MAX21000 sample to enable a complete track-ability of each of them, in terms of LOTs, assembly history and Test equipment.

Parameters

- **SERIAL_3** : Serial number, byte 3

1.3.24 SERIAL_4

REG Name	**SERIAL_4: Serial Number byte 4**							
REG Address	Bank – 0x1E (Hex) – 30 (Dec)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Type – Def. Value	R	R	R	R	R	R	R	R
Content	SERIAL_4							

Description

Serial number, byte 4 register.

Parameters

- **SERIAL_4** : Serial number, byte 4

1.3.25 SERIAL_5

REG Name	**SERIAL_5: Serial Number byte 5**							
REG Address	Bank 1- 0x1F (Hex) – 31 (Dec)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Type – Def. Value	R	R	R	R	R	R	R	R
Content	SERIAL_5							

Description

Serial number, byte 5 register.

Parameters

- **SERIAL_5** : Serial number, byte 5