DIMACS Workshop 2019

A universal MPC machine*

Dragos Rotaru

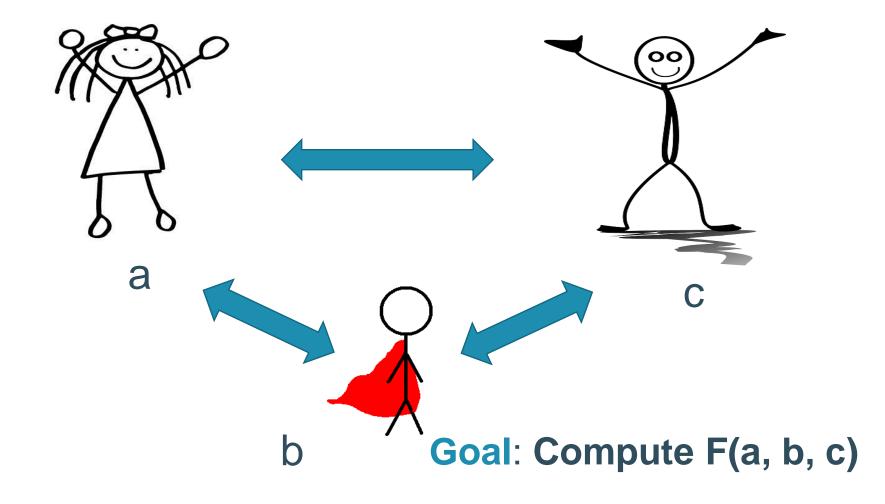
University of Bristol, KU Leuven

*MArBled Circuits: Mixing Arithmetic and Boolean Circuits with Active Security;

- Joint work with Tim Wood.
- https://ia.cr/2019/207

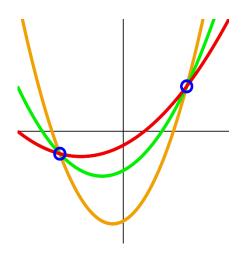


What is multiparty computation?





How can we achieve MPC?



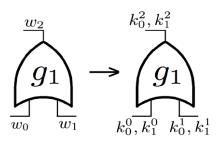


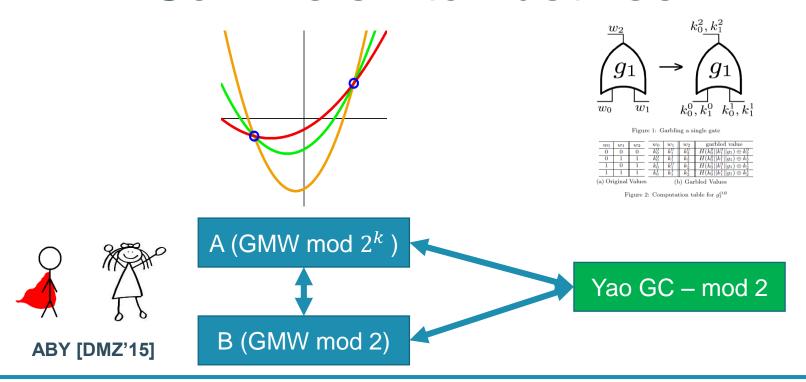
Figure 1: Garbling a single gate

w_0	w_1	w_2	w_0	w_1	w_2	garbled value	
0	0	0	k_0^0	k_1^0	k_2^0	$H(k_0^0 k_1^0 g_1) \oplus k_2^0$	
0	1	1	k_0^0	k_1^1	k_2^1	$H(k_0^0 k_1^1 g_1) \oplus k_2^1$	
1	0	1	k_0^1	k_1^0	k_2^1	$H(k_0^1 k_1^0 g_1) \oplus k_2^1$	
1	1	1	k_0^1	k_1^1	k_2^1	$H(k_0^1 k_1^1 g_1) \oplus k_2^1$	
(a) Or	(a) Original Values			(b) Garbled Values			

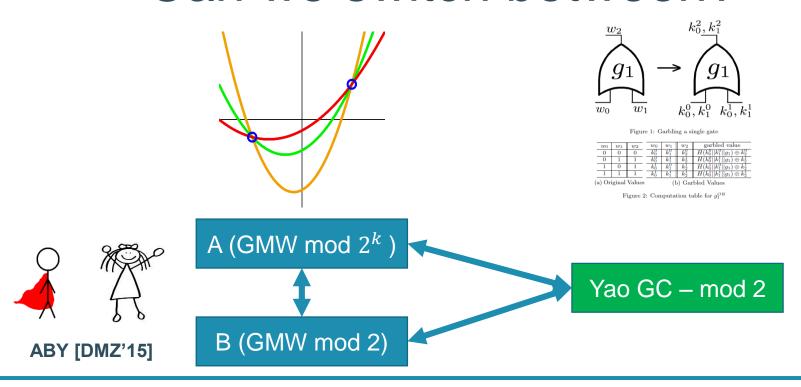
Figure 2: Computation table for g_1^{OR}

Secret Sharing	Garbled Circuits		
Fast networks (LAN)	Slow Networks (WAN)		
Arithmetic/Boolean circuits	Boolean circuits		
Low depth, many AND gates	Large depth, few AND gates		

Can we switch between?



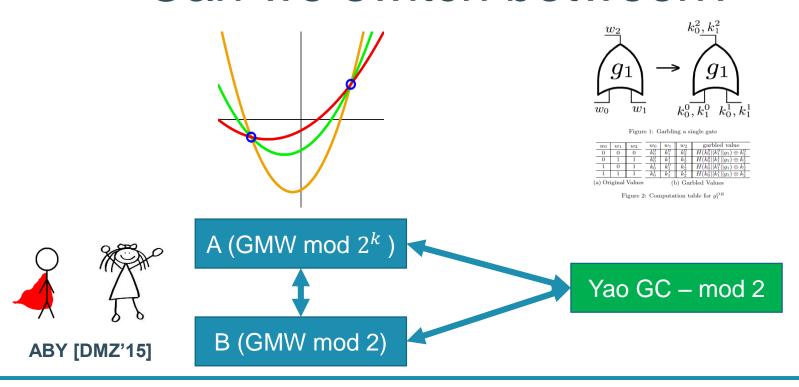
Can we switch between?





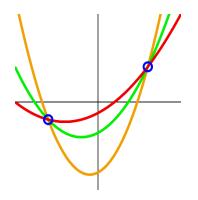


Can we switch between?





ABY3 [MR'18]



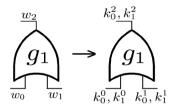
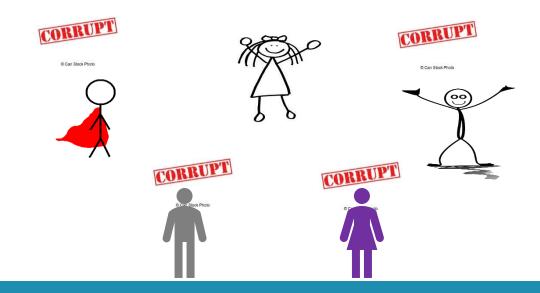
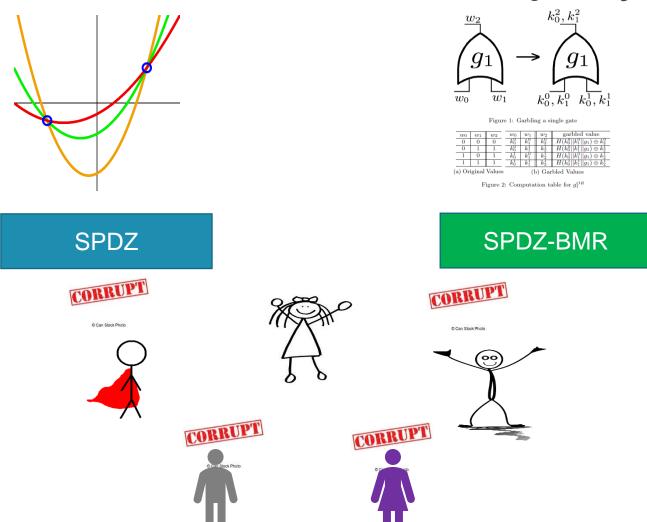


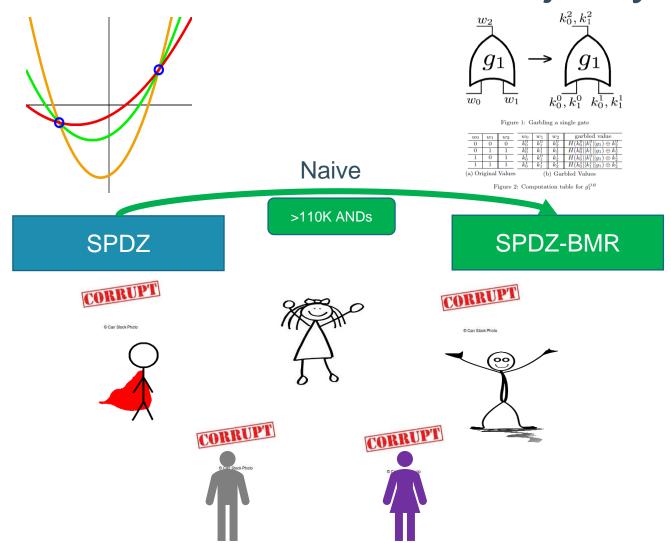
Figure 1: Garbling a single gate

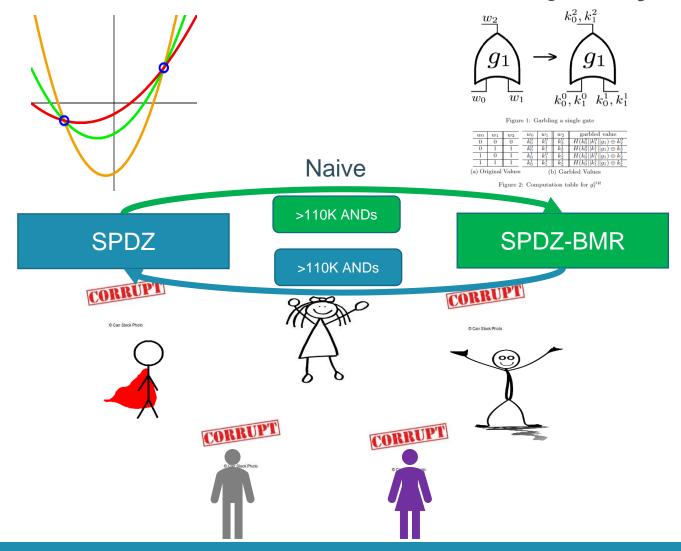
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1	0	1	k_0^1	k_1^0	k_2^1	$H(k_0^1 k_1^0 g_1) \oplus k_2^1$	
1	1	1	k_{0}^{1}	k_1^1	k_2^1	$H(k_0^1 k_1^1 g_1) \oplus k_2^1$	
(a) Or	(a) Original Values			(b) Garbled Values			

Figure 2: Computation table for g_1^{OR}

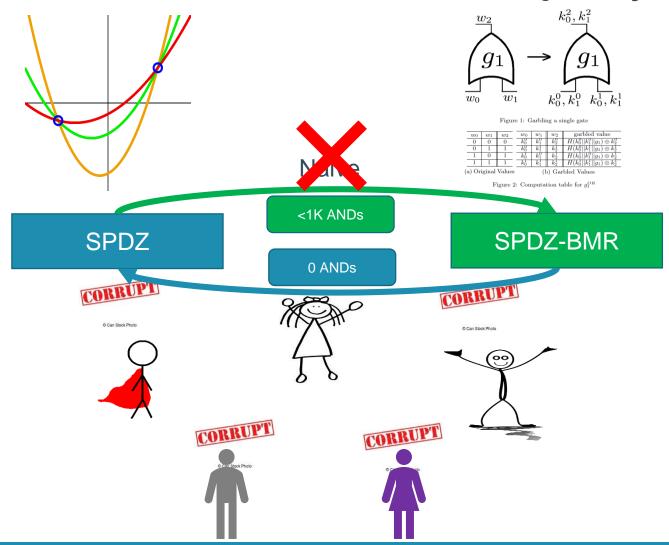


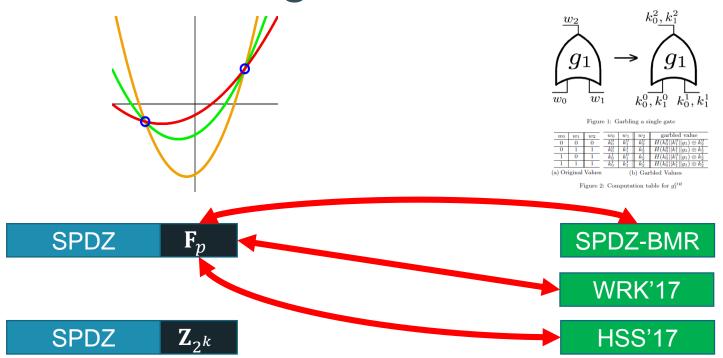


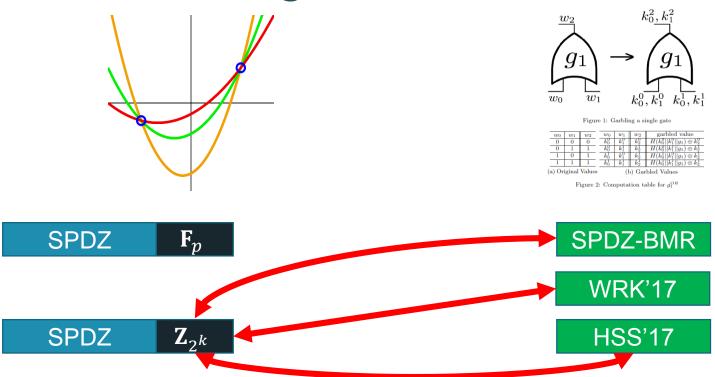


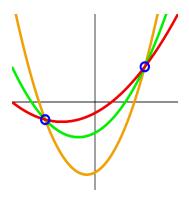


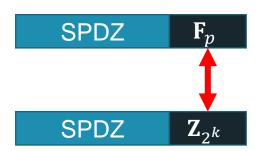












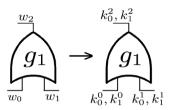


Figure 1: Garbling a single gate

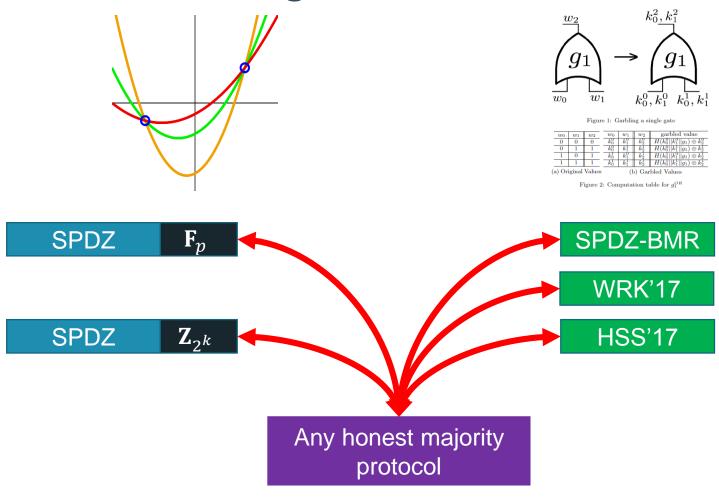
w_0	w_1	w_2	w_0	w_1	w_2	garbled value	
0	0	0	k_0^0	k_1^0	k_2^0	$H(k_0^0 k_1^0 g_1) \oplus k_2^0$	
0	1	1	k_0^0	k_1^1	k_2^1	$H(k_0^0 k_1^1 g_1) \oplus k_2^1$	
1	0	1	k_0^1	k_1^0	k_2^1	$H(k_0^1 k_1^0 g_1) \oplus k_2^1$	
1	1	1	$-k_{0}^{1}$	k_1^1	k_2^1	$H(k_0^1 k_1^1 g_1) \oplus k_2^1$	
(a) Or	(a) Original Values			(b) Garbled Values			

Figure 2: Computation table for g_1^{OR}

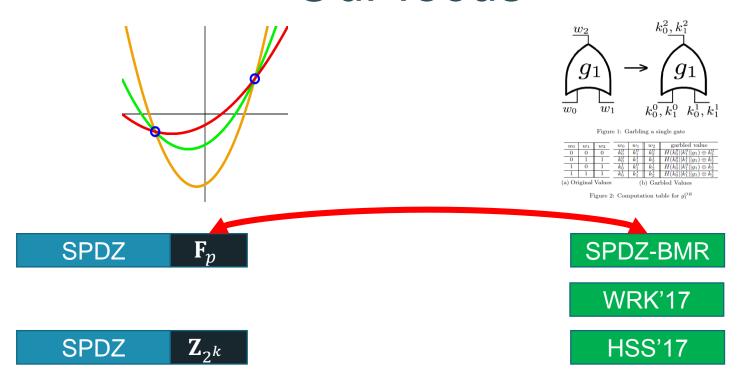


WRK'17

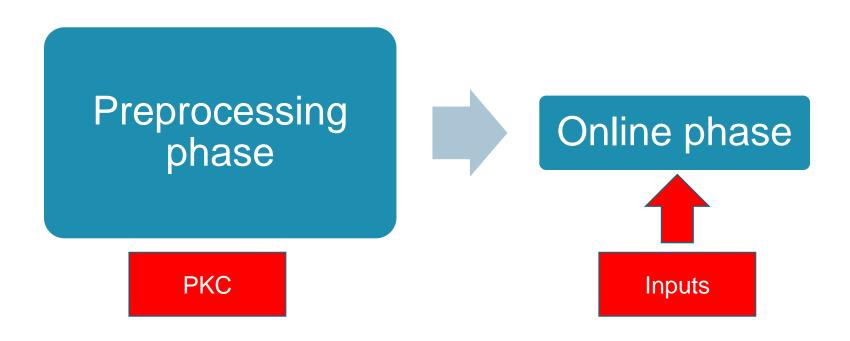
HSS'17



Our focus



Malicious MPC protocols



SPDZ, TinyOT, BDOZa, MASCOT, WRK'17, HSS'17, ...



Let's talk about

SPDZ \mathbf{F}_p







$$\alpha_1$$

$$\alpha_{2} \\$$

$$\alpha_3$$

$$x_1$$

$$\chi_2$$

$$\chi_3$$

$$\chi$$

$$\gamma(x)_1$$

$$\gamma(x)_2$$
 +

$$\gamma(x)_3 =$$

$$\alpha x$$







$$\alpha_1$$

$$\alpha_{2} \\$$

$$\alpha_3$$

$$x_1 + y_1$$

$$x_2 + y_2$$

$$+ x_2 + y_2 + x_3 + y_3 =$$

$$x + y$$

$$\gamma(x)_1 + \gamma(y)_1 + \gamma(x)_2 + \gamma(y)_2 + \gamma(x)_3 + \gamma(y)_3 = \alpha(x + y)$$

$$\gamma(x)_2 + \gamma(y)_2$$

$$\gamma(x)_3 + \gamma(y)_3$$

$$\alpha(x+y)$$





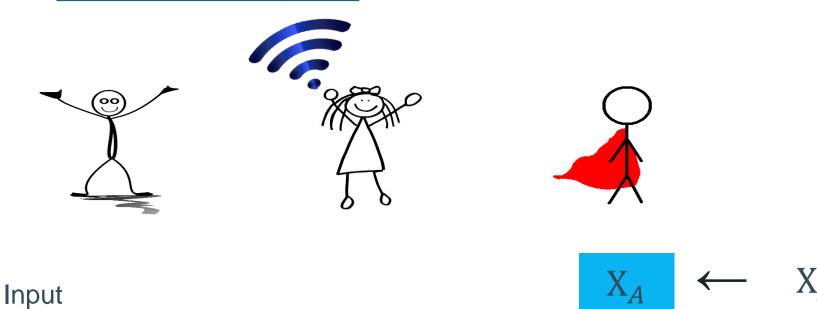


Input

Retrieve a random mask



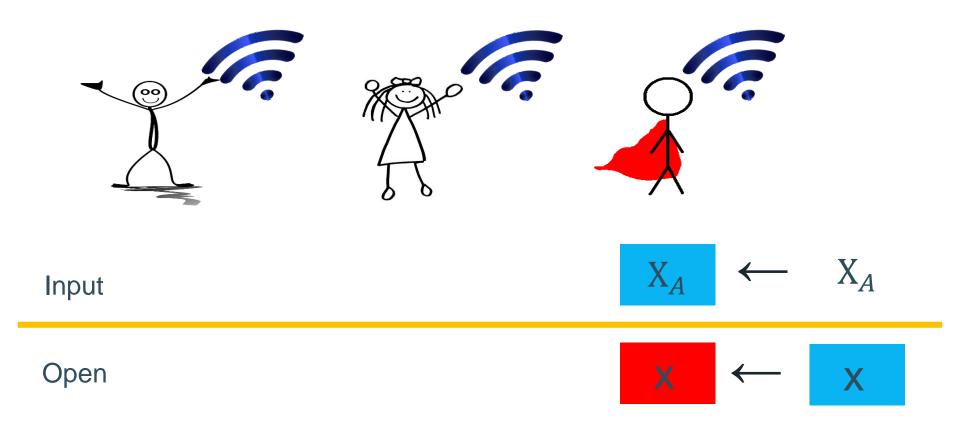






SPDZ

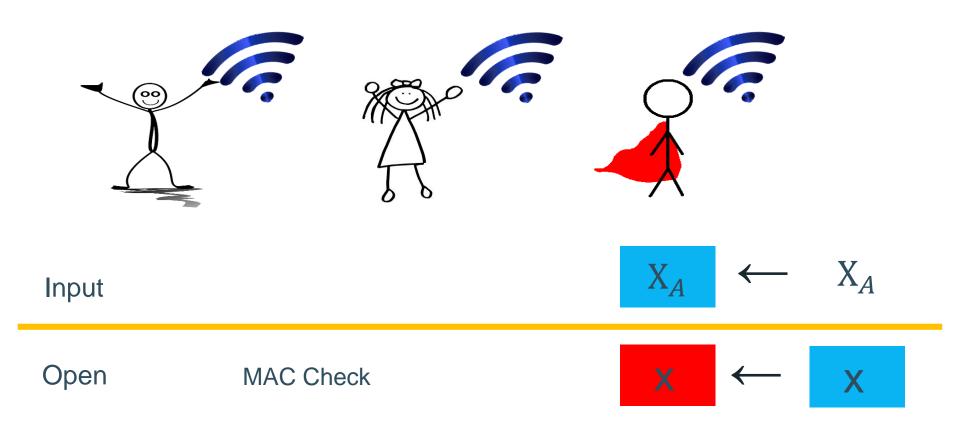
online phase





SPDZ

online phase











Input





Open







XOR

Retrieve a Beaver triple





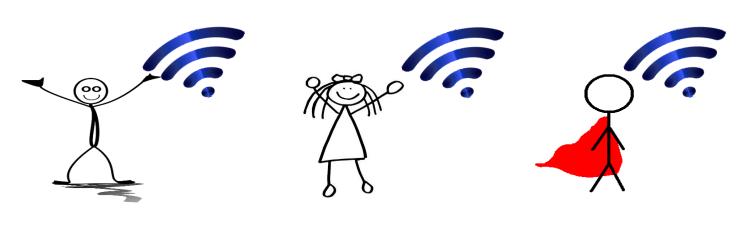






SPDZ

online phase



Input





Open

MAC Check







XOR











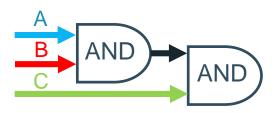
Let's talk about

SPDZ-BMR F₂



 \mathbf{F}_2

online phase





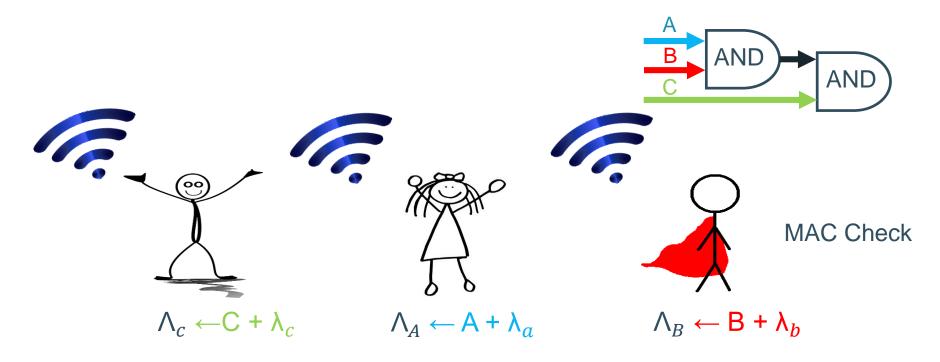






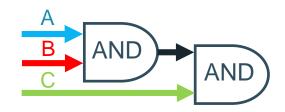
 \mathbf{F}_2

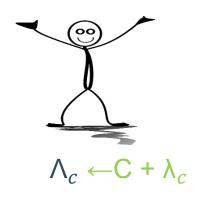
online phase

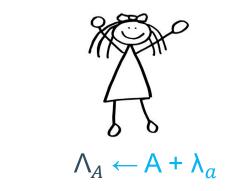


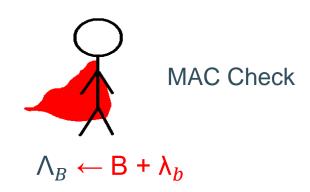
 \mathbf{F}_2

online phase









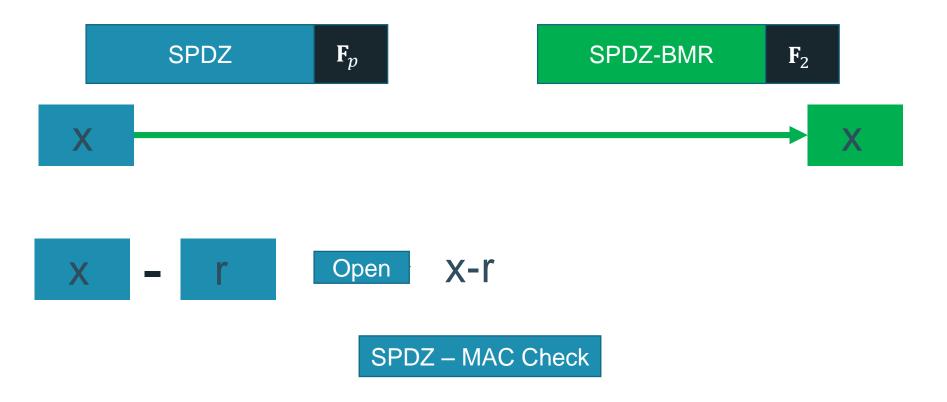
Inputs - cheap

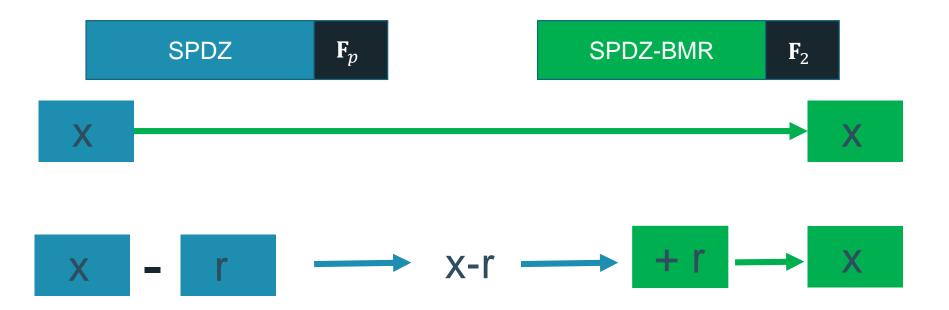
XOR - free

Mod p arithmetic - some AND gates









Introducing daBits





Introducing daBits

SPDZ

 \mathbf{F}_p

SPDZ-BMR

 \mathbf{F}_2



 \boldsymbol{b}_{A}



 \boldsymbol{b}_B



 $b_{\it C}$



SPDZ

 \mathbf{F}_p

SPDZ-BMR

 \mathbf{F}_2

SPDZ Input



 \boldsymbol{b}_{A}



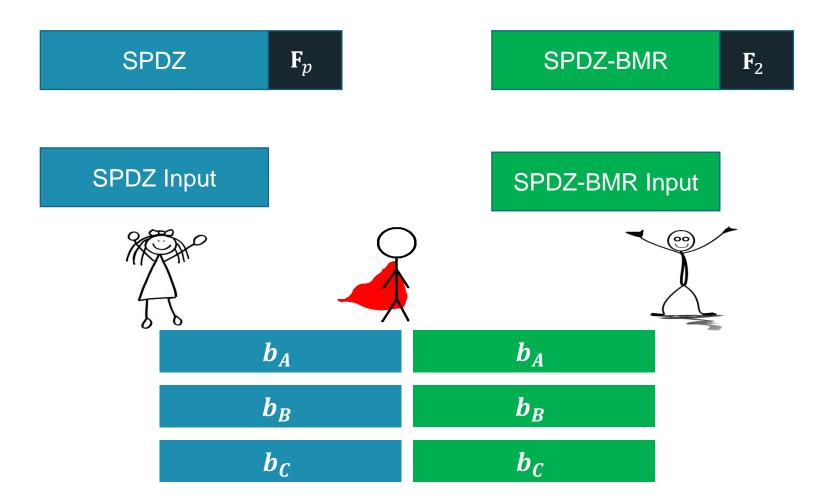
 b_B

SPDZ-BMR Input

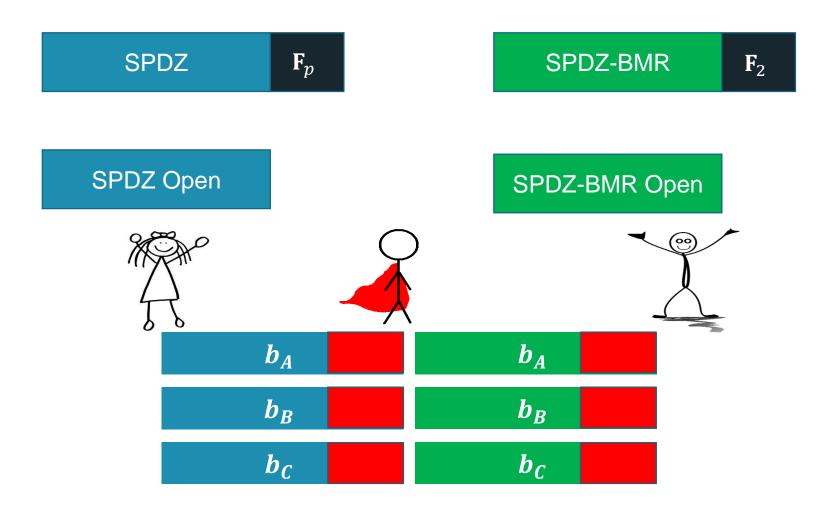


 $\boldsymbol{b}_{\mathcal{C}}$











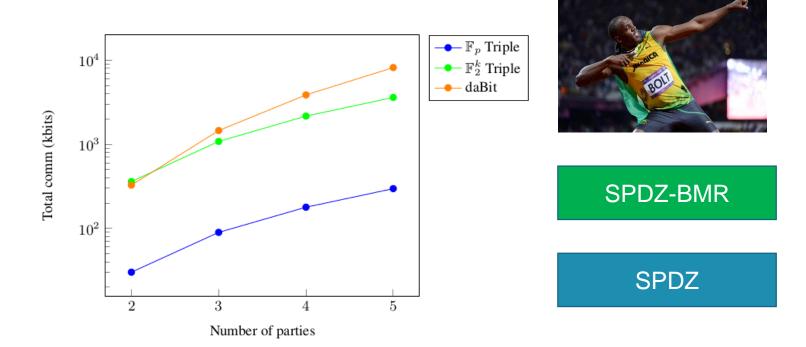
SPDZ \mathbf{F}_p SPDZ-BMR \mathbf{F}_2 SPDZ-BMR XOR $b_A \oplus b_B \oplus b_C$



SPDZ \mathbf{F}_p SPDZ-BMR \mathbf{F}_2 SPDZ-BMR Open SPDZ-BMR \mathbf{Open}



daBit cost



Total communication costs for all parties per preprocessed element.



Preprocessing cost per conversion

$\operatorname{sec} \log p$ k Comm. (kb)			Total (kb)	Time (ms)			Total(ms)	
	\mathcal{F}^p_MPC	${\mathcal{F}^2_MPC}^k$	daBitgen		\mathcal{F}^p_{MPC}	$\mathcal{F}^{2^k}_{MPC}$	daBitgen	
40 128 128	76.60	2.30	6.94	85.84	0.159	< 10ns	0.004	0.163

Table 2. 1Gb/s LAN experiments for two-party daBit generation per party. For all cases, the daBit batch has length 8192.

Example code in MP-SPDZ

```
1 bit_len = 7
2 x = sint(42) # mod p share
3 xb = sbits.switch_to_gc(bit_len, x) # mod 2 shares
4 bits = xb.bit_decompose(bit_len)
5
6 for i in range(len(bits)):
7     print_str('%s', bits[i].reveal())
8 # prints 0101010
```

Online cost per conversion

Conversion	SPDZ-BMR			
	ANDs	Online (ms)		
$sint \mapsto sbits$	379	0.106		
$sbits \mapsto sint$	0	0.005		

8X overhead than using ABY



45

Online cost per conversion

Conversion	SPDZ-BMR			
	ANDs	Online (ms)		
$sint \mapsto sbits$	379	0.106		
$sbits \mapsto sint$	0	0.005		

8X overhead than using ABY



What's next?

- SCALE-MAMBA has WRK'17.
- It also has all preprocessing phases connected ideal candidate for daBits in a more realistic system.
- Moral: Stitch your work together so it would be easier to build more efficient protocols on top of them.



Thank you!



Thank you!

- Questions?
- https://ia.cr/2019/207



