

Reply letter to #TCSVT 9275

“Hardware Reconfiguration Scheme Based on the Digital TV Signal”

June 13, 2015

Dear Editor,

We really appreciate the comments of the TCSVT reviewers, which were highly insightful and enabled us to greatly improve the quality of our manuscript. The following pages list our responses to each of the comments.

Attached to this letter, please find a revised version of our manuscript. We hope that the revisions in the manuscript and our responses will be sufficient to make our manuscript suitable for publication.

Best Regards,

Rodrigo de Oliveira, Lucas Cordeiro, Eddie de Lima Filho, and Vicente de Lucena Júnior

Federal University of Amazonas (UFAM), Brazil,

E-mail: rodrigo@dcc.ufam.edu.br

Associate editor's comments to the author

[1] The paper presents a way to reconfigure the DTV receiver. This might be good to compare the approach with what is done in the MPEG reconfigurable video coding standard whose has merely the same goal.

Response: Two paragraphs were added at the end of section II. They had not been previously included, because the proposed approach has a broader application than only video coding. However, they indeed present the same goal.

Key references that must be included:

[2] From reviewers' comments (please check this section):

The related work section is rather short. I think more work around agile software update can be added which can include some watermarking based approaches supporting both legacy systems and new systems.

Response: The related work section was completely reviewed and extended, while including a discussion regarding the suggested references.

[3] The motivations of this work are more or less the same that those of the MPEG Reconfigurable Video Coding. Authors should mention it in the background of their work, e.g.:

- S. S. Bhattacharyya, J. Eker, J. W. Janneck, C. Lucarz, M. Mattavelli, M. Raulet, Overview of the mpeg reconfigurable video coding framework, Jrnl. of Signal Proc. Systems 63 (2).

Considering also that, in that field, reconfiguration has already been tackled either at a finegrain (FPGA only):

- E. Bezati, S. CasaleBrunet, M. Mattavelli, J. Janneck, Synthesis and optimization of highlevel Stream programs, in: Electronic System Level Synthesis Conf., 2013, pp. 16.
 - J. Janneck, I. Miller, D. Parlour, G. Roquier, M. Wipliez, M. Raulet, Synthesizing Hardware from Dataflow Programs: An MPEG4 Simple Profile Decoder Case Study, Jrnl. of Signal Proc. Systems 63 (2) 241249.
- and at coarsegrain (including, but not limited to, FPGA implementations):
- Nezan J, Siret N, Wipliez M, Palumbo F., Raffo L (2012). MultiPurpose Systems: A Novel DataflowBased Generation and Mapping Strategy. Symp on Circuits and Systems (ISCAS), pp. 30733076
 - C. Sau, L. Raffo, F. Palumbo, E. Bezati, S. CasaleBrunet, M. Mattavelli, Automated design flow for coarsegrained reconfigurable platforms: An rvccal multistandard decoder usecase, in: 2014 International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation, pp 5966.

Response: All mentioned references were included and used in the text (see references [18] to [25]), along with others related work to the same area.

[4] Would suggest including a reference to the Transport Stream standard. ISO/IEC 138181, ITUT Recommendation H.222.0

Response: It was already there. Now it is reference [26].

Responses to the comments of Reviewer #1

[1] This paper covers very up to date topics: how to keep pace with the rapid evolution of the video standards without the need of completely changing the provided technologies and how to manage intelligent/adaptable systems.

According to my humble opinion the paper is too much pedantic. Section IV.A for example reports basic concepts for hardware designers.

Response: That was not our intention. Maybe, the broad applicability of the proposed technique may have caused that impression. Section IV was created in order to provide a better understanding of the framework, for readers of different areas (*e.g.*, video coding).

[2] Keeping pace with the rapid evolution of the video standards is one of the claims of the paper. Point is that reconfiguration help maintaining the same reference technology by means of reprogrammability.

Nevertheless, it does not help in passing from one standard to other in a flexible way. As far as I understood from the paper the designers would need to write the hardware description from scratch. Please comment on this aspect considering also the considerations made below with respect to Reconfigurable Video Coding.

Response: The proposed methodology does not aim to pass from one standard to another, in a flexible way, but to reprogram the target system. Indeed, a new hardware description is needed (if we take into account the current industrial approach, it will be developed anyway). A discussion was added to the last paragraph of section II.

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- C. Sau, L. Raffo, F. Palumbo, E. Bezati, S. CasaleBrunet, M. Mattavelli, Automated design flow for coarsegrained reconfigurable platforms: An rvccal multistandard decoder usecase, in: 2014 International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation, pp 5966.

Response: All mentioned references were included and used in the text (see references [18] to [25]), along with others related work to the same area.

[4] Methodology:

1. Is the proposed methodology limited to a specific vendor?

Response: No, it is not. The choice of SVF and the information provided in the proposed SI information allows its use in a wide variety of platforms. In order to clarify that, a new section was included: V.E.

2. What happen, from the functional point of view, if the bitstream I receive is not compatible with the available hardware?

Response: If there is no match between the hardware reconfiguration bit-stream and the working FPGA, the update content is rejected and the receiver will then wait for a suitable file. Some text regarding that was added to section V.E.

3. How long the reconfiguration process take? Are there any timing limitation?

Response: The time period used by reconfiguration process is given by RCT, in table VIII. The remount time (RCT), that is, the time needed for acquiring the reconfiguration bit-stream is also informed, in tables VII and VIII.

[5] Results:

1. Which boards did you use for prototyping activities?

Response: The test environment was described in the second paragraph of section V.F.

2. Did you get any result on complete decoders?

Response: Unfortunately, we did not. There is no restriction regarding that since the proposed applications are suitable to give a good idea of the complexity and the validity of the proposed methodology. This was mentioned in the third paragraph of the conclusions.

3. What is the reconfiguration overhead?

Response: There is some overhead related to the private section header and also the SVF file header. It was discussed in the fourth paragraph of section V.E and in the last paragraph of the conclusions.

Responses to the comments of Reviewer #2

[1] The paper is easy to understand and the proposed method is technically sound. I however had difficulties understanding what is the scientific novelty of the work as using part of a communication channel (DTV in this case) to achieve software update at the receiver's end does not sound a real research question, but an engineering issue. The way how the reconfiguration information is embedded in the DTV signal is naive in that it is merely mixed with other signals via time sharing. The syntax of the data transmitted and the steps of the processes involved are so detailed that they look very arbitrary and unnecessary as a research paper the main focus should be a novel technical concept and a proof of concept but this paper seems to have just the latter.

Response: To the best of our knowledge, there is no similar proposal for updating hardware modules through the digital TV signal, nor a specific methodology for their encapsulation and signaling. Besides, the use of data streaming through private sections was not arbitrarily chosen. Indeed, there was a study concerning this matter, which was added to a new section V.A, in such a way that the most suitable methodology, considering simplicity and required flexibility, was chosen and further developed. The detailed description was provided in order to allow an easy reproduction of the current research, which is a ongoing discussion in scientific communities (reproducible research).

[2] Another less relevant (for the proposed application) but very important (for ANY actual real applications of the proposed technique) is the implications of the proposed approach on systems security. What the proposed method allows is basically remote and automatic update of FPGA hardware (similar to automated software code update in agile software engineering context), but if this can be done in such a transparent manner and without a careful security-by-design approach, the technique will lead to easy attacks to hardware devices via the air which could cause large-scale system failure. While security is not a main concern of the paper, at least this should be discussed and the processes and data syntax should reserve some space for adding security into the overall solution.

Because of the above comments I cannot recommend this paper for acceptance. The authors may consider resubmitting their paper to a more practitioner-oriented venue such as a conference focusing on implementation aspects of DTV and hardware design for possible publication.

Response: Indeed, security is not the focus of the current paper. The main goals were to prove the feasibility of such an approach and also to provide a complete and consistent framework, which could be readily used and further extended. However, security tools can be added to the host system and some space, regarding SI, can be reserved for security information. A brief discussion about that was added to the second to last paragraph of section V.E.

Responses to the comments of Reviewer #3

[1] There are many reason why the proposed concept of reconfiguring FPGA systems through DTV channels will encounter problems in practice:

- Security: HW cores have access to unencrypted content, system busses, and raw memory access. Thus such a scheme will expose the system to piracy, identity theft, etc. Manufacturers of settop boxes and content owners will be very resistant to this approach.

Response: Indeed, security is not the focus of the current paper and such a transparent update may really expose the system. However, as mentioned above, the main goals were to prove the feasibility of such an approach and also provide a complete and consistent framework. Nonetheless, security tools can be added to the host system and the framework itself. A brief discussion was added to the second to last paragraph of section V.E.

[2] HW targets. It is nearly impossible to guarantee all clients will have a particular model of FPGA chip available in the settop box. It also heavily constrains what is possible from a HW code perspective. For example if a particular model of settop box can decode AVC with some FPGA core, it does not mean it could be reconfigured to decode HEVC on the same hardware due to larger requirements on the amount of available FPGA cells, memory, clock speed etc. Additionally, this approach all but rules out the use of SoCs with FPGA logic on the same die.

Response: As can be seen in Tables II to VI, the proposed framework provides enough information to identify any given hardware module for update. In particular, table V provides information related to the FPGA device itself. This way, there is no need for a particular FPGA model. Regarding the processing power, some care must be taken in order to choose a device that is capable of hosting more computationally-complex modules. Indeed, the goal is to reduce the hardware legacy caused by SoCs. In order to clarify the mentioned issues, brief comments were added to section V.E (second and seventh paragraphs).

[3] Cost. Set-top boxes are built with low profit margins, or even at loss since the idea is to recover the cost by selling the content and services that such devices enable. FPGA parts are not particularly cheap, and manufacturers of set-top boxes are not likely to include extra expensive hardware for a codec that may or may not show up one day.

Response: Indeed, that may be a problem for horizontal fixed-reception markets. However, regarding vertical ones, cable/satellite operators must provide receivers, in order to offer services. If the technology changes, they must then provide new receivers, which is very expensive. This way, the proposed approach may find a good environment in pay TV, since it may be cheaper to update receivers instead of buying new ones. A brief discussion regarding that matter was added to the eighth paragraph of the introduction.

[4] Not applicable to mobile space. FPGA implementations of a decoder, while they can be much faster than software, are much slower, more expensive in terms of device cost and more power hungry than ASIC implementations. Thus devices such as mobile phones and tablets

almost never contain useful FPGA resources. And mobile devices are the fastest growing users of DTV services.

Response: Indeed, there are heavy restrictions when considering mobiles devices. However, as already explained, the vertical fixed-reception markets are the main targets of the present approach. Apart from that, it is interesting to clarify that matter and we included a brief comment in the eighth paragraph introduction.

Responses to the comments of Reviewer #4

[1] Comments to the Author

This work presents a methodology to change the behavior of hardware components of TV receivers using FPGA dynamic reconfiguration based on digital TV signal content. Several hardware behaviors are already synthesized into configuration bitstreams. These bitstreams are sent using the same packeting method as other broadcast information (video, audio etc).

Remarks:

*abstract

reassemblies >

reassemblies

Response: It has been corrected.

[2] *Figure 3:

Video

"DENC" never explained before!

Response: DENC was defined in the paragraph above Figure 3.

[3] Unify the use of demultiplexer and demultiplexer

Response: Now we use only demultiplexer.

[4] *5.D

"The above rates this range have similar values ..." sentence not clear

Response: It has been corrected and extended, with a richer explanation.

[5] The FPGA used for implementation tests is not mentioned

Response: The test environment was described in the second paragraph of section V.F.

[6] The FPGA frequency that gave the timing results is not mentioned

Response: The test environment was described in the second paragraph of section V.F.

[7] *Tables 7 and 8 have the same title !

Response: It has been corrected.

[8] *comparison with litterature

In related works, the transmitted signal is not changed and the use of local predefined hardware configurations in the receiver is applied. In comparison, does the presented approach need to modify in a certain way the broadcast standard? In that case, what is the

impact on existing materials using such broadcast standard and is it simpler than continuously update the receiver with new configurations?

Response: Yes. Indeed, the proposal itself, as shown in section V, is based on an extension of the existing SI standards. In addition, it can be done as a proprietary solution, given that it has no impact on current structures. However, the complete framework proposed here is prominent and leaves no loose ends regarding feature updates towards FPGA devices, in digital TV environments, while a myriad of proprietary solutions would require more bandwidth (in order to update all different platforms, even using the same FPGA devices) and are more time consuming to implement. A discussion regarding such matter was included in section V.E.