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Single Event Transient Injection on an Operational Amplifier: A Case Study

John M. Espinosa-Duran, Jaime Velasco-Medina, Gloria Huertas, Raoul Velazco, Jose L. Huertas

***Abstract*—This paper reports a case study about effects produced by the radiation Single Event Transient (SET) injection on a custom operational amplifier. SETs were injected in the operational amplifier transistors in order to evaluate their sensitivity to the radiation transient faults. The circuit was designed using a non-rad-hard AMS-CMOS 0.8µm process. In this case, simulation results allow us to identify the operational amplifier most sensitive transistors. This work will form the basis to further development of design techniques for radiation hard analog circuits.**

***Index Terms*—Single Event Transient (SET), Single Event Simulation, Operational Amplifier, On-line Testing, Radiation Effects.**

I. INTRODUCTION

RADIATION-HARD Operational Amplifiers (OpAmp) are very used in radiation environments, such as nuclear weapons, nuclear reactors, particles accelerators and obviously in satellites and spaceships where can be found high energy particles (from *KeV* to *GeV*) [1].

Previous works on radiation-hard OpAmp are presented in [2], [3] and [4]. These works consider solutions at mask layout, fabrication process and system level. But these did not perform a hardening technique at circuit level.

The goal of this work is to analyze the OpAmp response to Single Event Transient (SET). In this case, SET injection allows the designer to identify the critical points of the OpAmp in order to look for design techniques to protect the OpAmp of these faults. SET injection simulation results will be valuable to design a rad-hard OpAmp suitable to be used in the design of radiation-tolerant switched-capacitor circuits.

This paper is organized as follows. In Section II, the OpAmp general characteristics are given. In Section III, the SET injection simulation results are analyzed. And finally, in Section IV conclusions and future work are presented.

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J. M. Espinosa-Duran and J. Velasco-Medina are with the Escuela de Ingenieria Electrica y Electronica, Univeridad del Valle, Cali, Colombia (e-mail: {michaele, jvelasco} @univalle.edu.co).

G. Huertas and J. L. Huertas are with the IMSE-CNM, Seville, Spain (e-mail: {gloria,huertas}@imse.cnm.es)

R. Velazco is with TIMA Laboratory INPG, Grenoble, France (e-mail: Raoul.Velazco@imag.fr).

II. OPERATIONAL AMPLIFIER CHARACTERISTICS

The design specifications of a high performance CMOS VLSI amplifier include a very wide unity bandwidth (>100MHz); a fast settling time over a variety of low-load capacitor values, suitability for fabrication in short-channel digital CMOS process, capability of near rail-to-rail input and output voltage, low power dissipation and small area occupancy [5].

The OpAmp designed (see Figure 1), is based on the one proposed in [5]. This is characterized by a near rail-to-rail input stage and a Complementary Folded Cascode (CFC) output, which made it capable to manage capacitive loads between 1pf and 20pF and suitable to be used in both continuous and discrete time domains.

In [6] the OpAmp proposed in [5] is modified, a Built-In Detector (BID) is included into the circuit (corresponding to the transistors M17 and M18 at Figure 1). The BID as is discused in [6], is intended to amplify the effect of the faults (permanent defects), that occurs in any of the OpAmp transistors. The BID is connected at the output of the differential input stage, in order to behave as a follower of the OpAmp input signal and "senses" the variations in the OpAmp currents. In the case studied in this work, the BID will be used to amplify the effect of the SETs in order to facilitate their detection, by comparing the OpAmp output with the BID output, rather than, with the input signal. In this way, it is possible to incorporate an On-Line SET detection capability to the OpAmp.

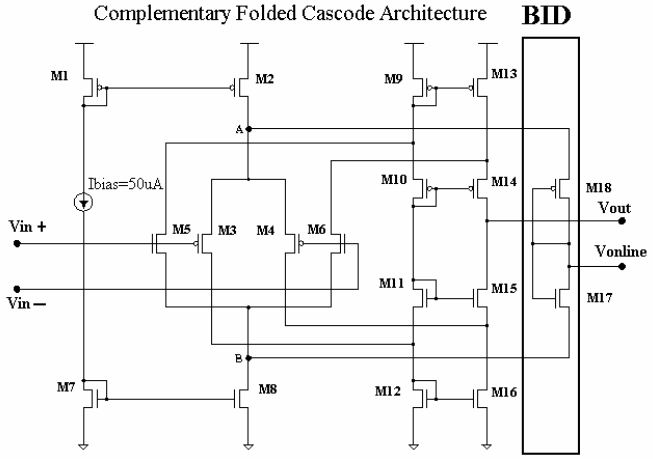

Figure 1. OpAmp with BID [6].

With a bias current of 50µA and capacitive loads (C_{LOAD}) of 1pF and 20pF, the OpAmp designed has respectively an open-loop unity-gain bandwidth of 118.2MHz and 7.67MHz, a phase margin of 47.1° and 87.2°, and a DC gain of 27.56dB, for an implementation in AMS-CMOS 0.8µm process. In order to ensure a symmetrical and compact layout for the matched transistors, the OpAmp employs proportional transistor sizes for the complementary output, current mirrors and differential input stages. Figure 2 shows the SET-free simulation results for the OpAmp in voltage-follower configuration, where the signal *Vonline* corresponds to the BID output.

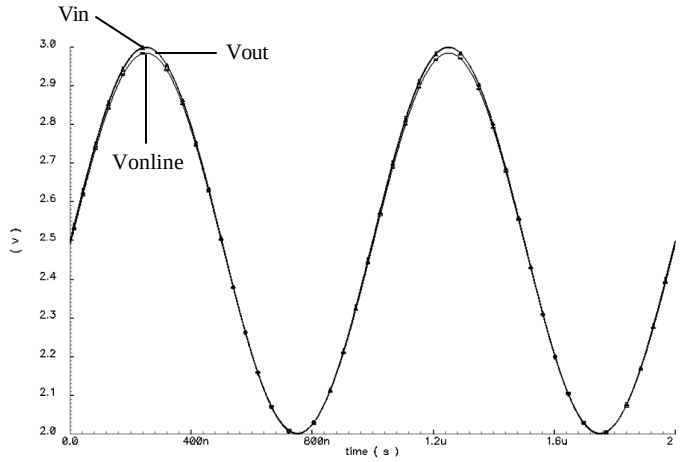

Figure 2. SET-free simulation results for the OpAmp in voltage-follower configuration using as stimuli a sinusoidal signal of 500mV @ 1MHz (C_{LOAD}= 1pF).

III. SINGLE EVENT TRANSIENT INJECTION ANALYSIS

A. SET Simulation Model

A device-level fault model presented in [7] is used to estimate the effects of a SET in the designed circuit. In this work, SETs are modeled using a double exponential current, which emulates the pulse resulting on the affected node.

$$I(t) = I_0 \left(e^{-t/tc} - e^{-t/te}\right) \quad (1)$$

In equation (1), I_0 is approximately the maximum current induced by the charge, *tc* is the collection time of the junction and *te* is the time constant for initially establishing the ion track [7]. According to the data provided in [8], four values of current were selected to be injected: 200µA, 500µA, 1mA and 2mA

B. SET Injection Simulation Results

In order to analyze the SET effects on the OpAmp, SET injection simulations were carried out using the OpAmp in voltage-follower configuration. For the simulations, it is assumed a complete set of single transient faults, modeled by equation (1), in the OpAmp transistors. The typical operation conditions of C_{LOAD}=0.1pF and a sinusoidal signal of 500mV @ 10MHz as input were used during the simulation of the SET injection.

SET injections were performed during simulation time and were analyzed according the following criteria:

- Analysis of changes in the output voltage
- Verification of the effects at the injection points

Since this OpAmp is for safety critical applications, it is considered that a SET produces an error, when the difference between signals (*Vout- Vin* and *Vout -Vonline*) is higher than a 1% of the input voltage, over the offset voltage. Adjusting this threshold to any particular application may be needed.

Already has been demonstrated that the SET effects depend of the bias conditions of the transistor [7]. In analog circuits, the bias conditions of each transistor are not like in digital circuits, for which only two states are possible for the transistors: *on* or *off*. Nevertheless, in this work three states are defined, because they are considered the most interesting conditions: the High Conduction State (HCS), similar to the *on* state in digital circuits, which corresponds to the state when the drain current of the transistor achieves its highest value; the Low Conduction State (LCS), similar to the *off* sate in digital circuits, which corresponds to the state when the drain current of the transistor achieves its lowest value; and the Intermediate Conduction State (ICS), not present in classical digital circuits, which is the state when the drain current is nearly the same for both, the NMOS and the PMOS, transistors of a the complementary pair. These three states are the most relevant because these are the cases when the collection junction (the p-n junction of the drain) is direct, reverse or transition biased. The SETs were mainly injected during each one of these states for every transistor in order to verify during which state the SET effects are higher. It is important to take in account that the state of PMOS transistors at a specific time (for a specific stimulus), is not the same for all of them. The same occurs for NMOS transistors.

C. Analysis of changes in the output voltage

As was mentioned in Section I, the BID was included to amplify the effect of the SETs in order to facilitate their detection, by comparing the OpAmp output with the BID output, rather than with the input signal. However, to demonstrate the effectiveness of the BID, the OpAmp output was also compared with the input. Figure 3 shows simulation results for *Vout – Vin*, from these results the 86% of the SETs were detected. Figure 4 correspond to the worst effect obtained from these results, which correspond to a SET injected in the PMOS transistor M3, during its LCS at 125ns, with a maximum difference between signals of 2.72V and a duration of 69.78ns. The worst effect of the SETs injected in NMOS transistors corresponds to M5 during its LCS at 175ns, with a maximum difference between signals of 2.01V and a duration of 65.36ns. The minor effects correspond to the SETs injected in M2 and M7 (always conducting because these are the PMOS and NMOS transistors of the input-stage current-mirror); in both cases, only 8 of the 36 SETs injected in each transistor were detected. The longest effects correspond to the

SETs injected in M3 at 150ns, with a duration of 100.39ns and a maximum voltage difference of 2.22V and in M6 at 175ns, with a duration of 75.79ns and a maximum voltage difference of 1.10V (these correspond to the PMOS and NMOS transistors of the differential input stage connected to Vin-), which correspond to the ICS for both cases. The shortest effects correspond to SETs injected in M2 and M8.

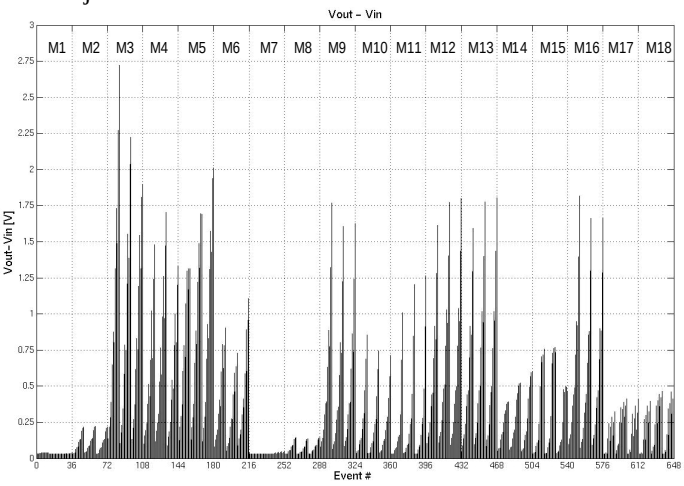

Figure 3. Simulation results for the SETs injected at the OpAmp. SET effects obtained from *Vout –Vin*. The letters and numbers above indicate which transistor correspond these data.

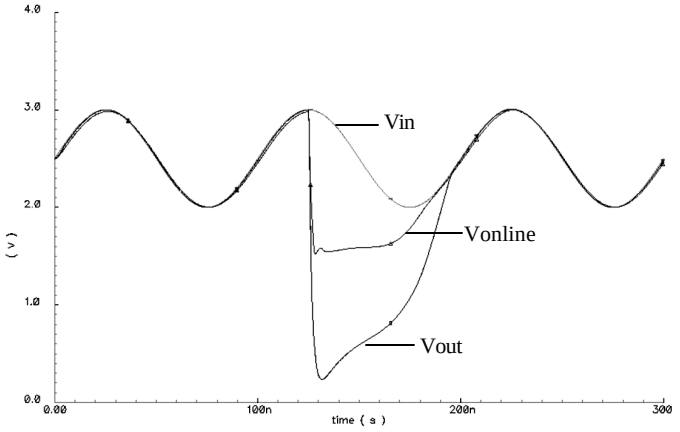

Figure 4. The worst effect obtained from *Vout – Vin*, corresponding to a SET injected in M3 at 125ns

On the other hand, Figure 5 shows simulation results for *Vout – Vonline*, from these results the 94% of the SETs were detected. Figure 6 corresponds to the worst effect obtained from these results, which corresponds to a SET injected in the NMOS transistor M6, during its ICS at 175ns, with a maximum difference between signals of 1.60V and a duration of 78.09ns. The worst effect of the SETs injected in PMOS transistors corresponds to M4, during its ICS at 175ns, with a maximum difference between signals of 1.40V and a duration of 88.58ns. The minor effects correspond to the SETs injected in M1 and M7 (always conducting because these are the PMOS and NMOS transistors of the input- stage current-mirror connected to *Ibias*). The longest effects are the same obtained for *Vout - Vin*. The shortest effects correspond to SETs injected in the PMOS transistor M9 and the NMOS transistor M11. In this case, the effect produced by a SET at any of the transistors of the input differential pair, M3 and M5, is minor that in the case *Vout-Vin*, due to the fact that SET in these transistors is interpreted by the BID as part of the input signal. In that way, the BID output, *Vonline*, tries to follow this with no much success, allowing us to measure a smaller error than in the initial case and therefore M3 and M5 do not appear as the worst cases.

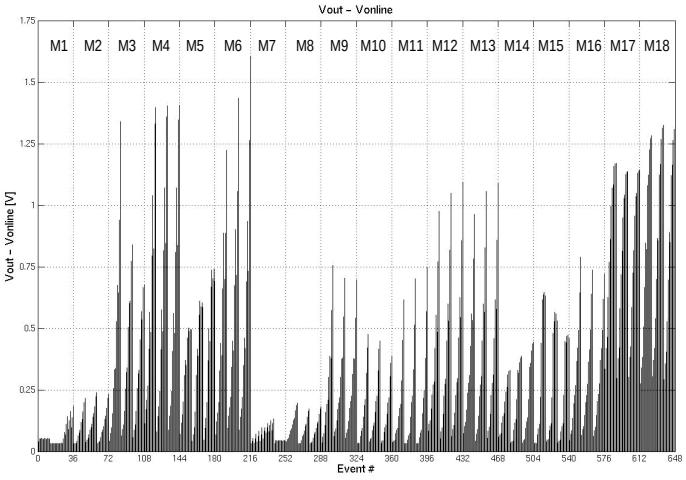

Figure 5. Simulation results for the SETs injected at the OpAmp. SET effects obtained from *Vout –Vonline* The letters and numbers above indicate which transistor correspond these data.

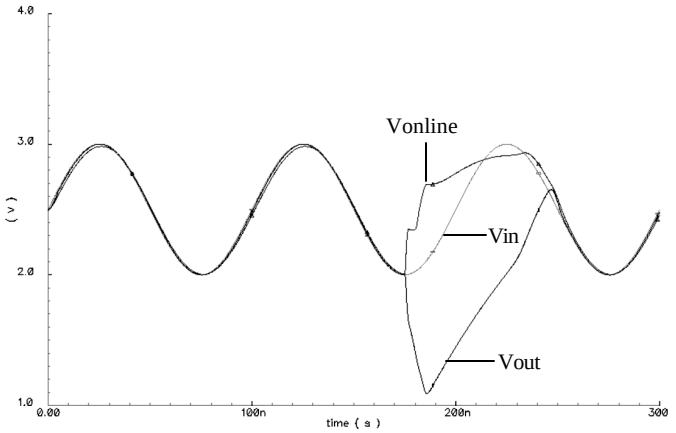

Figure 6. The worst effect obtained from *Vout – Vonline*, corresponding to a SET injected in M6 at 175ns

From the simulation results presented in Figure 4 and Figure 5, it is possible to obtain some information:

- The OpAmp response is more sensitive to the SETs injected in transistors M3, M4, M5 and M6. It should be clear that, using any of the measurements, it is possible to detect the SETs at these transis tors. It is important to take in account that these are the biggest transistors in the OpAmp.
- The results show that, in average, PMOS transistors produce larger errors than NMOS transistors (for PMOS transistors the average for *Vout-Vin* is 0.41V and for *Vout-Vonline* is 0.34V, for NMOS transistors the average for *Vout-Vin* is 0.36V and for *Vout-Vonline* is 0.33V). It is important to clarify that the PMOS transistors are (at

least), 1.5 times bigger than their NMOS counterpart, which can be interpreted as a bigger charge collection area, therefore a bigger current flow.

- The OpAmp response is less sensitive to the SETs injected in the transistors M1, M2, M7 and M8, but these SET effects are more visible using the *Vout-Vonline*.
- The longest effects produced by a SET, occurred during the ICS and the minor effects occurred during the HCS and in transistors that are always conducting with no so much variation (e.g. current mirror transistors M1 and M7). Most of the worst effects occurred during the LCS.
- The current-mirror PMOS transistors of the CFC output stage, M9 and M13, present a high sensitivity to produce errors when a SET occurs. This is possible due to their high collection area, and to the fact that they are the responsible to provide most of the current that the circuit needs. In that way, this pair of transistor "senses" any change in the current of the others transistors.
- The remaining transistors of the CFC exhibit what can be consider as a normal sensitivity, in the way that a SET occurring in any of these transistors, will produce an error within the limits established by the SET effect of others transistors.
- The effect of the SETs in the BID transistors is higher for the case *Vout – Vonline*. This is due to the fact that SETs affect more the BID output than the OpAmp Output. This can be observed in more detail in Figure 7, which presents the worst effect of a SET injected at the BID, in M18 during its LCS at 175ns. It should be clear that the effect on the OpAmp output is high enough to be detected, but the effect in the BID output is many times higher.
- The duration of the SETs effects observed are in average shorter than a period of the input signal (the longest is about 100.39ns). In this way, the duration is not a very critical parameter since the SET could be detected rapidly.
- The longest effects occurred during the ICS. This is an interesting result that has to be analyzed in a future work.

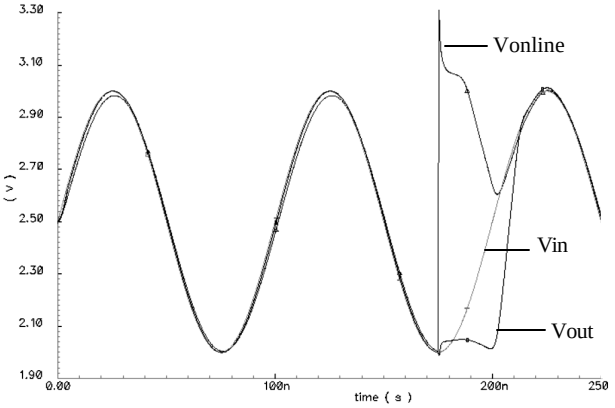

Figure 7. Transient response to a SET injected in M18 at 175ns

D. Verification of the effects at the injection points

In order to verify the results obtained above, the effects produced by SETs in the transistors operation conditions are analyzed, taking as reference measurements the drain voltage and current. Figure 8 shows the variations in the drain voltage (*Variations in Vdrain*) for every transistor of the OpAmp, for some of the SETs injected. Figure 9 corresponds to the worst effect obtained from these results, which corresponds to a SET injected in the PMOS transistor M3, during its LCS at 125ns, with a maximum variation of 2.54V and a duration of 15.85ns. The worst effect of the SETs injected in NMOS transistors corresponds to M6 during it LCS at 175ns, with a maximum variation of 1.89V and a duration of 17.18ns. The minor effects correspond to the SETs injected in M3 and M5, which correspond to the lowest and shortest SETs injected. The longest effects correspond to the SETs injected in M3 at 150ns (with a duration of 97.52ns and maximum variation of 229mV), and in M6 at 175ns (with a duration of 79.92ns and a maximum variation of 1.77V), which correspond to the ICS for both cases. The shortest effects correspond to SETs injected in M3 and M12. The above results are in agreement with the results obtained in the Section C, which indicated that the most sensible transistors are located in the differential input stage.

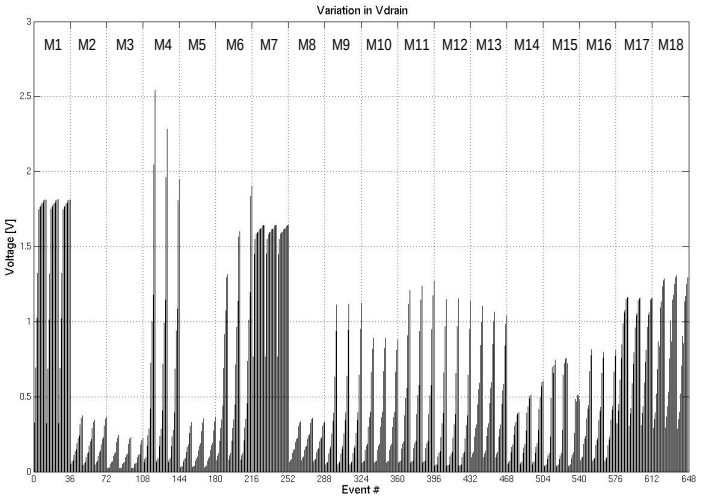

Figure 8. Simulation results for the SETs injected at the OpAmp. SET effects obtained from *Variations in Vdrain*. The letters and numbers above indicate which transistor correspond these data.

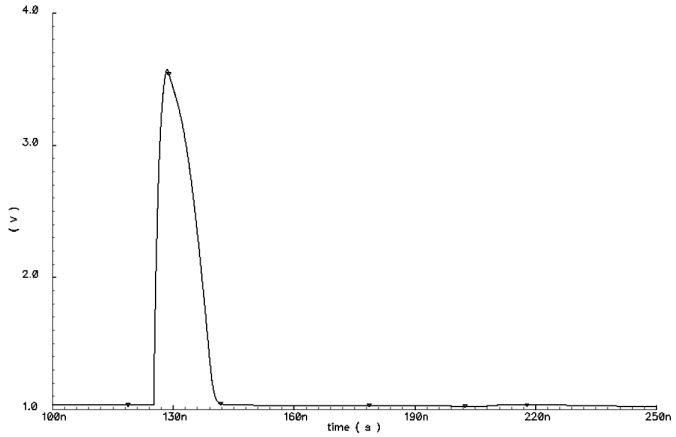

Figure 9. Variation in the drain voltage of M4 due to a SET injected at 125ns

In real life and device simulation [8], the SET current is generated "inside" the transistor, therefore the current leave the drain. In circuit level simulations, as the carried out in this work, the SET current is generated "outside" the transistor by a pair of exponential current sources, in this way, instead of leaving the drain, current enters towards the drain. Therefore, the maximum drain current was estimated using the SET-free drain current and the drain current during the SET, then the difference between these two signals (in absolute value), was added to the SET-free drain current, and the maximum of the obtained current (called *Drain Current*) was measured. Figure 10 shows the maximum drain current estimated in each one of the transistors for some of the simulated conditions. Figure 11 corresponds to the highest drain current pulse, which is associated to to a SET injected in the NMOS transistor M15, during its HCS at 150ns, with a maximum of 2.71mA and a duration of 37.17ns. In that Figure, the SET pulse is shown with illustrative purposes. The highest drain current pulse for a SET injected in PMOS transistors correspond to M14 during it HCS at 100ns, with a maximum of 2.71mA and a duration of 33.51ns. These data are not in agreement with the results obtained before, due to this pair of transistor is connected directly to the output capacitor, which means that when a SET injection is simulated, the current sources doing this, take the current that they need to inject the SET, from the capacitor with much effort than discharging it, thus the duration of these pulses is really short in comparison with any other drain pulse. The lowest drain current pulses correspond to the SETs injected in M2 and M8. The longest drain current pulses correspond to the SETs injected in M3 at 125ns, with a duration of 106.86ns and maximum of 1.24mA, and in M6 at 175ns, with a duration of 81.54ns and a maximum of 1.16mA,. The shortest effects correspond to SETs injected in M2 and M8. The above results are in agreement with the results obtained in the Section C, which indicated that the most sensitive transistors are located in the differential input stage and the less sensitive ones in the input-stage current -mirrors.

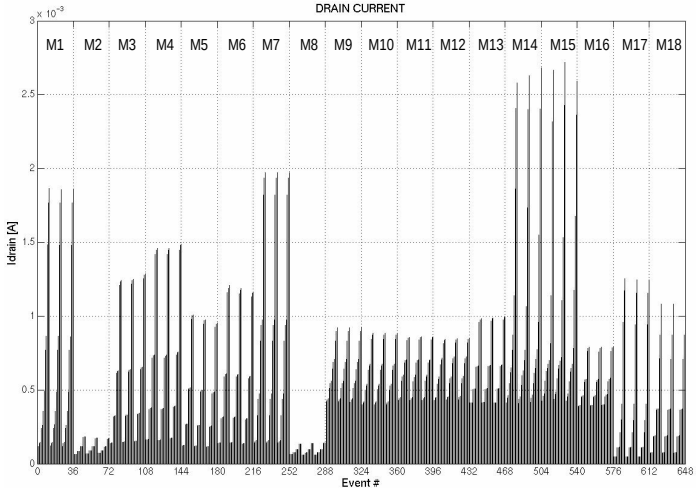

Figure 10. Simulation results for the SETs injected in the OpAmp. SET effects obtained from the *Drain Current*. The letters and numbers above indicate which transistor correspond these data.

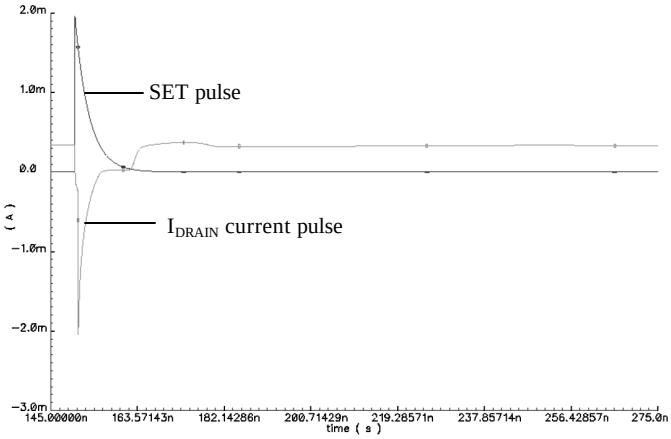

Figure 11. The highest drain current pulse estimated corresponding to a SET injected in M15 at 150ns

IV. CONCLUSIONS AND FUTURE WORK

This work has analyzed the effect of SET on a complementary folded cascode operational amplifier implemented in a non-rad-hard AMS-CMOS 0.8µm process. A BID, used in other references [6], is implemented to facilitate the detection of the SET.

The BID addition into the OpAmp allows to increase the detection of the SETs, from a 86 % without considering the BID output, to a 94% considering it. This BID can be use as part of a On-Line SET detection approach for the OpAmp.

The simulation results allow us to conclude that the PMOS are more sensitive than the NMOS, to produce errors due to SET. Furthermore, that SETs occurred during the transistor LCS, produce larger errors than, those occurred during HCS. In this way, the most sensitive transistors are those of the differential input stage: M3, M4, M5 and M6, and the least sensitive are those of the input-stage current-mirror: M1, M2, M3 and M4. The other transistors exhibit a sensitivity within the limits established by the group of transistors mentioned above

The current-mirror PMOS transistors of the CFC output stage, M9 and M13, present a high sensitivity to produce errors when a SET occurs. This is possible due to their high collection area, and to the fact that they are the responsible to provide most of the current that the circuit needs. In that way, this pair of transistor "senses" any change in the current of the others transistors

The effect of the SETs in the BID transistors is higher for the case *Vout – Vonline*, which is due to the fact that SETs affect more the BID output than the OpAmp Output

The bias conditions of the transistors during the ICS have to be studied in more detail, since during this state the longest effects produced by a SET occurred.

Future work will be oriented to the design of radiation-tolerant switched-capacitor filters, combining the approach applied here with other test techniques such as Oscillation-Based Test (OBT) [9]; and will be directed to extend the use of the BID to others OpAmp architectures.

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