A Bias-Dependent Single-Event Compact Model Implemented Into BSIM4 and a 90 nm CMOS Process Design Kit

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***Abstract*—A single-event model capable of capturing bias-dependent effects has been developed and integrated into the BSIM4 transistor model and a 90 nm CMOS process design kit. Simulation comparisons with mixed mode TCAD are presented.**

***Index Terms*—Integrated circuit radiation effects, MOSFETs, single-event effects, SPICE.**

I. Introduction

In this paper, we present a single-event compact model that captures the dynamic charge collection signatures observed in the response of sub-100 nm CMOS circuitry characterized by 3-D technology computer aided design (TCAD). The model utilizes a simple, efficient, and portable implementation with very few calibration parameters to accurately capture the bias-dependent single-event photo current. This model has been inserted into the BSIM4 transistor model and integrated with a Cadence-based 90 nm bulk CMOS process design kit (PDK) [1]–[3]. Comparisons of 3-D mixed-mode TCAD simulations and the bias-dependent single-event compact model are presented.

II. Background

A. Observations From Testing and TCAD

Circuit response times are now comparable with the characteristic times for single-event charge deposition and collection, meaning that the charge collection process dynamically interacts with and is "shaped" by the circuit response. With transient pulse widths approaching the period of GHz clock cycles, the time width of the pulse has become a key metric of circuit response [4], [5]. The transient shape of the pulse is critical to accurate circuit vulnerability predictions.

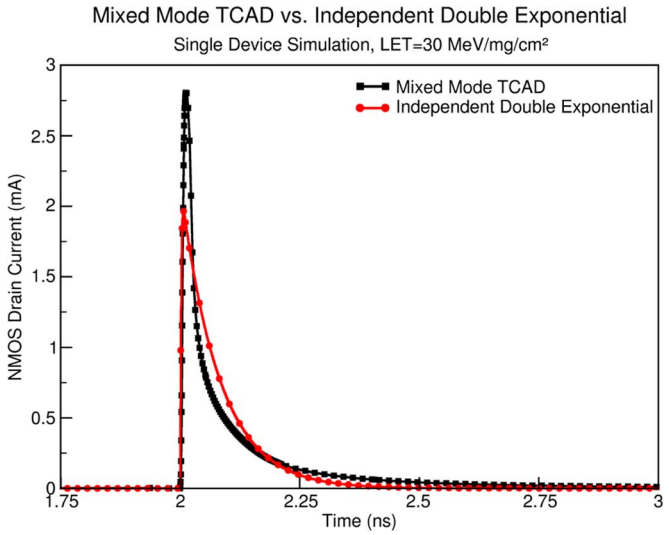

Fig. 1. Comparison of nMOS drain current in TCAD mixed-mode simulation of a single nMOS transistor and a SPICE double exponential current source. The resulting currents have similar time constants, peak currents, and total integrated charge.

Three-dimensional device simulations, utilizing mixed SPICE and TCAD, have been used to study the details of single-event effects (SEE) in deep sub-micron technologies [6]–[9]. These simulations have revealed the importance of capturing the bias-dependent characteristics of the generated single-event photo currents in order to accurately predict circuit upsets and errors. These simulations have also shown that the single-event currents in deep sub-micron technologies are not accurately modeled in circuit simulations using only the ideal independent double exponential current source [6], [7], [10].

However, when single-event effects are simulated in single devices in TCAD with ideal fixed voltage rails, the double exponential waveform is still a close approximation of the device response. Fig. 1 shows a comparison of the nMOS drain current from a single-device TCAD simulation and a double exponential waveform that has approximately the same time constants, peak current, and total accumulated charge. Because the

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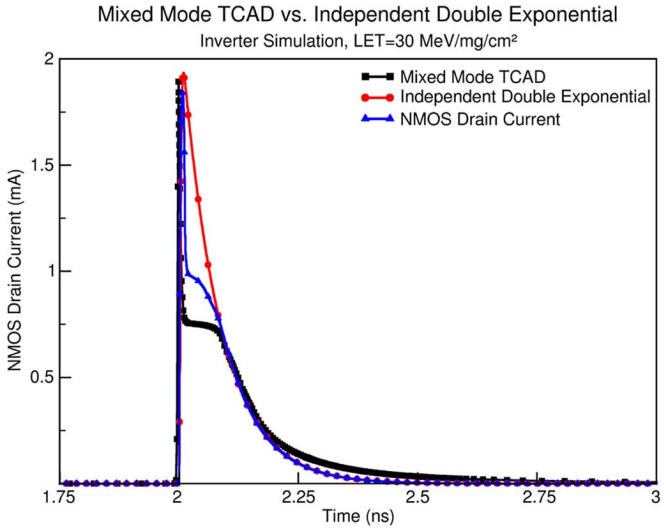

Fig. 2. Comparison of nMOS drain current in TCAD mixed-mode and SPICE simulation of an inverter, where the SPICE simulation used an independent current source to model the single-event pulse. The double exponential parameters from Fig. 1 were used in this simulation, as shown by the Independent Double Exponential (ISEE) plot. It can be observed that the integrated charge is different between the TCAD simulation and the nMOS drain current resulting from the use of an independent double exponential source.

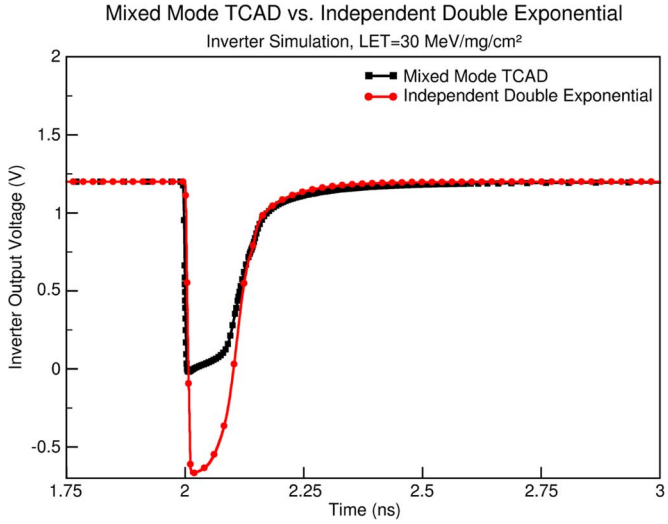

Fig 3. Comparison of TCAD and SPICE simulated inverter output voltages (NMOS drain voltages) shows the SPICE output voltage is forced well below the negative rail, but the TCAD simulated output voltage does not demonstrate this behavior.

single-device response is still closely approximated by a double exponential waveform, it has been used as a base function in other modeling approaches [14], and is used as a base function in this bias dependent model. The use of this waveform is discussed in detail in Section III.

In SPICE circuit simulations, the ideal independent double exponential current source does not accurately reproduce the results seen in mixed mode TCAD. Fig. 2 shows a comparison of the nMOS drain current from an inverter simulated in TCAD mixed mode and SPICE, where an independent double exponential current source was used to model the single-event current in SPICE. The double exponential current source was connected to the nMOS drain node and to the nMOS body node. These connections are external to the intrinsic SPICE MOSFET drain and body resistances. Additionally, the nMOS body is often tied directly to ground or a fixed VSS voltage in SPICE simulations, thus the current source is pushing current into an infinite current sink. The nMOS drain voltage is a function of the Ohm's Law relationship of the pMOS load resistance and the current being pulled through that resistance by the independent current source. As a result, the independent current source will force the nMOS drain below ground or the VSS voltage rail until the nMOS body diode turns on and the resulting diode current compensates the independent current source. Mixed mode TCAD simulations do not demonstrate this behavior because the single event current is a result of charge that is generated within the TCAD device. Fig. 3 shows the inverter output voltage (NMOS drain voltage) comparison for TCAD and SPICE simulations utilizing ideal independent double exponential current sources.

TCAD simulations of deep sub-micron devices have revealed an elongated "plateau" effect in the single-event generated current. The plateau effect has been observed in mixed-mode TCAD simulations of inverter chains, where the pMOS drive current limits of the plateau amplitude [6]–[10]. DasGupta showed that the width of the plateau directly controls the width of the propagating SET voltage pulse [10]. This "plateau" is dependent on the bias of the device and the surrounding circuitry's ability to source or sink the single-event generated current to restore the perturbed circuit node [6], [7], [10]. Fig. 4 shows the nMOS drain currents from a mixed mode TCAD simulation for multiple linear energy transfer (LET) values [9], [11]. For small LET values, the drain current is still well approximated by a double exponential waveform. However, with increasing LET, the drain current is clamped at the pMOS drive current.

B. Other Modeling Approaches

There have been other attempts to model these effects, ranging from piece-wise linear current sources to models that utilize many additional SPICE components to calculate the appropriate photo current response [12]–[14]. Piece-wise linear (PWL) based models have been derived from mixed mode TCAD simulations or from measured test data [12], [13]. While the PWL model accurately captures the characteristics of the single event current, it is inherently not scalable to other bias conditions, LET values, or device sizes. This implies that TCAD simulation or test data would need to be obtained for each desired SPICE simulation case. Additionally, as Turowski and Mavis have both observed, SPICE independent current sources can force unrealistic voltages at circuit nodes and the currents do not change with bias, as mixed-mode TCAD simulations have shown [7], [14].

Mavis *et. al* presented a bias-dependent model, the equivalent circuit model (ECM), that captures the plateau effect [14]. The ECM is implemented using a series of dependent current and voltage sources. These dependent sources are used to calculate the response of the single event current to the change in device bias. Because this model uses standard SPICE components, it has the potential to be portable across SPICE simulators.

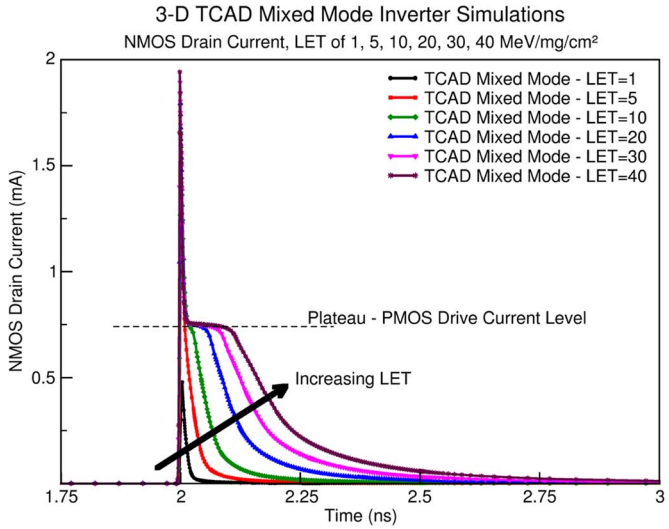

Fig. 4. 3-D TCAD mixed mode simulations results showing single-event induced nMOS drain current for various LET values. Low LET currents can be approximated by a double exponential waveform. As LET increases, the single-event induced drain current is clamped at a level equal to the pMOS drive current.

The ECM, however, uses many dependent SPICE components that must each be characterized, programmed, and calibrated for each technology and kernel function. Additionally, the presented implementation of the ECM is a subcircuit attached to a circuit node rather than being internal to the MOSFET model's intrinsic drain/source and body resistors.

C. Designer Use

The value of any modeling approach is increased tremendously by the ability of a circuit designer to use the model in his standard tool flow, without modifying the model by adding additional components. For the designer to maximize the usability of a radiation enabled model, it must be integrated with the tool flow and the process design kit. Ideally, model integration with the tool flow and the PDK are done in a manner that is almost transparent to the designer. In this work, we have integrated the bias dependent single-event model with a Cadence based 90 nm bulk CMOS PDK and the underlying BSIM4 transistor model [1]–[3].

III. Model Overview

Our bias-dependent single-event model has been implemented using the Verilog-AMS behavioral modeling language and has been inserted inside the SPICE BSIM4 transistor model for simulation in Cadence Spectre based commercial process design kits [1], [3], [15]. This integration, discussed in Section IV, has been achieved using the Lynguent ModLyng Integrated Modeling Environment (IME) [12], [16], [17]. The model is comprised of a system of four equations that calculate the bias dependent single-event current. These equations are presented in Section IV. For the purpose of visualizing and explaining the function of each part of the model, Fig. 5 shows a schematic representation using standard SPICE components.

The calculation portion of the model consists of four branches, and the current applied to the transistor is a mirror of

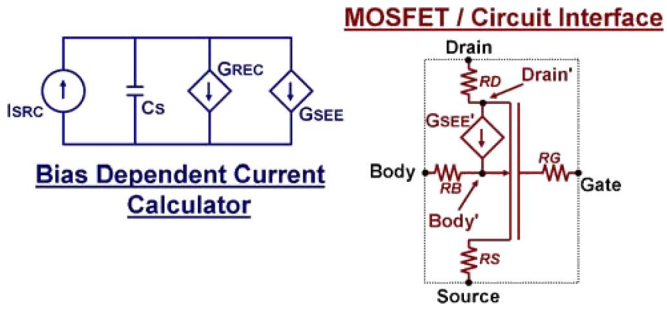

Fig. 5. Schematic representation of the bias dependent junction single-event model with an nMOS transistor. G'_{SEE} is a mirror of the G_{SEE} source with an optional gain factor as shown in Equation (4).

one of the branches. The independent current source, I_{SRC}, represents the basic time-current profile for depositing the desired amount of charge to the device. The integrated value of this source is the total amount of charge deposited in the system. In this work, I_{SRC} is implemented as a double-exponential current source, which is easily implemented, has good convergence in SPICE simulations, and still represents the basic single-event current waveform for single MOSFET devices, as shown in Fig. 1. The capacitor, C_S, is used to ensure charge conservation. Its value is not critical (outside of numerical considerations) and does not represent a physical capacitance. The voltage across the capacitor is proportional to the charge that has not been dissipated by the two dependent source branches.

The G_{REC} dependent current source accounts for recombination currents in the device, and the function and parameterization of this source are discussed at the end of this section. The G_{SEE} and G'_{SEE} dependent current sources represent the single-event junction current and are internal to the BSIM4 transistor model elements with access to all internal nodes and voltages. The current through G_{SEE} is a calculated value that is proportional to the voltage across C_S and is a function of the voltage across the internal transistor junction. The internal drain side of the junction is denoted as drain', and the internal body is likewise denoted as body'. If the drain'-body' junction is reverse biased, the calculated G_{SEE} current will follow the current generated by I_{SRC}. As the drain'-body' junction voltage collapses and approaches 0 V, the current through G_{SEE} is also reduced and will "plateau" at the limited supply current level, as determined by the surrounding circuitry. G'_{SEE} is a mirror of G_{SEE} and flows directly into the transistor. G_{SEE} is not directly connected to the transistor to isolate the calculation portion of the model from any undesired external influences, such as those that may charge C_S and cause errant charge collection. Additionally, this separation provides the ability to account for parasitic bipolar junction transistor (BJT) amplification in the MOSFET single-event current by making G'_{SEE} proportional to G_{SEE} by a factor greater than 1.0. With additional characterization of the parasitic BJT in the MOSFET device, the amplification factor can also be implemented using standard BJT current and voltage equations.

The dependent current source G_{REC} is the recombination current. Its value is typically small for cases where there is little bias change. However, when the bias collapses and the

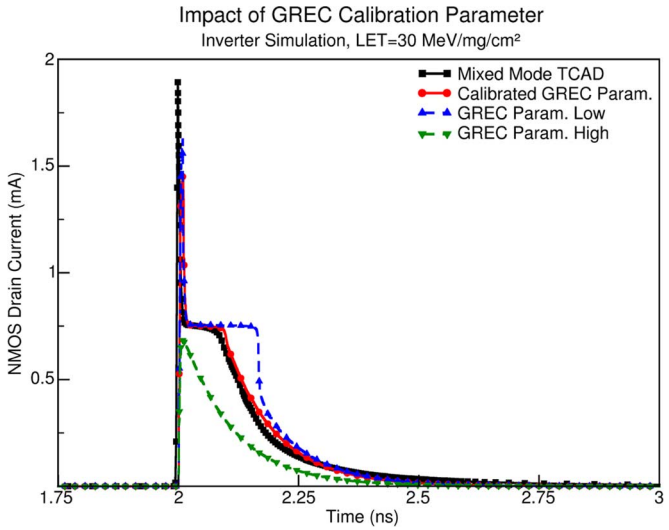

Fig. 6. The calibration parameter in the G_{REC} component controls the width of the plateau for a technology. As the parameter value is decreased, the plateau widens. If the parameter is too large, the ability to reproduce the plateau will be eliminated. Calibration of the G_{REC} component is best achieved using TCAD or test data that shows a plateau response.

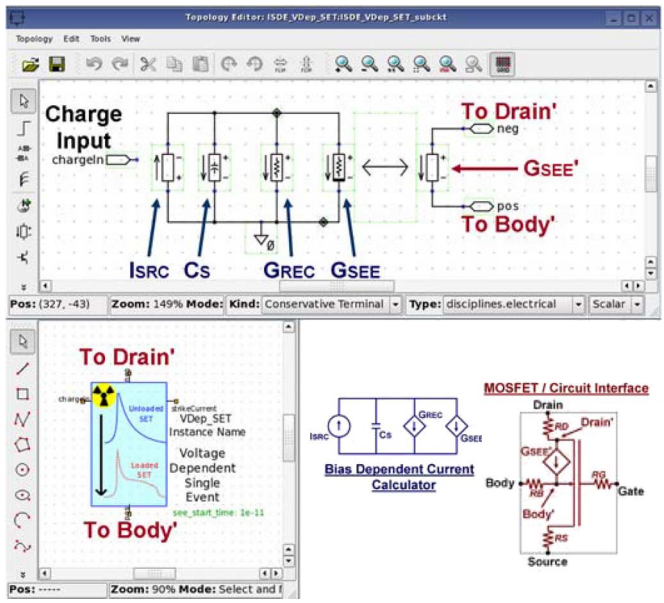

Fig. 7. The bias dependent single-event model is implemented in the ModLyng IME. The ModLyng schematic representation of Equations (1)–(4) and the ModLyng symbol are displayed. The schematic presented in Fig. 5 is included in the bottom right for reference.

G_{SEE} current is limited by the circuit, the G_{REC} current allows the voltage across C_S to decrease, shortening the length of the plateau. The value of G_{REC} is related to the minority carrier lifetimes in the device. We have observed that the calibration parameter for G_{REC} in a technology is related to the width of the plateau and falling edge time constant of the current pulse, as shown in the higher LET conditions from Fig. 4.

In its basic form, using deposited charge as the input parameter, the model has only one calibration parameter in G_{REC}, the $RecombParameter$ in (2), which is related to the lifetime of the carriers in the target technology. We have observed that the single calibration parameter should be fit to TCAD or data results that demonstrate a plateau effect. We have observed that the calibrated $RecombParameter$ value is applicable over a wide rage of deposited charge values in a given technology. Fig. 6 demonstrates the functionality of the calibration parameter in G_{REC} and shows its impact on the overall pulse shape.

The model is also easily expandable to allow parameterization of the I_{SRC} time-current profile function. The input parameter may also be changed to LET if the collection track length is known. The deposited charge could be calculated dynamically using the approximation that a charged particle with an LET of $30\ \mathrm{MeV}-\mathrm{cm}^2$ deposits $\sim 300\ \mathrm{fC}/\mu\mathrm{m}$ of track length [18].

IV. BSIM4 and PDK Integration

The model, presented in schematic form in Fig. 5, has been implemented using the Verilog-AMS behavioral modeling language with the system of equations,

$$I_{SRC}(t)+\frac{C_S dV(C_S)}{dt}=G_{REC}(t)+G_{SEE}(t) \quad (1)$$

$$G_{REC}(t)=f\left(V(C_S),C_S,\mathrm{RecombParameter}\right) \quad (2)$$

$$G_{SEE}(t)=f\left(V(C_S),C_S\right)f\left(V(drain',body')\right) \quad (3)$$

$$G'_{SEE}(t)=G_{SEE}(t)\times\mathrm{Gain} \quad (4)$$

that solve the differential equation for the four branches in the calculation portion and multiply the G_{SEE} output value by a gain factor. In this work, the gain factor is 1.0. The bias dependent single-event model has been inserted into the BSIM4 transistor model using the ModLyng IME [2], [16], [17]. The BSIM4 transistor model in the ModLyng IME is a Verilog-AMS implementation of BSIM4 and has been validated against the Cadence Spectre BSIM4 model [17]. The behavioral implementations of the BSIM4 and the single event model provide a means of connecting the single-event model to internal BSIM4 nodes. These internal connections are not possible using standard SPICE or Spectre releases of transistor models (without significant source code modifications). This internal insertion ability allows the model to perform its calculations using internal MOSFET node biases and is internal to the intrinsic drain/source and body resistances. This unified model provides increased fidelity and efficiency during simulation. The resulting single-event enabled BSIM4 model is a drop in replacement for the BSIM4 transistor model in the Cadence Spectre simulator. ModLyng uses a graphical representation of the Verilog-AMS code that shows the branches and flows within the code in a schematic format. Fig. 7 shows the ModLyng representation of the bias dependent single-event model. Fig. 8 shows the BSIM4 model schematic in the ModLyng IME. The insertion point for the single-event model is highlighted in the BSIM4 schematic.

In the PDK, the transistor model with the integrated bias dependent single-event model is used in the same manner that the PDK electrical models are used. The selection of the single-event enabled model is done by simply changing an include file in the list of model files. This change replaces the original PDK included nMOS and pMOS primitive models

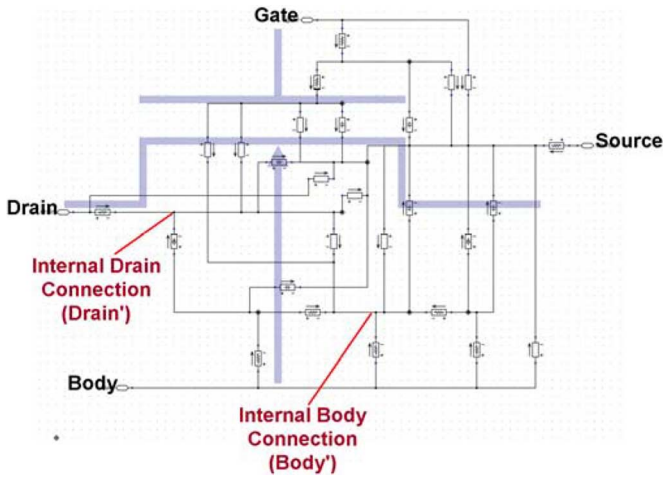

Fig. 8. The ModLyng IME provides a graphical representation of the Verilog-AMS version of the BSIM4 transistor model. The internal connection points, drain' and body' are highlighted. The symbol for the bias dependent single-event model, shown in Fig. 7, is connected to these internal connection points. The external MOSFET terminals are annotated, and a symbol of an NMOSFET has been overlaid for reference.

with the enhanced, single-event enabled nMOS and pMOS models that use the ModLyng BSIM4 with the bias dependent single-event model. This integration follows the typical design flow and model usage, and it eliminates the need to modify circuit schematics to include additional components for simulating single-events.

V. Simulation Results

The integrated BSIM4 and bias-dependent model has been compared to 3-D mixed-mode TCAD simulations of an inverter in a bulk 90 nm CMOS process [9], [11]. This inverter has a pMOS to nMOS width ratio of 2.5/1. The bias-dependent model shows excellent agreement with the mixed-mode TCAD results. Additionally, the bias-dependent model does not force the output voltage of the inverter below the rail as the independent current source was shown to do in Fig. 3. Fig. 9 shows the nMOS drain current and inverter output voltage resulting from 3-D mixed mode TCAD and simulations using the bias dependent single-event model for various amounts of deposited charge.

VI. Conclusion

A single-event model has been developed that is capable of capturing the bias-dependent effects observed in recently published 3-D mixed-mode TCAD and test data. Specifically, the model is capable of reproducing the current limited "plateau" effect and includes additional capability to factor in effects such as recombination and parasitic bipolar transistor gain. The model has been implemented in a simple, efficient, and portable manner with a limited number of calibration parameters. Using the Lynguent ModLyng IME, the model has been integrated inside the BSIM4 model and a Cadence 90 nm bulk CMOS PDK. Simulations using the integrated BSIM4 transistor and bias-dependent single-event model have shown good agreement with 3-D mixed-mode TCAD simulations. Simulating the

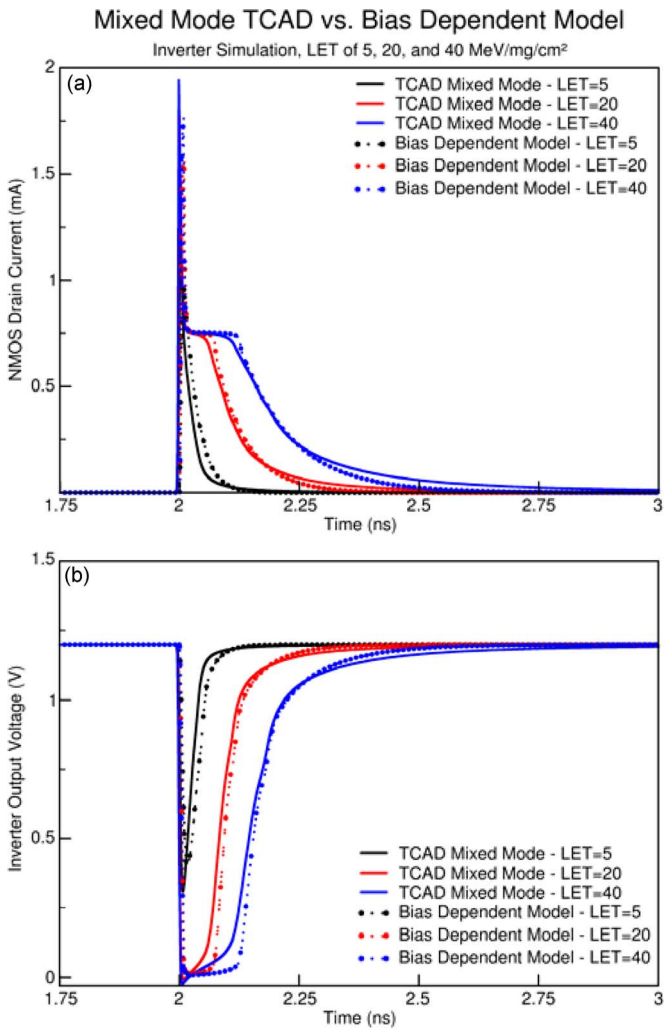

Fig. 9. The nMOS drain current (a) and the inverter output voltage (NMOS drain voltage) (b) from 3-D mixed mode TCAD and Spectre simulations using the bias dependent single-event model for various amounts of deposited charge. Deposited charge has been converted to approximate LET values using the approximation that a charged particle with an LET of 30 $\mathrm{MeV}-\mathrm{cm}^2$ deposits $\sim$ 300 $\mathrm{fC}/\mu\mathrm{m}$ of track length [18].

bias dependencies in the single-event response are critical as technologies continue to scale. The integration of the bias-dependent single-event model, the BSIM4 transistor model, and the commercial process design kit provide a powerful analysis tool for integrated circuit designers.

References

[1] Cadence Spectre Circuit Simulator, Release MMSIM6.2 [Online]. Available: http://www.cadence.com/rl/Resources/datasheets/virtuoso_mmsim.pdf

[2] BSIM4 MOSFET Users Manual [Online]. Available: http://www-device.eecs.berkeley.edu/~bsim3/bsim4.html

[3] IBM CMOS9SF PDK, Design Manual and Model Reference Guide, Version 2.0.0.1 2006.

[4] J. M. Benedetto, P. H. Eaton, D. G. Mavis, M. Gadlage, and T. Turflinger, "Digital single event transient trends with technology node scaling," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3462–3465, Dec. 2006.

[5] M. P. Baze, J. Wert, J. W. Clement, M. G. Hubert, A. Witulski, O. A. Amusan, L. W. Massengill, and D. McMorrow, "Propagating SET characterization technique for digital CMOS libraries," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3472–3478, Dec. 2006.

[6] S. DasGupta, A. F. Witulski, B. L. Bhuva, M. L. Alles, R. A. Reed, O. A. Amusan, J. R. Ahlbin, R. D. Schrimpf, and L. W. Massengill, "Effect of well and substrate potential modulation on single event pulse shape in deep submicron CMOS," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2407–2412, Dec. 2007.

[7] M. Turowski, A. Raman, and G. Jablonski, "Mixed-mode simulation and analysis of digital single event transients in fast CMOS ICs," in *Proc. 14th Int. Conf. MIXDES 2007*, Jun. 2007, pp. 433–439.

[8] O. Amusan, A. F. Witulski, L. W. Massengill, B. L. Bhuva, P. R. Fleming, M. L. Alles, A. L. Sternberg, J. D. Black, and R. D. Schrimpf, "Charge collection and charge sharing in a 130 nm CMOS technology," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3253–3258, Dec. 2006.

[9] O. Amusan, L. W. Massengill, M. P. Baze, B. L. Bhuva, A. F. Witulski, J. D. Black, J. R. Ahlbin, R. A. Reed, and M. W. McCurdy, "Mitigation techniques for single event induced charge sharing in a 90 nm bulk CMOS process," in *Proc. 46th IEEE IRPS*, 2008, pp. 468–472.

[10] S. DasGupta, "Trends in Single Event Pulse Widths and Pulse Shapes in Deep Submicron CMOS," M. S. thesis, Dept. Elect. Eng. and Comp. Science, Vanderbilt University, , Dec. 2007.

[11] Synopsis Sentarus Sdevice, Release 2007.12 [Online]. Available: http://www.synopsys.com/Tools/TCAD/Pages

[12] A. M. Francis, M. Turowski, J. A. Holmes, and H. A. Mantooth, "Efficient modeling of single event transients directly in compact device models," in *Proc. IEEE Int. BMAS 2007*, Sep. 2007, pp. 73–77.

[13] V. Ferlet-Cavrois *et al.*, "Statistical analysis of the charge collected in SOI and bulk devices under heavy ion and proton irradiation—Implications for digital SETs," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3242–3252, Dec. 2006.

[14] D. G. Mavis and P. H. Eaton, "SEU and SET modeling and mitigation in deep submicron technologues," in *Proc. 45th IEEE IRPS*, 2007, pp. 293–305.

[15] Verilog-AMS LRM, Version 2.3 [Online]. Available: http://www.eda.org/verilog-ams Aug. 2008

[16] ModLyng Integrated Modeling Environment Lynguent, Inc., 2007 [Online]. Available: http://www.lynguent.com/products/modlyng-IME.html

[17] A. M. Francis, D. Dimitrov, J. A. Holmes, and H. A. Mantooth, "Modeling and analysis method for radiation-induced upsets in modern IC device models," in *Proc. 2008 IEEE Aerospace Conf.*, 2008, pp. 1–10.

[18] L. W. Massengill, "SEU modeling and prediction techniques," in *IEEE NSREC Short Course*, 1993.