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HSPICE model and circuit simulation for a single-event effect caused by ions at different incident positions

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Abstract
A 3D model of the negative-channel metal-oxide semiconductor (NMOS) structure in a 65-nm complementary metal-oxide semiconductor (CMOS) inverter was built based on technology computer-aided design (TCAD) three-dimensional (3D) device simulation software. The single-event effect caused by a heavy ion at different incident positions was simulated and analyzed using the TCAD–HSPICE mixed-mode simulation. Then, an analytical model was established to describe the relationship between the incident position of the ion and the charge collected by the NMOS drain. Finally, an HSPICE simulation approach based on this model was developed and verified by simulations.

Keywords Analytical model · CMOS · HSPICE · SEE · TCAD

1 Introduction

In space environments, single-event effects (SEEs) are important factors causing functional failure and performance degradation of circuits [1–3]. When a CMOS combinational logic circuit is bombarded by an ion, a transient current pulse is generated, and the output voltage exhibits a transient, known as a single-event transient (SET) effect [1–3]. Due to the high cost of SEE experiments and limitations on measurement methods for real circuits under SEEs, structural simulation methods and design of experiments for evaluation of circuit performance under SEEs are very important, requiring establishment of HSPICE models for SEEs to support such circuit simulations.

Previous studies on device-level models for SEEs have covered various aspects. Kauppila et al. built a compact bias-dependent model for SEEs and implemented it into a 90-nm CMOS BSIM4 model, then studied corresponding compact geometry-aware single-event models for sub-50-nm partially depleted silicon-on-insulator technology [4,5]. Saremi et al. provided a physically based predictive model for single-event transients in CMOS device gates [6]. The double-exponential-type current source model has been used by many researchers and engineers to describe the current during a single-event process. Black et al. [7] modified this traditional model by proposing an improved double-exponential current source model. However, a mature SEE model considering different incident positions of the particle, different incident angles, linear energy transfers (LETs), etc. has not yet been built developed.

In this paper, the influence of vertical impact of particles at or near the *p–n* junction of a metal-oxide semiconductor field-effect transistor (MOSFET) was studied. Moreover, an analytical model was established to describe the relationship between the incident position of the particle and the charge collected by the MOSFET drain, and an HSPICE simulation approach based on this analytical model was developed. First, a 3D NMOS TCAD structure was established, then TCAD–HSPICE mixed-mode simulations were carried out. Then, based on analysis of simulation results for particles at different incident positions, an analytical model was established. Finally, an HSPICE simulation approach based on this model was developed and verified by comparison with simulation results.

2 Single-event effect mechanism

A single-event effect is the phenomenon of electron–hole pair generation caused by a high-energy charged particle inci-

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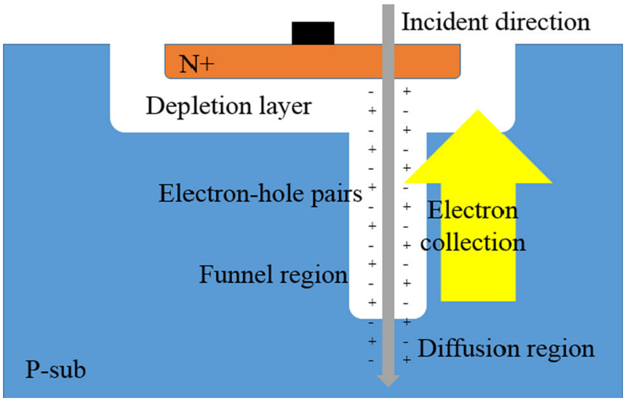

Fig. 1 Diagram of funnel effect

dence on the sensitive area of a device, representing a type of ionization effect. When a high-energy charged particle bombards an integrated circuit, a large number of electron–hole pairs are generated due to its ionization effect, and soft errors can occur in the semiconductor device, including single-event transient (SET), single-event upset (SEU), single-event latchup (SEL), etc.

When a heavy ion bombards a material, it collides with atoms in the material, forming a high-density ionization track that represents the energy deposition process. The charge density along this ionization track is very high, and it interacts with the depletion layer of the negatively biased *p–n* junction consisting of the drain and substrate of the MOSFET. Therefore, the ionization track leads to distortion of the electric field structure of the depletion layer, extending the field to a certain depth along the ionization track and forming a funnel-type electric field expansion area that results in a funnel effect [8,9]. Under the action of the electric field, charges are collected by both sides of the *p–n* junction consisting of the drain and substrate of the MOSFET from the funnel, resulting in a transient current pulse. A diagram of this funnel effect is shown in Fig. 1. When the incident particle crosses the *p–n* junction, the main effect is this funnel mechanism. However, when the particle does not cross the *p–n* junction, such a funnel does not appear, and the physical mechanism only involves diffusion of carriers. In this case, the current is purely diffusive and much of the charge is lost in the surrounding junctions. For CMOS combinational logic circuits, the output voltage will exhibit a transient under the influence of the current caused by such an incident particle.

3 TCAD–HSPICE mixed-mode simulation

Based on 65-nm CMOS technology provided by Semiconductor Manufacturing International Corporation (SMIC), the main parameters of the NMOS structure of a 65-nm CMOS inverter were obtained, and a 3D TCAD structure of the 65-nm CMOS device established using Cogenda Visual TCAD software [10]. Table 1 presents the main parameters of the NMOS structure in the 65-nm CMOS inverter. Based on a heavy ion model in the TCAD structure, TCAD–HSPICE mixed-mode simulations were carried out, using a 3D TCAD structure for the NMOS and an HSPICE model for the positive-channel metal-oxide semiconductor (PMOS) structure. To describe an actual application environment of the NMOS more accurately, an active area of the PMOS was retained in the 3D TCAD structure. The 3D TCAD structure of the NMOS is presented in Fig. 2.

For the NMOS structure, to achieve a bias state sensitive to SEEs, the gate voltage was set to $V_g = 0$ and the input voltage of the inverter was set to zero. The width and length of the PMOS structure in the inverter were 585 and 60 nm, respectively. These simulations were carried out based on the “heavy ion” model, whose input variables are the LET, incident position, incident angle, and track length. The particles used in the TCAD–HSPICE mixed-mode simulations were chlorine ions ($E = 160$ MeV, length $= 46\,\mu$m, LET $= 13.1$ MeV cm^2/mg). When a device is bombarded by a chlorine ion, the SET is obvious. The NMOS drain center was used as the origin, and the incident position was scanned in the *x*-axis direction as shown in Fig. 1, with incident direction perpendicular to the device surface, then the electrical characteristics of the NMOS under the action of particle incident at different positions were simulated based on the TCAD–HSPICE mixed-mode simulation.

4 Analysis of TCAD–HSPICE mixed-mode simulation results and analytical model

When a MOSFET in a sensitive bias state is bombarded by a heavy ion, it is turned on, and a current pulse is formed. The current of the NMOS drain shows a typical “burst–plateau” characteristic during an ion incidence process [7,11–13]. At the start, there is a burst pulse, followed by a plateau stage due to the constraint of the electrical conductivity of the MOSFET, which is in a saturation bias state. The current waveform of the NMOS drain when the NMOS drain center is bombarded by an ion is presented in Fig. 3.

The curves of the NMOS drain current can be obtained from the TCAD–HSPICE mixed-mode simulation results, and the charge collected by the NMOS drain calculated as the time integral of the NMOS drain current. The relationship between the charge collected by the NMOS drain and the incident position of the ion is shown in Fig. 4, where the horizontal axis denotes the distance of the ion incident position from the NMOS drain center along the *x*-axis direction.

In 65-nm CMOS devices, the diameter of an ionization track generated by an ion is slightly larger than the drain scale.

Table 1 Main parameters of NMOS structure in a 65-nm CMOS inverter

Channel length (nm)	60
Channel width (nm)	420
Gate oxide thickness (nm)	1.9
Source/drain doping concentration (cm^{-3})	1.2×10^{20}
Source/drain diffusion-zone doping concentration (cm^{-3})	1.2×10^{19}

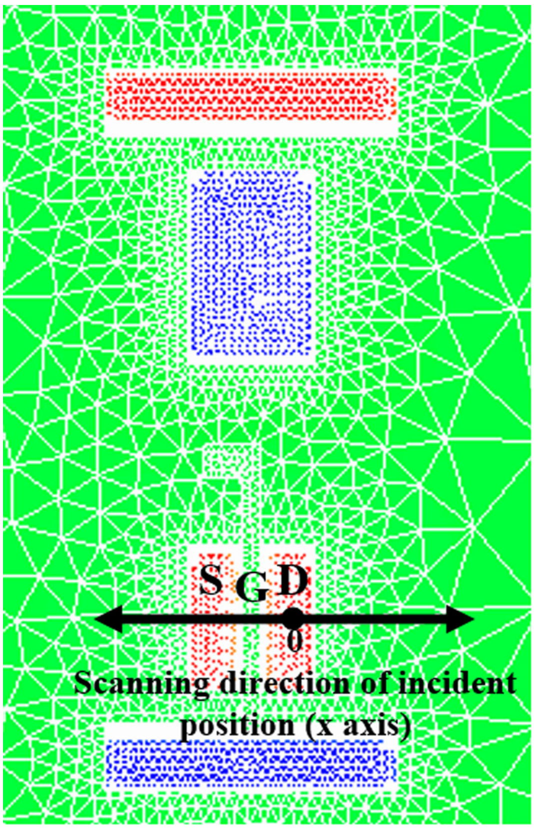

Fig. 2 3D TCAD structure of NMOS structure in a 65-nm CMOS inverter

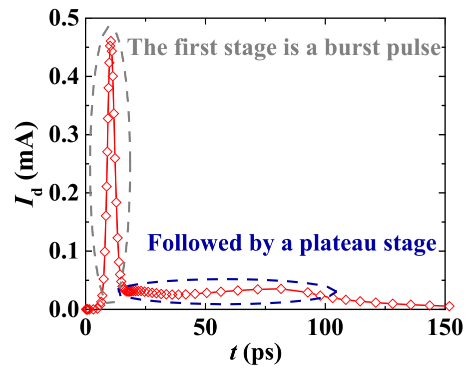

Fig. 3 Burst–plateau-type current pulse waveform of NMOS drain

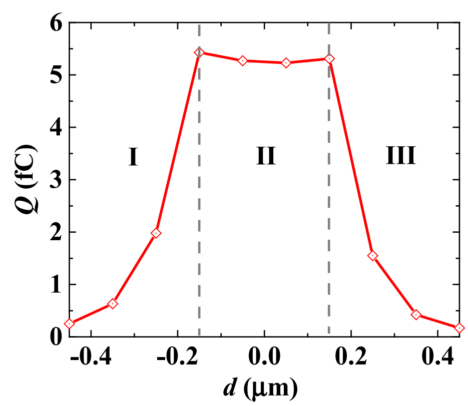

Fig. 4 Relationship between charge collected by NMOS drain and ion incident position

Figure 5a, b shows ionization tracks generated by heavy ions incident at different positions. As the negatively biased *p*–*n* junction consisting of the drain and substrate is the area sensitive to SEEs, when the ion incident position is not far from the NMOS drain center, the horizontal cross-section of the ionization track can completely cover the drain area, and the charge collected by the drain reaches its maximum level (region II in Fig. 4). As the ion incident position continues to move toward any of the sides, the overlapping area between the ionization track and the drain region decreases, as does the charge collected by the drain, and when the incident position is far enough from the drain, the SET is slight (regions I and III in Fig. 4).

The radial distribution of the charge density of the ionization track can be described by a Gaussian function, as presented in Fig. 6. The Gaussian function $D(x, y)$ is given by

$$D(x, y) = D_0 * \exp\left(-\left(\sqrt{x^2 + y^2}/a_0\right)^2\right), \tag{1}$$

where D_0 is the electron density at the center of the ionization track (here $D_0 = 6.9 \times 10^{18} \text{cm}^{-3}$) and a_0 is the coefficient of the Gaussian function (obtained by fitting as $a_0 = 0.09$); the units on the x- and y-axes are μm.

The relationship between the distance of the ion incident position from the drain center and the charge collected by the drain can then be described by an empirical model based on an integral Gaussian function in a rectangular sensitive area. The charge collected by the drain is given by

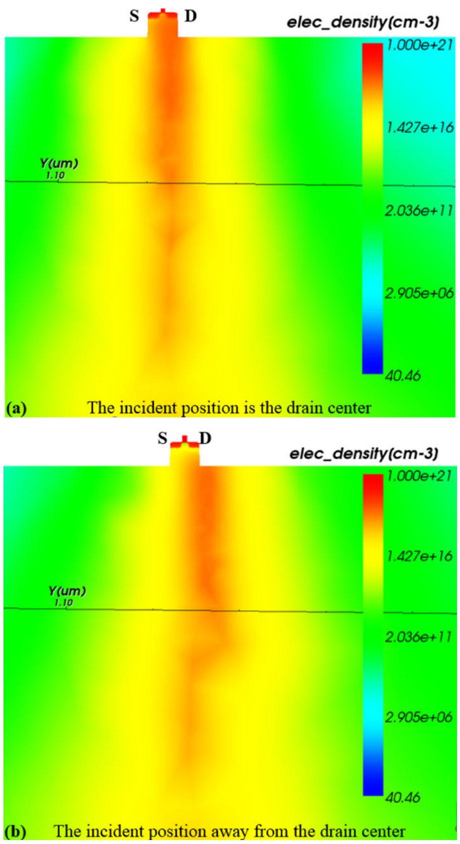

Fig. 5 Ionization tracks generated by ions at different incident positions

$$Q(d) = Q_0 * \frac{\int_{-\frac{w}{2}}^{\frac{w}{2}} \int_{-\frac{l}{2}}^{\frac{l}{2}} \exp\left(-\left(\sqrt{(x-d)^2+y^2}/a_0\right)^2\right) \mathrm{d}x\mathrm{d}y}{\int_{-\frac{w}{2}}^{\frac{w}{2}} \int_{-\frac{l}{2}}^{\frac{l}{2}} \exp\left(-\left(\sqrt{x^2+y^2}/a_0\right)^2\right) \mathrm{d}x\mathrm{d}y}, \quad (2)$$

where Q_0 is the charge collected by the NMOS drain when the ion incident position is the NMOS drain center, w and l are the width and length of the sensitive region (along the y- and x-direction, respectively), and d is the distance of the ion incident position from the drain center along the x-direction. Here, their values are $Q_0 = 5.3\,\text{fC}$, $l = 0.5\,\mu\text{m}$, and $w = 0.42\,\mu\text{m}$. Using the relationship in (2), the time parameters of the current pulse generated by heavy ions in the HSPICE simulations can be calculated. The relationship between the charge collected by the NMOS drain and the ion incident position obtained from the TCAD–HSPICE mixed-mode simulation results, and the corresponding fitting curve calculated using the analytical model, are presented in Fig. 7.

5 HSPICE simulation and discussion

The circuit structure of the inverter used in the HSPICE simulations is shown in Fig. 8, where R_b is the substrate resistance

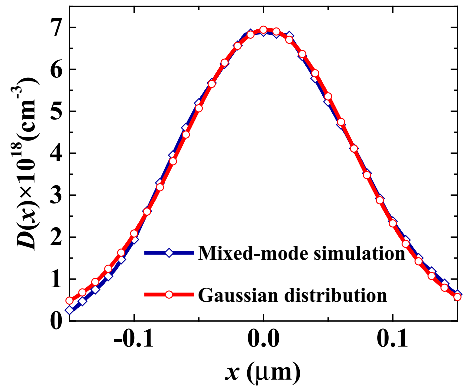

Fig. 6 Radial distribution of electron density of a free-charge region and its Gaussian fitting curve

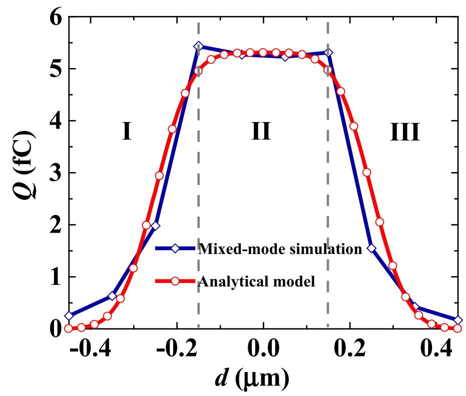

Fig. 7 Relationship between charge collected by NMOS drain and ion incident position obtained from the TCAD–HSPICE simulation results, and corresponding fitting curve calculated by the analytical model

of the NMOS structure ($2\,\text{k}\Omega$), and C_1 and C_2 represent the diffusion capacitors of the drain–substrate parasitic p–n junction and source–substrate parasitic p–n junction, respectively. Two voltage-controlled capacitors (VCCAP) were used to simulate these two p–n-junction diffusion capacitors, having the same values and the parameters presented in Table 2 [14–16]. In Fig. 8, I_{ion} denotes the ion equivalent current source. When the NMOS structure in the inverter is bombarded by an ion, a transient current pulse forms. However, the current at the inverter output comprises the current from both the NMOS and PMOS structures, thus the inverter output current is much larger than the NMOS drain current. The duration of the inverter output current is determined by the NMOS turn-on duration, thus the duration of these two currents is the same. The waveforms of the NMOS drain current and the inverter output current when the NMOS drain center is bombarded by an ion can be obtained from the TCAD–HSPICE simulation results. These current waveforms are shown in Fig. 9. Due to the difference between the HSPICE model and TCAD model, further details inside the NMOS cannot be described in the HSPICE model, so the

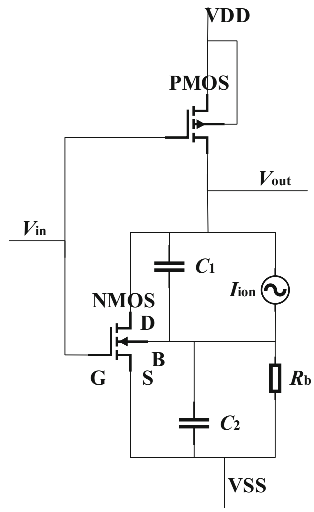

Fig. 8 Circuit structure of inverter in HSPICE simulations

Table 2 Parameters of diffusion capacitors C_1 and C_2

Voltage (V)	0	0.5	1.0	1.5	2.0
Capacitance ($C1 = C2$) (fF)	0	4	8	12	10

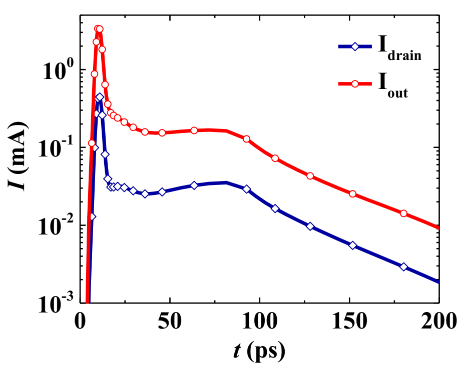

Fig. 9 Waveforms of NMOS drain current and inverter output current obtained from TCAD–HSPICE mixed-mode simulations

current source I_{ion} was introduced to describe the inverter output current characteristic. The current source I_{ion} can be described by a double-exponential model, given by

$$I(t) = \begin{cases} 0; \quad t < t_{d1} \\ I_{Peak}*(1 - \exp(-(t - t_{d1})/\tau_1)); \quad t_{d1} < t < t_{d2} \\ I_{Peak}*(\exp(-(t - t_{d2})/\tau_2) - \exp(-(t - t_{d1})/\tau_1)); \quad t > t_{d2} \end{cases} \tag{3}$$

where I_{Peak} is the peak value of the inverter output current, t_{d1} is the onset of the current rise, t_{d2} is the onset of the current fall, τ_1 is the rise time constant, and τ_2 is the fall time constant [7].

For a burst–plateau-type current waveform, the peak value of the burst stage is determined by the electron–hole pair density due to the incident particle. Due to the generation characteristics (reaching a maximum at about 10 ps) of

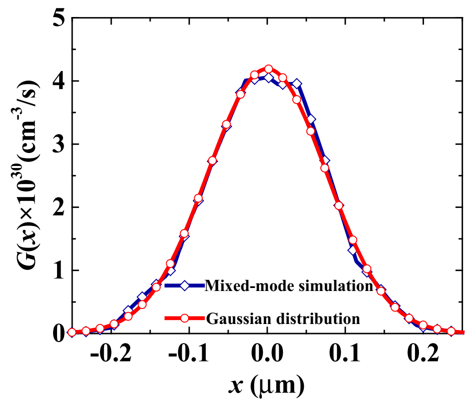

Fig. 10 Radial distribution of electron–hole pair density generation caused by incident particle and its Gaussian fitting curve at 10 ps

the incident particle from the center to the periphery, the electron–hole pair density is very similar to a Gaussian function, so the relationship between the peak drain current I_{Burst} and the incident position of the particle can be described by a Gaussian function, as can the peak inverter output current I_{Peak}. Figure 10 shows the radial distribution of the generation by the incident particle $G(x)$ and its Gaussian fitting curve. Furthermore, Fig. 11 shows the relationship between the peak current value of the drain I_{Burst} and the incident position of the particle obtained from the TCAD–HSPICE mixed-mode simulation results and its Gaussian fitting curve. Moreover, Fig. 12 shows the relationship between the peak current of the inverter output I_{Peak} and the incident position of the particle obtained from the TCAD–HSPICE mixed-mode simulation results and its Gaussian fitting curve. The relationship between I_{Brust} and the distance of the incident position from the drain center along the x-direction is given by

$$I_{Burst}(d) = I_{Burst0}* \exp(-(d/a_1)^2), \tag{4}$$

where I_{Burst0} is the peak drain current when the incident position of the particle is the drain center ($I_{Brust0} = 0.48$ mA), d is the distance in μm of the incident position of the particle from the drain center along the x-direction, and a_1 is the coefficient of the Gaussian function (whose value can be obtained by fitting as $a_1 = 0.17$).

The relationship between I_{Peak} and the distance of the incident position of the particle from the drain center along the x-direction is given by

$$I_{Peak}(d) = I_{Peak0}* \exp(-(d/a_2)^2), \tag{5}$$

where I_{Peak0} is the peak value of the inverter output current when the incident position is the drain center ($I_{Peak0} = 3.5$ mA), d is the distance in μm of the incident position of the particle from the drain center alone the x-axis, and a_2 is

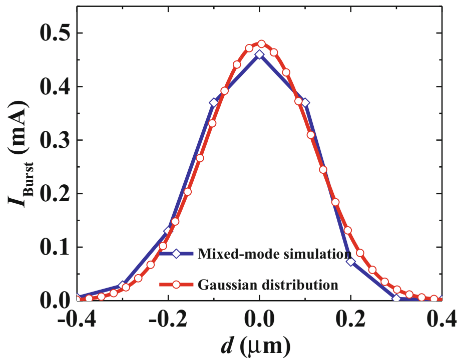

Fig. 11 Relationship between peak drain current I_{Burst} and incident position of particle obtained from the TCAD–HSPICE mixed-mode simulation results and its Gaussian fitting curve

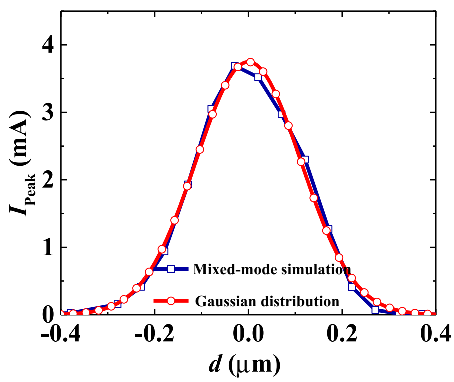

Fig. 12 Relationship between peak current of inverter output I_{Peak} and incident position of particle obtained from the TCAD–HSPICE mixed-mode simulation results and its Gaussian fitting curve

the coefficient in this Gaussian function (whose value can be obtained by fitting as $a_2 = 0.16$).

The parameter t_t is the drain current pulse duration in the plateau stage, defined as

$$t_t = \frac{Q - Q_{\mathrm{Burst}}}{I_{\mathrm{Plateau}}}, \tag{6}$$

where Q is the charge collected by the NMOS drain calculated using (2), Q_{Burst} is the charge in the burst stage given by (7), and I_{Plateau} is the drain current in the plateau stage with a value of about 40 μA.

$$Q_{\mathrm{Burst}} = I_{\mathrm{Burst}} * (t_{\mathrm{d2}} - t_{\mathrm{d1}}). \tag{7}$$

In the HSPICE simulations, the current source was built using the relationship in (3). Moreover, the value of I_{Peak} was calculated by (5), where $t_{\mathrm{d1}} = 5$ ps, $t_{\mathrm{d2}} = 10$ ps, $\tau_1 = 1.2$ ps, and τ_2 was calculated by (3) and (6).

Using the relationships presented above, the HSPICE simulations were carried out, and the results compared with those of the TCAD–HSPICE mixed-mode simulations. When the NMOS structure in the CMOS inverter was bombarded by particles incident at different positions, the current peak and duration of the inverter output changed accordingly. Based on the funnel mechanism and distribution of the ionization track, an analytical model was established to describe the relationship between the incident position of the particle and the charge collected by the NMOS drain. Moreover, an HSPICE simulation approach for a CMOS inverter under the action of particles incident at different positions was developed based on the established analytical model. Figure 13a, b presents the peak and duration of the inverter output current under the action of particles at different incident positions, respectively, obtained from the TCAD–HSPICE mixed-mode simulation results and HSPICE simulation results. The waveforms of

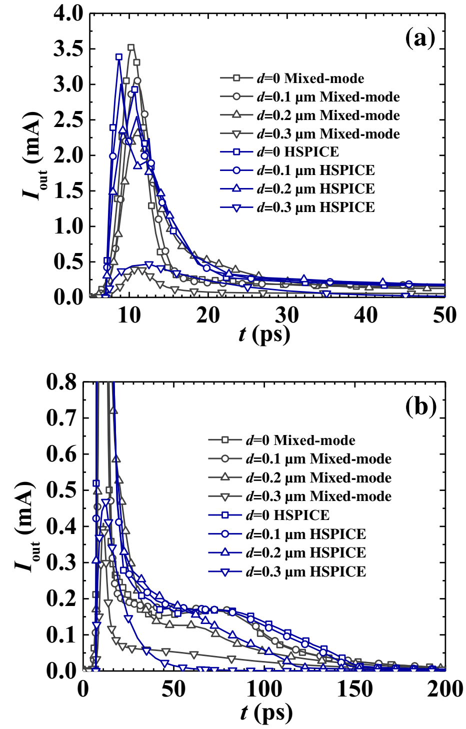

Fig. 13 Peak current **a** and duration **b** of inverter output

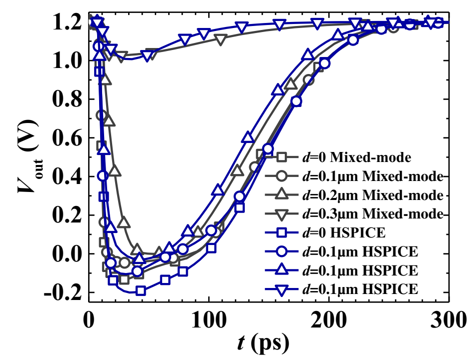

Fig. 14 Waveforms of inverter output voltage

the inverter output voltage under the action of particles incident at different positions obtained from the TCAD–HSPICE mixed-mode simulation results and HSPICE simulation results are shown in Fig. 14. The results obtained using these two different simulation approaches are basically consistent, and also with test data from the National University of Defense Technology [17].

6 Conclusions

The action of particles incident at different positions was simulated using TCAD–HSPICE mixed-mode simulations. Based on the funnel mechanism, the relationship between the incident position of the particle and the NMOS current is discussed, and an analytical model built. Furthermore, based on this analytical model, an HSPICE simulation approach was developed. Then, HSPICE simulations of the CMOS inverter under the action of particles incident at different positions were carried out, and the approach verified by comparison of the results obtained using these two different simulation approaches.

Future work will include development of a more comprehensive HSPICE model including consideration of many factors not discussed herein. Besides, HSPICE models of MOSFETs considering additional particle parameters (incident angle, trajectory length, LET, etc.), parasitic parameters of the MOSFET, the case where the particle does not cross the *p*–*n* junction, the supply voltage, and circuit-level effects [propagation-induced pulse broadening (PIPB), charge sharing, etc.] require further study.

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