Single-Event Transient Measurements in nMOS and pMOS Transistors in a 65-nm Bulk CMOS Technology at Elevated Temperatures

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***Abstract*—In this paper, heavy-ion-induced single-event transient (SET) pulsewidths measured in a 65-nm bulk CMOS technology at temperatures ranging from 25 °C to 100 °C with an autonomous SET capture circuit are presented. The experimental results for the SETs induced in two different inverter chain circuits indicate an increase in the average SET pulsewidth as a function of the operating temperature. Unique SET test structures were also designed to differentiate between SETs induced in an nMOS transistor and those induced in a pMOS transistor. The SET widths induced in a pMOS transistor increase more with temperature than the SETs induced in an nMOS transistor.**

***Index Terms*—Pulsewidth, radiation environment, soft error rate (SER), single event, single-event transient (SET), soft error, temperature.**

I. Introduction

A KEY FACTOR affecting soft-error rates is the time duration of the single-event transient (SET) signals induced by energetic particles. For combinational logic circuits, the time duration of these transients determines the probability that they will arrive at a storage cell during a latching edge of the clock signal (and thus be recorded as an error). The transient pulsewidth is influenced by the charge-collection process which is a strong function of temperature, particularly when enhanced by a parasitic-bipolar action. Thus, for electronic circuits operating in extreme environments where both temperature and radiation are the concern, the effects of temperature changes on the soft-error rate are of vital importance. Recent work has shown that an enhancement in the parasitic-bipolar action at elevated temperatures is the dominant mechanism that causes SET pulsewidths to increase with temperature [1]–[3]. In bulk CMOS processes with a p-substrate and an n-well, the simulation work has shown that the parasitic-bipolar effect is worse in pMOS transistors than in nMOS transistors, which results in larger pulsewidths for SETs induced in pMOS transistors [4], [5]. Because of the difficulties associated with the SET width measurements, a separate measurement of the SETs induced in either pMOS or nMOS transistors has not been reported before. In addition, previous simulation work has shown that the SET pulsewidths induced in pMOS transistors increase more with temperature than the SETs induced in nMOS transistors [2], [3]. However, no experimental measurements over the temperature of the individual SETs in nMOS and pMOS transistors have been made in an advanced CMOS technology.

In this paper, the SET pulsewidths at elevated temperatures are measured for the nMOS and pMOS transistors separately using a novel autonomous SET pulsewidth measurement circuit. The SET measurements in the nMOS and pMOS transistors are also compared to the SETs measured in the long inverter chains. The aim of this paper is the following: 1) to determine the temperature dependence of the heavy-ion-induced SETs in a 65-nm bulk technology and 2) to experimentally determine if the SETs induced in pMOS transistors show a larger change with temperature than the SET widths induced in nMOS transistors.

II. SET Measurement Structures

Four test structures in characterizing the SET pulses were fabricated in an IBM 65-nm bulk CMOS technology [6]. Each of the test structures consists of a target circuit in which the SETs are generated, followed by an on-chip measurement circuit. The measurement circuit is identical for all target circuits used in this paper. The measurement portion of the test structure measures the SET pulsewidth in terms of inverter stage delays. The measurement circuit is based on the principle that, within an inverter chain, a SET pulse will affect a number of inverters, which is directly related to the pulsewidth. The measurement circuit was first described by Narasimham *et al.* [7], and it has been implemented and tested successfully in multiple technologies [8]–[10]. In the implementation of the measurement circuit used here, 80 inverter stages are connected to latches to store the number of inverter stages affected by a SET. A SET pulse detection circuit is used to trigger the latches. With an individual inverter stage delay of 25 ps at room temperature, this circuit allows the measurement of full-width

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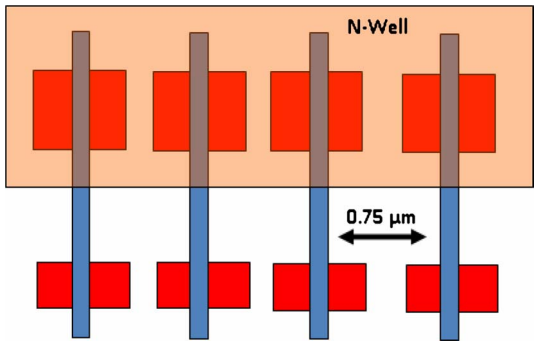

Fig. 1. Top-down view of the layout of four inverters in the same-well inverter chain target circuit. The gate-to-gate spacing between each inverter was 0.75 μm.

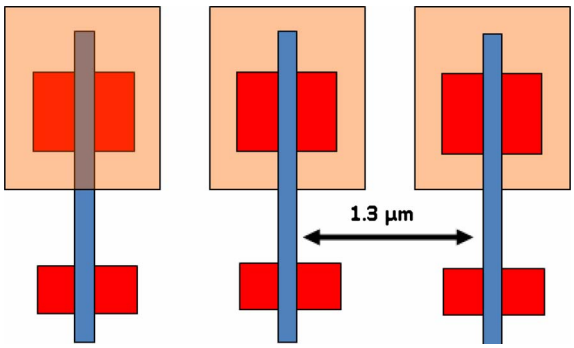

Fig. 2. Top-down view of the layout of three inverters in the separate-well inverter chain target circuit. The gate-to-gate spacing between each inverter was 1.3 μm.

at half-maximum SET pulsewidths ranging from 25 ps to 2 ns, with a 12.5-ps measurement resolution.

The four target circuits used in this paper consist of the following: 1) a minimum-sized 1000-inverter chain with evenly spaced ten rows of 100 inverters in which each pMOS transistor in a row was in the same n-well; 2) a schematically identical 1000-inverter chain circuit, with each pMOS transistor in a separate n-well; 3) an "N-hit" circuit; and 4) a "P-hit" circuit. Figs. 1 and 2 show the illustrations of the layout of the inverter chain target circuits. For the same-well target circuit (the circuit with each pMOS transistor in a row in the same n-well), the distance from the center of one inverter to the next was 0.75 μm. The gate-to-gate spacing between the inverters for the separate-well circuit was 1.3 μm. This was the minimum spacing allowed by the design for each configuration.

Figs. 3 and 4 show the basic blocks of the "N-hit" and "P-hit" target circuits. The "N-hit" ("P-hit") target circuit consists of four chains of 100 NAND (NOR) gate/inverter blocks "OR"-ed together to form a single output. In both circuits, the individual ion strikes on the inverters are unable to propagate through the logic chain due to logic masking. (Logic masking is a term used to describe a situation in which a signal such as a SET is unable to propagate through a combinational logic block due to the state of the remaining logic. For example, in a two-input NAND gate, if one input is at a logic "0," the output will always be at a logic "1" regardless of the state of the other input to the gate.) In the "N-hit" circuit stage shown in Fig. 3, a SET generated by an ion hit in one of the inverters will not

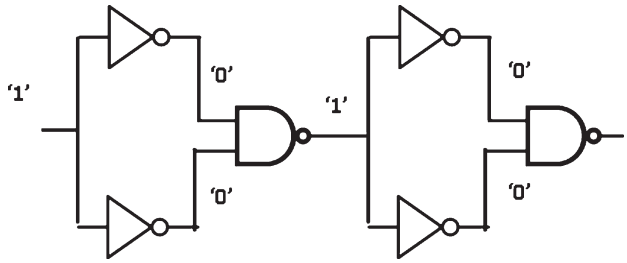

Fig. 3. Schematic of two of the blocks of the "N-hit" target circuit. The target circuit used in this paper consisted of four linear chains of 100 of these combinational logic blocks "OR"-ed together to form a single output.

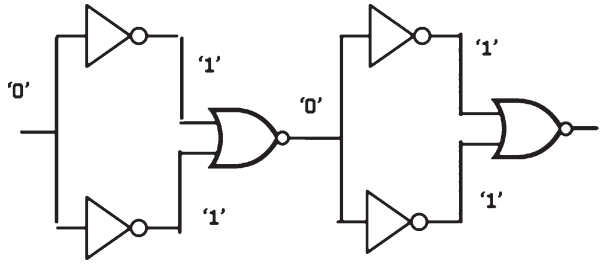

Fig. 4. Schematic of two of the blocks of the "P-hit" target circuit. The target circuit used in this paper consisted of four linear chains of 100 of these combinational logic blocks "OR"-ed together to form a single output.

propagate through the NAND gate. Only an ion hit on an nMOS transistor in the NAND gate will propagate through the chain. Therefore, only a SET generated in the "OFF" nMOS transistor connected to the output of the NAND gate will be measured. All other SETs will be blocked and will not be measured. The "P-hit" target circuit works in a similar manner, with the NAND gates replaced by the NOR gates.

One important item to take note is the spacing of the two inverters in the "N-hit" and "P-hit" circuits. If the inverters are spaced close together in the layout, it may be possible for an ion strike to create a simultaneous SET on each inverter. If this was to happen, a SET may be able to propagate through either the NAND or NOR gate, and as a result, the circuit would no longer allow only hits on the nMOS or pMOS devices to be measured. To ensure that a transient was not induced on both inverters by a single ion, the inverters were placed at the top and bottom of the NAND/NOR gates, with a separation of 3.5 μm, as shown in Fig. 5. This distance has been determined to be sufficient to prevent transistors in both inverters to collect charge due to a single ion hit [11].

III. Heavy Ion Experimental Results

The SET measurement structures were tested at an elevated temperature with heavy ions at the Lawrence Berkeley National Laboratory Cyclotron facility using xenon ions with a linear energy transfer (LET) of 58.8 MeV $\cdot$ cm^2/mg. (The room temperature data were also taken using ion species with smaller LET values, but the results will not be presented here. These room temperature results can be found in [12] and [13].) The temperature of the device-under-test (DUT) was controlled through a resistive heater attached to the package of the DUT, and the temperature measurements were taken using a sensor that is also attached to the package. The ion

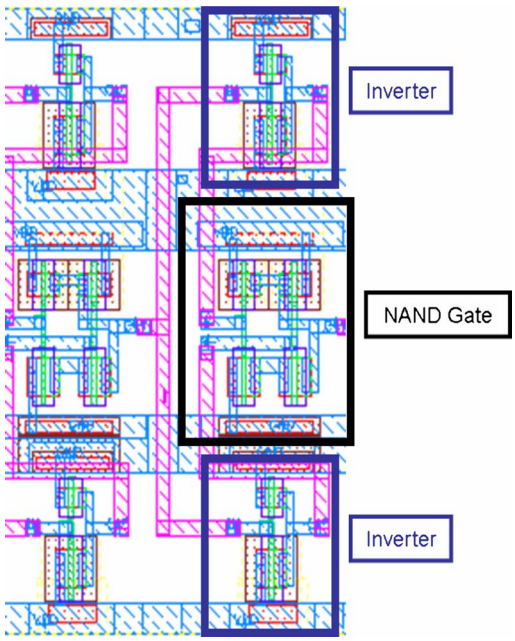

Fig. 5. Layout of two of the blocks of the "N-hit" target circuit. The spacing between the two inverters needs to be large enough to ensure that an ion cannot induce a SET on both at the same time.

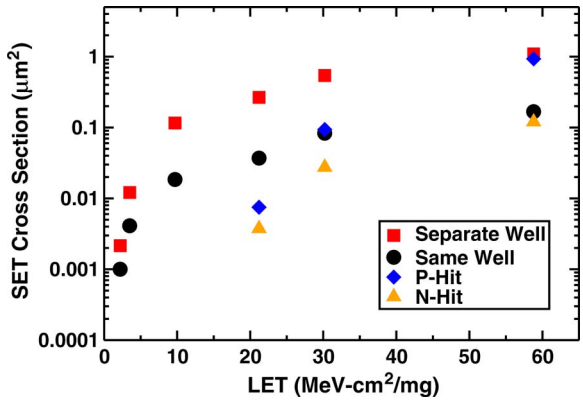

Fig. 6. SET cross section for the different 65-nm test structures. Note that the threshold LET for the "P-hit" and "N-hit" circuits is much larger than the threshold LET for the inverter chain circuits.

exposures were carried out at temperatures of 25 °C, 50 °C, and 100 °C. The temperature reported in the following section is the package temperature, as measured by the temperature sensor. The variations in the inverter stage delays for this temperature range were recorded using a ring oscillator that was designed using the same inverter stages used in the measurement circuit. The ring oscillator frequency was measured at the temperatures used for the heavy ion experiment to determine the individual stage delay of the measurement circuit. The inverter stage delay increased linearly with temperature from approximately 25 ps at 25 °C to 34 ps at 100 °C.

For comparison purposes, the room temperature SET cross section for the inverter chains, "N-hit," and "P-hit" target circuits is shown in Fig. 6. The plotted SET cross section is simply the number of measured SETs divided by the total fluence of the ions normalized to one logic block. For the inverter chains, the cross section is plotted per inverter, while for the "N-hit" and "P-hit" circuits, the cross section is plotted per one NAND/NOR inverter block combination. As can be seen in the plot, the threshold LET in creating a measurable SET for the "N-hit" and "P-hit" circuits is much larger than that for the inverter chain circuits. Also, we need to note that the cross section of the "P-hit" circuit is larger than that of the "N-hit" circuit. One reason for this is that the size of the sensitive pMOS transistor in the "P-hit" circuit is much larger than the sensitive nMOS transistor in the "N-hit" circuit. The W/L ratio of the sensitive pMOS transistor is 1.3 μm/50 nm, while the W/L ratio of the sensitive nMOS transistor is 400/50 nm. This means that the drain area of the sensitive pMOS transistor was over four times as large as the area of the sensitive nMOS transistor.

The histograms of the measured SET pulsewidth distributions at three different temperatures for exposures to xenon ions for the 1000-inverter chain same-well target circuit are shown in Fig. 7. As can be seen in the histograms, the SET pulsewidth distribution clearly shifts toward longer SET widths as the temperature increases. An 82% increase in the average pulsewidth was observed as the temperature increased from 25 °C to 100 °C (as shown in Fig. 9). The longest measured SET pulsewidth increased from 200 to 304 ps. The total ion fluence was 10^8 ions/cm^2 for each exposure. The number of SETs measured for the total fluence of ions was 139 at 25 °C, 163 at 50 °C, and 235 at 100 °C. The increase in the number of transients measured, implying an increased cross section, indicates that ion hits at more distant locations from a sensitive node are able to produce enough collected charge for a measurable SET at the higher temperatures. The SET measurements using inverter chains in 90- and 130-nm bulk technologies showed no increase in the number of SET events with temperature [2], [3].

A similar trend with increasing temperature was also observed in the separate-well inverter chain circuit, as shown in Figs. 8 and 9. The average SET width increased by 88% from 25 °C to 100 °C, and the longest measured SET width increased from 200 to 408 ps. The pulsewidths for the separate-well circuit were consistently larger than those for the same-well circuit for all temperatures. This is likely due to a SET "pulse quenching" mechanism first described by Ahlbin *et al.* [14]. "Pulse quenching" can occur when multiple devices in an electrically connected logic chain (like the inverter chain used in this paper) collect charge. The end result of this charge-sharing mechanism is that the SET widths are shorter than when only a single device collects charge. The closer spacing of the same-well circuit increases this charge-sharing effect, thus leading to shorter (or "quenched") SET widths. Since the rate of change in the average SET width with temperature was not significantly different between separate-well and same-well circuits, this suggests that the "pulse quenching" mechanism also did not change much with temperature.

Another interesting fact about the separate-well data is that a significantly larger number of SET events were observed for the same ion fluence as the same-well circuit. (This fact is also evident in the cross section plot in Fig. 6.) The number of SETs measured for the total fluence of ions for the separate-well circuit was 710 at 25 °C, 943 at 50 °C, and 1041 at 100 °C.

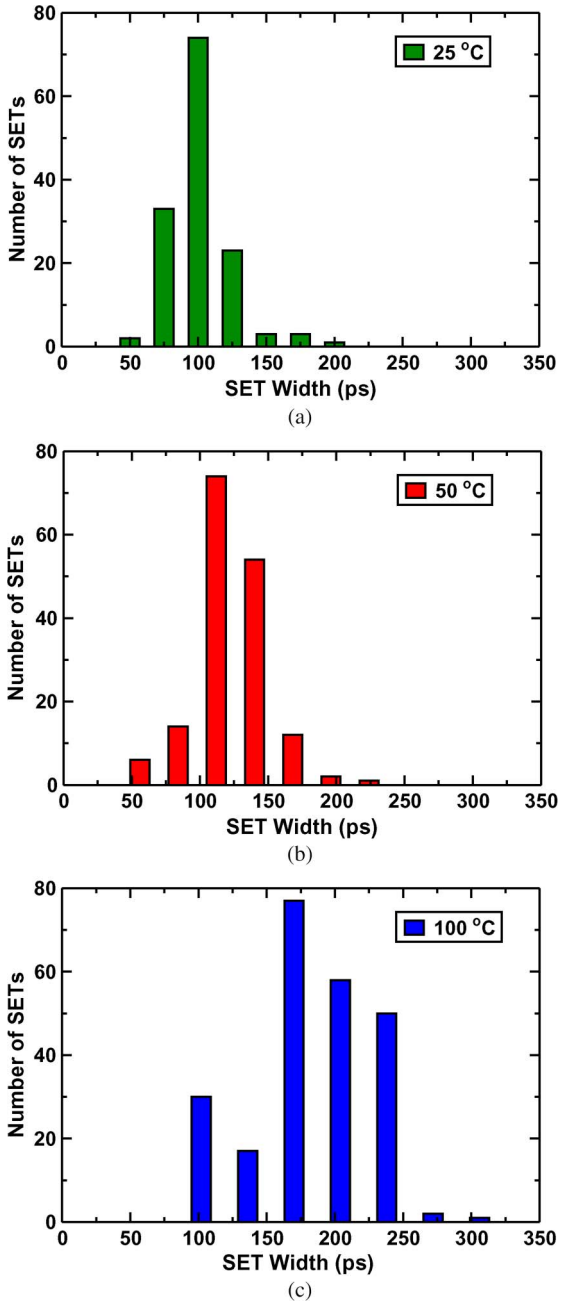

Fig. 7. Measured SET pulsewidth distribution for the same-well inverter chain circuit at (a) 25 °C, (b) 50 °C, and (c) 100 °C. Note that, as the temperature increases, the distribution shifts to the longer SET widths.

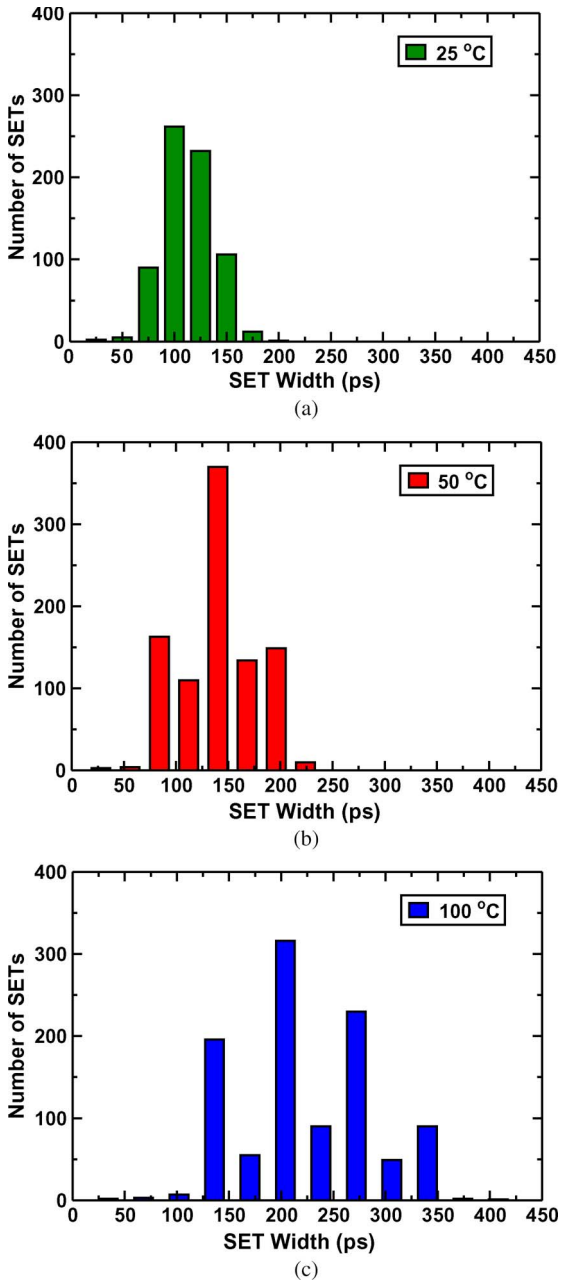

Fig. 8. Measured SET pulsewidth distribution for the separate-well inverter chain circuit at (a) 25 °C, (b) 50 °C, and (c) 100 °C.

In Figs. 10 and 11, the measured SET pulsewidth distributions for the "N-hit" and "P-hit" circuits are shown. Several important items to note from the histograms are the following: 1) the number of SETs measured for the "P-hit" circuit is about an order of magnitude larger than that for the "N-hit" circuit (this is also shown in the cross section in Fig. 6); 2) the shift in the SET width distribution toward longer SET widths with temperature is clear for the "P-hit" circuit; and 3) the change in the SET width with temperature for the "N-hit" circuit is not quite obvious. The changes in the SET width for the "N-hit" circuit may not be apparent due to the small number of SET events measured.

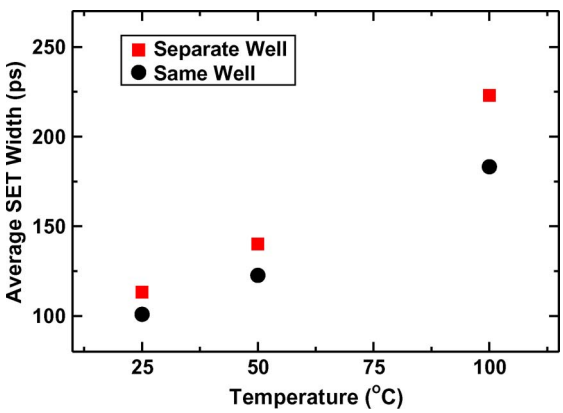

Fig. 9. Average SET width measurements as a function of temperature for the test structures with the 1000-inverter chain target circuit.

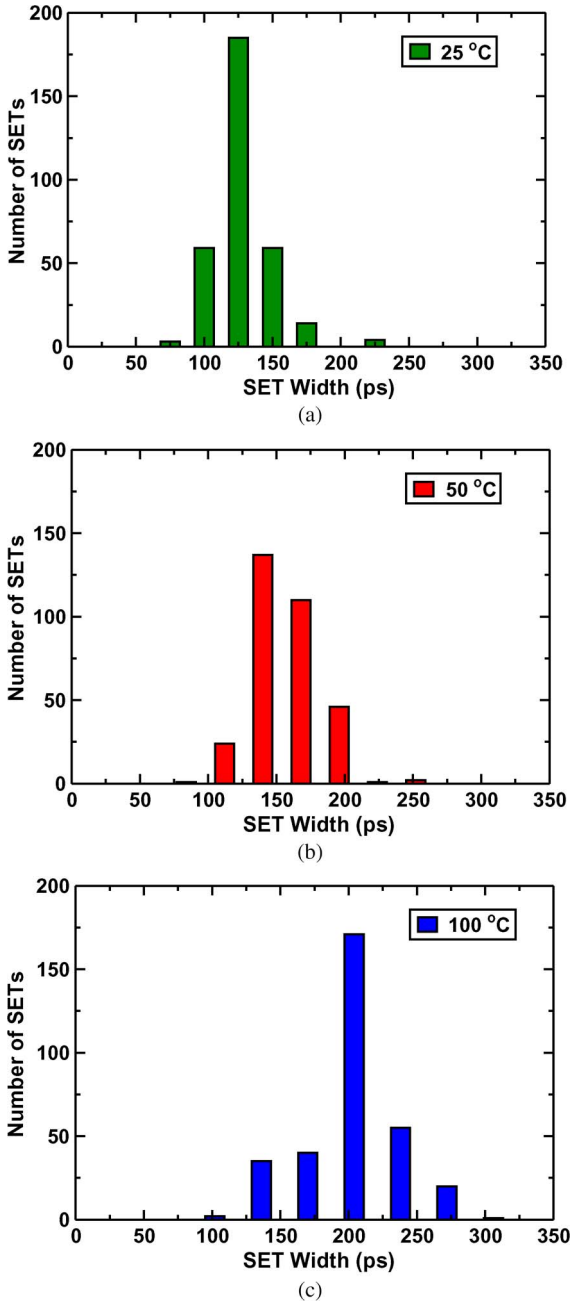

Fig. 10. Measured SET pulsewidth distribution for the "P-hit" circuit at (a) 25 °C, (b) 50 °C, and (c) 100 °C. Note that, as the temperature increases, the distribution clearly shifts to the longer SET widths.

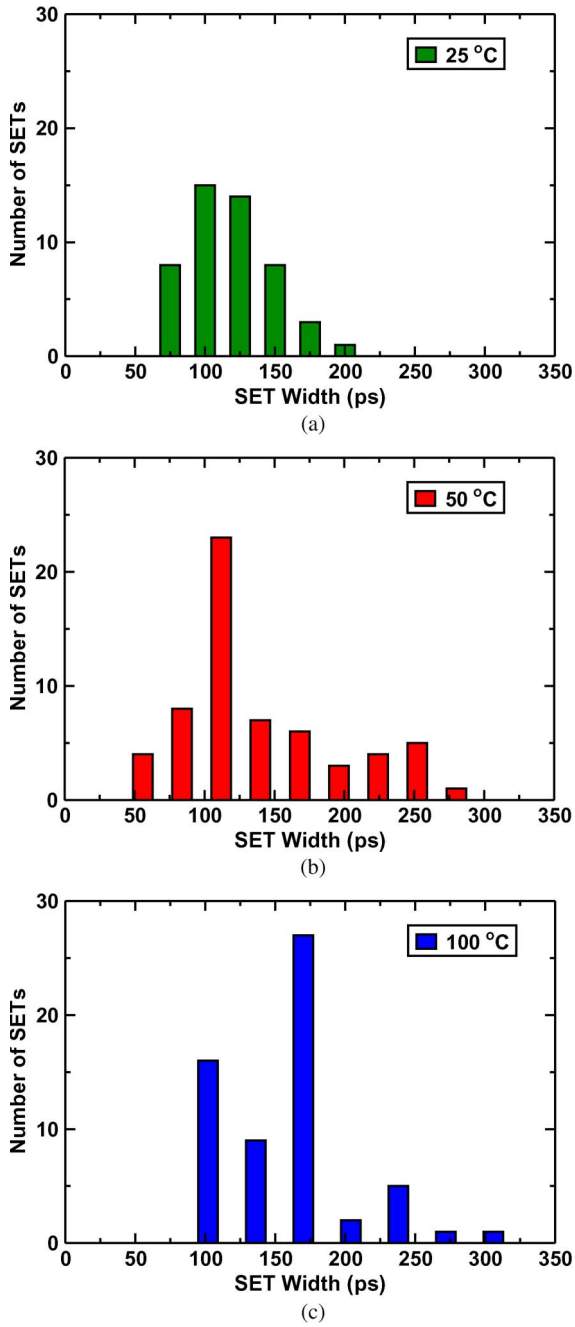

Fig. 11. Measured SET pulsewidth distribution for the "N-hit" circuit at (a) 25 °C, (b) 50 °C, and (c) 100 °C. Due primarily to the small number of SETs measured, the changes in the SET width distribution are difficult to observe.

The average measured SET widths for the "N-hit" and "P-hit" circuits are shown in Fig. 12. At room temperature, the average SET width in the "P-hit" circuit was only slightly ($\sim$10 ps) larger than the average SET width in the "N-hit" circuit. However, the average SET width increased from 128 to 202 ps from 25 °C to 100 °C for the "P-hit" circuit (58% increase), while the average SET width for the "N-hit" circuit increased from 118 to 158 ps (34% increase). The error bars for the "N-hit" data represent the standard error in the average measured width. The standard error is found by dividing the standard deviation by the square root of the number of counts.

IV. Discussion

The larger increase in SET width with temperature for the "P-hit" circuit suggests that the enhancement of the parasitic-bipolar effect with temperature is greater for the pMOS transistor than for the nMOS transistor. This parasitic-bipolar effect is mainly caused by the debiasing of the n-well region surrounding the pMOS transistor [4], [5]. The enhancement in the parasitic-bipolar effect with temperature and its impact on the SET widths in bulk technologies have been explored in detail by Shuming *et al.* [1] and Gadlage *et al.* [2], [3]. The simulation results from Gadlage *et al.* [3] showing the

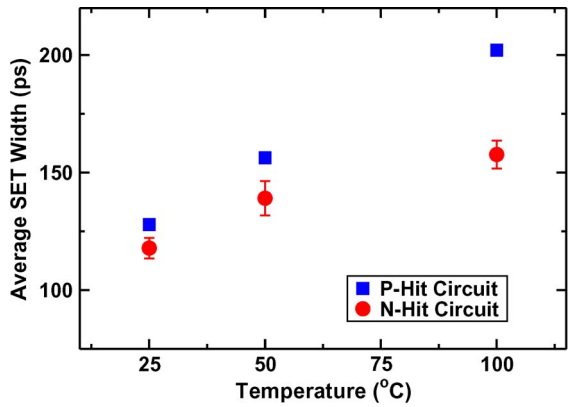

Fig. 12. Average SET width measurements as a function of temperature for the test structures with the "N-hit" and "P-hit" target circuits.

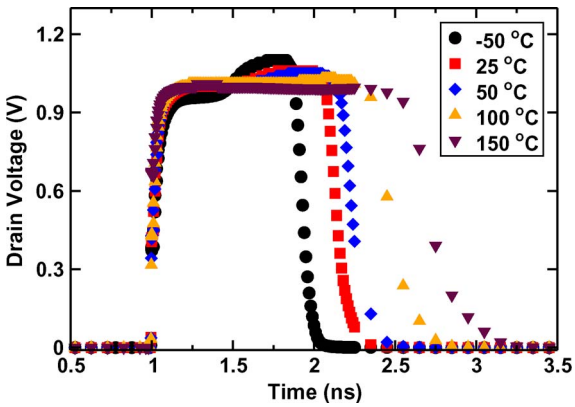

Fig. 13. Results of the 130-nm mixed-mode simulations of the SETs on pMOS transistors as a function of temperature from [3].

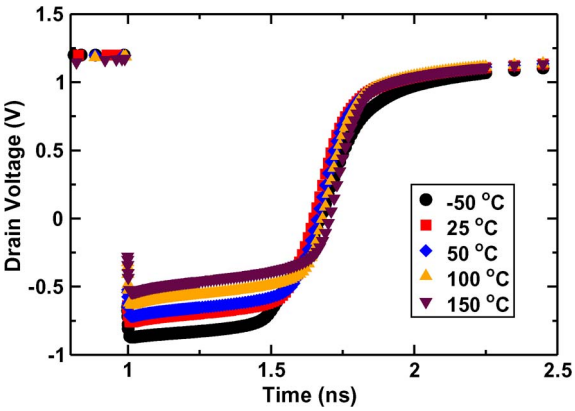

Fig. 14. Results of the 130-nm mixed-mode simulations of the SETs on nMOS transistors as a function of temperature from [3].

impact of temperature on the SET widths induced in a 130-nm bulk CMOS technology in pMOS and nMOS transistors are shown in Figs. 13 and 14. These results clearly show that the SET induced in pMOS transistors exhibits a larger change with temperature than the SETs induced in nMOS transistors. The experimental measurements performed in this work in a 65-nm bulk CMOS technology also show a larger change in the SET widths with temperature for pMOS transistors.

In the histograms of the inverter chains shown in Figs. 7 and 8, the SET widths diverge from a normal distribution at the higher temperatures, while for the "P-hit" circuit (shown in Fig. 10), the distribution remains approximately normal at the increased temperatures. One possible explanation for the divergence from a normal distribution in the inverter chains is that, at high temperatures, the SETs induced in the pMOS transistors in the inverter chain are increasing, while the SETs induced in the nMOS transistors are not. This difference in temperature response between the two transistors may be the cause of the divergence in the SET pulsewidth distribution shown in Figs. 7 and 8.

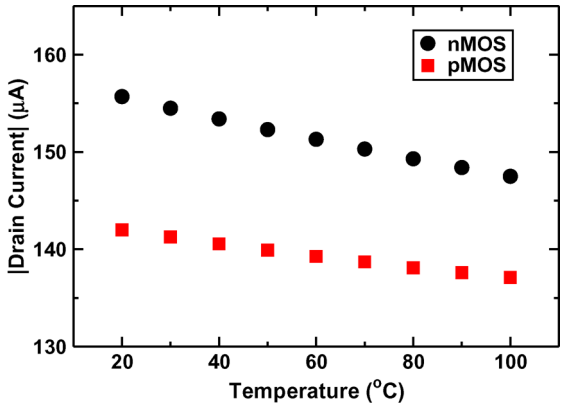

Fig. 15. Simulated drain current as a function of temperature for the 65-nm nMOS and pMOS transistors used in the inverter chain target circuits.

Another potential mechanism that can contribute to the lengthening of the SET pulses (that has not been previously explored) is the change in individual transistor currents with temperature. After a single event hit on an "OFF" transistor, the corresponding "ON" transistor connected to the circuit node restores the original voltage. In the "N-hit" stage shown in Fig. 3, the restoring transistors are pMOS transistors in the NAND gate for hits on the nMOS transistor. The drive strength of the restoring transistor is proportional to mobility, which, in turn, is directly related to temperature. In the temperature range of concern here, mobility decreases with an increasing temperature. A decrease in the restoring current means that it will take a longer time for the "ON" transistor to restore the same amount of charge to a struck node, resulting in longer SET pulses. To further explore how the restoring current changes with temperature, the maximum drive currents for the nMOS and pMOS transistors were simulated at different temperatures at the circuit-level using the PDK for this technology. In Fig. 15, the drain currents for an nMOS transistor with a W/L ratio of 200/50 nm and for a pMOS transistor with a W/L ratio of 400/50 nm are plotted as a function of temperature. These W/L ratios correspond to the W/L ratios of the transistors in the inverter chain circuit, and they were chosen in the design to ensure that the inverters had approximately equal rise and fall times. As can be seen, the drain current decreases with temperature, but the change from 20 °C to 100 °C is less than 6% for both devices. The small change in drain current leads to a correspondingly small change in the circuit response. As a result, these simulations show that the change in the restoring current with temperature has a small impact on the SET widths compared to the enhancement in the parasitic-bipolar action with temperature.

V. Conclusion

The soft-error rates are a strong function of the SET pulsewidths generated by incident neutrons and ions. In extreme environments, electronic devices are often required to operate over wide temperature ranges so that any potential change in the soft-error rate with temperature is of great concern. In this paper, the experimental measurements of the heavy-ion-induced SET pulsewidths are reported for a 65-nm bulk CMOS process over a large temperature range. The average SET pulsewidth increases by over 80% as the temperature increases from 25 °C to 100 °C for transients induced in two different inverter chain circuits. The results from a unique test structure designed to separate transients from strikes on nMOS and pMOS transistors show that the SET widths increase more with temperature (58% compared to 34%) for ion strikes on pMOS transistors than for ion strikes on nMOS transistors. The predominant mechanism causing the increase in the SET width with temperature is an enhancement in the parasitic-bipolar transistor as the temperature is increased. The change in the restoring current with temperature was shown to have a little impact on the SET widths.

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