SAND2014-20130J

Modeling of Single Event Transients with Dual Double-Exponential Current Sources: Implications for Logic Cell Characterization

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***Abstract*—Single event effects (SEE) are a reliability concern for modern microelectronics. Bit corruptions can be caused by single event upsets (SEUs) in the storage cells or by sampling single event transients (SETs) from a logic path. An accurate prediction of soft error rates (SER) due to SEUs and SETs requires good models to convert radiating particle energy to compact descriptions of the current injection process. This paper describes a simple, yet effective method to model the current waveform resulting from a charge collection event for SET circuit simulations. The model uses two double-exponential current sources in parallel, and the results illustrate why a conventional model based on one double-exponential source is insufficient to model long SETs. A small set of logic cells with varying input conditions, drive strength, and output loading are simulated to extract the parameters for the dual double-exponential current sources. The parameters are based upon both the node capacitance and the restoring current (i.e., drive strength) of the logic cell.**

***Index Terms*—Circuit simulation, Combinatorial circuits, Integrated circuit modeling, Logic cells, Semiconductor device modeling, Radiation effects**

I. Introduction

A single event transient (SET) [1] may be produced when an energetic ionizing particle passes near a sensitive p-n junction [2] [3] [4] [5] [6]. The particle produces a dense column of electron-hole pairs. If the ionization track traverses close enough to the depletion region, then the non-equilibrium charge distribution can induce a temporary modulation of the potential along the trajectory of the event. A period of prompt collection typically follows as the potential collapses to the normal state. Subsequently, motion of carriers by diffusion to the p-n junction dominates the collection process until all the excess carriers are collected, recombine, or diffuse away from the junction area [7] [8] [9]. The charge collected from the radiation event produces a current pulse at the node. The time constants depend strongly on the type of ion, its energy, and the properties of the specific technology.

Digital Integrated Circuits (ICs) exhibit complex responses due to interactions with ionizing radiation. Soft error calculations depend on the circuit characteristics, specifically the impact of charge collection, Q_{coll}, for SET pulse-width generation and propagation through digital ICs created with standard cell libraries [3] [7] [8] [9] [10] [11] [12]. Traditionally, the current resulting from the charge collected on a sensitive node is modeled as a double exponential waveform [13]. However, this model is not sufficient to model long single event transients that have been observed experimentally [14] [15]. This paper introduces a technique that uses dual double-exponential current sources to capture the complex behavior within an IC caused by a particle strike. The model has been used to simulate the response within inverters, two-input NAND gates, and two-input NOR gates. The responses were in agreement with semiconductor device modeling the results are compared to actual experimental data reported by Cannon et al. in 2009 [16].

This paper is organized as follows. Section II provides a discussion on the basic mechanisms to be modeled. Section III discusses the new approach to model single event transients. Section IV describes the methodology of how key parameters were determined. Section V presents a validation of the modeling approach. Finally, Section VI summarizes the paper.

II. Background

After an ion passes through a sensitive volume in a digital cell, a voltage SET can appear at the cell's output (Fig. 1). After the transient propagates through a few library cells, the response of the circuit shapes the SET into a square-wave (Fig. 2).

In advanced ICs, the circuit response time can be comparable to the characteristic time for single-event charge collection event; the charge collection process dynamically interacts with the cell's circuit response to the event [6] [17] [18]. Correctly modeling the transient shape of the pulse is critical to providing accurate predictions of soft errors in

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circuits [19] [20] [21]. The remainder of this section discusses how transients are modeled as well as the limitations of using the traditional double-exponential current source model.

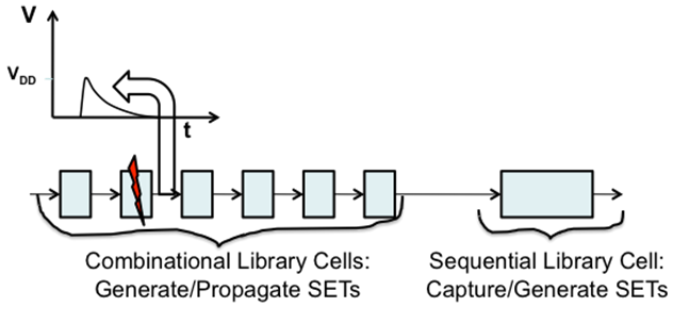


Fig. 1. Ion strike on combinatorial library cell modeled as double exponential current source.

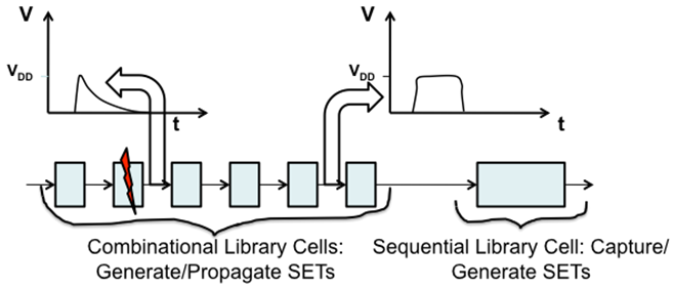


Fig. 2. Propagation of double-exponential current source to square wave.

A. Transient Modeling

A commonly used analytical model to approximate the induced transient current waveform is the double-exponential function with a rapid rise time and gradual fall time (Fig. 3) [7] [9]. This waveform is the most common form used in transistor-level simulations. The equation for this current pulse, *I(t)*, in SPICE is:

$$I(t) = \begin{cases} 0 & ;t < t_{d1} \\ I_{Peak}\left(1 - e^{\frac{-(t-t_{d1})}{\tau_1}}\right) & ;\ t_{d1} < t < t_{d2} \\ I_{Peak}\left(e^{\frac{-(t-t_{d2})}{\tau_2}} - e^{\frac{-(t-t_{d1})}{\tau_1}}\right) & ;t > t_{d2} \end{cases} \quad (1)$$

where, t_{d1} is the onset of the rise of the current, t_{d2} is the onset of the fall of the current, I_{Peak} is the maximum current to be approached, τ_1 is the rise time constant, and τ_2 is the fall time constant. The total charge delivered by the current pulse, Q_{Total}, is the integral over time of *I(t)*:

$$Q_{Total} = I_{Peak}\left[\tau_1 + \tau_2 + (t_{d2} - t_{d1}) - \tau_1 e^{\frac{-(t_{d2}-t_{d1})}{\tau_1}}\right] \quad (2)$$

If τ_1 is small compared to the difference in time between the rising and falling edges of the double-exponential waveform (t_{d2} - t_{d1}), then the last term is insignificant, and the calculation of total charge is simple.

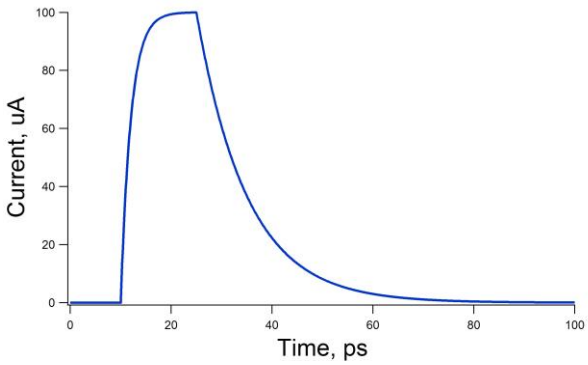


Fig. 3. Example of a double-exponential current pulse (I_{Peak} = 100 μA, t_{d1} = 10 ps, t_{d2} = 5 ps, τ_1 = 2 ps, τ_2 = 10 ps).

B. Limitations of the Double-Exponential Current Source Model for SETs

Previous research has shown that SET pulse-widths may be upwards of hundreds of picoseconds under some conditions [4] [22]. When these long pulses are modeled with one double-exponential current source, the resulting voltage transient either overdrives the circuit significantly or has a very slow leading edge, depending on the selection of parameters. If (t_{d2} – t_{d1}) is increased or if I_{Peak} is increased, then the current pulse can overdrive the circuit, forward-biasing the source-body junction(s). This property is shown in Fig. 4, where the transient voltage drops below V_{SS} = 0 volts. This overdrive will result in the simulation over-predicting the amount of charge needed to produce longer SET pulse-widths. On the other hand, if (t_{d2} – t_{d1}) is increased and if I_{Peak} is decreased to compensate for the overdrive, then the resulting voltage transient will have a slow leading edge (Fig. 5). Neither of these results describes SET pulses accurately [17] [18].

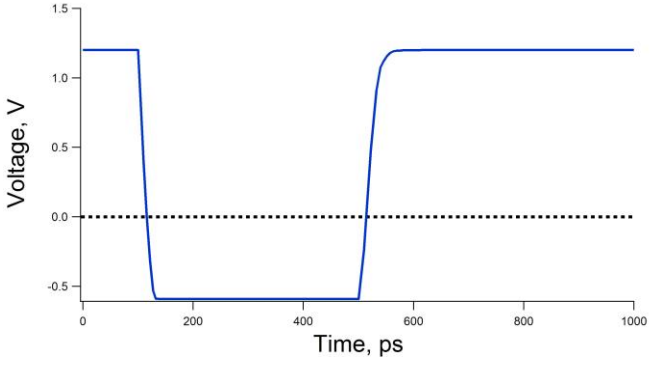


Fig. 4. Example of a voltage transient that overdrives the circuit (i.e., the voltage drops below V_{SS} = 0 volts).

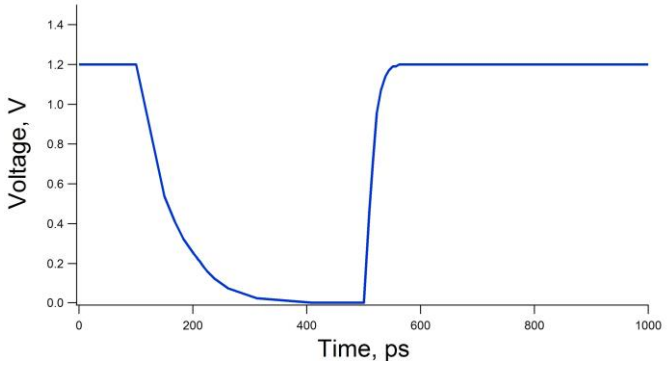


Fig. 5. Example of a voltage transient with a slow leading edge.

Other researchers have proposed single event models that make use of the node voltage to control the single event current source to overcome these limitations, but the implementation in a transistor simulation is no longer simple [17]. This paper introduces an extension of the double-exponential current source: the dual double-exponential current source. The dual double-exponential current source model is composed of two parallel double-exponential current sources, one for prompt charge collection and one for sustained charge collection. This model can be used to perform SET simulations.

III. Dual Double-Exponential Current Source Model

The dual double-exponential current source is based upon single event device-level simulations, as shown in Fig. 6 [17] [18] and identified in the schematic in Fig. 8. There is a short high current peak, followed by a sustained shelf of lower current. This behavior can be described by a long double-exponential current source with I_{Peak} equal to the shelf current and a short double-exponential current source to add the extra current for the short peak. Fig. 7 shows an example of the two individual current sources and the result of their parallel combination for the dual double-exponential current source model.

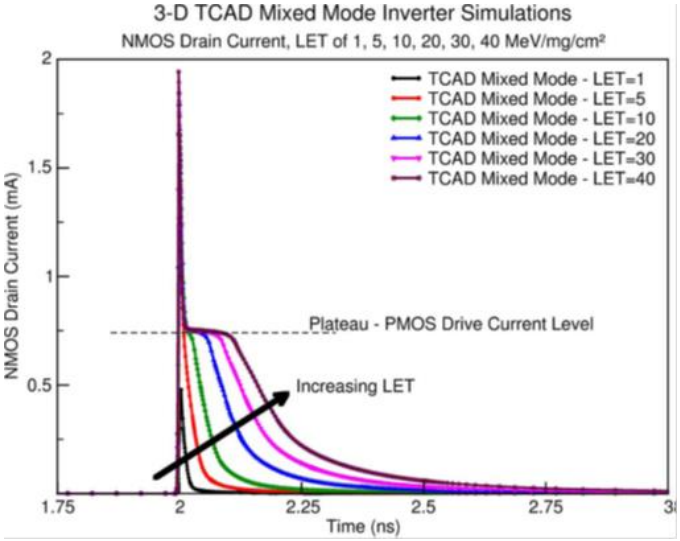


Fig. 6. Device-level simulation results showing short burst of high current followed by a sustained shelf of lower current (after [2]).

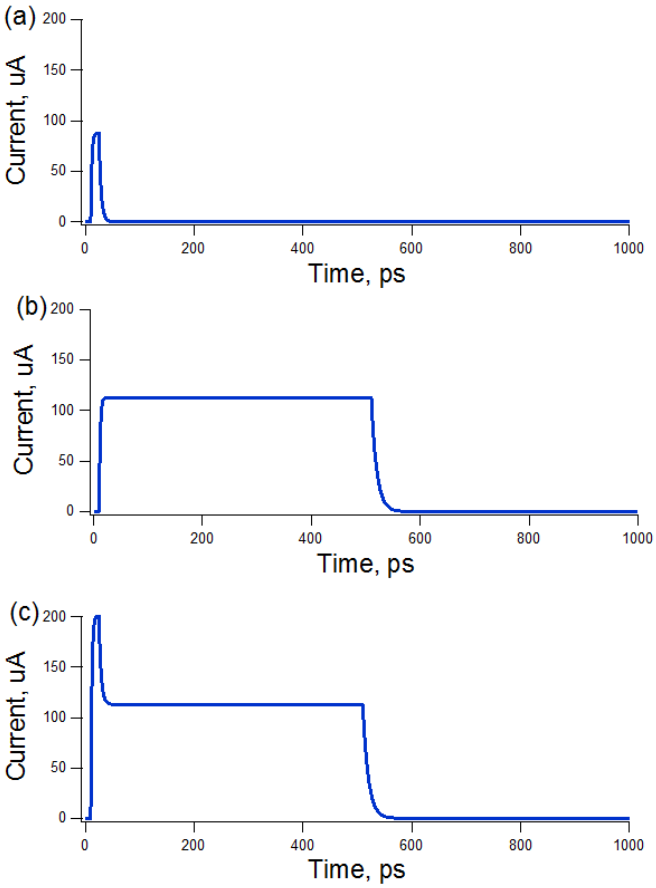


Fig. 7. Examples of: (a) short peak, $I_{Prompt}(t)$, (b) sustained, $I_{Hold}(t)$, and (c) dual double-exponential current sources.

A. Current Source Parameter Extraction

Both current sources have four parameters that need to be determined: I_{Peak}, $(t_{d2} - t_{d1})$, τ_1, and τ_2. For the short duration current source, $I_{Prompt}(t)$, the three time parameters are set from device-level single event simulations of a single transistor, which are calibrated to experimental data. Based on results obtained for a 90-nm technology, these are $(t_{d2} - t_{d1})$ = 15 ps, τ_1 = 2 ps, and τ_2 = 4 ps [18]. For the longer duration current source, $I_{Hold}(t)$, τ_1 = 2 ps and τ_2 = 10 ps provide a good fit, and $(t_{d2} - t_{d1})$ is used as a variable that depends on the amount of deposited charge.

The peak values for I_{Prompt} and I_{Hold} are determined through transistor-level simulations. The first set of simulations determines the peak current in a short-duration, double-exponential current source that causes the voltage output to change from one voltage rail to the other. For a basic inverter with its input held low, we simulated one double-exponential current source with $(t_{d2} - t_{d1})$ = 15 ps, τ_1 = 2 ps, and τ_2 = 10 ps and determined what I_{Peak} value drives the loaded inverter's voltage output to switch from V_{DD} to V_{SS}. This peak value is defined as I_{Thresh}, which equals the sum of I_{Prompt} and I_{Hold}. The second set of simulations determines I_{Hold} by applying the dual double-exponential current sources. We define the $I_{Prompt}(t)$ current source with the timing parameters from the 90-nm technology and $I_{Prompt} = I_{Thresh} - I_{Hold}$. We define the $I_{Hold}(t)$ current source with τ_1 = 2 ps, τ_2 = 10 ps, and $(t_{d2} - t_{d1})$ = 500

ps. We identify the I_{Hold} that will result in a transient voltage near the opposite rail at the end of the 500 ps, referenced as a longer transient by [4] [18]. The transient voltage may not remain near the opposite rail for the entire duration of the hold current.

B. Current Source Extraction from Given Charge Collection

Once the I_{Prompt} and I_{Hold} values have been extracted for the circuit, the total charge for the injected current is obtained as the sum of the charge from $I_{Prompt}(t)$ and the charge from $I_{Hold}(t)$, which are calculated from equation (3), separately. Determining the current sources from a given charge is a little more complicated, but still straightforward. For long SETs, $I_{Prompt}(t)$ does not depend on the total charge, so the charge from $I_{Prompt}(t)$ is independent of the details of the pulse plateau. The charge associated with $I_{Prompt}(t)$, namely Q_{Prompt}, is subtracted from the total charge (Q_{Total}) to obtain Q_{Hold}, the charge provided by $I_{Hold}(t)$:

$$Q_{Hold} = Q_{Total} - Q_{Prompt} \quad (3)$$

The second step is to apply equation (2) to Q_{Hold}, using ($t_{d2} - t_{d1}$) as a variable that depends on the total charge. As an example, consider I_{Prompt} = 97 μA, I_{Hold} = 114 μA, Q_{Total} = 25 fC, and the timing parameters given in this section. The calculation for Q_{Prompt} using equation (2) without the last term is:

$$Q_{Prompt} = (97x10^{-6})(2x10^{-12} + 4x10^{-12} + 15x10^{-12})\ C = 2.04\ fC \quad (4)$$

This means that Q_{Hold} is 2.04 fC less than 25 fC, or 22.96 fC. Applying equation (2) again for Q_{Hold} gives:

$$Q_{Hold} = (114x10^{-6})(2x10^{-12} + 4x10^{-12} + [t_{d2} - t_{d1}])\ C = 22.96\ fC \quad (5)$$

Solving equation (5) for ($t_{d2} - t_{d1}$) results in 151 ps.

IV. Dual Double-Exponential Current Source Parameters

A SPICE deck was created implementing both a baseline 4-inverter chain and the dual double-exponential current source model. A schematic of the baseline 4-inverter chain is shown below (Fig. 8).

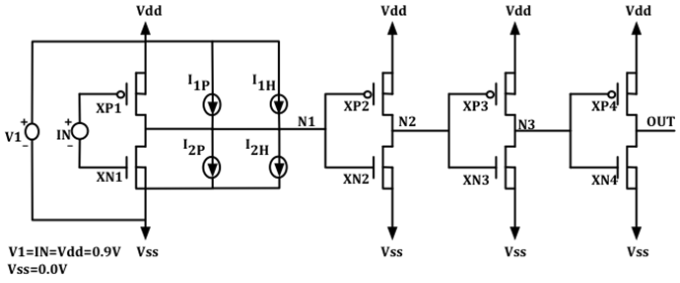


Fig. 8. Baseline 4-inverter chain schematic.

Automated scripting is used to determine the important parameters for the simulations. This process incorporates the implementation of the dual double-exponential current source model for SET pulses for both the NMOSFETs and PMOSFETs in the 90-nm inverter design. The flowchart that searches for I_{Thresh} is shown in Fig. 9. A flow chart for I_{Prompt} and I_{Hold} is shown in Fig. 10.

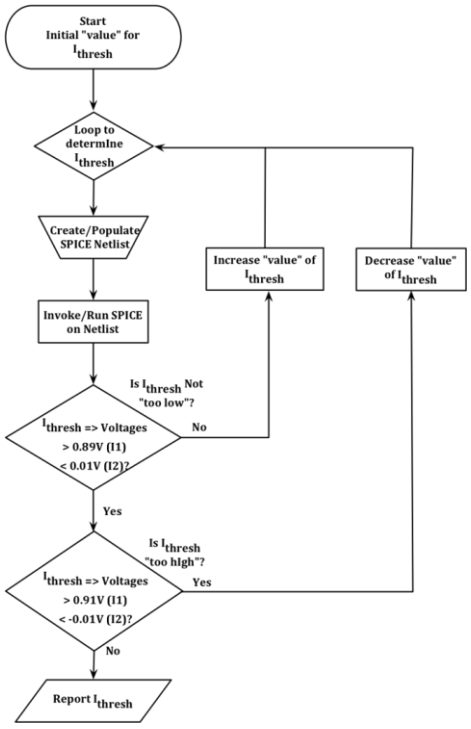


Fig. 9. Flowchart to identify I_{Thresh} variable for implementation with the dual double-exponential current source model.

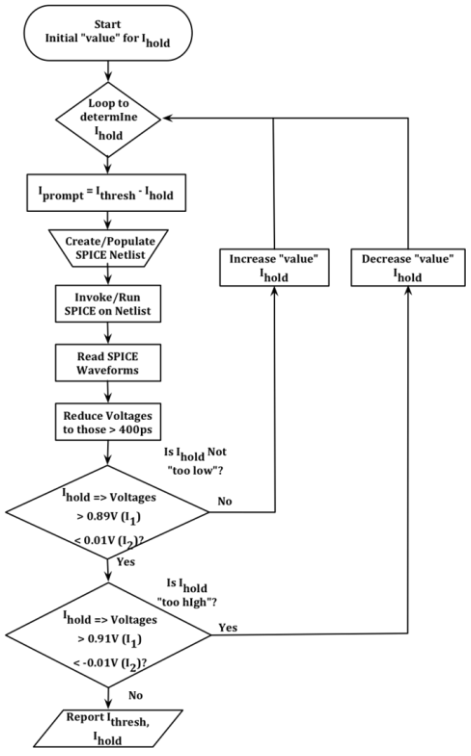


Fig. 10. Flowchart to identify I_{Prompt} and I_{Hold} variables for implementation into the dual double-exponential current source model.

A. *Digital Library Parameters*

We constructed several library cells for an IBM 90-nm technology and simulated them to determine I_{Prompt} and I_{Hold} for different input conditions and loads. The results are given in Tables I through IV. The first column of each table gives the cell name. For the inverter (INV1) cell, the W/L for the PMOSFET was 480 nm / 100 nm, and the NMOSFET was 200 nm / 100 nm. The INV2 cell used transistors with double-width transistors and the INV4 cell used quadruple-width transistors. The two-input NAND (NAND2) cell used the same width for the PMOSFETs and double the width for the NMOSFETs as the INV1 cell. Likewise, the two-input NOR (NOR2) cell used double the width for the PMOSFETs and the same width for the NMOSFETs as the INV1 cell.

The second column gives the input condition for each cell. For IN or IN1 = V_{DD}, the current sources were injected on the PMOSFET drain, and for IN or IN1 = V_{SS}, the current sources were injected on the NMOSFET drain(s).

The third column lists the load simulated with the number in parentheses giving the number of loads. The NAND2 and NOR2 cells were loaded by connecting the output to Input1 of the next cell. Input2 tied to appropriate rail voltage. This is the same configuration as the 90-nm logic cell chains that were radiation tested [16].

The fourth column provides the estimated node capacitance in fC. This value was calculated from model parameters and used output drain and load gate capacitance.

The fifth and sixth columns provide the determined I_{Prompt} and I_{Hold} levels in μA. The seventh column provides the calculated Q_{Prompt} for the $I_{Prompt}(t)$ current source. Finally, the eighth column gives an estimate for the total charge, Q_{Total}, to provide an SET with a 200 ps pulse-width. Example injected currents and resulting SET voltage waveforms are provided in Fig. 11 and Fig. 12, respectively.

TABLE I
SIMULATION RESULTS FOR INV1, NAND2, NOR2 CELLS FOR THE V_{DD} INPUT CONFIGURATION

Cell Name	Input Config.	Load	~C-Node, fC	I_{Prompt}, μA	I_{Hold}, μA	Q_{Prompt}, fC	~Q_{Total}, fC 200 ps
INV1	IN=V_{DD}	INV1 (1)	1.38	97	141	2.0	30.2
INV1	IN=V_{DD}	INV1 (2)	2.20	169	141	3.5	31.7
INV1	IN=V_{DD}	INV1 (4)	3.83	270	140	5.7	33.7
NAND2	IN1=V_{DD}, IN2=V_{DD}	NAND2 (1)	1.74	157	153	3.3	33.9
NOR2	IN1=V_{DD}, IN2=V_{SS}	NOR2 (1)	2.23	169	141	3.5	31.7

TABLE II
SIMULATION RESULTS FOR INV1, NAND2, NOR2 CELLS FOR THE V_{SS} INPUT CONFIGURATION

Cell Name	Input Config.	Load	~C-Node, fC	I_{Prompt}, μA	I_{Hold}, μA	Q_{Prompt}, fC	~Q_{Total}, fC 200 ps
INV1	IN=V_{SS}	INV1 (1)	1.38	88	113	1.8	24.4
INV1	IN=V_{SS}	INV1 (2)	2.20	173	113	3.6	26.2
INV1	IN=V_{SS}	INV1 (4)	3.83	271	113	5.7	28.3
NAND2	IN1=V_{SS}, IN2=V_{DD}	NAND2 (1)	1.74	131	113	2.8	25.4
NOR2	IN1=V_{SS}, IN2=V_{SS}	NOR2 (1)	2.23	180	110	3.8	25.8

TABLE III
SIMULATION RESULTS FOR INVERTER CELLS OF INCREASING DRIVE STRENGTH FOR THE V_{DD} INPUT CONFIGURATION

Cell Name	Input Config.	Load	~C-Node, fC	I_{Prompt}, μA	I_{Hold}, μA	Q_{Prompt}, fC	~Q_{Total}, fC 200 ps
INV1	IN=V_{DD}	INV1 (1)	1.38	97	141	2.0	30.2
INV2	IN=V_{DD}	INV2 (1)	2.59	196	264	4.1	56.9
INV4	IN=V_{DD}	INV4 (1)	4.99	388	512	8.1	110.5

TABLE IV
SIMULATION RESULTS FOR INVERTER CELLS OF INCREASING DRIVE STRENGTH FOR THE V_{SS} INPUT CONFIGURATION

Cell Name	Input Config.	Load	~C-Node, fC	I_{Prompt}, μA	I_{Hold}, μA	Q_{Prompt}, fC	~Q_{Total}, fC 200 ps
INV1	IN=V_{SS}	INV1 (1)	1.38	88	113	1.8	24.4
INV2	IN=V_{SS}	INV2 (1)	2.59	175	225	3.7	48.7
INV4	IN=V_{SS}	INV4 (1)	4.99	356	454	7.5	98.3

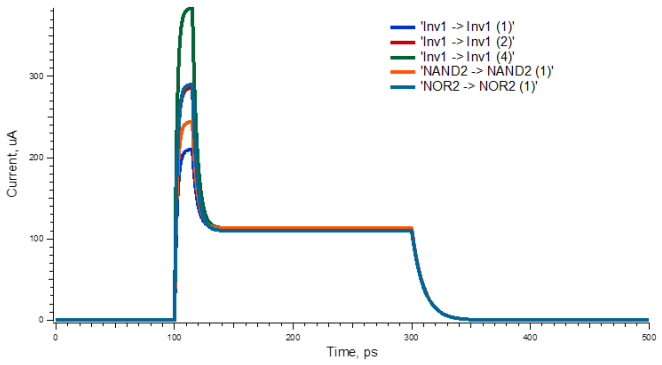


Fig. 11. Injected current waveforms for circuit configurations with loads listed in Table II to produce ~200 ps SETs.

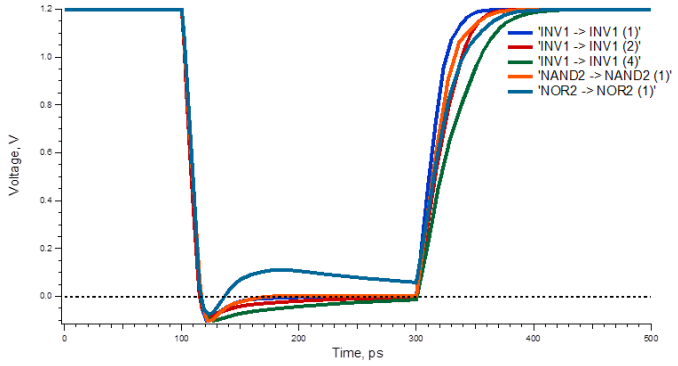


Fig. 12. Resulting SET voltage waveforms for the circuit configurations with loads listed in Table II and for the injected current waveforms shown in Fig. 11.

I_{Hold} is a strong function of the restoring current in the circuit (i.e., drive strength). The INV1, NAND2, and NOR2 cells have similar restoring currents, and I_{Hold} is nearly constant in these cells, as seen in Table I and Table II. INV2 has twice the restoring current and INV4 has four times the restoring current. I_{Hold} in these cells generally scales with the increase in restoring current (Table III and Table IV). I_{Hold} does not depend upon the load, demonstrated by the first three rows in each of Table I and Table II. On the other hand, I_{Prompt} is a strong function of the node capacitance, as the ratio between I_{Prompt} and the node capacitance remains fairly constant throughout all tables. For all base cells (INV1, NAND2, NOR2), the charge that results in a 200 ps SET varies between 24.4 and 28.3 fC for NMOSFET simulations and 30.2 and 33.9 fC for PMOSFET simulations. As a result, SET pulse-widths show little variation for different loads and different cell types for logic cells with similar drive strengths.

B. Comparison of models

Fig. 12 shows the resulting voltage waveforms from the model proposed in the paper and Fig. 13 shows similar results from device-level modeling. A comparison illustrates the potential inaccuracies of this model. The inaccuracies arise from driving the voltage to the opposite voltage rail at the end of a long SET, where the device-level simulations show a slow drift away from the opposite voltage rail. All but one of the voltage transients shown in Fig. 12 will drive the output voltage slightly below V_{SS} following the initiation of the single event current sources. These simulation results will produce a slight over prediction of the amount of charge needed to produce that SET pulse. The other voltage transient, NOR2 –> NOR2 (1), shows the output voltage going back above V_{SS} and staying above until the end of the transient. This simulation result will produce a slight under-prediction of the amount of charge needed to produce that SET pulse. However, the dual double-exponential current source model will still be more accurate than the one double-exponential current source model.

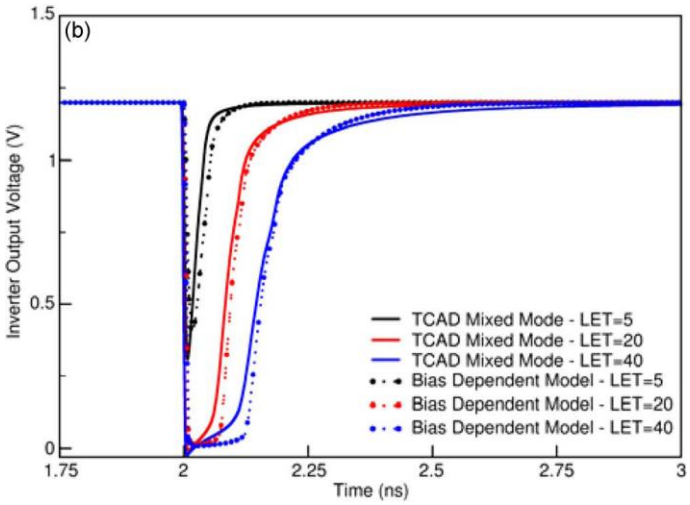


Fig. 13. Device-level simulation results showing voltage transients (solid lines) for various deposited charges (after [2]).

V. Validation to Experimental Data for CMOS Combinatorial Cells

We used SPICE circuit analysis for data comparison and detail the process to characterize combinatorial cells from a 90-nm technology. The results of the implementation are reported. The results are compared to actual experimental data reported by Cannon et al. in 2009 [16].

Monte Carlo Radiative Energy Deposition (MRED) was used in conjunction with nested sensitive volumes to determine the critical charge collection. This process is described in detail in [11] [23] [24] [25]. The sensitive volumes are defined identically for the three specific combinatorial cells (INVx1, NAND2x1 and NOR2x1) from this library. Experimental data published in Cannon et al. [16] is used for calibration of the sensitive volumes and their efficiencies. The efficiencies tracked the work given in Warren et al. [10] [23] very well. Each PMOSFET and NMOSFET transistor (or set of transistors in the same active area) contains four sensitive volumes and is described in detail in [25].

The charge deposited in each sensitive volume is summed by specific charge collection efficiencies to determine the total amount of charge collected in each transistor type. The charge is then used to create the independent current sources described in Section III to be used for the SPICE simulation.

There were three different configurations given for the NAND2x1 and NOR2x1 circuits: (1) a chain of circuits connecting the output of one cell to the first input of the following cell with the other in put tied high or low, (2) a chain of circuits connecting the output of one cell to the second input of the following cell with the other in put tied high or low, and (3) a chain of circuits connecting the outputs of one cell to both inputs of the following cell.

The circuits simulated are duplicates of the circuits in [16]. The circuits consist of 65 combinatorial cells followed by delay elements, a guard gate, and an asynchronous latch. An example of the INVx1 is shown in Fig. 14. The SPICE simulation randomly selects a node to apply the single event and checks to determine if the latch has changed states. If

so, then it records the event. This simulation method recreates the single event experiment.

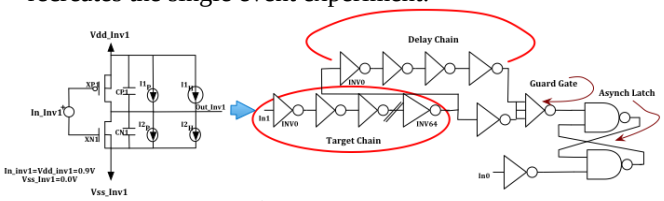


Fig. 14. Example core circuit for SET characterization test structure.

A. *Comparison of Model to Experimental Data*

Nested sensitive volumes are used to determine the charge collected for the inverter, NAND gate, and the NOR gate for a variety of ion species and energies. Fig. 15, Fig. 16, and Fig. 17 compare the SPICE predictions of SET cross section to the experimental data presented by Cannon et al. [16]. These data show that, for the most part, the SPICE predictions are in closer agreement with the experimental data at lower LETs than at higher LETs. The lack of agreement at the highest LETs is most likely do the limited applicability of the simple double-exponential current source, e.g., it does not contain appropriate terms to model multi-node charge collection. These figures demonstrate that the model shows an increase in SET pulse-width vs. LET as well as high variations in the pulse-width under specific ion test conditions.

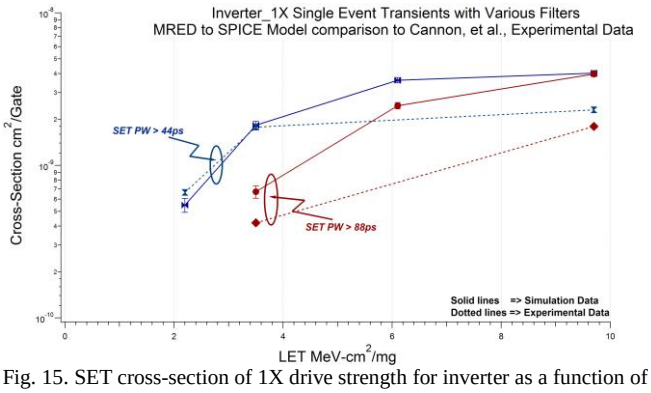


Fig. 15. SET cross-section of 1X drive strength for inverter as a function of LET. MRED to SPICE predictions are drawn with solid lines and SEE data is drawn with dashed lines.

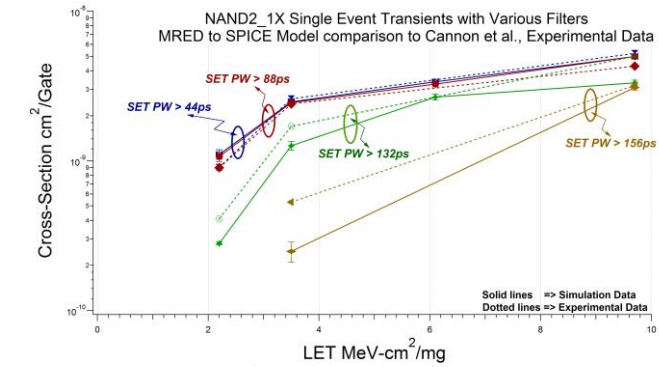


Fig. 16. SET cross-section of 1X drive strength of 2-input NAND gate as a function of LET. MRED to SPICE predictions are drawn with solid lines and SEE data are drawn with dashed lines (after [26]).

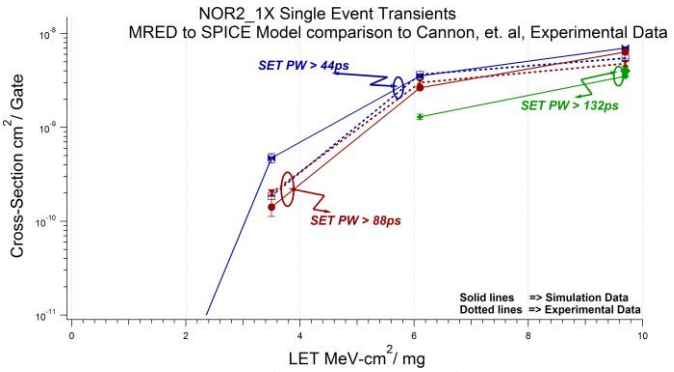
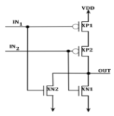


Fig. 17. SET cross-section of 1X drive strength for 2-input NOR gate as function of LET. MRED to SPICE predictions are drawn with solid lines and SEE data are drawn with dashed lines.

B. *Applicability of the model*

One application for this model is the ability to predict the SET response for a logic cell and its different input configurations when the gate accepts multiple inputs. An inverter chain only has one option, while 2-input gates (i.e., IN1, IN2) can receive one or both inputs from the previous gate. The three different configurations are listed in Table V.

TABLE V
INPUT CONFIGURATIONS FOR 2-INPUT NOR GATE

Cell	Schematic	Chain Configuration
NOR2x1		**(v1)** IN_1 = "Chain", $IN_2 = V_{ss}$
		(v2) $IN_1 = V_{ss}$, IN_2 = "Chain"
		(v3) $IN_1 = IN_2$ = "Chain"

The first chain configuration in Table 9, v1, is designed with IN1 receiving its signal from the logic chain, while IN2 is tied to Vss. Another configuration, v3, is designed with IN1 tied to IN2 and also tied to the logic chain. These two configurations have the output drain electrically connected to the intermediate drain. Therefore, these two configurations have the highest drain cross-section. The last configuration, v2, is designed with IN1 tied to Vss while IN2 is tied to the logic chain. This configuration has the intermediate drain electrically connected to the source, so it has the smallest drain cross-section. The intermediate drain layout is designed three times as large as the output drain. In Table V., Q_{thresh} is the smallest value for Configuration v2. Therefore, it has the highest cross-section at the lower LETs. Finally, all of these chains attenuate the SET pulse as it propagates down the chain with v3 having the largest attenuation. Pulse attenuation gives an apparent decrease in cross-section and that is why the v3 configuration is lower than the v1 configuration.

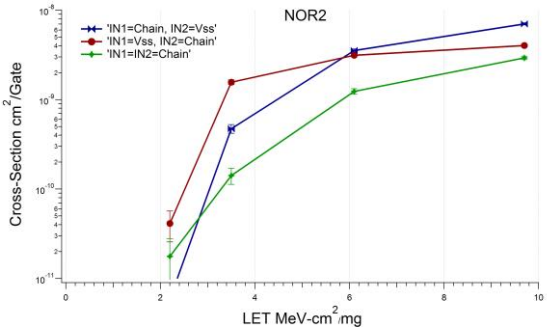


Fig. 18. SET cross-section of 1X drive strength NOR2 MRED to SPICE results with different input chain configurations from Table V.

VI. Summary

We modified the traditional double-exponential current source for single event transistor-level simulation for the generation of long SET pulses. This modification split the double-exponential current source into two parallel double-exponential current sources. We provided a methodology for determining the current source parameters and demonstrated this methodology on several library cells. From this work, we conclude that the charge needed to generate long SET pulses is most dependent on the restoring current of the library cell and less dependent on the cell type or load.

The SPICE simulations allow analysis of SET experiments on combinatorial logic chains when the incident particles produce low levels of charge deposition. The models can predict the SET response of the combinatorial logic given different input configurations. The SPICE simulation can also predict the SET response of other combinatorial logic cells in the same technology.

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