INTEGRATED CIRCUITS

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF40106B gates HEX inverting Schmitt trigger

Product specification
File under Integrated Circuits, IC04

January 1995





HEF40106B gates

HEX INVERTING SCHMITT TRIGGER

Each circuit of the HEF40106B functions as an inverter with Schmitt-trigger action. The Schmitt-trigger switches at different points for the positive and negative-going input signals. The difference between the positive-going voltage (V_P) and the negative-going voltage (V_N) is defined as hysteresis voltage (V_H).

This device may be used for enhanced noise immunity or to "square up" slowly changing waveforms.

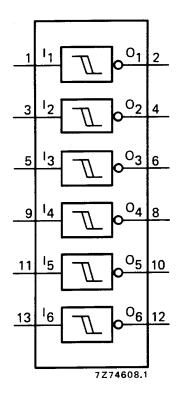


Fig. 1 Functional diagram.

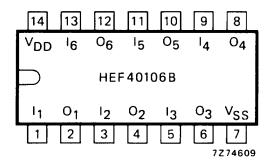


Fig. 2 Pinning diagram.

HEF40106BP(N): 14-lead DIL; plastic

(SOT27-1)

HEF40106BD(F): 14-lead DIL; ceramic (cerdip)

(SOT73)

HEF40106BT(D): 14-lead SO; plastic

(SOT108-1)

(): Package Designator North America

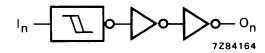


Fig. 3 Logic diagram (one inverter).

FAMILY DATA

IDD LIMITS category GATES

see Family Specifications

D.C. CHARACTERISTICS

 $V_{SS} = 0 V; T_{amb} = 25 °C$

| | V _{DD} V | symbol | min. | typ. | max. | |
|------------------|----------------------|----------------|------|------|------|---|
| Hysteresis | 5 | | 0,5 | 0,8 | | V |
| voltage | 10 | v_H | 0,7 | 1,3 | | V |
| | 15 | | 0,9 | 1,8 | | V |
| Switching levels | 5 | | 2 | 3,0 | 3,5 | V |
| positive-going | 10 | Vp | 3,7 | 5,8 | 7 | V |
| input voltage | 15 | • | 4,9 | 8,3 | 11 | V |
| negative-going | 5 | | 1,5 | 2,2 | 3 | V |
| input voltage | 10 | V _N | 3 | 4,5 | 6,3 | V |
| | 15 | ., | 4 | 6,5 | 10,1 | V |

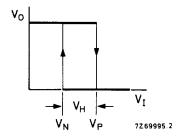


Fig. 4 Transfer characteristic.

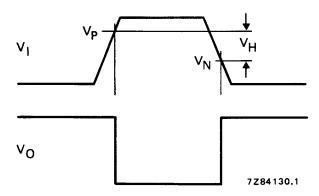


Fig. 5 Waveforms showing definition of V_P , V_N and V_H , where V_N and V_P are between limits of 30% and 70%.

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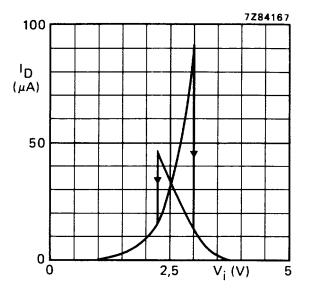
A.C. CHARACTERISTICS

 V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times \leq 20 ns

| | V _{DD} | symbol | typ. | max. | | typical extrapolation formula |
|---------------------------------|-----------------|--------|------|------|----|-------------------------------------|
| Propagation delays | | | | | | |
| I _n → O _n | 5 | | 90 | 180 | ns | 63 ns + (0,55 ns/pF) C ₁ |
| HIGH to LOW | 10 | tPHL | 35 | 70 | ns | 24 ns + (0,23 ns/pF) C |
| | 15 | | 30 | 60 | ns | 22 ns + (0,16 ns/pF) C |
| | 5 | | 75 | 150 | ns | 48 ns + (0,55 ns/pF) C ₁ |
| LOW to HIGH | 10 | tPLH | 35 | 70 | ns | 24 ns + (0,23 ns/pF) C |
| | 15 | | 30 | 60 | ns | 22 ns + (0,16 ns/pF) C |
| Output transition | | | | | | ; |
| times | 5 | | 60 | 120 | ns | 10 ns + (1,0 ns/pF) Cլ |
| HIGH to LOW | 10 | tTHL | 30 | 60 | ns | 9 ns + (0,42 ns/pF) C _L |
| | 15 | | 20 | 40 | ns | 6 ns + (0,28 ns/pF) C |
| | 5 | | 60 | 120 | ns | 10 ns + (1,0 ns/pF) Cլ |
| LOW to HIGH | 10 | tTLH | 30 | 60 | ns | 9 ns + (0,42 ns/pF) CL |
| | 15 | | 20 | 40 | ns | 6 ns + (0,28 ns/pF) C_ |

| | V _{DD} V | typical formula for P (μW) | where $f_i = \text{input freq. (MHz)}$ |
|---|----------------------|--|---|
| Dynamic power dissipation per package (P) | 5 10 15 | 2 300 f _i + Σ (f _o C _L) × V _{DD} ² 9 000 f _i + Σ (f _o C _L) × V _{DD} ² 20 000 f _i + Σ (f _o C _L) × V _{DD} ² | f_{O} = output freq. (MHz) C_{L} = load capacitance (pF) $\Sigma(f_{O}C_{L})$ = sum of outputs V_{DD} = supply voltage (V) |

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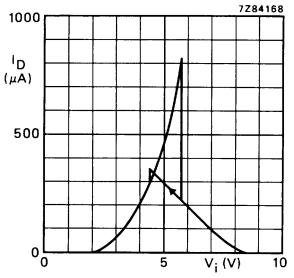


Fig. 6 Typical drain current as a function of input voltage; $V_{DD} = 5 \text{ V}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$.

Fig. 7 Typical drain current as a function of input voltage; $V_{DD} = 10 \text{ V}$; $T_{amb} = 25 \text{ °C}$.

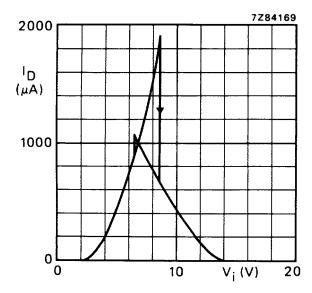


Fig. 8 Typical drain current as a function of input voltage; V_{DD} = 15 V; T_{amb} = 25 °C.

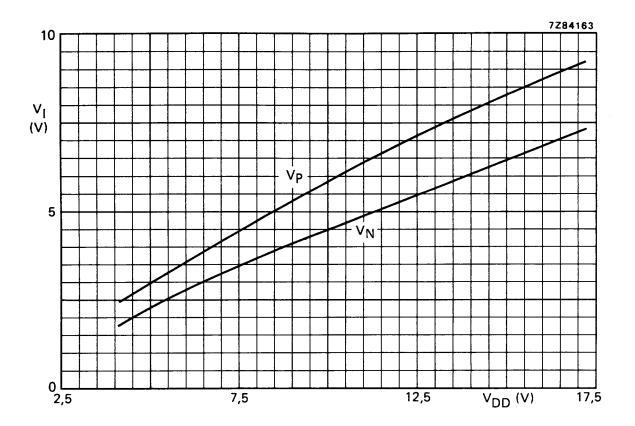


Fig. 9 Typical switching levels as a function of supply voltage V_{DD}; T_{amb} = 25 °C.

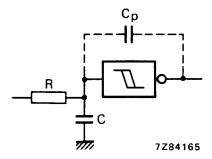


Fig. 10 Schmitt trigger driven via a high impedance (R > 1 k Ω).

If a Schmitt trigger is driven via a high impedance (R > 1 k Ω) then it is necessary to incorporate a capacitor C of such value that: $\frac{C}{C_p} > \frac{V_{DD} - V_{SS}}{V_H}$, otherwise oscillation can occur on the edges of a pulse.

 C_{p} is the external parasitic capacitance between input and output; the value depends on the circuit board layout.

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APPLICATION INFORMATION

Some examples of applications for the HEF40106B are:

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators.

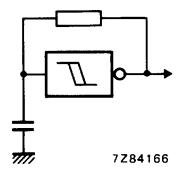


Fig. 11 The HEF40106B used as an astable multivibrator.