

DSP3210 Digital Signal Processor The Multimedia Solution



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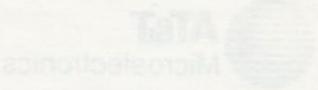


September 1991

AT&T DSP3210
Digital Signal Processor
Information Manual



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Foreword

This manual contains detailed information regarding the design and applications of the AT&T DSP3210 Digital Signal Processor that is essential to engineers designing systems using this device. The AT&T DSP3210 Support Software Tools, AT&T DSP3210 C-Compiler, and the AT&T DSP3210 Application Library are available to aid in developing software for the devices and integrating them into system environments.

Additional information on the digital signal processor product line is available in the form of manuals, data sheets, and application notes.



Foreword

Dear Friends, Colleagues, and Stakeholders,

This foreword is intended to provide a brief overview of the purpose and scope of the report, which is the result of a collaborative effort between the World Health Organization (WHO) and the International Agency for Research on Cancer (IARC). The report aims to provide a comprehensive assessment of the evidence linking exposure to environmental tobacco smoke (ETS) with various health outcomes, including cancer.

The report is based on a systematic review of the scientific literature, including observational studies, case-control studies, cohort studies, and experimental studies. The evidence is evaluated using strict criteria to ensure its validity and relevance. The report also considers the potential mechanisms through which ETS may contribute to health outcomes, such as the effects on the cardiovascular system, respiratory system, and nervous system.

The findings of the report indicate that exposure to ETS is associated with an increased risk of several types of cancer, including lung cancer, oral cavity cancer, esophageal cancer, and bladder cancer. The report also highlights the significant health risks associated with ETS, particularly for non-smokers and children.

We hope that this report will contribute to the global efforts to reduce the health risks associated with ETS and promote a healthier environment for all. We thank all the authors and reviewers who contributed to this important work.

AT&T DSP3210 DIGITAL SIGNAL PROCESSOR

INFORMATION MANUAL

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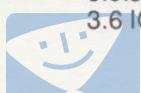
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Chapter 1
Introduction



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1. INTRODUCTION

The AT&T DSP3210 brings the power of floating-point signal processing to personal computers and workstations opening a wide range of multimedia applications. From its conception, the DSP3210 has been engineered with a single focus: enabling advanced multimedia functions on personal computers and workstations. Based on AT&T's very successful DSP32C architecture, the DSP3210 breaks new ground in its ability to be easily integrated into personal computer and workstation system designs. Particular attention was paid to primary bus interfacing; the DSP3210 is compatible with both Intel and Motorola microprocessor signalling. This allows designers to easily create low-cost systems using the DSP3210 as a bus-master device. A full bus-level *SmartModel** of the DSP3210 is offered by Logic Automation for system simulation of designs incorporating the DSP3210.

In addition to its optimizing C compiler and assembly language support tools, the DSP3210 features a powerful real-time operating system, the *AT&T Visible Caching Operating System™* (VCOS™), which supports both multi-tasking and multi-processing. The VCOS operating system is an open development environment that allows the DSP3210 to use existing system memory in PCs and workstations rather than requiring expensive dedicated SRAM. Complete real-time debugging tools are included with the VCOS operating system to speed both application and algorithm development. By separating the application and algorithm development phases of multimedia software development, development schedules are simplified and shortened. The VCOS operating system includes its own multimedia function library complete with speech processing, speech recognition, graphics, music processing, and modem functions. In addition to new application software, the DSP3210 has access to the large base of existing DSP32C application software.

This document is a reference guide for the DSP3210 device. It describes the architecture, instruction set, and interfacing specifications of the device. The information necessary to write programs for the DSP3210 is also given in this manual. Separate documents are available with detailed information on the software and hardware development tools. No previous experience with digital signal processors is necessary to use this document, but an understanding of digital signal processing concepts and assembly language programming on microprocessors or minicomputers is recommended.

1.1 Digital Signal Processing With The DSP3210

A key element shared by all DSP applications is a large number of repetitive mathematical operations combined with extreme memory bandwidth requirements. To perform floating-point arithmetic operations, conventional microprocessors and co-processors use software routines and/or microcode. Newer RISC- and CISC-based microprocessors offer much higher floating-point performance but lack the memory bandwidth and signal processing architecture required for DSP applications. Microprocessors also include many functions unnecessary for signal processing resulting in an unacceptable price/performance ratio for high-volume, low-cost signal processing applications.

The DSP3210 architecture combines a hardware floating-point arithmetic unit with an architecture that supports 4 memory accesses per instruction cycle, allowing the device to perform up to 33 million floating-point operations per second (with a clock rate of 66.7 MHz). This raw floating-point performance is combined with the DSP3210's signal processing architecture to enable real-time applications such as speech compression/recognition/synthesis, 3D graphics transformations, high-quality music coding/decoding, image processing, and real-time handwriting analysis/recognition. New functions can easily be added to DSP3210-based systems with the addition of application software. Multiple DSP3210s can be combined easily to increase system performance. (AT&T's VCOS real-time operating system directly supports multiple DSP3210 implementations.)

The use of floating-point arithmetic in the DSP3210 simplifies application development because it eliminates the effects of scaling, normalization, and overflow (which complicate development when using a fixed-point device). Also, many existing algorithms developed for use on large computers and array processors (using floating-point arithmetic) can be easily converted for use on the DSP3210. Program development is typically 3 to 10 times faster on the DSP3210 than similar program development on fixed-point processors. This is especially critical in multimedia applications where time-to market is a critical parameter, and a large percentage of application development is performed by third-party application developers. In addition to ease of program development, 32-bit floating-point is often required for advanced algorithm implementations.

* SmartModel is a registered trademark of Logic Automation.



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Early in the development of a particular application, one must determine the dynamic range and precision requirements for the given algorithm. The following is a comparison of the dynamic range and precision attainable for various data word sizes. The floating-point representation of a number in the DSP3210 consists of a 24-bit mantissa and an 8-bit exponent. The magnitude of the mantissa is normalized to lie between 1 and 2. Thus, the range for the magnitude of a floating-point number N is approximately:

$$|N| = (1 \times 2^{-127}, 2 \times 2^{127}) \text{ or } (5.9 \times 10^{-39}, 3.4 \times 10^{38}),$$

providing an overall dynamic range in excess of 1500 dB.

Figure 1-1 shows the dynamic range for DSP3210 floating-point numbers as compared with the dynamic range of 16- and 24-bit fixed-point devices.

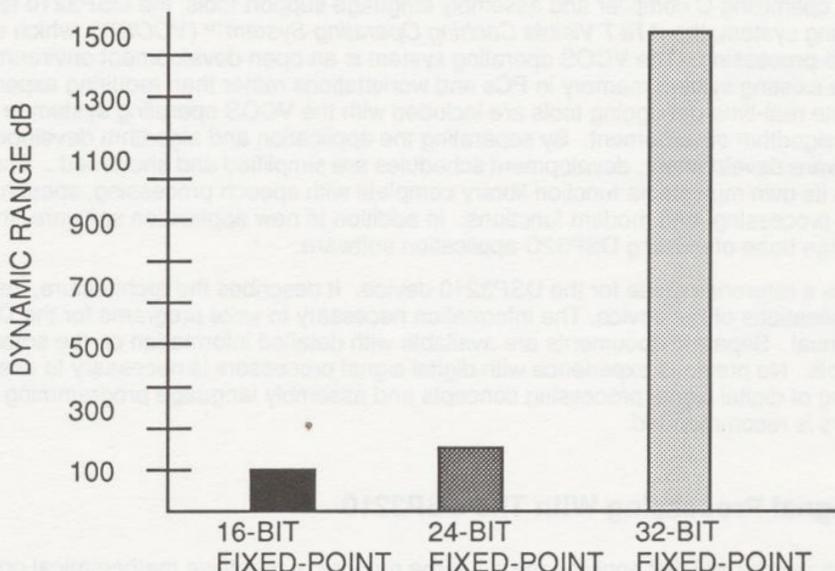


Figure 1-1 Dynamic Range of Fixed- and Floating-Point DSPs

The precision of a floating-point number is determined by the size of the mantissa. The DSP3210 floating-point format provides 24 bits of precision at all magnitudes within the range of numbers represented by the 24-bit mantissa and 8-bit exponent. (Note that the DSP3210 also has eight extra bits, the guard bits, in the mantissa of the 40-bit floating-point adder and accumulators. These guard bits provide added precision during accumulation operations). In contrast, the precision of a fixed-point format is a function of its word size and the magnitude of the given number. Figure 1-2 shows the bits of precision versus magnitude of a number for the DSP3210 floating-point format, as well as 16- and 24-bit fixed-point formats.



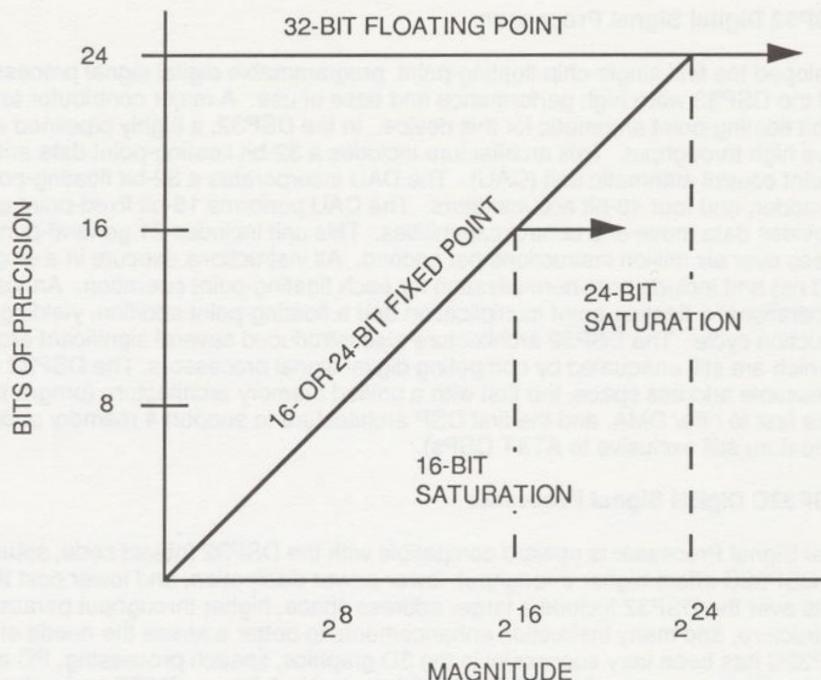


Figure 1-2 Precision of Fixed- and Floating-Point DSPs

1.2 The AT&T Floating-Point Digital Signal Processor Family

AT&T was the first to produce floating-point digital signal processors and has continued to play a leadership role in the floating-point marketplace. Figure 1-3 shows the evolution of the AT&T family of floating-point digital signal processors.

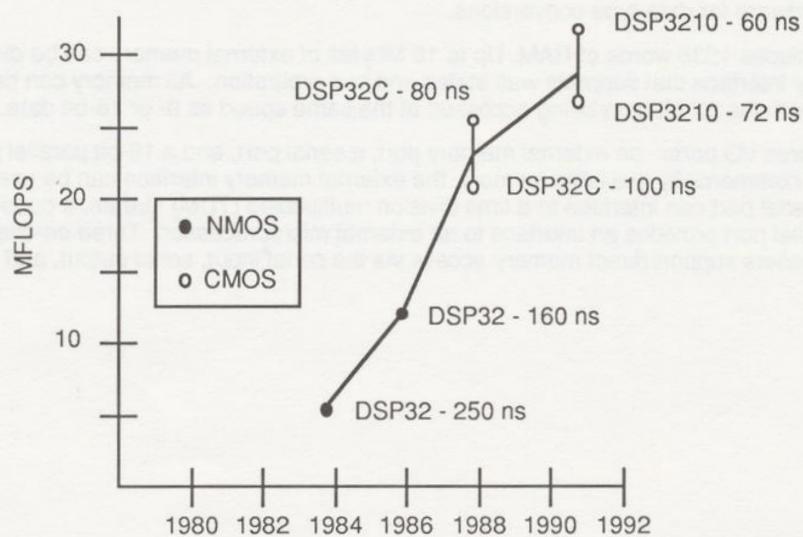


Figure 1-3 AT&T Floating-Point DSP Family Evolution

1.2.1 The AT&T DSP32 Digital Signal Processor

In 1984, AT&T developed the first single-chip floating-point programmable digital signal processor, the DSP32. The design goals of the DSP32 were high performance and ease of use. A major contributor to these goals was the selection of 32-bit floating-point arithmetic for this device. In the DSP32, a highly pipelined architecture allows the device to achieve high throughput. This architecture includes a 32-bit floating-point data arithmetic unit (DAU) and a 16-bit fixed-point control arithmetic unit (CAU). The DAU incorporates a 32-bit floating-point multiplier, a 40-bit floating-point adder, and four 40-bit accumulators. The CAU performs 16-bit fixed-point arithmetic and logic operations, and provides data move and control capabilities. This unit includes 21 general-purpose registers. The DSP32 processes over six million instructions per second. All instructions execute in a single cycle (four clock periods or 160 ns) and include post-normalization for each floating-point operation. An instruction may have two floating-point operations: a floating-point multiplication and a floating-point addition, yielding two floating-point operations per instruction cycle. The DSP32 architecture also introduced several significant architectural features, many of which are still unequaled by competing digital signal processors. The DSP32 was the first DSP to offer a byte-addressable address space, the first with a unified memory architecture (program and data share the same space), the first to offer DMA, and the first DSP architecture to support 4 memory accesses per instruction cycle (a feature still exclusive to AT&T DSPs).

1.2.2 The AT&T DSP32C Digital Signal Processor

The DSP32C Digital Signal Processor is upward compatible with the DSP32 (object code, source code, and pin compatibility). The DSP32C offers higher throughput, lower power dissipation, and lower cost than the DSP32. Major enhancements over the DSP32 include a larger address space, higher throughput parallel I/O, a fully vectored interrupt structure, and many instruction enhancements to better address the needs of DSP systems designers. The DSP32C has been very successful in the 3D graphics, speech processing, PC add-on card, and telecommunications application areas. The DSP32C is fabricated in 0.75 μm CMOS technology and is packaged in standard 164-pin and 68-pin (microcomputer version) plastic packages as well as a 133-pin ceramic PGA package.

The DSP32C's two execution units, the control arithmetic unit (CAU) and the data arithmetic unit (DAU), are used to achieve the high throughput of 12.5 million instructions per second. The CAU performs 16- or 24-bit integer arithmetic and logic operations, and provides data-move and control capabilities. This unit includes 22 general-purpose registers. The DAU performs 32-bit floating-point arithmetic for signal processing functions. It includes a 32-bit floating-point multiplier, a 40-bit floating-point adder, and four 40-bit accumulators. The multiplier and the adder work in parallel to perform 25 million floating-point computations per second. The DAU also incorporates special-purpose hardware for data-type conversions.

On-chip memory includes 1536 words of RAM. Up to 16 Mbytes of external memory can be directly addressed by the external memory interface that supports wait states and bus arbitration. All memory can be addressed as 8-, 16-, or 32-bit data, with the 32-bit data being accessed at the same speed as 8- or 16-bit data.

The DSP32C has three I/O ports: an external memory port, a serial port, and a 16-bit parallel port. In addition to providing access to commercially available memory, the external memory interface can be used for memory-mapped I/O. The serial port can interface to a time division multiplexed (TDM) stream, a codec, or another DSP32C. The parallel port provides an interface to an external microprocessor. Three on-chip direct-memory-access (DMA) controllers support direct memory access via the serial input, serial output, and parallel I/O ports.

A single-level interrupt facility can respond to four internal and two external, individually maskable sources. A relocatable vector table controls program flow based on the source of the interrupt.

The DSP32C has two general types of instructions that correspond to the two execution units: data arithmetic (DA) instructions and control arithmetic (CA) instructions. Primarily, DA instructions perform 32-bit floating-point multiply/accumulate operations for signal processing algorithms. Other DA instructions convert the DSP32C internal floating-point data to and from each of the following types: 8-, 16-, or 24-bit 2's complement integer, 8-bit μ -law, 8-bit A-law, or 32-bit single-precision IEEE standard floating-point. The CA instructions perform microprocessor operations such as 16- and 24-bit integer arithmetic and logic functions, conditional branching, and moving data.

In summary, some of the key features of the DSP32C are as follows:

- Full, 32-bit floating-point arithmetic
- Four memory accesses per instruction cycle
- Single, linear address space
- Byte addressable internal and external memory
- Up to 16 Mbytes of external memory
- 1536 words of on-chip RAM
- 16 Mbits/s serial I/O ports and 16-bit parallel I/O port with DMA options
- 8- or 16-bit microprocessor interface requiring no additional logic
- Single-precision, single-cycle, IEEE floating-point conversion capability
- Bit reverse addressing mode
- Four 40-bit accumulators
- Zero-overhead looping
- 16- and 24-bit integer operations
- Vectored Internal and external interrupts with hardware context save
- Low-power CMOS technology

The DSP32C also includes extensive hardware and software support from both AT&T and many third parties. A bus functional simulation model is offered by Logic Automation, a complete DSP32C hardware emulator is available from Hewlett-Packard (64773). For more information on the DSP32C, refer to the DSP32C Information Manual, DSP32C Data Sheet, or any of several software support documentation manuals available from your AT&T account manager.

1.2.3 The AT&T DSP3210 Digital Signal Processor

The DSP3210 Digital Signal Processor is the newest member of AT&T's Floating-Point DSP Family. The DSP3210 is an enhancement of the DSP32C architecture designed specifically to meet the needs of the PC/Workstation multimedia market. The DSP3210 is a three-part product composed of the DSP3210 device, the VCOS real-time OS, and the VCOS multimedia function library. The DSP3210 is a very low-cost systems solution (no local DSP RAM is required for systems solutions) with complete applications support and full, 32-bit floating-point processing power. The DSP3210 is source code compatible with the DSP32C via AT&T's DSP32C to DSP3210 source code translator. New features added to the DSP3210 are briefly outlined in Table 1-1.



Table 1-1 DSP3210 Features

Feature	Benefit
32-bit addressing	Compatible with host address space.
Barrel Shifter	Better bit manipulation.
2048 32-bit words of contiguous on-chip RAM	RAM easily traded between program and data.
Big or little endian byte ordering	Compatible with Motorola and Intel processors.
Compatibility with Motorola and Intel bus protocols (byte select or size/offset)	Simplifies hardware design.
Quad-word transfer capability	Increased system performance.
Programmable 32-bit timer	Reduces system cost.
Interruptible do-loops that can be used in interrupt routines	Improves software performance.
Powerdown mode (wait for interrupt)	Reduces power dissipation.
SIO with DMA transfer counters	Simplifies control of serial DMA channels.
Bit I/O Unit	Simplifies hardware design.
Memory mapped I/O	Expandable architecture.
Boot ROM	Flexible initialization, including EPROM boot routine.
Repeat facility for single instruction do loops (no re-fetching of instruction)	Speeds block move operations.
Page break detect signal for DRAMs	Improves memory system performance.
Support for signed characters and unsigned shorts	Improved compiler performance.
Packaged in a low cost 132 PQFP	Low cost, small footprint.

1.3 Support Software Tools

A variety of tools are available to aid in application program development for the DSP3210. These tools are initially offered under the *UNIX®*, *MS-DOS**, or *Macintosh II†* operating systems. In addition to Assembler/Simulator/Compiler support tools, the DSP3210 includes the AT&T VCOS real-time operating system complete with its multimedia function library as well as powerful debugging and testing tools.

AT&T DSP3210 Support Software Tools

Software tools used to create, test, and debug DSP3210 application programs at the assembly language level are packaged in the DSP3210 Support Software Tools package. An assembler, link editor, simulator, and other utilities are included. The simulator, which has capabilities such as single-stepping, breakpointing, and execution profiling, performs precise simulations of the device.

* MS-DOS is a registered trademark of Microsoft.

† Macintosh II is a registered trademark of Apple Inc.

AT&T DSP3210 Application Software Library

The DSP3210 Application Software Library is a collection of commonly-used signal processing and 3D graphics functions. Each function is carefully benchmarked to allow applications to easily be built from collections of assembly language functions while meeting real-time processing requirements. Many functions are offered in several implementations, giving the programmer flexibility in balancing speed and memory requirements.

AT&T DSP3210 C Language Compiler

The optimizing C Language compiler for the DSP3210 allows application programs to be written in a general, high-level language. In applications where preliminary program development is performed using the C-language on a minicomputer or supercomputer, the source code can be ported to the DSP3210 with a minimal amount of time and effort. A symbolic debugger and several libraries of commonly used arithmetic and signal processing functions are included with the compiler.

1.4 Other Applicable Documentation

The following documents provide specific information on the DSP3210 and its hardware and software development tools. When designing application hardware and software, it is important to have accurate information. Contact your local account representative for the latest issue of a document.

The *AT&T DSP3210 Digital Signal Processor Data Sheet* contains up-to-date timing requirements and specifications, electrical characteristics, and a summary of the instruction set and device architecture.

The *AT&T DSP3210 Support Software Tools User Manual* describes how to install and use the DSP3210 support software.

The *AT&T DSP3210 Application Software Library Reference Manual* contains information on the use and design of each assembly-language routine included in the DSP3210 Application Software Library.

The *AT&T DSP3210 C-Language Compiler User Manual* describes how to set up and use the DSP3210 C compiler.

The *AT&T DSP3210 C-Language Compiler Library Reference Manual* provides the information necessary to implement the C programming language with the DSP3210.

1.5 Assistance

Assistance is available throughout the life of the product. These services include:

- Technical documentation and product samples
- Information on determining and selecting the appropriate hardware and software

The AT&T DSP Bulletin Board provides the latest and most up-to-date information about AT&T DSP products and application assistance:

1200/2400 baud
7 data bits, 1 stop bit, even parity
215-778-4444



DSP3210 Information Manual

For technical assistance or further information including ordering information and part numbers, please contact the nearest office through the following phone numbers:

Domestic (USA & Canada)

Northeast Region 508-626-2161	Mid-Atlantic Region 215-768-2626	Southeast Region 404-446-4700
North Central Region 612-885-4300	South Central Region 214-869-2040	Southwest Region 602-244-1100
Rocky Mountain Region 303-850-5415	Pacific Northwest 408-522-5555	Southern California 714-220-6223

International

Europe (except Spain & Portugal) +49 89 950 86 0 Telefax: +49 89 950 86 111	Spain and Portugal +34 1 404 6012 Telefax: +34 1 404 6252
Japan 813-593-3301 Telex: J32562 ATTIJ Telefax: 813-593-3307	Pacific Rim 65-225-5233 Telex: RS 42898 Telefax: 65-225-8725

Internal (AT&T Customers)

AT&T internal customers should contact their local AT&T Account Management Office.

If the Account Management telephone number is not known, call 1-800-372-2447 and ask for the telephone number of your account representative.

