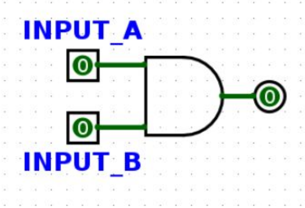
midterm review: sds

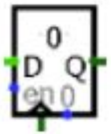
ta: sophie xie

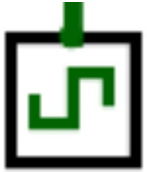
credit to: su24 61c, nikhil kandkur, erik yang, andrew liu

3 types of components

- combinational logic
  - output changes based on inputs after *x* seconds of delay
- state elements (e.g. registers)
  - output changes according to the clock signal; remembers input even after input changes due to the output only changing according to the clock
- clock
  - ticks at steady rate going from 0->1->0->1... etc.

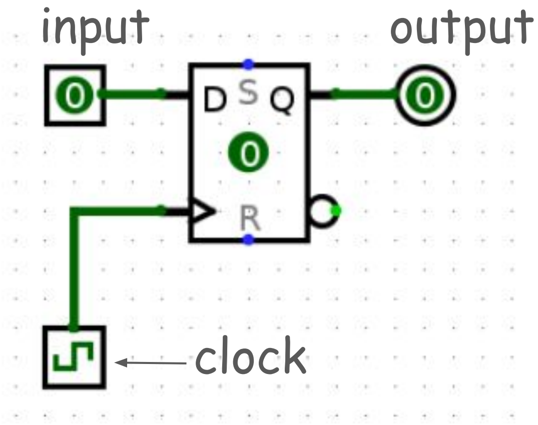






registers

- a **register** is a small and fast storage object that is controlled by a clock
- at the **rising edge** of the clock, the output updates to match the input
- at all other times, the output remains constant regardless of input value

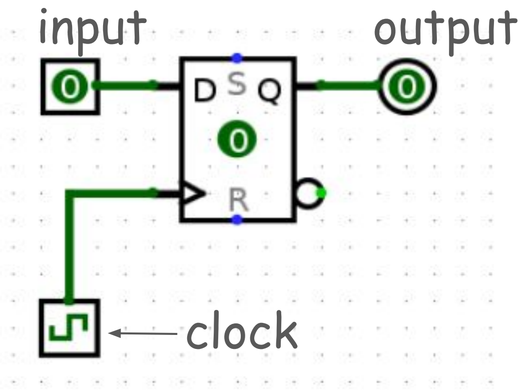


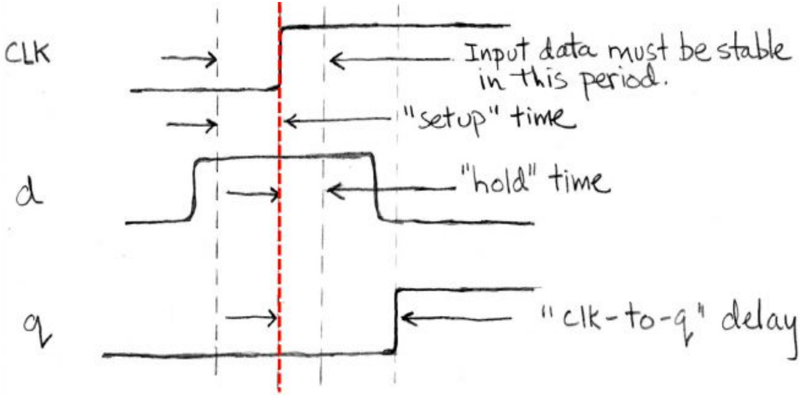
some helpful definitions:

- **rising clock edge**: when the clock goes from 0 -> 1
- **falling clock edge**: when the clock goes from 1 -> 0

registers, more definitions

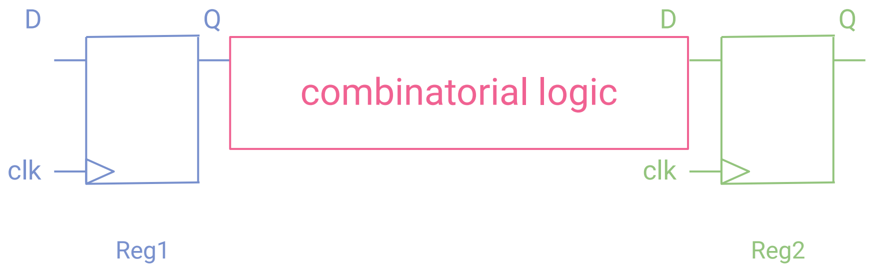
- **setup time:** time before the rising edge of the clock in which the input must be stable
- **hold time:** time after the rising edge of the clock in which the input must be stable
- **clock-to-q delay:** time it takes for the register's input to become its output after the rising edge of the clock
- **clk-to-q delay >= hold time**: if it takes clk-to-q to propagate value, why have a longer hold time?





more definitions

- **combinational logic delay**
  - combinatorial delay between 2 state elements
- **critical path:**
  - longest delay between 2 state elements
  - clock period must be longer than critical path
- **minimum clock period** (ns) = critical path
- **maximum clock frequency** (Hz) = 1/(min. clk period) = 1/CP



CP = clk-to-q + longest CL delay + setup time

Reg1 max(for all sum(all in-series CL delays)) Reg2

important formulas (put on cheatsheet!)

$$t_{\text{clk-to-q}} + t_{\text{shortest-combinational-path}} \geq t_{\text{hold}}$$

$$t_{\text{clk-to-q}} + t_{\text{longest-combinational-path}} + t_{\text{setup}} \leq t_{\text{clk-period}}$$

Max hold time: Signal feeding into the register needs to be stable long enough after clock tick, and the shortest path might affect that

Min clock period: Want to guarantee that the entire circuit is stable before we start the next clock cycle.

A circuit must fulfill these conditions in order to exhibit consistently correct behavior

Satisfying Hold Time Constraints

- Hold time constraint:

Hold time ≤ clk-to-q delay + shortest combinational path

  - After the rising edge, we have to wait clk-to-q seconds for the Q output to change
  - Then, after the shortest combinational path, one of the D inputs will change
  - We need the hold time to be over by the time the D input changes

Maximizing Clock Frequency

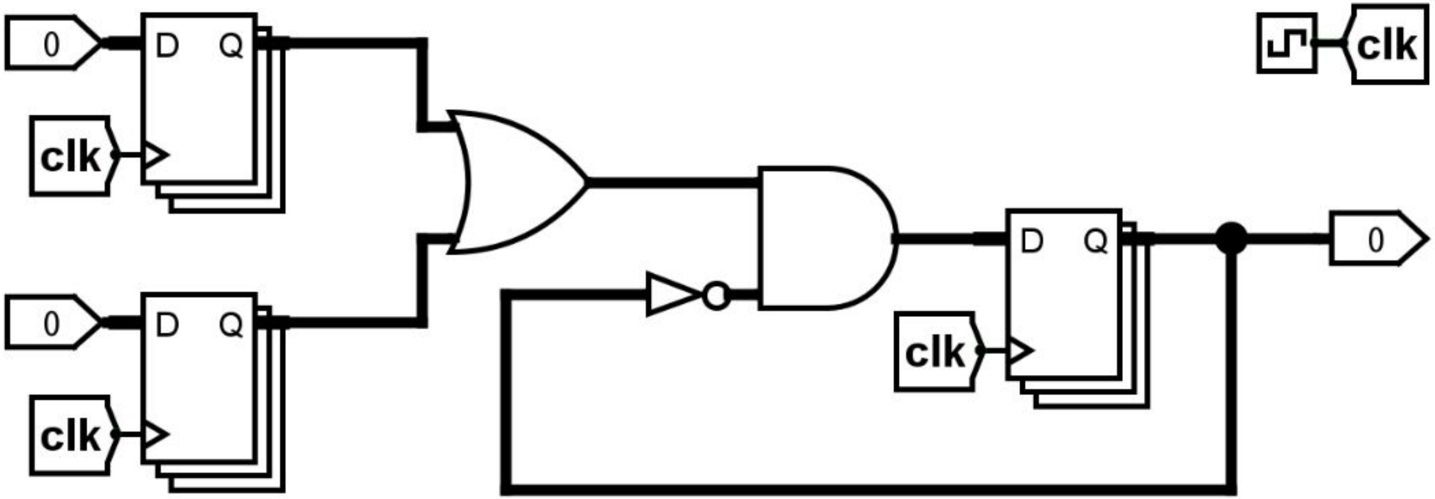
- Setup time and combinational delay constraint:

Clock period ≥ clk-to-q delay + longest combinational path + setup time

  - After the rising edge, we have to wait clk-to-q seconds for the Q output to change
  - Then, we have to wait for the longest combinational path for the result to appear at the D input
  - Then, we have to hold that D input stable for the setup time

FA21 Final Q4

Consider the following circuit. Assume that AND and OR gates have a delay of 8 ps (picoseconds), NOT gates have a delay of 4 ps, and all registers have a setup time constraint of 6 ps and clock-to-Q delay of 3 ps. Assume all wires are ideal, i.e. they have zero delay.



FA21 Final Q4

a. What is the largest combinational delay of all paths in this circuit, in picoseconds?

16 ps = 8 (AND) + 8 (OR)

b. What is the smallest combinational delay of all paths in this circuit, in picoseconds?

12 ps = 4 (NOT) + 8 (AND)

c. What is the maximum possible hold time constraint for registers to function properly in this circuit, in picoseconds?

15 ps = 12 + 3 (c2q)

d. What is the minimum allowable clock period for this circuit to function properly, in picoseconds?

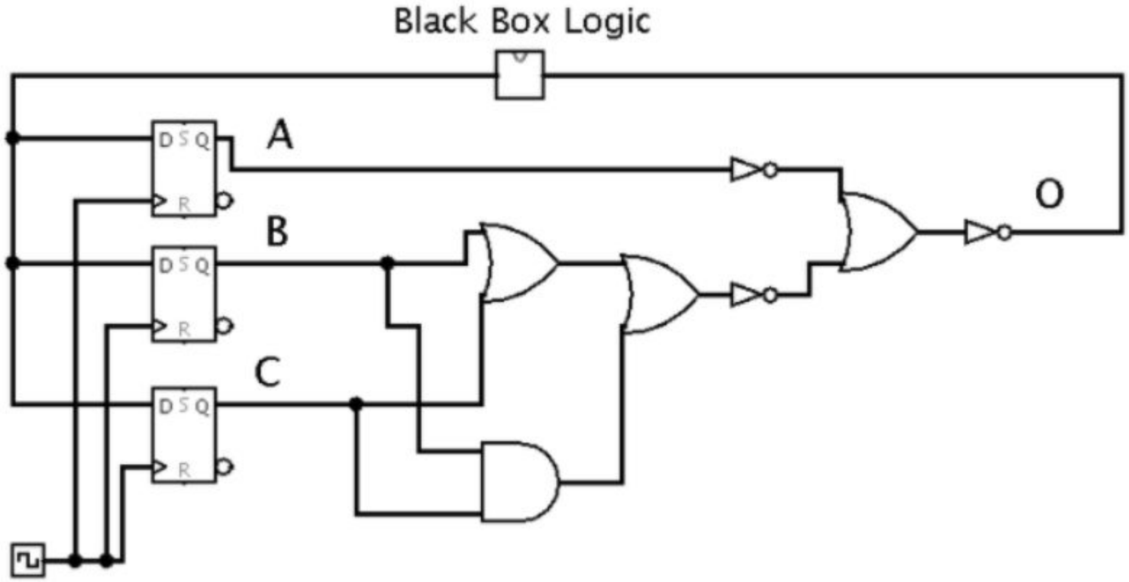
25 ps = 16 + 6 (setup) + 3 (c2q)

e. What is the maximum allowable clock frequency for this circuit to function properly, in gigahertz?

40 GHz = 1/(25 ps)

SP21 MT Q3

In the following circuit, the registers have a clk-to-q delay of 6ns and setup times of 5ns. NOT gates have a delay of 3ns, AND and OR gates have a delay of 7ns, and the "Black Box" logic component has a delay of 9ns.



SP21 MT Q3

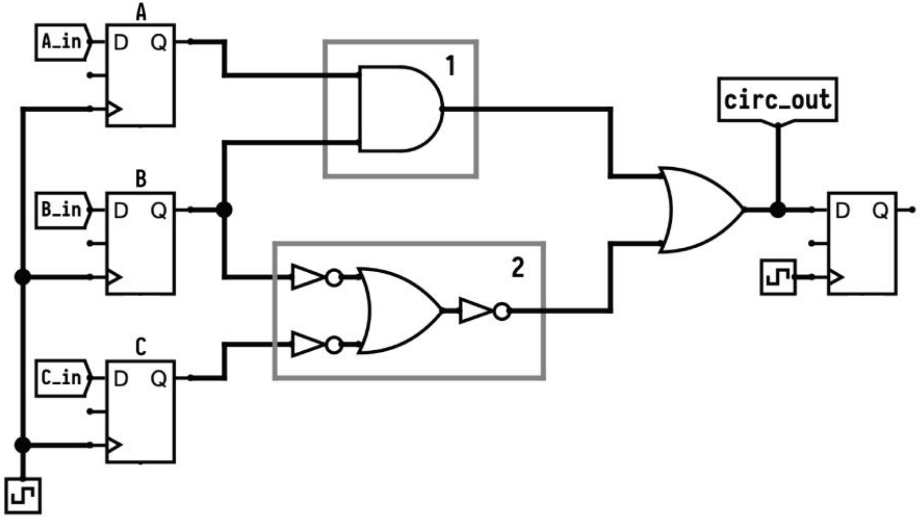
a. What is the maximum allowable hold time of the registers?

28 ns = 6 (c2q) + 3 (NOT) + 7 (OR) + 3 (NOT) + 9 (BBL)

b. What is the minimum acceptable clock period for this circuit?

47 ns = 6 (c2q) + 7 (AND) + 7 (OR) + 3 (NOT) + 7 (OR) + 3 (NOT) + 9 (BBL) + 5 (setup)

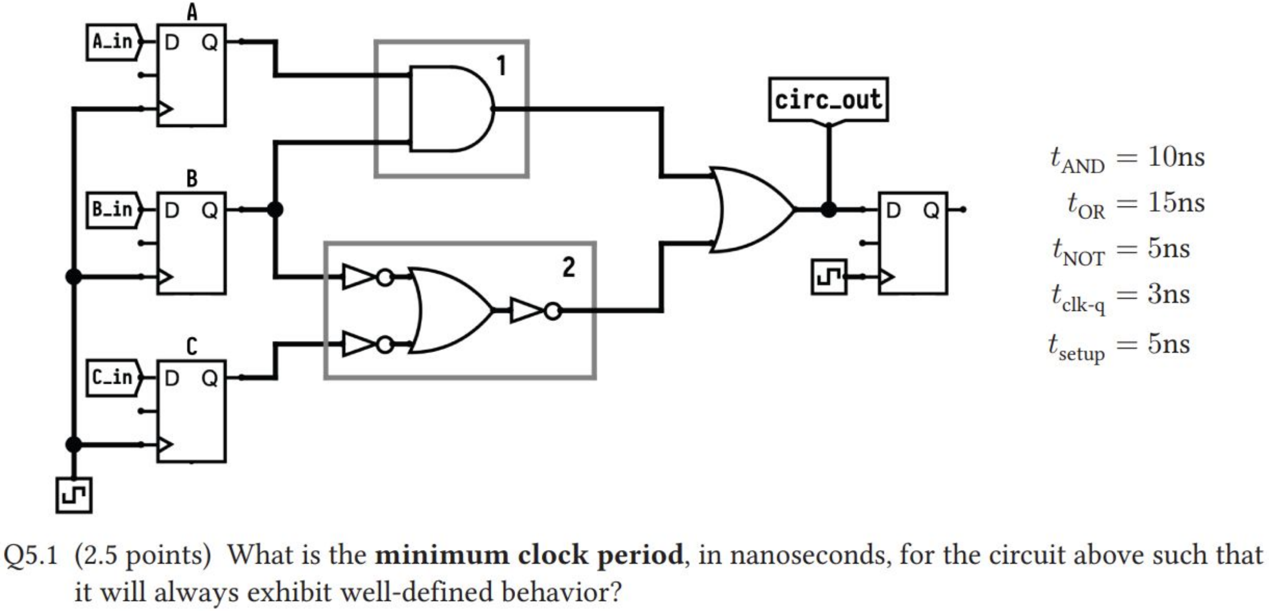
FA23 MT Q5



$$t_{\text{AND}} = 10\text{ns}$$
$$t_{\text{OR}} = 15\text{ns}$$
$$t_{\text{NOT}} = 5\text{ns}$$
$$t_{\text{clk-q}} = 3\text{ns}$$
$$t_{\text{setup}} = 5\text{ns}$$

Q5.1 (2.5 points) What is the **minimum clock period**, in nanoseconds, for the circuit above such that it will always exhibit well-defined behavior?

FA23 MT Q5



$t_{\text{AND}} = 10\text{ns}$

$t_{\text{OR}} = 15\text{ns}$

$t_{\text{NOT}} = 5\text{ns}$

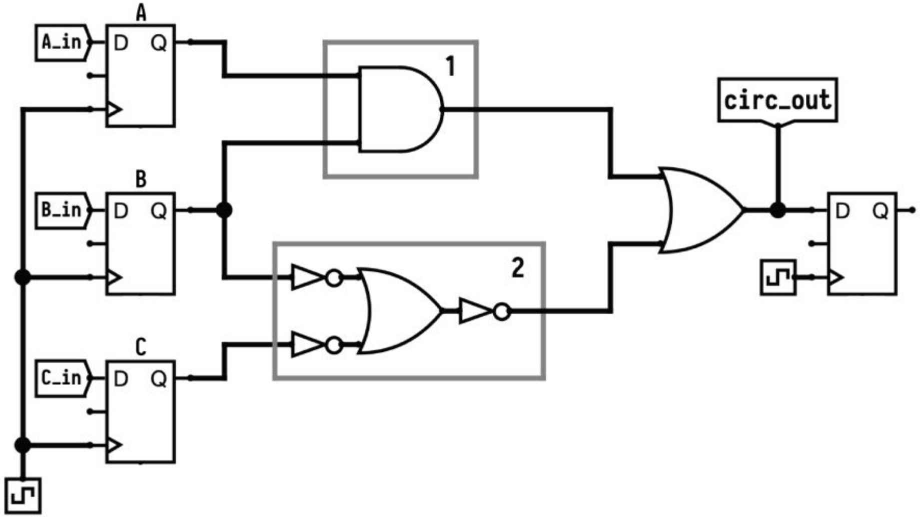
$t_{\text{clk-q}} = 3\text{ns}$

$t_{\text{setup}} = 5\text{ns}$

Q5.1 (2.5 points) What is the **minimum clock period**, in nanoseconds, for the circuit above such that it will always exhibit well-defined behavior?

48ns => 3ns (clk-q) + 5ns (NOT) + 15ns (OR) + 5ns (NOT) + 15ns (OR) + 5ns (setup)

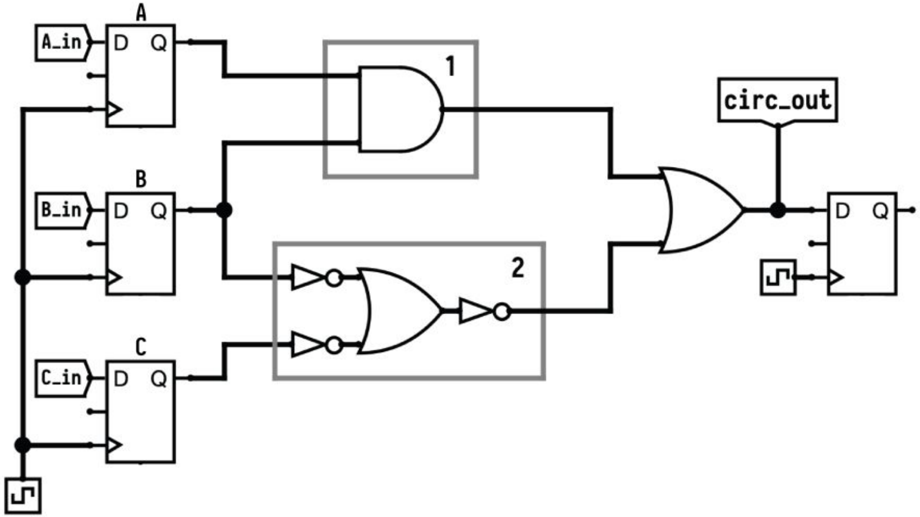
FA23 MT Q5



$$t_{\text{AND}} = 10\text{ns}$$
$$t_{\text{OR}} = 15\text{ns}$$
$$t_{\text{NOT}} = 5\text{ns}$$
$$t_{\text{clk-q}} = 3\text{ns}$$
$$t_{\text{setup}} = 5\text{ns}$$

Q5.2 (2.5 points) What is the **maximum hold time**, in nanoseconds, for the circuit above such that it will always exhibit well-defined behavior?

FA23 MT Q5



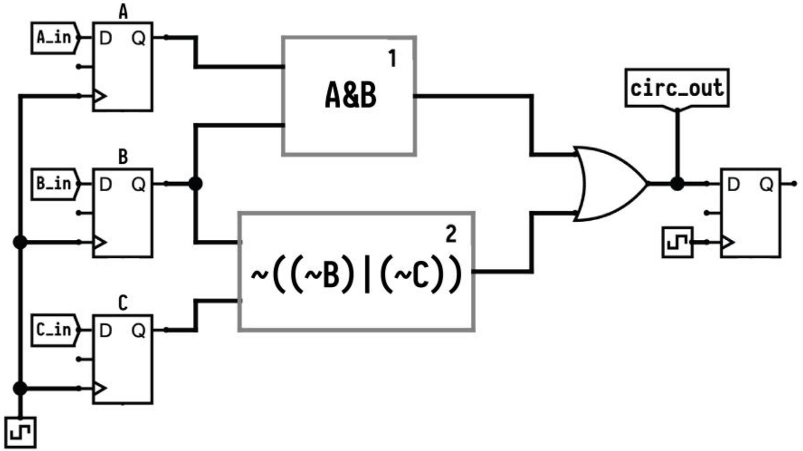
$$t_{\text{AND}} = 10\text{ns}$$
$$t_{\text{OR}} = 15\text{ns}$$
$$t_{\text{NOT}} = 5\text{ns}$$
$$t_{\text{clk-q}} = 3\text{ns}$$
$$t_{\text{setup}} = 5\text{ns}$$

Q5.2 (2.5 points) What is the **maximum hold time**, in nanoseconds, for the circuit above such that it will always exhibit well-defined behavior?

28ns => 3ns (clk-q) + 10ns (AND) + 15ns (OR)

FA23 MT Q5

For the rest of this question, consider the updated circuit diagram and timings below. Subcircuits 1 and 2 are black-boxes that compute the Boolean expressions shown in the diagram. Regardless of your previous answers, assume the clock period is 80ns, and for subcircuits 1 and 2, their respective minimum and maximum combinational logic delays are equal. For example, if the input to subcircuit 1 changed at $t = 0$ (and no other changes occur), then the output to subcircuit 1 will change at $t = 13$ only.



$t_{\text{OR}} = 15\text{ns}$

$t_{\text{subcircuit 1}} = 13\text{ns}$

$t_{\text{subcircuit 2}} = 24\text{ns}$

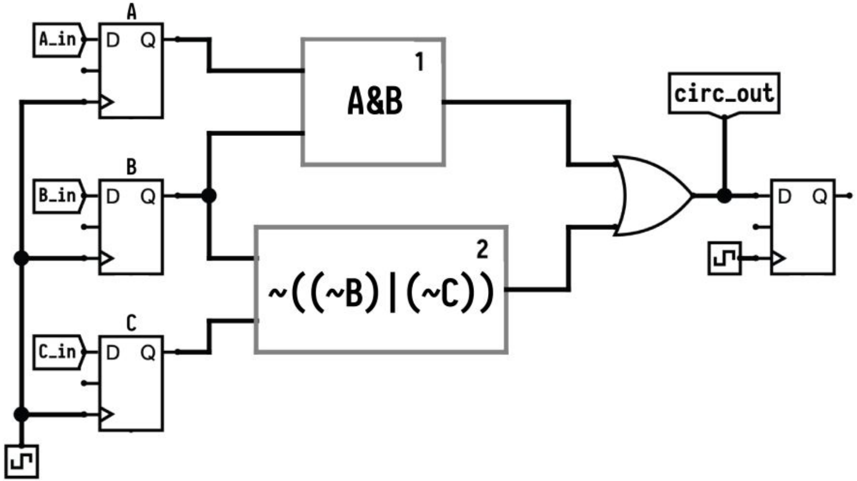
$t_{\text{clk-q}} = 3\text{ns}$

$t_{\text{setup}} = 5\text{ns}$

Until this circuit settles at the correct input, it calculates two other Boolean expressions at the tunnel `circ_out`. Assume that register outputs are all 0 at $t = 0$, and that there are no setup or hold time violations.

Q5.3 (2 points) Let t_1 be the first time that `circ_out` changes. What is t_1 in nanoseconds? Clarified during exam: t_1 is the first time that `circ_out` *may change.*

FA23 MT Q5



$t_{\text{OR}} = 15\text{ns}$

$t_{\text{subcircuit 1}} = 13\text{ns}$

$t_{\text{subcircuit 2}} = 24\text{ns}$

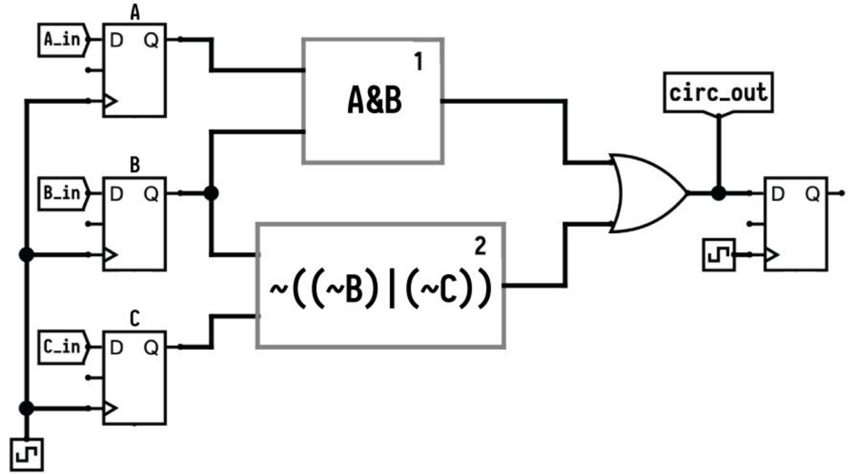
$t_{\text{clk-q}} = 3\text{ns}$

$t_{\text{setup}} = 5\text{ns}$

Q5.3 (2 points) Let t_1 be the first time that `circ_out` changes. What is t_1 in nanoseconds? Clarified during exam: t_1 is the first time that `circ_out` *may change.*

31ns => 3ns (clk-q) + 13ns (subcircuit 1) + 15ns (OR)

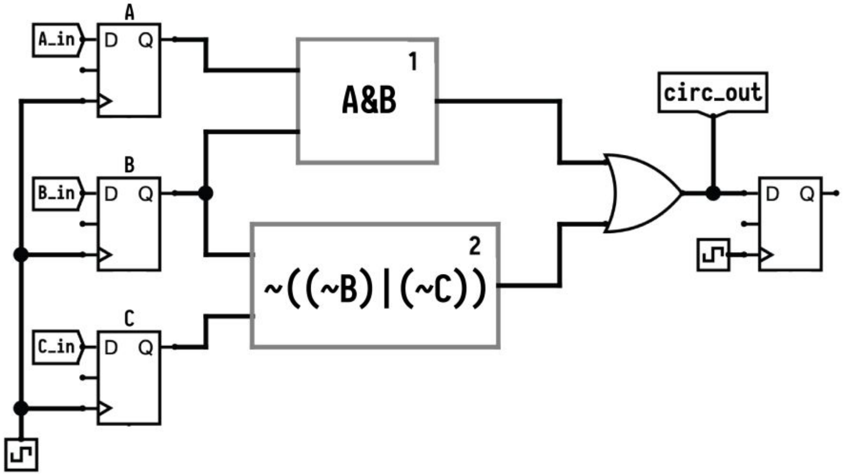
FA23 MT Q5



$$t_{\text{OR}} = 15\text{ns}$$
$$t_{\text{subcircuit 1}} = 13\text{ns}$$
$$t_{\text{subcircuit 2}} = 24\text{ns}$$
$$t_{\text{clk-q}} = 3\text{ns}$$
$$t_{\text{setup}} = 5\text{ns}$$

Q5.4 (2 points) Let t_2 be the second time that `circ_out` changes. What is t_2 in nanoseconds?

FA23 MT Q5

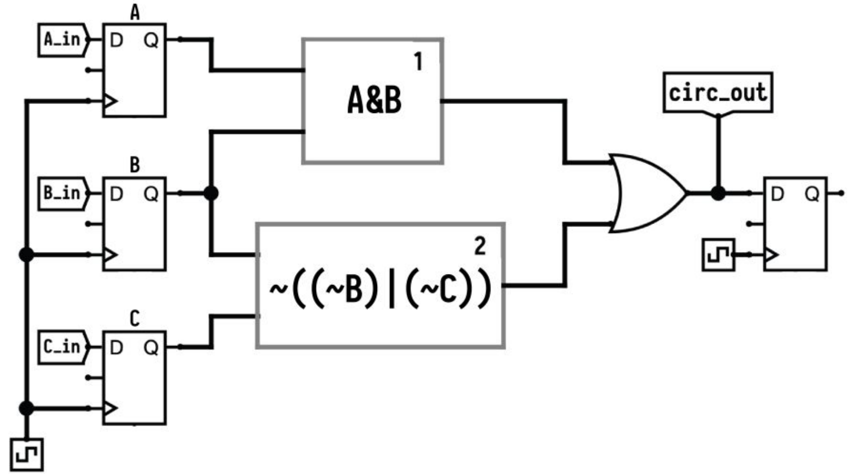


$$t_{\text{OR}} = 15\text{ns}$$
$$t_{\text{subcircuit 1}} = 13\text{ns}$$
$$t_{\text{subcircuit 2}} = 24\text{ns}$$
$$t_{\text{clk-q}} = 3\text{ns}$$
$$t_{\text{setup}} = 5\text{ns}$$

Q5.4 (2 points) Let t_2 be the second time that **circ_out** changes. What is t_2 in nanoseconds?

42ns => 3ns (clk-q) + 24ns (subcircuit 2) + 15ns (OR)

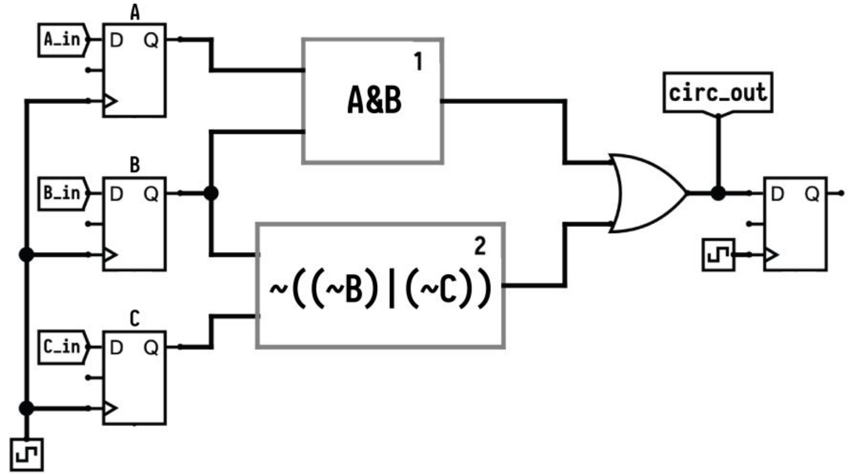
FA23 MT Q5



$t_{\text{OR}} = 15\text{ns}$
$t_{\text{subcircuit 1}} = 13\text{ns}$
$t_{\text{subcircuit 2}} = 24\text{ns}$
$t_{\text{clk-q}} = 3\text{ns}$
$t_{\text{setup}} = 5\text{ns}$

Q5.5 (2 points) What simplified Boolean expression does the circuit calculate while $0\text{ns} \leq t < t_1$?

FA23 MT Q5



$t_{\text{OR}} = 15\text{ns}$

$t_{\text{subcircuit 1}} = 13\text{ns}$

$t_{\text{subcircuit 2}} = 24\text{ns}$

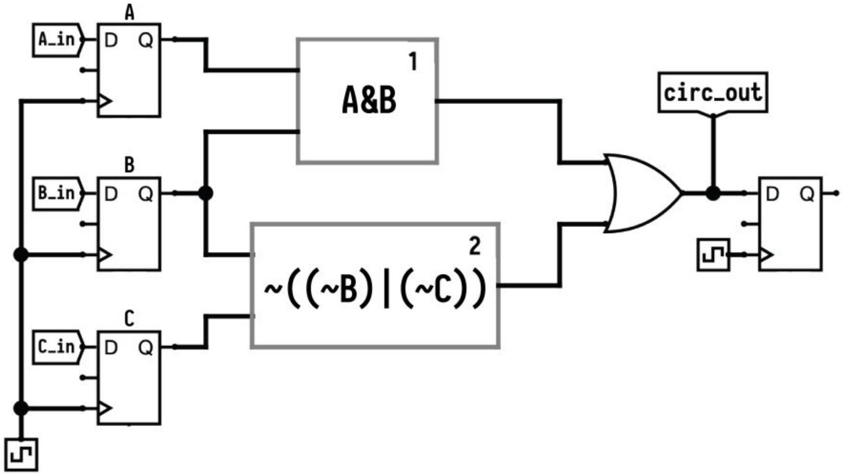
$t_{\text{clk-q}} = 3\text{ns}$

$t_{\text{setup}} = 5\text{ns}$

Q5.5 (2 points) What simplified Boolean expression does the circuit calculate while $0\text{ns} \leq t < t_1$?

0, since wires are initialized to 0, the output at circ_out will be 0.

FA23 MT Q5



$t_{\text{OR}} = 15\text{ns}$

$t_{\text{subcircuit 1}} = 13\text{ns}$

$t_{\text{subcircuit 2}} = 24\text{ns}$

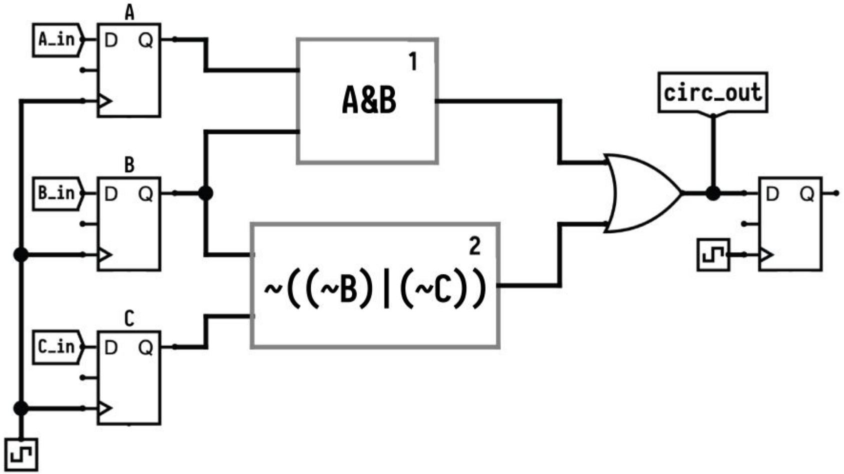
$t_{\text{clk-q}} = 3\text{ns}$

$t_{\text{setup}} = 5\text{ns}$

Q5.6 (2 points) What simplified Boolean expression does the circuit calculate while $t_1 \leq t < t_2$?

A&B => this is the output of subcircuit 1 ORed with 0

FA23 MT Q5



$t_{\text{OR}} = 15\text{ns}$

$t_{\text{subcircuit 1}} = 13\text{ns}$

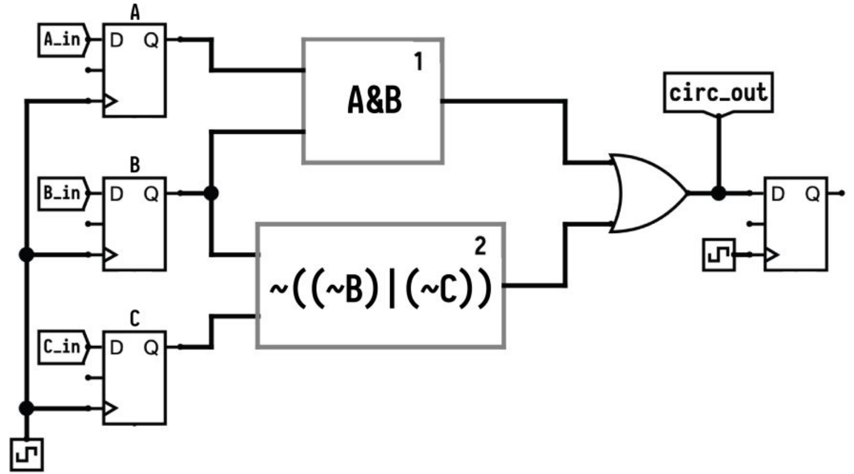
$t_{\text{subcircuit 2}} = 24\text{ns}$

$t_{\text{clk-q}} = 3\text{ns}$

$t_{\text{setup}} = 5\text{ns}$

Q5.7 (2 points) What simplified Boolean expression does the circuit calculate while $t_2 \leq t < 80\text{ns}$?

FA23 MT Q5



$$t_{\mathrm{OR}} = 15\mathrm{ns}$$
$$t_{\text{subcircuit 1}} = 13\mathrm{ns}$$
$$t_{\text{subcircuit 2}} = 24\mathrm{ns}$$
$$t_{\text{clk-q}} = 3\mathrm{ns}$$
$$t_{\text{setup}} = 5\mathrm{ns}$$

Q5.7 (2 points) What simplified Boolean expression does the circuit calculate while $t_2 \le t < 80$ns?

(A&B) | (~((~B) | (~C))) => (A&B) | (~(~(B&C))) => (A&B) | (B&C) => (A|C)&B