A Novel Low-Cost Capacitive-Sensor Interface

Frank M. L. van der Goes and Gerard C. M. Meijer

Abstract—**This paper describes the design of a new capacitive sensor interface. The interface is based on the use of a novel type of oscillator whose frequency is insensitive to low- and high-frequency interfering signals by the application of a third order high-pass filter and special dither techniques. The fully integrated 0.7 μm CMOS circuit shows an inaccuracy of less than 100 aF with respect to a 2 pF reference capacitor over a $-30°$ to $+70°$C temperature range. The applied measurement concept guarantees high stability, high accuracy and a negligible influence of parasitic capacitances without the need for calibration.**

I. Introduction

RECENTLY, an architecture for a low-cost capacitive sensor interface has been proposed [1]. The system is based on a first-order switched capacitor (SC) relaxation oscillator. Its capacitor-dependent frequency is measured by a microcontroller. Continuous autocalibration of the offset and gain of the complete interface is performed. This technique, known as the three-signal technique, has been successfully used before in [2]–[4].

A serious problem when measuring off-chip capacitors can be the effects of power-line interference. Another problem when applying free-running oscillators can be the effects of microcontroller interference, which can result in locking to the microcontroller clock signal, thereby deteriorating the accuracy.

The new first-order oscillator, described in this paper, applies a third-order filter to suppress low-frequency (LF) interference. This also results in a very low sensitivity to $1/f$ noise, enabling the use of low-cost CMOS processes for the implementation of accurate circuits. The locking effects to the microcontroller have been reduced by applying special dithering techniques.

II. Measurement Concepts

The system architecture is based on three measurement concepts, which will be explained below.

A. Two-Port Measurement

The sensor capacitor C_x is cursed with parasitic capacitors C_{p1} and C_{p2} modeling the capacitances of the connecting cables, as displayed in Fig. 1. The only way to eliminate the effects of both parasitics is to force a voltage $V_{\rm tp}$ on the transmitting electrode and to sense the current $I_{\rm tp}$. The current $I_{\rm tp}$ depends only on $V_{\rm tp}$ and C_x.

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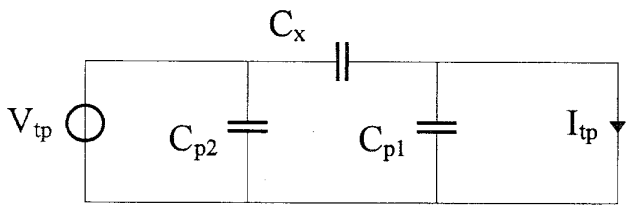

Fig. 1. Two-port measurement of C_x. C_{p1} and C_{p2} model the capacitances of the connecting cables.

B. Use of First-Order Relaxation Oscillators

The sensor system consists of a first-order capacitance-controlled oscillator and a microcontroller. The microcontroller measures the oscillator period by counting the number of clock cycles that fit into a period. This system has been successfully used before [1]–[3].

C. Continuous Autocalibration

The system is continuously autocalibrated for additive and multiplicative errors of the electronics. To implement the autocalibration, a reference capacitor $C_{\rm ref}$ and the offset are measured in exactly the same way as the sensor capacitor C_x. This results in three different periods $T_{\rm ref}$, $T_{\rm off}$, and T_x, which are given by

$$\begin{aligned} T_{\rm ref} &= T_0 + KC_{\rm ref} \\ T_{\rm off} &= T_0 \\ T_x &= T_0 + KC_x \end{aligned} \tag{1}$$

where T_0 and K represent the offset and gain, respectively. These periods are measured by the microcontroller, yielding digital numbers $N_{\rm ref}$, $N_{\rm off}$, and N_x. The final measurement result M is calculated by the microcontroller

$$\begin{aligned} M &= \frac{N_x - N_{\rm off}}{N_{\rm ref} - N_{\rm off}} \\ &= \frac{C_x}{C_{\rm ref}}. \end{aligned} \tag{2}$$

This ratio does not depend on T_0 and K and since this calibration is done continuously, also slow variations of T_0 and K do not affect M. One full measurement cycle consists of three time intervals, which we refer to as measurement phases.

When we combine these three measurement concepts, we obtain the sensor system as depicted in Fig. 2(a). In order to minimize the number of terminals of the interface, the selection of the three measurement phases is done by the interface itself. Only one terminal is used for the communication with the microcontroller.

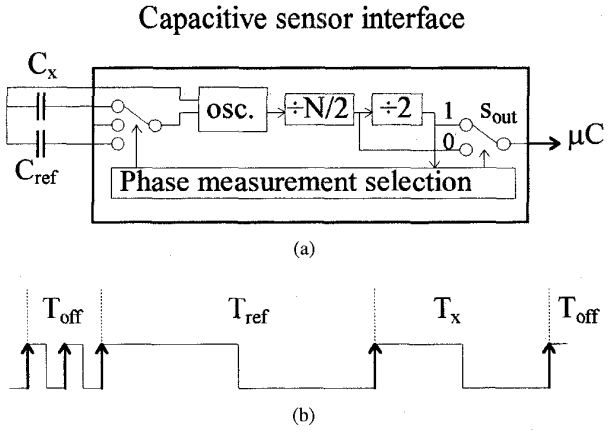

Fig. 2. (a) The sensor system and (b) the output signal of the interface.

Fig. 2(b) shows the output signal of the sensor interface over a full measurement cycle. This signal is sampled by the microcontroller. Every measurement phase consists of an equal number (N) of oscillator periods. The microcontroller should be able to identify the various phases $T_{\rm off}$, $T_{\rm ref}$, and T_x. To enable this identification, the output frequency during $T_{\rm off}$ is doubled (switch s_{out} is in position "0"). The divide-by-$N/2$ stage is used to increase the phase duration, thus reducing the quantization noise level. A practical value for common sampling frequencies is $N = 256$.

A great advantage of the signal type shown in Fig. 2(b) is that low-pass filtering of this signal does not affect M as long as the applied time constants are about 10 times smaller than $T_{\rm off}/4$. Further, this signal can be very easily handled by the microcontroller.

A serious problem when using the above-mentioned system is the effect of LF interference [for instance, the mains supply (50/60 Hz)]. These interfering signals need to be filtered. A good method to remove this interference is to apply a measurement time equal to a complete set of periods of the interfering signal. However, this method cannot be used here, since the signal protocol of the interface output does not allow this. Therefore, the oscillator frequency should be immune to LF interference. For this reason, a new oscillator has been designed which provides filtering for LF signals.

Another problem related to the use of free-running oscillators is the locking of the oscillator to high-frequency (HF) disturbing signals from the microcontroller. Special dithering techniques have been used to reduce the locking effects, as shown in the next section.

III. The New Oscillator

A. The Principle of Operation

The new first-order oscillator, which is based on SC techniques, is depicted in Fig. 3. The current $I_{\rm int}$ is continuously being integrated. All switches in the oscillator are controlled by the logic circuitry. The comparator monitors the output voltage $V_{\rm int}$ of the integrator. After the threshold voltage $V_{\rm comp}$ has been reached, some switches change to the alternate position, depending on the logic, and charge is transferred from C_s and/or $C_{{\rm off}i}$, $i = 1, 2$ to $C_{\rm int}$. After a certain time, this charge

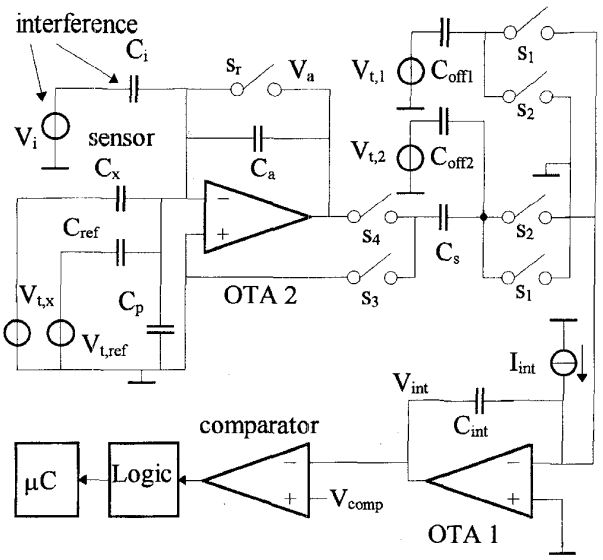

Fig. 3. The new SC oscillator.

is completely removed from $C_{\rm int}$ by the integration of $I_{\rm int}$, and the threshold is reached again. This process results in periodic signals.

Fig. 4 shows the signals $V_{\rm int}$ and V_a, the signal on the transmitting electrodes of $C_{\rm off1}$ and $C_{\rm off2}$ ($V_{t,1}$ and $V_{t,2}$, respectively) and the integration current. A positive current flows in the direction of the arrow. Also displayed is the signal $V_{t,x}$ on the transmitting electrode of C_x during measurement of C_x. In this case, this signal follows the pattern of $V_{t,1}$. Finally, the control signals of several switches are displayed. When the control signal for a switch is a "1," the switch is closed (conducting).

The signal $V_{t,\rm ref}$ follows the pattern of $V_{t,1}$ during a reference measurement phase. To guarantee a positive charge flow to the integrator, even when $C_x = 0$, a capacitor $C_{\rm off2}$ is added. At the beginning of $T_{s,i}$ $i \in [1, 4]$, charge on $C_{\rm off2}$ is transferred to $C_{\rm int}$ in parallel with C_s. At the end of $T_{s,i}$, the charge on C_s and $C_{\rm off2}$ has to be rebuilt. This is done during the sufficiently long time interval $T_{0,i}$. To generate this time interval, an offset capacitor $C_{\rm off1}$ is added. Charge on this capacitor is transferred to $C_{\rm int}$ at the beginning of $T_{0,i}$. The peak-to-peak amplitude of $V_{t,1}$, $V_{t,2}$, $V_{t,x}$, and $V_{t,\rm ref}$ equals V_{DD}. The period $T_{{\rm osc},x}$ during the signal measurement phase is given by

$$T_{{\rm osc},x} = \frac{4V_{DD}\left(C_{\rm off1} + C_{\rm off2} + C_x\dfrac{C_s}{C_a}\right)}{\hat{I}_{\rm int}} \tag{3}$$

where $\hat{I}_{\rm int}$ is the amplitude of $I_{\rm int}$, and V_{DD} is the power supply voltage.

As will be seen later, it is very important that the charge and discharge currents are closely matched. This is required for optimal LF filtering properties. In our case, the mismatch should be smaller than 0.1%. A novel method to generate two closely matched currents with opposite sign has been developed. This method is based on switched current (SI) techniques (Fig. 5).

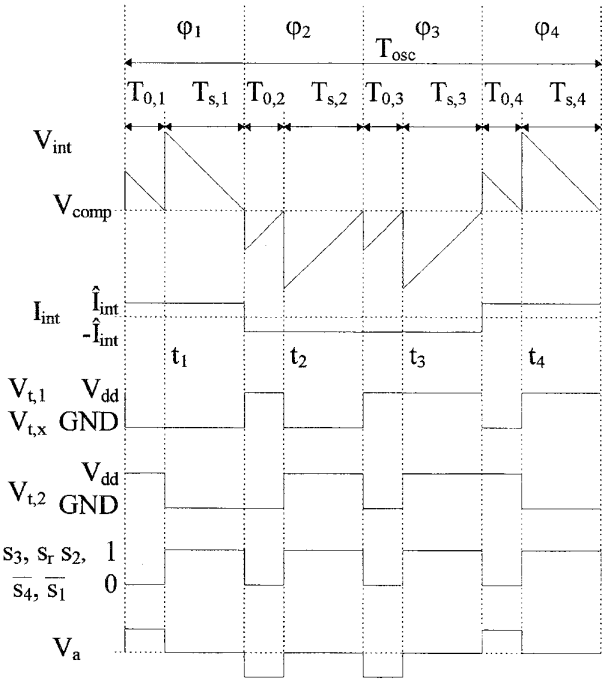

Fig. 4. Important signals in the new oscillator during the measurement of C_x.

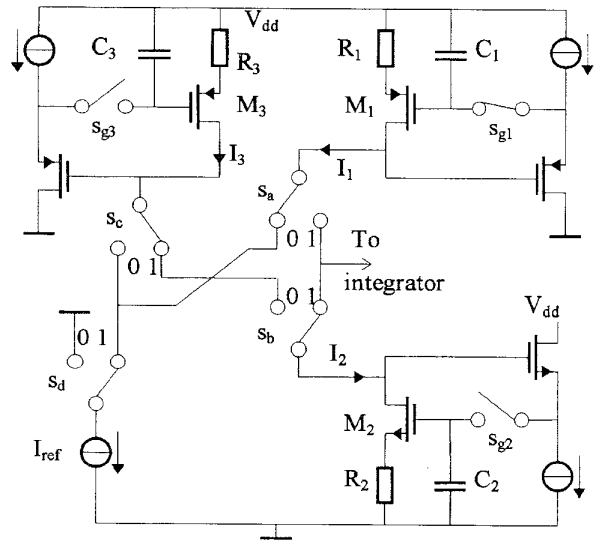

Fig. 5. SI-based implementation of $I_{\rm int}$ to generate two matched currents.

The circuit consists of three cells which are designed to sample and hold currents. The currents which are integrated are I_1 and I_2. We now explain the principle of operation. During phases φ_2 and φ_3 (Fig. 4), I_2 is being integrated ($s_b = 1$), and I_3 is zero. The current I_1 tracks the reference current $I_{\rm ref}$ because $s_a = 0$, $s_d = 1$ and $s_{g1} = 1$. This situation is depicted in Fig. 5. At the end of this tracking phase, s_{g1} opens (sampling), a voltage is stored on C_1, and I_1 is the sampled value of $I_{\rm ref}$. During phase φ_1, I_2 tracks I_3, while I_3 tracks $I_{\rm ref}$ during phase φ_4. One complete sample-and-hold cycle for all cells takes four phases (one oscillator period) and is displayed in Table I.

TABLE I
INTEGRATION AND TRACK SEQUENCE OF THE CURRENTS I_1, I_2, AND I_3

action	φ_1	φ_2	φ_3	φ_4
integration	I_1	I_2	I_2	I_1
track	I_2	I_1	I_1	I_3

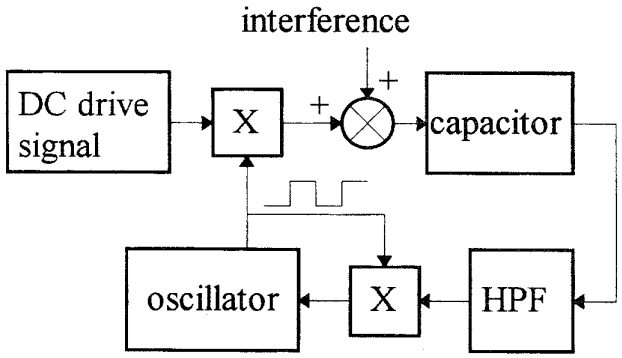

Fig. 6. Synchronous detection based on an HPF to remove the interference.

After one complete cycle, two matched integration currents with opposite sign equal to $I_{\rm ref}$ are obtained.

B. The Low-Frequency Filter

The LF interfering signal is modeled in Fig. 3 by the voltage V_i and the capacitor C_i. As discussed before, the oscillator frequency should be immune to LF interference. The oscillator uses synchronous detection based on a high-pass filter (HPF), as displayed in Fig. 6.

The LF interference is coupled into the capacitor and high-pass filtered. The oscillator is assumed to have a DC input. The HPF does not contain any time constants, but is derived from an SC filter. The filter has a third-order behavior and is actually a cascade of a first-order and a second-order HPF. The switch s_r performs a differential operation $1-\exp(-j\omega T_0)$, resulting in a first-order high-pass behavior for low frequencies. The second-order HPF is formed by the switching of C_s. The interference is sampled on the equidistant moments t_i (see Fig. 4). In the z-domain [$z = \exp(j\omega T_{\rm osc}/4)$], the resulting filter can be described by $H(z)$

$$H(z) = 1 - z^{-1} - z^{-2} + z^{-3}. \tag{4}$$

Note that all coefficients are equal to 1. Transformation to the frequency domain of (4) results in a second-order behavior for low frequencies. Combining both filters results in a total relative error $\delta_1(\omega)$, which corresponds to the maximum relative deviation of a single oscillator period with normalized input signals

$$\delta_1(\omega) = 4\alpha \sin\left(\tfrac{1}{2}\omega T_0\right) \sin^2\left(\tfrac{1}{8}\omega T_{\rm osc}\right) \cos\left(\tfrac{1}{8}\omega T_{\rm osc}\right). \tag{5}$$

Normal transformations from the z-domain to the frequency domain require an infinite number of samples. Since a single oscillator period is only based on four samples, we use another approach. The same result as a common transformation can also be obtained by infinite values of the phase of the interference. The factor a α, $\alpha \in [0, 1]$, represents the effect

of the offset capacitors $C_{\text{off}1}$ and $C_{\text{off}2}$. Very large offset capacitors tend to stabilize the period so $\alpha \downarrow 0$. However, the period cannot be modulated in this case. We assume $\alpha = 1$.

The problem with an oscillator implementing an SC filter is that the sampling moments depend on the interference. The sampling moments will therefore not be equidistant for large interfering signals. This is a nonlinear behavior. Large interfering signals will therefore be less suppressed than predicted by (5). The actual suppression of large interfering signals has to be simulated. Simulation results [5] for a practical situation where $T_0 = 10\,\mu$s, $T_s = 25\,\mu$s, $C_x = C_i = 1$ pF, $V_{DD} = 5$ V, $\omega_i = 2\pi \cdot 50$ rad/s, $V_{i,\text{amp}} = 220\,V_{eff}$ (V_i is a sine wave with amplitude $V_{i,\text{amp}}$) showed that the maximum relative deviation $\delta_{32}(\omega_i, V_{i,\text{amp}})$ of a measurement phase consisting of 32 periods amounts to $1.5 \cdot 10^{-5}$. This is approximately 5 times larger than the small-signal relative error. The filtering of LF interfering signals also holds for the $1/f$noise. Thanks to the applied filtering concept, the oscillator frequency is insensitive to $1/f$ noise, as long as the $1/f$ noise corner frequency is below the oscillator frequency. This holds for all noise sources in the oscillator. This enables the use of low-cost CMOS processes to realize accurate circuits.

C. The High-Frequency Filter Properties

Another problem is the interference from the microcontroller. It is possible that the oscillator locks to the clock frequency of the microcontroller. The result is a decreased accuracy and resolution. This situation has to be avoided. We applied two methods to remove the locking effects.

The first method is based on low-pass filtering. The bandwidth of all parts of the oscillator is far below the frequency of the interference.

The second method is based on dithering techniques. We assume that the interference is sampled in parallel with the sensor signal. These samples tend to synchronize the oscillator period to that of the interfering signal. By applying dither techniques, this synchronization process is disturbed. The dither is implemented by adding pseudo noise to the oscillator, which is the same for all measurement phases. The effect of the pseudo noise itself is eliminated by the three-signal technique. A very good implementation of the pseudo noise is to increase $C_{\text{off}1}$ every period with a small part $\Delta C_{\text{off}1}$, as shown by Mulder [6]. When a new measurement phase starts, $C_{\text{off}1}$ starts with its initial value. The maximum value of $C_{\text{off}1}$ is reached at the end of a measurement phase and is only a few percent larger than the initial value.

IV. Nonidealities

In this section, we consider the effect of the most important nonidealities on the measurement result M and on the LF filter properties. Nonidealities such as parasitic capacitances, finite DC gain, finite CMRR and offset of the OTA's, switch charge injection (SCI) and voltage dependence of on-chip capacitors all appear in (1) as additive or multiplicative factors [5]. The effect of these nonidealities is canceled by the continuous autocalibration. Some effects result in a nonlinear capacitor-to-period conversion and are not canceled by the continuous autocalibration. Such a nonlinearity occurs when the oscillator contains LF or HF poles. These poles originate, for instance, from the limited bandwidth of the OTA's (HF pole at $1/\tau_{\text{HF}}$) or the output resistance of the integration current source (LF pole at $1/\tau_{\text{LF}}$). The nonlinearity is smaller than a certain value γ if the oscillator period T_{osc} lies in the range [5]

$$-\tau_{\text{HF}} \ln(\gamma) < \frac{T_{\text{osc}}}{8} < \gamma\tau_{\text{LF}}. \tag{6}$$

It is not very difficult to meet this condition for $\gamma = 1$ ppm.

To test the nonlinearity of the oscillator, four measurement phases are performed. Besides the offset and a capacitor C_{x1}, another capacitor C_{x2} is measured. During the fourth measurement phase, the sum $C_{x1} + C_{x2}$ is measured. These four measurement phases are sampled by the microcontroller, resulting in 4 digital numbers N_{off}, N_{x1}, N_{x2}, and N_{x1+x2}. A measure of the nonlinearity is given by ε

$$\varepsilon = \frac{N_{x1} + N_{x2} - N_{x1+x2} - N_{\text{off}}}{N_{x1+x2} - N_{\text{off}}}. \tag{7}$$

Some of the above-mentioned nonidealities also deteriorate the rejection parameter for interference $\delta_{32}(\omega, V_{i,\text{amp}})$. The main causes of decreased LF filter properties have been verified with simulations and are found to be offset voltage, current mismatch and SCI. For instance, a current mismatch of $3 \cdot 10^{-4}$ causes an increase of $\delta_{32}(\omega, V_{i,\text{amp}})$ by a factor of two. Several measures, such as the use of well-matched transistors, the use of SI techniques (Fig. 4) to realize matched currents and the use of dummy switches to decrease the SCI, have been taken to reduce these effects.

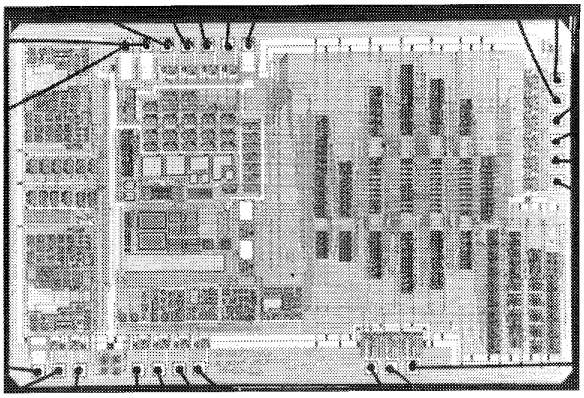

Fig. 7 Photomicrograph of the previous version of the interface, realized in a 3 μm process

V. Measurement Results

A photomicrograph of the previous version of the interface is depicted in Fig. 7. This interface is realized in a 3 μm process and measures 18 mm^2.

A recent version of the interface has been implemented in a 0.7 μm CMOS process. This chip measured 5.5 mm^2 and all measurement results hold for this chip. The measurement range is 0–2 pF. The values of C_{x1} and C_{x2} are approximately 1 pF. All test capacitors have a Teflon dielectric, which shows very good properties with respect to dielectric absorption [7].

TABLE II
SIMULATED AND MEASURED RESULTS OF THE LF SUPPRESSION

Parameter	value	condition
$\delta_{32}(\omega_i, V_{i,\mathrm{amp}})$	$1.5 \cdot 10^{-5}$	simulation
$\delta_{32,\mathrm{meas}}(\omega_i, V_{i,\mathrm{amp}})$	$5.5 \cdot 10^{-5}$	measured
$\delta_{32,dif}(\omega_i, V_{i,\mathrm{amp}})$	$5 \cdot 10^{-2}$	simulation

The parasitic capacitor amounts to 50 pF. The frequency of the oscillator varies between 7.5 and 12.5 kHz. The time intervals $T_{0,1}$ amount to 10 μs. One complete measurement takes less than 100 ms. The sampling time of the microcontroller, an Intel 87C51FA running at 12 MHz and operating from the same power supply as the interface, is 330 ns.

The measured nonlinearity ε is 50 ppm, corresponding to 100 aF with respect to a 2 pF reference capacitor. This accuracy holds for the large temperature range from -30 to 70°C. This is a very good result. Changing of the parasitic capacitance has no significant influence on this result. The 50 aF resolution is mainly determined by the noise voltage of OTA2. The offset capacitor measures 3 fF which results from imperfect on-chip shielding and compensating. This offset can be reduced by a different layout of the circuit. The offset when using an external capacitor selection circuit measures only 50 aF, showing that the autocalibration works very well.

To measure the LF suppression, we coupled a 220 V_{eff}, 50 Hz sinusoidal signal into the oscillator ($T_{0,i} = 10\,\mu$s, $T_{s,i} = 25\,\mu$s) through a 1 pF capacitor. During this test, the sensor capacitor amounted to 1 pF. This test corresponds to the most extreme practical situation. The measured relative deviation of one measurement phase $\delta_{32,\mathrm{meas}}(\omega_i, V_{i,\mathrm{amp}})$ containing 32 oscillator periods is given in Table II.

In this table, $\delta_{32,\mathrm{dif}}(\omega_i, V_{i,\mathrm{amp}})$ represents the relative deviation of a measurement phase when the second filter is omitted and only the differentiation (switch s_r) is active. The contribution of the second-order filter itself equals the ratio of $\delta_{32,\mathrm{dif}}(\omega_i, V_{i,\mathrm{amp}})$ and $\delta_{32,\mathrm{meas}}(\omega_i, V_{i,\mathrm{amp}})$ and amounts to 900. This is a very satisfactory result.

The measured deviation $\delta_{32,meas}(\omega_i, V_{i,\mathrm{amp}})$ is only four times larger than the simulated value $\delta_{32}(\omega_i, V_{i,\mathrm{amp}})$. One of the causes of this difference is a mismatch between the positive and negative value of the integration current. Another cause is SCI. The largest contribution to SCI comes from the switch channel charge Q_{ox}. Since $Q_{\mathrm{ox}} \sim L^2$ (L> being the length of a transistor) for different switches with a certain ON resistance, the SCI will be reduced when using a smaller process, but only very little improvement can be expected.

To test the locking effect caused by the microcontroller clock signal, both the interface and the microcontroller are connected to the same power supply (a 5 V voltage regulator IC 7805). In this case, HF clock signals can directly enter the interface. No locking effects could be detected.

The main measurement results are listed in Table III.

TABLE III
OVERVIEW OF THE MAIN MEASUREMENT RESULTS

Parameter	Value
Power supply V_{DD}	5 V
Range	0–2 pF
Accuracy	100 aF
Resolution 100 ms meas. Time ($N = 256$)	5 aF
Resolution 10 ms meas. Time ($N = 32$)	200 aF
Offset with internal MUX	3 fF
Offset with external MUX	50 aF
Range of period $T_{\mathrm{osc,x}}$	80 μ–160 μs
Sensitivity of period $T_{\mathrm{osc,x}}$	40 μs/pF
Rel. deviation $\delta_{32,\mathrm{meas}}(\omega_i, V_{i,\mathrm{amp}})$ (50 Hz, 1 pF, 220 V_{eff})	$5.5 \cdot 10^{-5}$

VI. CONCLUSION

A new capacitive sensor interface has been realized. The fully integrated 0.7 μm CMOS interface is based on a first-order relaxation oscillator. To suppress LF interfering signals, a third-order SC filter has been applied successfully. The HF interfering signals have been suppressed by special dithering techniques. The measured nonlinearity over a 100°C temperature range amounts to 100 aF with respect to a 2 pF reference capacitor. A parasitic capacitance up to 300 pF shows a negligible effect on this result. This accuracy has been obtained thanks to the continuous autocalibration. The system shows a very low sensitivity to $1/f$ noise, thus enabling the use of low-cost CMOS processes.

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Since 1990, he has been part of the Laboratory of Electronics, Delft University of Technology, where he is working towards the Ph.D. degree. His main interest lies in the field of A-to-D conversion and low-cost interfacing.

Gerard C. M. Meijer, for a photograph and biography, see this issue, p. 520.