



# VeriSilicon GPU IP Update– GCNanoUltraV

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**DDR-Less 2.5D GPU**

**December 2020**

# Interacting with the Digital World Naturally

## Sound and Speech. Sight and Gesture.



# VeriSilicon IP Portfolio – Scalable IPs

*NPU*

*Compute*

*GPU*

*ISP*

*Video*

*Audio/Voice*

*Compression/  
Encryption*

*DISPLAY*

*Computer Vision  
Imaging DSP*

*FLEXA API*



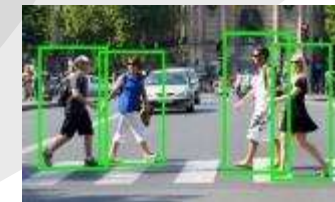
**Server Class**



**Automotive**



**Tablets**



**Smartphone**

**Wearables & IoT**





# VeriSilicon GPU IP – Nano Series GPUs



# Leading Adopters of Verisilicon Vivante GCNano GPUs

15+ customers in Wearable and IoT market

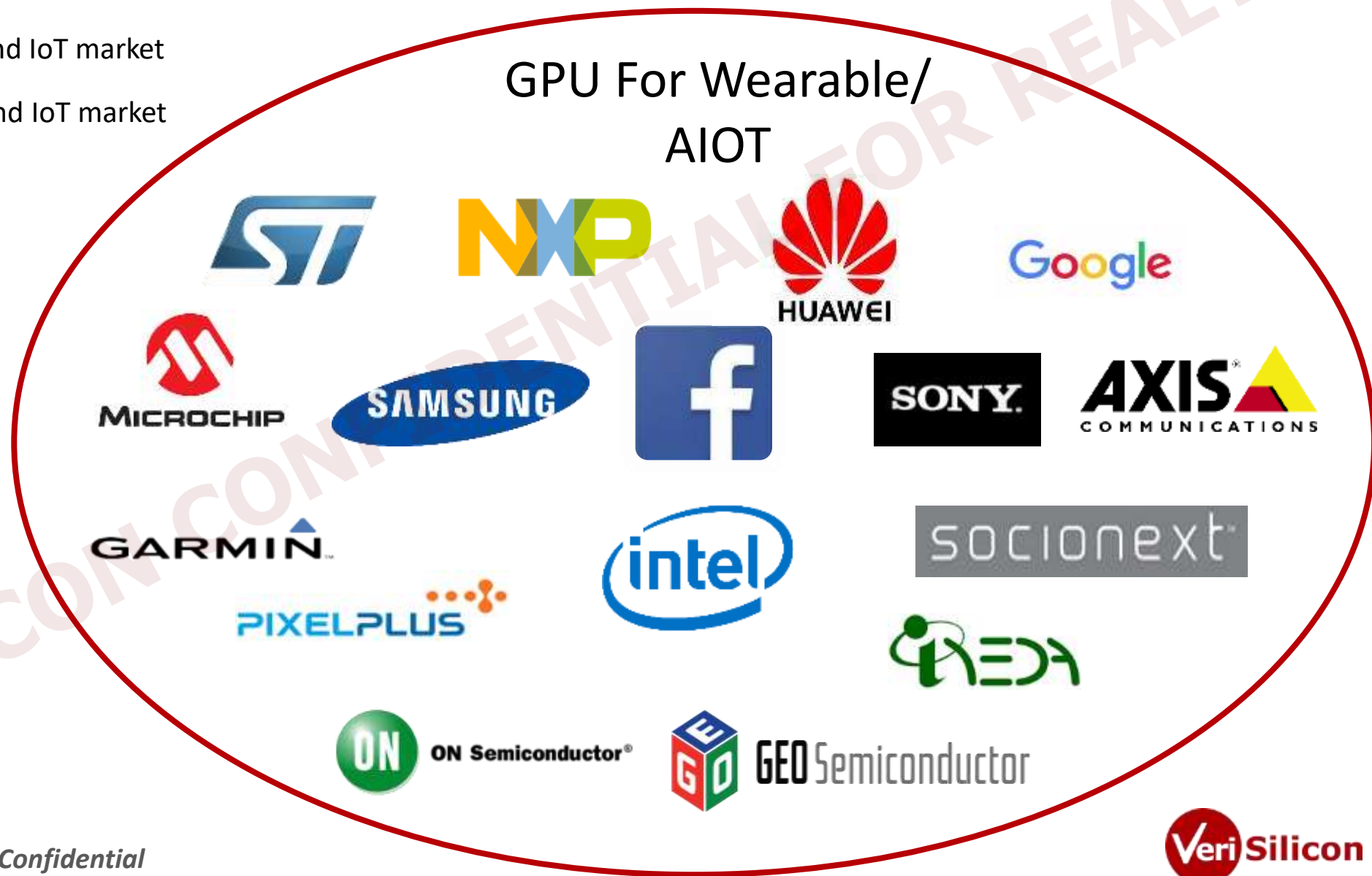
20+ products in Wearable and IoT market

**2D Pixel GPU**

**2.5D Vector GPU**

**3D OES 3.1/  
Vulkan GPU**

GPU For Wearable/  
AIOT



# VeriSilicon Extremely Low Power IP Leading Wearable Products

GARMIN

Leading  
Smart Watch  
Vendor



Airoha



GPU

GPU

NPU

ISP

ISP

GPU

NPU

Audio  
DSP

NPU

Audio  
DSP

VeriSilicon Low Power IP Portfolio

# Customer Watch Example

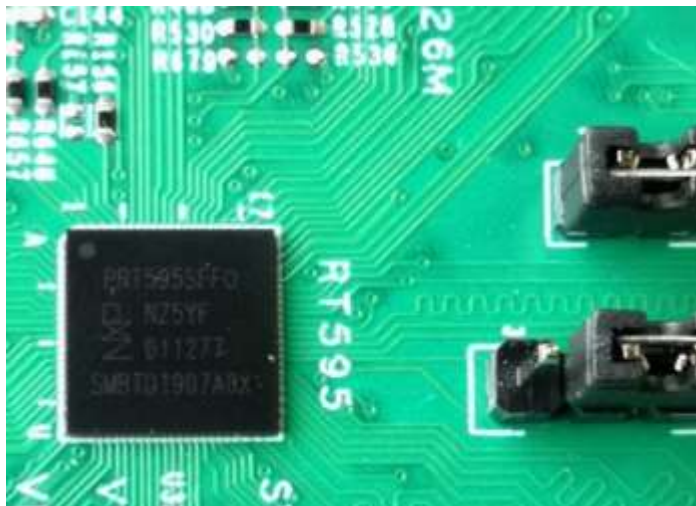
▲ GCNanoLiteV + DCNano sample application using VGLite driver

▲ <https://www.korulab.com/>





# GCNanoLiteV Success Story in NXP i.MX RT595 Silicon



- Arm Cortex-M7 core delivering 3020 CoreMark/1284 DMIPS @ 600 MHz
- Fastest real-time response with latency as low as 20ns
- Industry's lowest dynamic power with integrated the DC-DC converter

- 2D graphics acceleration engine
- LCD display and camera interface
- Multichannel high-performance audio

## Connect and Protect

- High Assurance Boot (HAB) with on-the-fly QSPI Flash Decryption
- 128-bit AES Cryptography and True Random Number Generator

## Save Time and Money

- Leverage existing MCU toolchains—MCUXpresso, IAR, and Keil
- FreeRTOS, SDK, Arm® mbed™, and the global Arm ecosystem

▲ Sample demo:

[https://microej.nxp.com/Powered\\_by\\_MicroEJ\\_imxRT/](https://microej.nxp.com/Powered_by_MicroEJ_imxRT/)



# MicroEJ VEE for i.MX RT

- ▲ MicroEJ VEE for i.MX RT is a standard Virtual Execution Environment focusing on Security, embedded GUI and Low-Power.
- ▲ This NXP+MicroEJ combined solution targets following markets: thermostats, wearable, appliances, industrial computing, automation, automotive, medical, smart meters and printers.



## Demo Links

▲ [https://www.youtube.com/watch?v=NA\\_eJI0wvQk](https://www.youtube.com/watch?v=NA_eJI0wvQk)

▲ [https://www.microej.com/nxp\\_rt595\\_vg\\_watch\\_demo.mp4](https://www.microej.com/nxp_rt595_vg_watch_demo.mp4)

▲ [https://microej.nxp.com/Powered\\_by\\_MicroEJ\\_imxRT](https://microej.nxp.com/Powered_by_MicroEJ_imxRT)

▲ <https://www.youtube.com/watch?v=an4f5KNBkiY>

▲ <https://www.youtube.com/watch?v=XOEDSeh84IM>

▲ <https://www.youtube.com/watch?v=AdRSVpkNzR4>

▲ [https://www.youtube.com/watch?v=OyNPp\\_5nOsA](https://www.youtube.com/watch?v=OyNPp_5nOsA)

▲ [https://www.youtube.com/watch?v=sJkvxZsC7WQ&feature=emb\\_logo&ab\\_channel=Qt](https://www.youtube.com/watch?v=sJkvxZsC7WQ&feature=emb_logo&ab_channel=Qt)

# Low Power GPU

## GCNanoUltraV



# VeriSilicon GPU IP – Wearables 2.5D GPU Specs

IP Product	GCNanoUltraV DDRLESS
DDR or DDRLESS	DDR_LESS (SRAM) version
Graphics and Compute API Support	Vector Graphics VGLite
Pixel Rate (Pixel/Cycle)	1
Achievable Clock Speed (MHz)	600
Display Resolution	Up to 1920x1080, 4K video overlay
SRAM Requirement (390x390, one background layer and one watch hand layer)	1.3MB(NOAA) 1.3MB(16xAA)
Firmware Size	64KB
Synthesis Logic Gates (MGates)	0.5
Memories Bits (KBytes)	8
Synthesis Area in 14nm (mm2)	0.1
MAX Power(Tiger Render) in 14nm TT/0.8v/25C (mW@100 MHz)	3mW
Average Power(Watch UI) in 14nm TT/0.8v/25C (mW@40 MHz)	0.6mW

# GCNanoUltraV Key Features

Key Features	
Hardware Components	<ul style="list-style-type: none"><li>● Programmable Shader engine with a VLIW instruction set</li><li>● Command list based DMAs to minimize CPU overhead</li><li>● Primitive Rasterizer</li><li>● Texture Mapping Unit</li><li>● Blending Unit</li><li>● <b>Tessellation</b></li><li>● <b>Out-of-order response support AXI master</b></li><li>● <b>Display Controller (optional)</b></li></ul>
Image Transformation	<ul style="list-style-type: none"><li>● Texture mapping, Point sampling, Bilinear filtering</li><li>● Blit support, Stretch (independently on x and y axis)</li><li>● Rotation any angle, Mirroring</li><li>● Source and/or destination color keying, Format conversions on the fly</li><li>● 2.5D Perspective Correct Projections</li><li>● <b>Configurable Coordinate Systems and Transformations (3x3 matrix)</b></li><li>● <b>Scissoring and viewport clipping, Mip Interpolation, Paint</b></li><li>● <b>Odd/even and non-zero fill rules</b></li></ul>
Blending Support	<ul style="list-style-type: none"><li>● Fully Programmable Alpha blending modes (src and dst)</li><li>● Source/Destination color keying</li><li>● HW Blender Unit</li></ul>

# GCNanoUltraV Key Features

Key Features	
Drawing Primitives	<ul style="list-style-type: none"><li>● Pixel / Line drawing,</li><li>● Filled rectangles,</li><li>● Triangles (Gouraud Shaded)</li><li>● <b>Path Generation</b></li><li>● <b>Linear and radial gradient paint paths</b></li></ul>
Text rendering supports	<ul style="list-style-type: none"><li>● Bitmap antialiased (A1 / A2 / A4 / A8 )</li><li>● Font Kerning, Unicode (UTF8)</li></ul>
Color formats	<ul style="list-style-type: none"><li>● 32-bit RGBA8888 / BGRA8888 / ABGR8888,</li><li>● 16-bit RGBA5551 / RGB565</li><li>● 8-bit A8 / L8 / RGB332, 4-bit A4 / L4 &amp; 2-bit A2 / L2 &amp; 1-bit A1 / L1</li><li>● <b>1/2/4/8-bit index format</b></li><li>● <b>YUV Format</b></li></ul>
Antialiasing	<ul style="list-style-type: none"><li>● <b>16x MSAA</b>, 8x MSAA</li><li>● Quadrilaterals per edge,</li><li>● Triangles per edge,</li><li>● Thick lines</li></ul>

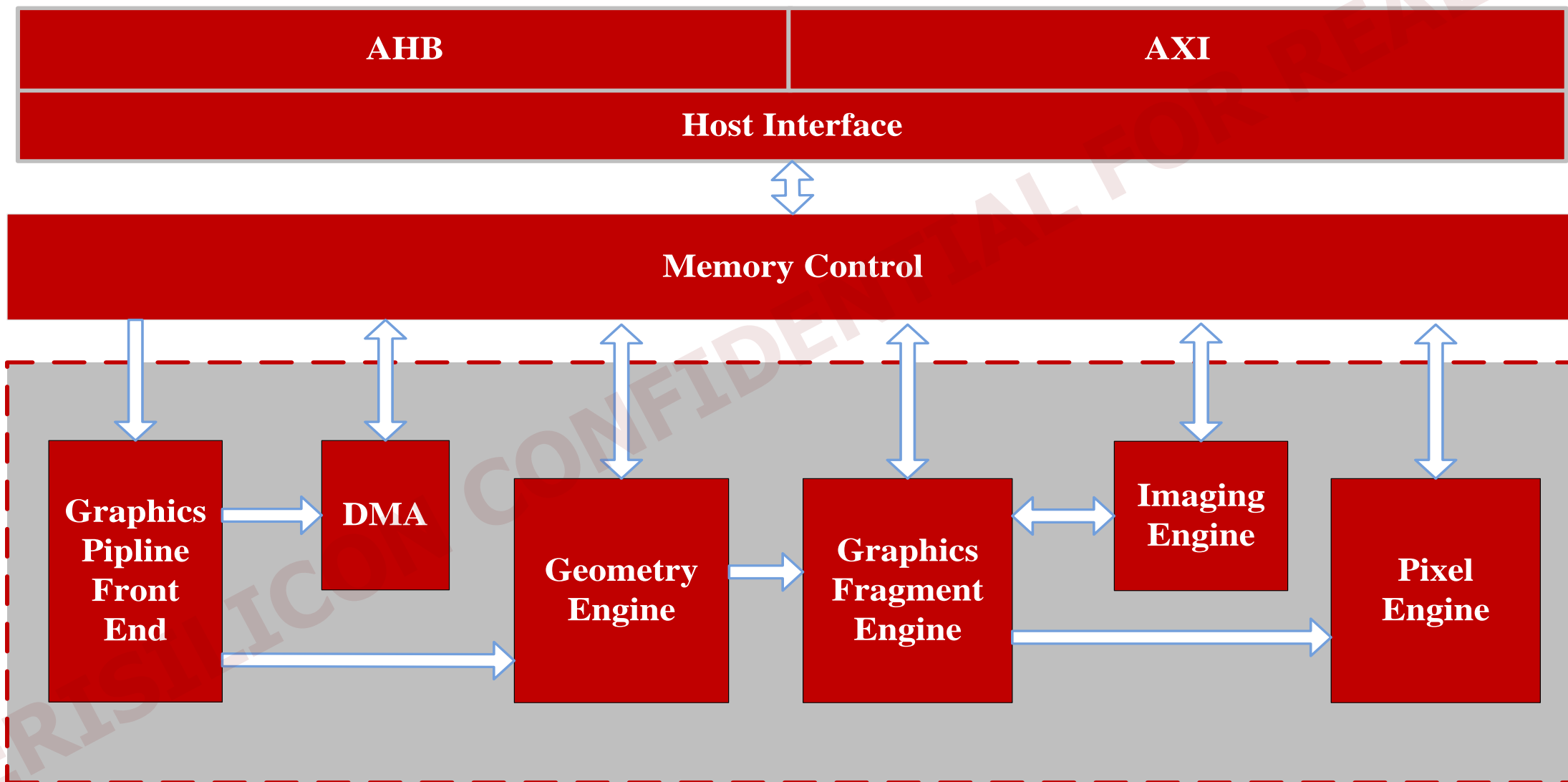


# VeriSilicon Vivante Display Processor Series PPA in SEC14LPP

Verisilicon Vivante DC8000 Series @SEC14LPP	DC8000Nano
Target Display Resolution	1080P
MIPI-DBI Interfaces Support	Yes
MIPI-DPI Interfaces Support	Yes
HDMI/DP/eDP Interfaces Support	No
Default Layers	1
Max Layers	0
CSC, Gamma correction, Dither, Cursor	Yes
Rotation/Scaling	Optional
Unified Compression Support	Optional
10-bit Format Support	Optional
3D-LUT Support	NA
Security Support	Optional
Achievable Clock Speed (GHz)	1.2
Synthesis Logic Gates (MGates) <sup>①</sup>	0.06
Memories Bits (KBytes)	13
Total Synthesis Area (mm <sup>2</sup> )	0.04
Average Power @100MHz (mW) (TT/0.8V/25°C)	2.2

① Gate count is calculated using NAND2 unit size of 0.145152  $\mu\text{m}^2$

# GCNanoUltraV Architecture Overview



## 2.5D GPU DDR-Less Solution Usage Scenario (1)

### ▲ UI for Watch and AIoT

- ▶ Resolution: 390x390
- ▶ Performance: 30fps
- ▶ GCNanoUltraV DDR-Less Solution
  - Frequency requirement: 8MHz
  - Power: 0.2mW (SEC14nm, 0.8v/25C)
  - Memory Footprint : 1.3MB

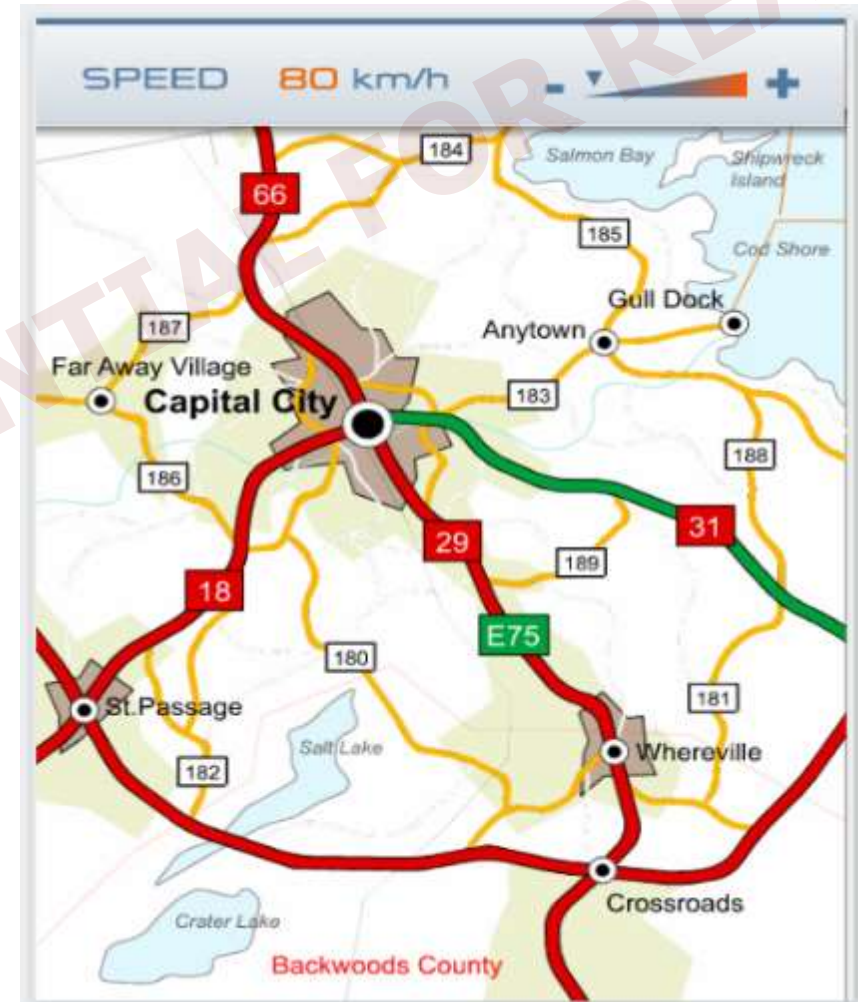




## 2.5D GPU DDR-Less Solution Usage Scenario (2)

### ▲ Navigation Benchmark

- ▶ Resolution: 480x640
- ▶ Performance: 30fps
- ▶ GCNanoUltraV DDR-Less Solution
  - Frequency requirement: 40MHz
  - Power: 1.2mW (SEC14nm, 0.8v/25C)
  - Memory Footprint: 1.8MB



## 2.5D GPU DDR-Less Solution Usage Scenario (3)

### ▲ Tiger Benchmark

- ▶ Resolution: 640x480
- ▶ Performance: 30fps
- ▶ GCNanoUltraV DDR-Less Solution
  - Frequency requirement: 100MHz
  - Power: 3mW (SEC14nm, 0.8v/25C)
  - Memory Footprint: 1.6MB



## 2.5D GPU DDR-Less Solution Usage Scenario (4)

### ▲ Draw complex path – Font rendering

- ▶ Resolution: 640x480
- ▶ Performance: 30fps
- ▶ GCNanoUltraV DDR-Less Solution
  - Frequency requirement: 50MHz
  - Power: 1.6mw (SEC14nm, 0.8v/25C)
  - Memory Footprint: 1.6MB

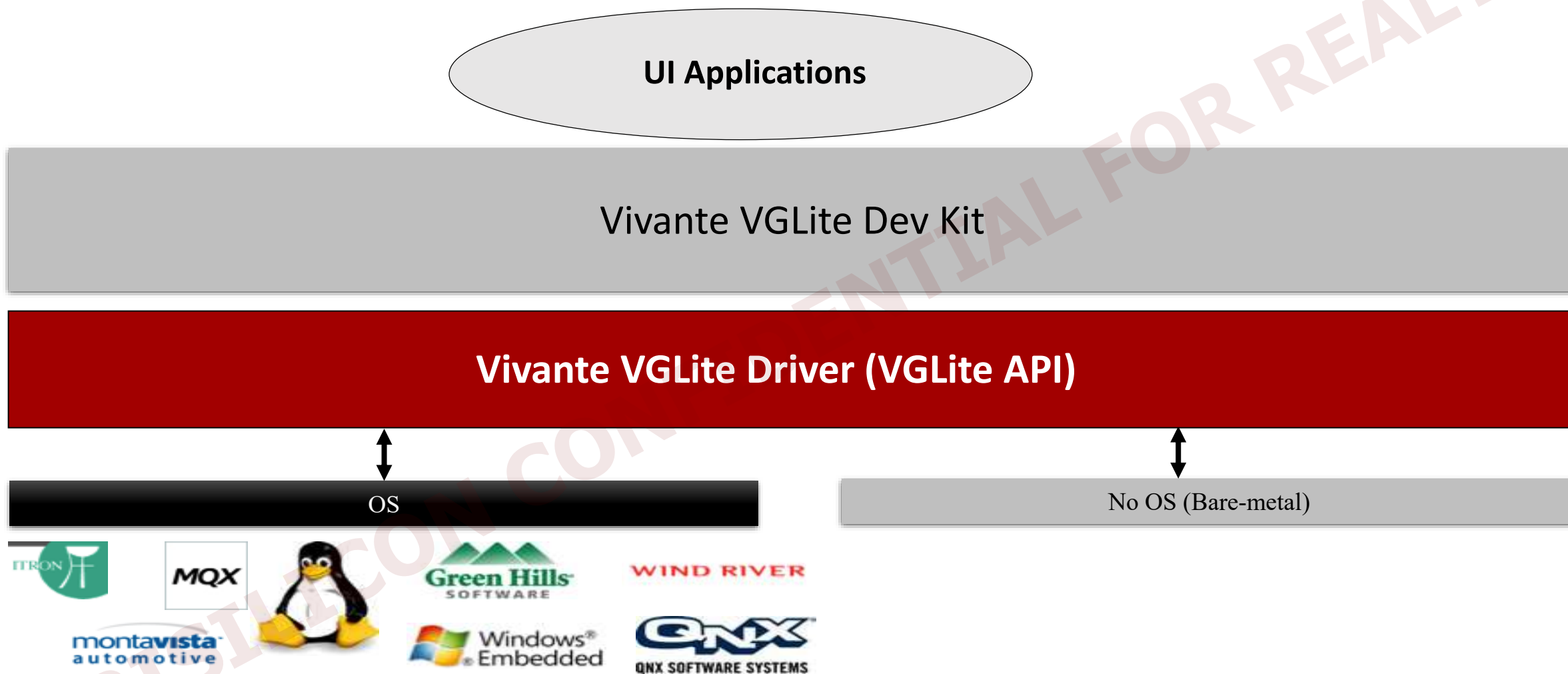
There are two potential cases can cause a path restart. 1.The num of intersections of a scan line is over 16/48/48in NOMSAA/MSAA4X4/MSAA2X2 mode; The GE module to do one more round of the same path to handle the xNode exceeding. TSClear state is a the beginning of path, 2.The size of tessellation buffer is overflow. GE report tessellation buffer overflow after the end of a path. FE will restart this path again GE module has to record the GE buffer overflow status. GE module will scissor the path's bounding box into small ones by the vertical direction, the number of small boxes depend on the GE buffer size and the Y-stride of this path (more details see section 3.6.2). GE will process the path with different small



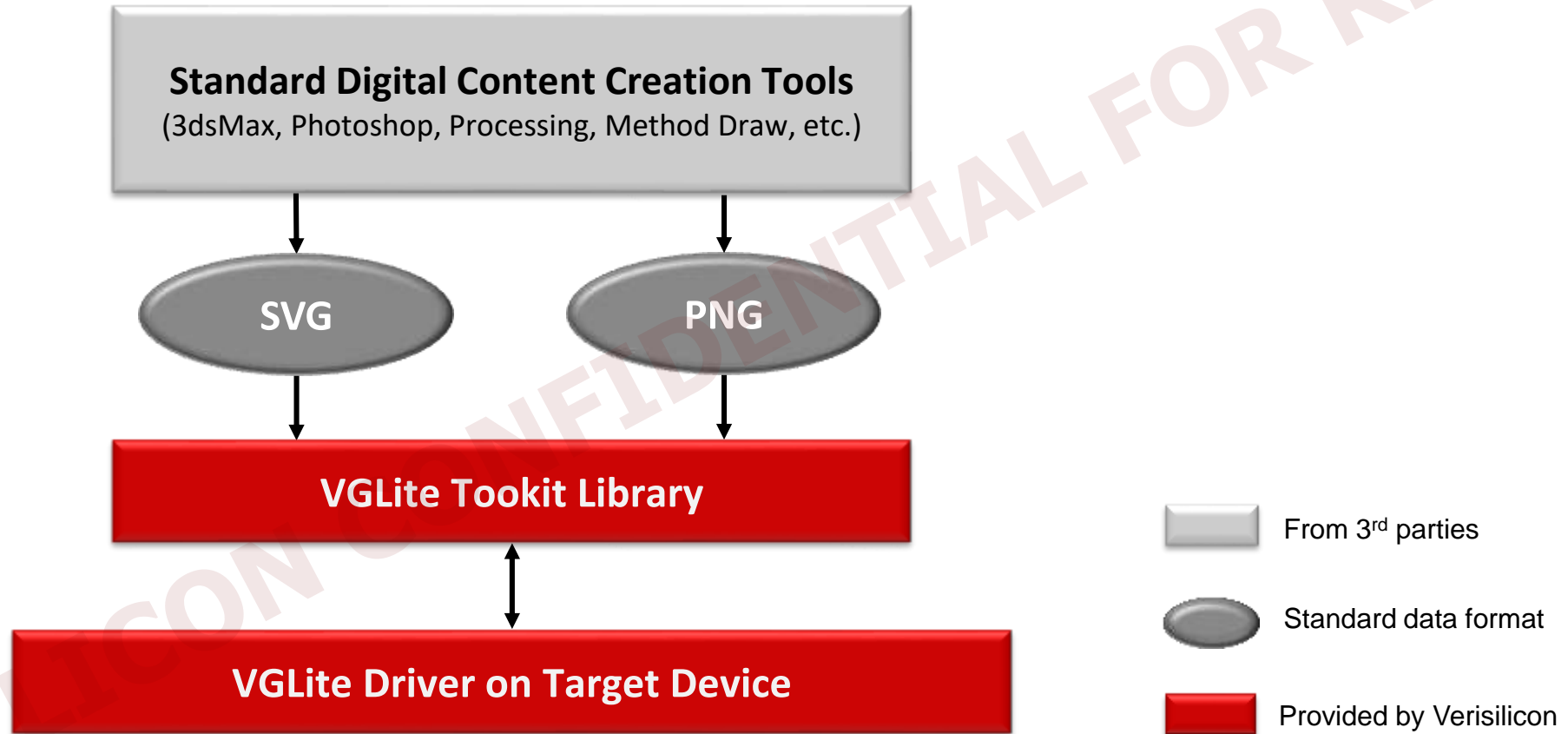
# Software Stack

## VGLite

# VGLite Software Overview



# VGLite ToolKit – User Flow



# Vivante VGLite Dev Kit

## ▲ SVG to EVO converter

- ▶ EVO is an opaque vector object in elementary library.
- ▶ The converter can translate SVG assets to EVO objects.
- ▶ SVG assets could be created from authoring tools available on websites, like processing.

## ▲ PNG to EBO converter

- ▶ EBO is an opaque bitmap object in elementary library.
- ▶ The converter is responsible to translate PNG files to EBO objects.

## ▲ Elementary library

- ▶ A helper library which is built on top of Vivante VGLite driver, and it provides interface to render and manipulate EVO/EBO objects, like blend/rotates etc. For detail please refer to DevKit document.

# VGLite GUI Development ECO System

▲ Crank

▲ MicroEJ Studio

▶ <https://developer.microej.com/supported-hardware/nxp-imx-rt595/>

▲ Monotype

▲ Express Logic GUIX STUDIO

▲ Altia

▲ Korulab

▶ <https://www.korulab.com/product.html>





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