



Vivante GCNanoUltraV GPU IP

V2.0.0

Accessible Registers

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Preface

This preface introduces this document, including the intended audience, conventions used, and reference documents for additional reading.

Intended Audience

This document is prepared for both hardware and software integrators who are familiar with system on chip (SoC) digital design and related support devices. Those who would benefit from this technical manual are:

- Engineers and managers who are evaluating this Vivante DC IP for use in a system
- Engineers who are designing this Vivante DC IP into a system

Using This Document

Vivante maintains a consistent register definition scheme across all its cores. For this reason, some field bits may have a field name defined in this document, but the field may not be in use for the core or specific core revision described in this document

You must not access register bits that are not defined in this document. All undefined bits within the valid register address range are designated as reserved register bits. These reserved bits are used for internal functions and any illegal operations may cause unpredictable behavior including, but not limited to, an IP/data bus hang.

Other conventions used in this document include:

- Hexadecimal numbers are indicated by the prefix "0x".
For example, 0x32CF.
- Binary numbers are indicated by the prefix "0b".
For example, 0b0011.0010.1100.1111.
- Rows with fields which are obsolete or not applicable for this core are not present are grayed out.

Additional Reading

The following documents are provided in the release package:

- Vivante GCNanoUltraV Hardware Features: Feature set available with this IP core
- Vivante GCNanoUltraV Hardware Integration Guide: Integration reference manual for this IP core
- Vivante GCNanoUltraV Accessible Registers: This document
- Vivante GCNanoUltraV Hardware Implementation Manual: Implementation reference material for the physical design implementation of this IP core

1 Introduction

This document is a register reference of exposed AHB/APB accessible registers for this Vivante IP core and includes only registers which Vivante customers may expose to their customers.

The register description chapter provides details about these registers, including their addresses, meanings, read/write attributes, field bits, reset values, and field meanings.

Register and field descriptions are not verbose, as their functions may be discerned from the module and register and/or field name. Registers are read/write unless specified otherwise.

Reset values for some registers will change for each release. These include those registers which uniquely identify a given release for a Vivante core. The reset value for these fields can be ignored during test.

A field or register may be noted as double-buffered. Double buffered means there are two sets of registers/register bits. One set is the working set used for the current frame. The other set is for configuration, so when you configure a register, the configuration does not take effect until the next frame begins.

2 Register Description

AQHiClockControl				
0x00000 = Byte Address		0x0000 = DWord Address		count = 1
Description: Clock Control Register.				
Sub-Field Name	Bits	rw	Reset	Description
FSCALE_VAL	8:2	rw	0x40	Core clock frequency scale value.
FSCALE_CMD_LOAD	9:9	rw	0x0	Core clock frequency scale value enable. When writing a 1 to this bit, it updates the frequency scale factor with the value FSCALE_VAL[6:0]. The bit must be set back to 0 after that. If this bit is set and FSCALE_VAL=0 (an invalid combination), the HREADYOUT output signal will get stuck to 0.
DISABLE_RAM_CLOCK_GATING	10:10	rw	0x0	Disables clock gating for rams.
DISABLE_DEBUG_REGISTERS	11:11	rw	0x1	Disable debug registers. If this bit is 1, debug registers are clock gated.
SOFT_RESET	12:12	rw	0x0	Soft resets the IP.
IDLE3_D	16:16	r	0x1	3D pipe is idle or not present.
IDLE2_D	17:17	r	0x1	2D pipe is idle or not present.
IDLE_VG	18:18	r	0x1	VG pipe is idle.
AQHidle				
0x00004 = Byte Address		0x0001 = DWord Address		count = 1
Description: Idle Status Register.				
Sub-Field Name	Bits	rw	Reset	Description

IDLE_FE	0:0	r	0x1	FE (Fetch Engine): 0=FE is busy; 1=FE is idle.
IDLE_DE	1:1	r	0x1	DE is idle or not present.
IDLE_PE	2:2	r	0x1	PE (Pixel Engine): 1=PE is idle.
IDLE_SH	3:3	r	0x1	SH is idle or not present.
IDLE_PA	4:4	r	0x1	PA is idle or not present.
IDLE_SE	5:5	r	0x1	SE is idle or not present.
IDLE_RA	6:6	r	0x1	RA is idle or not present.
IDLE_TX	7:7	r	0x1	TX is idle or not present.
IDLE_VG	8:8	r	0x1	VG (Vector Graphics Engine): 1= VG is idle.
IDLE_IM	9:9	r	0x1	IM (Image Engine): 1= IM is idle.
IDLE_FP	10:10	r	0x1	FP is idle or not present.
IDLE_TS	11:11	r	0x1	TS (Tessellation Engine): 1=TS is idle.
IDLE_BLT	12:12	r	0x1	BLT is idle or not present.
UNUSED	30:13	r	0x3FFF	Unused bits reserved for future expansion.
AXI_LP	31:31	r	0x0	AXI is in low power mode.

AQAxConfig

0x00008 = Byte Address **0x0002** = DWord Address count = 1

Description: AXI Configuration Register.

Sub-Field Name	Bits	rw	Reset	Description
AWCACHE	11:8	rw	0x2	Set AWCACHE[3:0] value.
ARCACHE	15:12	rw	0x2	Set ARCACHE[3:0] value.
AXDOMAIN_SHARED	17:16	rw	0x2	Configure AxDOMAIN value for shareable request. Not used for VG cores
AXDOMAIN_NON_SHARED	19:18	rw	0x0	Configure AxDOMAIN value for non-shareable request. Not used for VG cores
AXCACHE_OVERRIDE_SHARED	23:20	rw	0x2	Configure AxCACHE value for shareable request. Not used for VG cores

AQAxStatus

0x0000C = Byte Address **0x0003** = DWord Address count = 1

Description: AXI Status Register. READ ONLY

Sub-Field Name	Bits	rw	Reset	Description
WR_ERR_ID	3:0	r	0x0	The ID which caused illegal write access error.
RD_ERR_ID	7:4	r	0x0	The ID which caused illegal read access error.
DET_WR_ERR	8:8	r	0x0	1=A write error is detected.
DET_RD_ERR	9:9	r	0x0	1=A read error is detected.

AQIntrAcknowledge

0x00010 = Byte Address	0x0004 = DWord Address	count = 1
Description: Interrupt Acknowledge Register. Each bit represents a corresponding event being triggered. Reading from this register clears the outstanding interrupt. READ ONLY.		

<i>Sub-Field Name</i>	<i>Bits</i>	<i>rw</i>	<i>Reset</i>	<i>Description</i>
INTR_VEC	31:0	r	0x00000000	For each interrupt event, 0=Clear, 1=Interrupt Active. For all cores: Bit 31 is AXI_BUS_ERROR. 0=No error, 1=Interrupt Active.

AQIntrEnbl

0x00014 = Byte Address	0x0005 = DWord Address	count = 1		
Description: Interrupt Enable Register. Each bit enables a corresponding event.				
<i>Sub-Field Name</i>	<i>Bits</i>	<i>rw</i>	<i>Reset</i>	<i>Description</i>
INTR_ENBL_VEC	31:0	rw	0x00000000	0=Disable Interrupt; 1=Enable interrupt.

GCChipRev

0x00024 = Byte Address	0x0009 = DWord Address	count = 1		
Description: Chip Revision Register. Shows the revision for the chip in BCD. This register has no set reset value. It varies with the implementation. READ ONLY.				
<i>Sub-Field Name</i>	<i>Bits</i>	<i>rw</i>	<i>Reset</i>	<i>Description</i>
REV	31:0	r	0x00002003	Revision. This value may vary between releases and can be ignored during test.

GCChipDate

0x00028 = Byte Address	0x000A = DWord Address	count = 1		
Description: Chip Date Register. Shows the release date for the IP in YYYYMMDD (year/month/day) format. This register has no set reset value. It varies with the implementation. READ ONLY.				
<i>Sub-Field Name</i>	<i>Bits</i>	<i>rw</i>	<i>Reset</i>	<i>Description</i>
DATE	31:0	r	0x00000000	Date. This value will vary each release and can be ignored during test.

gcregHIChipPatchRev

0x00098 = Byte Address	0x0026 = DWord Address	count = 1		
Description: Chip Patch Revision Register. Patch revision level for the chip. It varies per release. READ ONLY				
<i>Sub-Field Name</i>	<i>Bits</i>	<i>rw</i>	<i>Reset</i>	<i>Description</i>
PATCH_REV	7:0	r	0x00	Patch Revision. This value will vary each release and can be ignored during test.

gcProductId

0x000A8 = Byte Address	0x002A = DWord Address	count = 1		
Description: Product Identification Register. Shows Product ID. READ ONLY.				
<i>Sub-Field Name</i>	<i>Bits</i>	<i>rw</i>	<i>Reset</i>	<i>Description</i>

GRADE_LEVEL	3:0	r	0x5	0:None-no extra letter on the product name for this core; 1:Nano; 5:NanoUltra.
NUM	23:4	r	0x00265	Product number is 265.
TYPE	27:24	r	0x3	Product Type is 3: VG (Vector Graphics).

gcModulePowerControls**0x00100** = Byte Address **0x0040** = DWord Address count = 1

Description: Module Power Control Register. Control register for module level power controls.

<i>Sub-Field Name</i>	<i>Bits</i>	<i>rw</i>	<i>Reset</i>	<i>Description</i>
ENABLE_MODULE_CLOCK_GATING	0:0	rw	0x0	Enables module level clock gating.
DISABLE_STALL_MODULE_CLOCK_GATING	1:1	rw	0x0	Disables module level clock gating for stall condition.
DISABLE_STARVE_MODULE_CLOCK_GATING	2:2	rw	0x0	Disables module level clock gating for starve/idle condition.
TURN_ON_COUNTER	7:4	rw	0x2	Number of clock cycles to wait after turning on the clock.
TURN_OFF_COUNTER	31:16	rw	0x0014	Counter value for clock gating the module if the module is idle for this amount of clock cycles.

gcModulePowerModuleControl**0x00104** = Byte Address **0x0041** = DWord Address count = 1

Description: Module Power Module Control Register. Module level control register.

<i>Sub-Field Name</i>	<i>Bits</i>	<i>rw</i>	<i>Reset</i>	<i>Description</i>
DISABLE_MODULE_CLOCK_GATING_FE	0:0	rw	0x0	Disables module level clock gating for FE.
DISABLE_MODULE_CLOCK_GATING_PE	2:2	rw	0x0	Disables module level clock gating for PE.
DISABLE_MODULE_CLOCK_GATING_VG	8:8	rw	0x0	Disables module level clock gating for VG.
DISABLE_MODULE_CLOCK_GATING_IM	9:9	rw	0x0	Disables module level clock gating for IM.
DISABLE_MODULE_CLOCK_GATING_TS	11:11	rw	0x0	Disables module level clock gating for TS.

gcModulePowerModuleStatus**0x00108** = Byte Address **0x0042** = DWord Address count = 1

Description: Module Power Module Status Register. Module level control status.

<i>Sub-Field Name</i>	<i>Bits</i>	<i>rw</i>	<i>Reset</i>	<i>Description</i>
MODULE_CLOCK_GATED_FE	0:0	r	0x0	Module level clock gating is ON for FE.

MODULE_CLOCK_GATED_PE	2:2	r	0x0	Module level clock gating is ON for PE.
MODULE_CLOCK_GATED_VG	8:8	r	0x0	Module level clock gating is ON for VG.
MODULE_CLOCK_GATED_IM	9:9	r	0x0	Module level clock gating is ON for IM.
MODULE_CLOCK_GATED_TS	11:11	r	0x0	Module level clock gating is ON for TS.
MODULE_CLOCK_GATED_FLE	12:12	r	0x0	Module level clock gating is ON for Flexa. Not supported for all variants.

AQMemoryDebug**0x00414** = Byte Address **0x0105** = DWord Address count = 1

Description: Memory Debug Register.

Sub-Field Name	Bits	rw	Reset	Description
MAX_OUTSTANDING_READS	7:0	rw	0x00	Limits the total number of outstanding read requests.

AQRegisterTimingControl**0x0042C** = Byte Address **0x010B** = DWord Address count = 1

Description: Timing Control Register.

Sub-Field Name	Bits	rw	Reset	Description
FOR_RF1P	7:0	rw	0x00	For 1 port ram.
FOR_RF2P	15:8	rw	0x00	For 2 port ram.
FAST_RTC	17:16	rw	0x3	RTC for fast rams.
FAST_WTC	19:18	rw	0x0	WTC for fast rams.
POWER_DOWN	20:20	rw	0x0	Powerdown memory.

gcregFetchAddress**0x00500** = Byte Address **0x0140** = DWord Address count = 1

Description: Fetch Command Buffer Base Address Register. Address of the command buffer. The address must be 64-byte aligned.

Sub-Field Name	Bits	rw	Reset	Description
TYPE	1:0	rw	0x0	
0 => SYSTEM				
1 => LOCAL				
2 => VIRTUAL				

ADDRESS 31:2 rw 0x00000000

gcregFetchControl**0x00504** = Byte Address **0x0141** = DWord Address count = 1

Description: Fetch Control Register. Writing a non-zero value to this register starts the fetch engine. The FE will start fetching 64-bit commands and data starting at the address specified by the gcregFetchAddress register. Make sure this count is large enough to fetch the END command, otherwise the FE will wait until more data is coming.

<i>Sub-Field Name</i>	<i>Bits</i>	<i>rw</i>	<i>Reset</i>	<i>Description</i>
COUNT	20:0	rw	0x0000000	Number of 64-bit words to fetch. 21 bits is enough for 16 MB.
TRIGGER_DC	31:31	rw	0x0	Specify whether to enable DC HW trigger in FE 0 => DISABLE 1 => ENABLE
gcregCurrentFetchAddress				
0x00508 = Byte Address		0x0142 = DWord Address		count = 1
Description: Current Fetch Command Address Register. Debugging register that defines the current address the FE is fetching data from. READ ONLY.				
<i>Sub-Field Name</i>	<i>Bits</i>	<i>rw</i>	<i>Reset</i>	<i>Description</i>
ADDRESS	31:0	r	0x00000000	Address of data for FE to fetch.

Document Revision History

This section describes differences between document revisions.

Note: This document is not necessarily updated for each patch or minor revision. The information in this document tends to be stable across a revision (nnn) series.

Document Revision	Date	Compatible Core	Description
0.80	2024-05-13	GCNanoUltraV gcnanoultrav_2_0_0_rc3z	Initial release