

**TFT LCD Driver Integrates
Capacitive Touch Controller
For Wearable/IoT Application**

ILITEK CONFIDENTIAL

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1 Introduction

The IL79400A-XX is a single chip highly integrates Amorphous TFT LCD driver and in-cell touch controller. IL79400A-XX combines with in-cell panel technology and provides high performance display and touch control for wearable consumer electronic applications.

The LCD driver in IL79400A-XX supports resolution up to 400(RGB) × 400 with 1/2 data compressed RAM and provides the number of colors up to 16.7M. The LCD driver is comprised of a 600-channel source driver, a dual-gate GIP driving circuits and a power supply circuit. In addition, Column / 1-dot / 1+2-dot / 2-dot / 4-dot liquid crystal inversion mode and D3G function to achieve high-quality display and vision experience.

For high-speed serial interface, the MIPI DSI interface mode, the LCD driver in IL79400A-XX supports one data lane and one clock lane for high-speed and low power transmission in both directions with low EMI noise. For other-speed interface, the IL79400A-XX supports SPI and MCU interface. The IL79400A-XX operates a wide range of an analog power supplies. The IL79400A-XX supports idle mode, sleep mode and deep standby power management functions, making the IL79400A-XX an ideal LCD driver for wearable products such as smart watch, band and IoT devices with color graphics display where conserving battery power is desired. Additionally, it has an internal step-up circuits and regulator that generates the LCD driving voltage and the voltage follower circuit for LCD driver.

The touch panel controller of IL79400A-XX is uses a 32-bit high-performance single-cycle instruction-set MCU. With its built-in high-speed high-performance hardware-accelerated computing modules, it provides superior data processing capabilities. IL79400A-XX AFE can scan and detect panel, so that it reaches point reporting rate over 60Hz. With ILITEK's driving technology and algorithms, the touch controller has excellent waterproof performance, strong anti-noise-and-interference ability and high signal to noise ratio. Its touch experience can achieve up to 2points. Moreover, IL79400A-XX also supports up to four virtual touch keys, wakeup-button enabling and other functions, to provide customers with better touch experience.

As to its application, IL79400A-XX supports the touch screen display panel, and it can be widely used in smart watch, band, IoT and other wearable devices.

2 Features

Display resolution options:

- 400RGB × 400
- 360RGB × 360
- 320RGB × 320
- 280RGB × 280
- 240RGB × 240
- 128RGB × 128
- (120~400)RGB × 2N (Max. = 960) for bypass RAM Video mode (Note)

Display color modes:

- Full color mode: 16.7M colors (24-bit)
- Color depth with supported Interface

Color depth	Interface
16.7M colors (24-bits, 8/8/8)	MIPI/SPI/MCU
262K colors (18-bits, 6/6/6)	MIPI/SPI/MCU
65K colors (16-bits, 5/6/5)	MIPI/SPI/MCU
256 colors (8-bits, 3/3/2)	SPI

- Idle Mode: 8-color

Display module:

- Supports 600(RGB) source channel outputs (S1~S600)
- Supports GOUTR[16:1] / GOUTL[16:1] dual gate control signals to GIP in the panel
- Supports inversion type: Column / 1-dot / 1+2-dot / 2-dot / 4-dot
- Support source scan type: Z / BOW

System interface types:

- 8-bit MCU interface
- Standard Serial Peripheral Interface (SPI)
- Dual/ Quad SPI mode
- DSI interface (DSI version 1.2 and D-PHY version 1.1):
- Support 1 lane (maximum speed 750Mbps)
- Command mode and Video mode

Direct compressed data input:

- Command mode: 1/2 data compressed data input

Power saving modes:

- Deep-standby mode
- Sleep mode
- Idle mode
- Gesture wake Up mode

Other on-chip functions / Miscellaneous

- Separate RGB gamma correction (1 analog gamma & 3 digital gamma)
- Support CABC (Content Adaptive Brightness Control) function
- Provide Internal NVM store initialization register settings
- NVM: 4 times for ID1~4, SID, MID, RID and IC version; 2 times for gamma settings, 2 times for other registers
- Support BIST (Built-In Self-Test) function

Input power:

- VCI = 2.7V ~ 3.6V
- VDDI = 1.65V ~ 3.6V

Source/ Gate power supply voltage:

- GVDDP = 3V ~ 5.9V (20mv/step)
- GVDDN = -3V ~ -5.9V (20mv/step)
- VGH = 8.4V ~ 20V (50mv/step)
- VGLO = -6V ~ -16V (50mv/step)
- AVDD = 4.5V ~ 6.3V (100mv/step)
- AVEE = -4.36V ~ -6.28V (80mv/step)
- VCL = -2.76V ~ -3.32V (80mv/step)
- VCOM = -0.2V ~ -4V (10mv/step)

Touch Spec:

- 32-bit embedded MCU
- Self-type capacitance
- 64 channels
- 60Hz / 120Hz report rate (120Hz data is calculated from 60Hz data)
- Wake-up gesture
- Water proof
- High Accuracy & Linearity
- Noise Immunity
- 4 virtual button support
- 2 fingers support
- Touch FW host download

Note:

1. Max number of 960 gate lines varied by vertical resolution & frame rate, for further application, contact ILITEK for detail information.
2. Part number description:

IL79400A-XX	Operating temperature
-00	-30°C ~ 70°C
-X1	-40°C ~ 80°C
-H1	-40°C ~ 85°C

3 Device Overview

3.1 Block Diagram

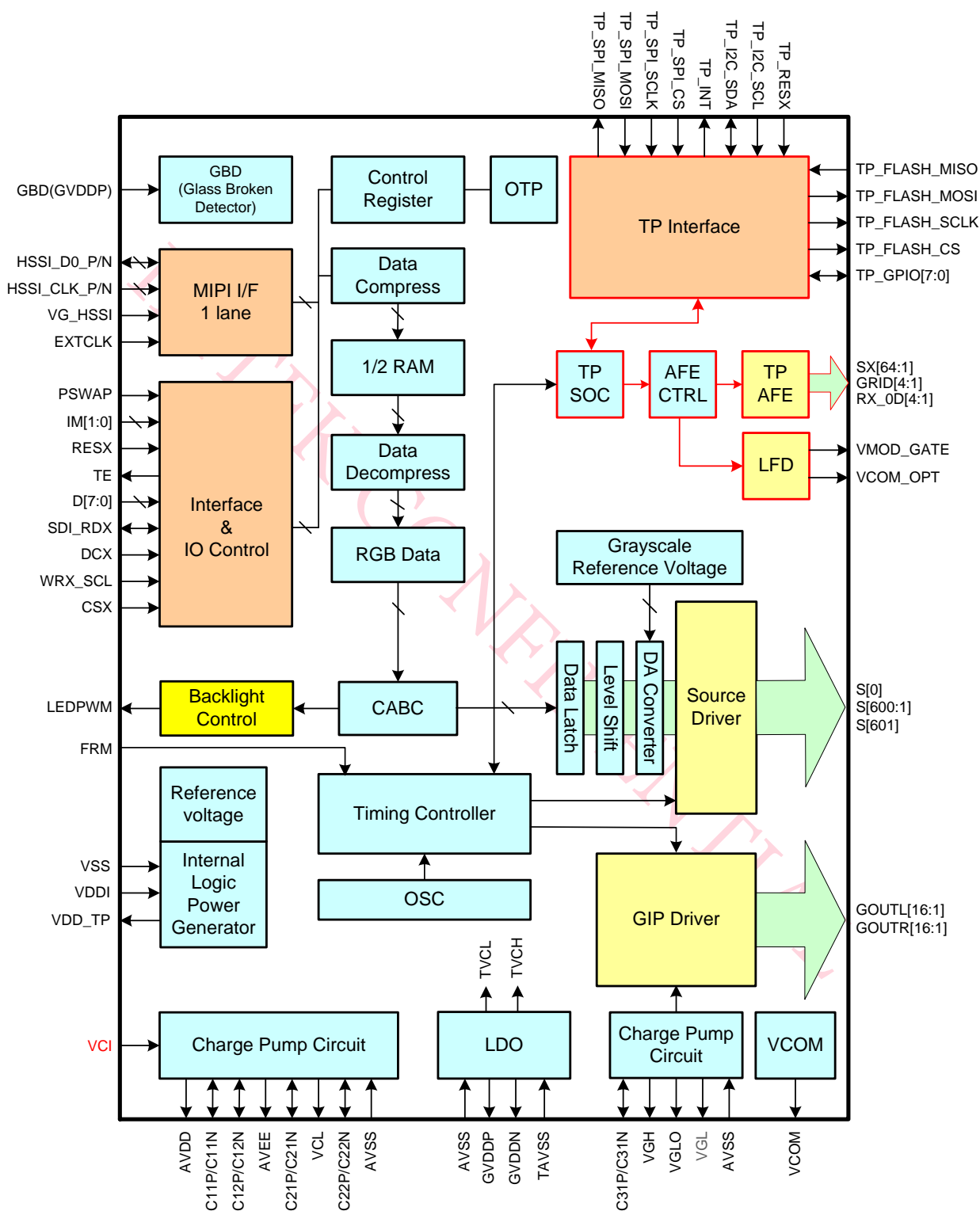


Figure 1. Block Diagram

3.2 Block Function Description

3.2.1 System Interface for Display

The IL79400A-XX supports DSI interfaces. The swap definition of MIPI DSI output signals is controlled by hardware pin PSWAP.

3.2.2 Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates the LCD drive voltage. The IL79400A-XX can display up to 16.7M colors at the maximum.

3.2.3 Timing Controller

The timing generator is used to generate timing signals for operating internal circuits. Timing for display operations and internal operations are outputted separately so that they do not interfere with each other.

3.2.4 Oscillator

The IL79400A-XX incorporates an RC oscillator circuit.

3.2.5 Source Driver Circuit

The LCD display driver circuit consists of a 600-output source driver. The display pattern data is latched when 400RGB pixels of data are input. The voltage is output from the source driver according to the latched data.

3.2.6 GIP Driver Circuit

The panel control circuit outputs GOUTR[16:1] and GOUTL[16:1] signals at either VGH, VGLO level.

3.2.7 Charge Pump Circuit

The LCD driver charge pump circuit generates the voltage levels for driving a panel. Voltage levels are adjusted according to register setting.

3.2.8 MIPI DSI Controller Circuit

The MIPI DSI controller circuit consists of the D-PHY controller, Protocol Control Unit (PCU), Packet Processing Unit (PPU), ECC generating circuit and analog transceiver. The D-PHY controls communication with the analog block and the ECC generating circuit generates the ECC to check the outgoing data stream for accuracy of the receiving data packet. The PCU controls outgoing and incoming data streams and the PPU controls transmitting packet distribution and merging.

3.2.9 CABC (Content Adaptive Brightness Control) Function

Content Adaptive Brightness Control (CABC), the backlight control circuit adjusts backlight brightness according to the histogram of image to reduce power consumption at the backlight. Brightness of the backlight and display data is adjusted.

3.2.10 D3G (3 Digital Gamma) Function

The IL79400A-XX provides D3G function that can make RGB gamma correction settings separately for RGB dots.

3.2.11 1/2 Compressed RAM

The IL79400A-XX provides 1/2 data compressed RAM (400 × 400 × 24bits × 1/2) to store display data.

3.2.12 AFE Controller

AFE controller completes the driving and scanning of the sensors in the touch panel, and sends the data of touch sensors after scanning to the MCU for data processing.

3.2.13 TP SOC (Embedded MCU)

SOC complete the control, data processing, LCD operation and coordination, HOST communication and other functions of the whole touch systems. Firmware, stored in external flash memory, can be loaded into the internal SRAM by HOST via the SPI interface.

3.2.14 TP Interface

The interface of IL79400A-XX for touch communication with host can be I2C or SPI. Whenever there is effective touch sensed on the touch screen, Touch controller will send data transfer request to the HOST via I2C or SPI port, and complete the point report to the HOST. HOST can communicate with IL79400A-XX via I2C or SPI. HOST can also reset Touch controller through TP_RESX port.

3.2.15 External Flash

External flash is used to store the Firmware, and uses SPI interface to communicate with it.

3.2.16 SX Driving Circuit

Supply VCOM level when LCD driving. Generates TP sensing pulse when TP driving.

3.3 Pad Descriptions

Table 1. Global Control Pins

Pin Name	I/O	Type	Descriptions		
IM[1:0]	I	VDDI	- Selects the interface to MPU.		
			IM1	IM0	Interface Selection
			0	0	DSI MIPI / 3-wire SPI
			0	1	DSI MIPI / 4-wire SPI
			1	0	DSI MIPI / Quad-SPI
1	1	MCU IF			
Note: D-IC cannot receive MIPI and SPI command or data at the same time.					
PSWAP	I	VDDI	- PSWAP is used for polarity swap of MIPI DSI. Please pull it to VDDI or GND.		
RESX	I	VDDI	- The external reset pin for LCD Display (Active low) Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power. If not used, please pull it to VDDI.		
TE	O	VDDI	- Tearing effect output signal. If not used, please leave it open.		
FRM	I	VDDI	- Control Built-in Self-Test (BIST) function on/off. FRM = "0": Disable. (default) FRM = "1": Enable. If not used, please pull it to GND.		
CSX	I	VDDI	- Chip Select Input CSX = "0" : accessible CSX = "1" : inaccessible If not used, please pull it to VDDI.		
WRX_SCL	I	VDDI	- Serial Clock Input in SPI interface - Write execution control pin in MCU interface. If not used, please pull it to GND.		
SDI_RDX	I/O	VDDI	- Data Input in SPI interface. - Read execution control pin in MCU interface. If not used, please pull it to VDDI.		
DCX	I	VDDI	-Display data / command selection DCX = "0" : Command DCX = "1" : Display data or Parameter If not used, please pull it to GND.		
D[7:0]	I/O	VDDI	- MCU parallel interface data bus. - D[1:0] Use in QSPI interface. - D[2]: Data Output in SPI interface. - D[3]: MIPI error report flag and ESD Detection output pin. If not used, D[7:3], D[1:0] pull to GND, D[2] leaves to open.		

Table 2. MIPI DSI Interface Signal Pins

Pin Name	I/O	Type	Descriptions
HSSI_CLK_P HSSI_CLK_N	I	VDDI	- MIPI DSI differential clock pair. If not used, please fix to VG_HSSI. Note: If deep standby mode is used, please pull HSSI_CLK_P / HSSI_CLK_N to VG_HSSI after issuing deep standby command.
HSSI_D0_P HSSI_D0_N	I	VDDI	- MIPI DSI differential data pair. (Data lane 0) If not used, please fix to VG_HSSI. Note: If deep standby mode is used, please pull HSSI_D0_P / HSSI_D0_N to VG_HSSI after issuing deep standby command.

Table 3. Source / Panel Control Signal Pins

Pin Name	I/O	Type	Descriptions
S[600:1]	O	Analog	- Liquid crystal application voltage output lines. If not used, please leave it open.
S[601], S[0]	O	Analog	- Liquid crystal application dummy voltage output lines. (For R/G/B shift use) If not used, please leave it open.
GOUTL[16:1]	O	Analog	- Gate control signals for panel in left side of IC. If not used, please leave it open.
GOUTR[16:1]	O	Analog	- Gate control signals for panel in right side of IC. If not used, please leave it open.

Table 4. Power Supply Pins

Pin Name	I/O	Type	Descriptions
VCI	I	Power Supply	- Power supply for analog circuit Connect to an external power supply of 2.7V to 3.6V.
VDDI	I	Power Supply	- Power supply for I/O pads Connect to an external power supply of 1.65V to 3.6V.
AVSS	I	Ground	- System Ground for the analog circuit.
AVSS_BG	I	Ground	- System Ground for the analog circuit.
VSS	I	Ground	- System Ground for the digital circuit.
TAVSS	I	Ground	- System Ground for the TP circuit.
VG_HSSI	I	Ground	- System Ground for MIPI DSI analog ground.

Table 5. DC-to-DC Circuit Pins

Pin Name	I/O	Type	Descriptions
VDD_TP	O	Analog	- Internal logic regulator output Connect to a stabilizing capacitor between VDD_TP and GND.
AVDD	O	Analog	- Power supply for step-up circuit.
GVDDP	O	Analog	- Output voltage generated from AVDD - Test pin for Glass Break detection (GBD) Positive LDO output for gamma circuit. If not used, please leave it open.
GVDDN	O	Analog	- Output voltage generated from AVEE Negative LDO output for gamma circuit. If not used, please leave it open.
AVEE	O	Analog	- Output voltage from step-up circuit Connect to a stabilizing capacitor between AVEE and GND.
VCL	O	Analog	- Output voltage from step-up circuit Connect to a stabilizing capacitor between VCL and GND.
VGH	O	Analog	- Output voltage from step-up circuit Connect to a stabilizing capacitor between VGH and VMOD_GATE.
VGLO	O	Analog	- Output voltage from step-up circuit Connect to a stabilizing capacitor between VGLO and VMOD_GATE.
C11P/C11N C12P/C12N	C	Step-up Capacitor	- Connect the charge-pumping capacitor for generating AVDD level.
C21P/C21N	C	Step-up Capacitor	- Connect the charge-pumping capacitor for generating AVEE level.
C22P/C22N	C	Step-up Capacitor	- Connect the charge-pumping capacitor for generating VCL level.

C31P/C31N	C	Step-up Capacitor	- Connect the charge-pumping capacitor for generating VGH/VGLO level.
VCOM	O	Analog	- Common voltage to the liquid crystal panel. Connect to a stabilizing capacitor between VCOM and GND.
VCOM_PASS	I/O	Pass	- Pass line for VCOM or VCOM_OPT from ILB.
TAVDD	O	Analog	- Output positive voltage for TP circuit Connect to AVDD on the FPC.

Table 6. Touch Panel Control Pins

Pin Name	I/O	Type	Descriptions
SX[64:1]	I/O	Analog	- Separate COM Electrode Sensing pins. (TP Sensor Pins)
RX_0D[4:1]	I/O	Analog	- Touch button key Please reserve these pin on the FPC. If not used, please leave it open.
GRID[4:1]	O	Analog	- Dummy Pad or output VCOM modulation signal. If not used, please leave it open.
VMOD_GATE	O	Analog	- Touch Modulation signal output. Bypass modulation signal to VGH and VGLO with capacitors.
VCOM_OPT	O	Analog	- Optional Touch Modulation signal buffer output.

Table 7. TP Interface Logic Pads

Pin Name	I/O	Type	Descriptions
TP_RESX	I	VDDI	- The external reset pin for touch (Active low) Connection to Host Processor or external RC circuit.
TP_I2C_SCL	I	VDDI	- TP I2C Clock IC internal pull high.
TP_I2C_SDA	I/O	VDDI	- TP I2C Data IC internal pull high.
TP_INT	O	VDDI	- Touch communication interrupt.
TP_FLASH_CS	O	VDDI	- SPI chip select signal to Flash If not used, please leave it open.
TP_FLASH_SCK	O	VDDI	- SPI serial clock to Flash If not used, please leave it open.
TP_FLASH_MOSI	O	VDDI	- SPI data output to Flash If not used, please leave it open.
TP_FLASH_MISO	I	VDDI	- SPI data input from Flash IC internal pull Low. If not used, please leave it open.
TP_SPI_CS	I	VDDI	- SPI chip select signal from Host If not used, please pull it to VDDI or leave it open.
TP_SPI_SCLK	I	VDDI	- SPI clock form Host If not used, please pull it to GND or leave it open.
TP_SPI_MOSI	I	VDDI	- SPI data Input form Host If not used, please pull it to GND or leave it open.
TP_SPI_MISO	O	VDDI	- SPI data output to Host If not used, please leave it open.

Table 8. LED Driver Control Pins

Pin Name	I/O	Type	Descriptions
LEDPWM	O	VDDI	- Control signal for brightness of LED backlight PWM signal's width is between 0% (Low) and 100% (HIGH). Signal amplitude: VDDI – VSS If not used, please leave it open.

Table 9. Test / Dummy Pins

Pin Name	I/O	Type	Descriptions
EXTCLK	I	VDDI	- Test pin. Please pull it to GND or leave it open.
TEST[2:0]	I	VDDI	- Test pin. Please pull it to GND or leave it open.
TESTEN	I	VDDI	- Test pin. Please pull it to GND or leave it open.
TP_GPIO[7:0]	I/O	VDDI	- Touch digital test pin Please leave it open.
TP_EXTCLK	I	VDDI	- Touch test pin. Please leave it open.
TP_UART_TX	O	VDDI	- UART TX pad Please leave it open.
TP_TEST_EN	I	VDDI	- Touch test pin. Please pull it to GND or leave it open.
TP_TCKC	I/O	VDDI	- Touch test pin. Please leave it open.
TP_TMSC	I/O	VDDI	- Touch test pin. Please leave it open.
VGL	O	-	- Test pin. Please leave it open.
DUMMY	-	-	- Dummy pin. Please leave it open.

3.3.1 Max series resistance table

Pin Name	Type	Max Series Resistance	Unit
VCI, AVSS, VG_HSSI	Input	3	Ω
HSSI_D0_P, HSSI_D0_N	Input / Output	5	Ω
HSSI_CLK_P, HSSI_CLK_N	Input	5	Ω
C11P, C11N, C12P, C12N, C21P, C21N, C22P, C22N, VDDI, VDD_TP, AVDD, AVEE, VCL, TAVDD, TAVSS, VSS	Output	5	Ω
VGH, VGL, VGLO, VMOD_GATE, VCOM	Output	10	Ω
TP_FLASH_MISO, VCOM_OPT, VCOM_PASS, GRID	Input	20	Ω
VCOM_PASS	Input / Output	20	Ω
C31P, C31N, RX_0D[4:1], AVSS_BG, TP_FLASH_CS, TP_FLASH_SCLK, TP_FLASH_MOSI	Output	20	Ω
RESX, IM[1:0], PSWAP, WRX_SCL, DCX, CSX, TP_RESX, TP_I2C_SCL, TP_SPI_CS, TP_SPI_SCK, TP_SPI_MOSI, FRM.	Input	50	Ω
GOUTL[16:1], GOUTR[16:1], TP_INT, TP_SPI_MISO, LEDPWM, TE, GVDDP, GVDDN.	Output	50	Ω
SDI_RDx, D[7:0], TP_I2C_SDA.	Input / Output	50	Ω

3.4 Power Supply Generation Circuit

The following figure shows the configuration of the liquid crystal drive voltage generating circuit.

3.4.1 Power Block

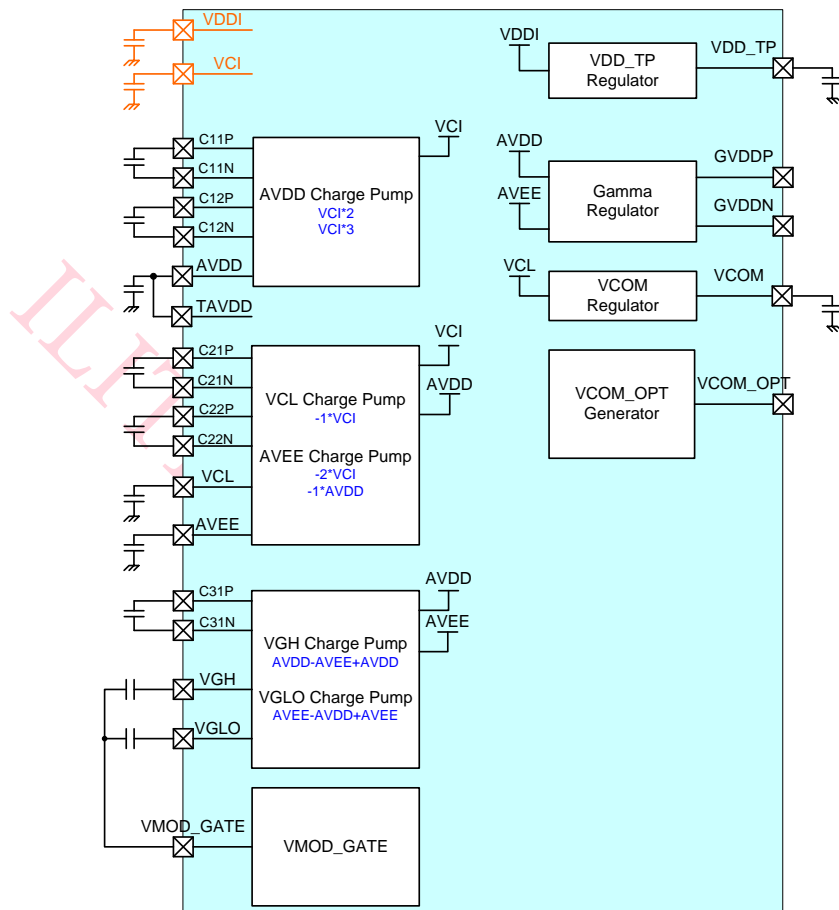


Figure 2. Supply Generating Circuit for Two Power Mode

Table 10. External Component List

Capacitor					
NO.	Pad Name	Connection		Value	Note
1	VDDI	VDDI	GND	1.0uF / 6.3V	Option
2	VCI	VCI	GND	1.0uF / 6.3V	Option
3	AVDD	AVDD	GND	1.0uF / 10V	
4	AVEE	AVEE	GND	1.0uF / 10V	
5	VCL	VCL	GND	1.0uF / 6.3V	
6	VGH	VGH	VMOD_GATE	1.0uF / 25V	
7	VGLO	VGLO	VMOD_GATE	1.0uF / 25V	
8	C11	C11P	C11N	1.0uF / 6.3V	
9	C12	C12P	C12N	1.0uF / 6.3V	Option for dual pump or x3 VCI
10	C21	C21P	C21N	1.0uF / 10V	
11	C22	C22P	C22N	1.0uF / 6.3V	
12	C31	C31P	C31N	1.0uF / 16V	
13	VDD_TP	VDD_TP	GND	1.0uF / 6.3V	
14	VCOM	VCOM	GND	1.0uF / 6.3V	

Resistance					
NO.	Pad Name	Connection		Value	Note
1	R1	VCOM_PASS	VCOM_OPT	0 ohm	Option
2	R2	RESX	RESX	0 ohm	Option
3	R3	LEDPWM	LEDPWM	0 ohm	Option
4	R4	TP_RESX	TP_RESX	0 ohm	Option
5	R5	TP_I2C_SDA	TP_I2C_SDA	0 ohm	Option
6	R6	TP_I2C_SCL	TP_I2C_SCL	0 ohm	Option
7	R7	TE	TE	0 ohm	Option
8	R8	RESX	TP_RESX	0 ohm	Option

Note: Capacitance +/-10% at temperature range -25 to 85°C

3.4.2 Voltage Setting Pattern

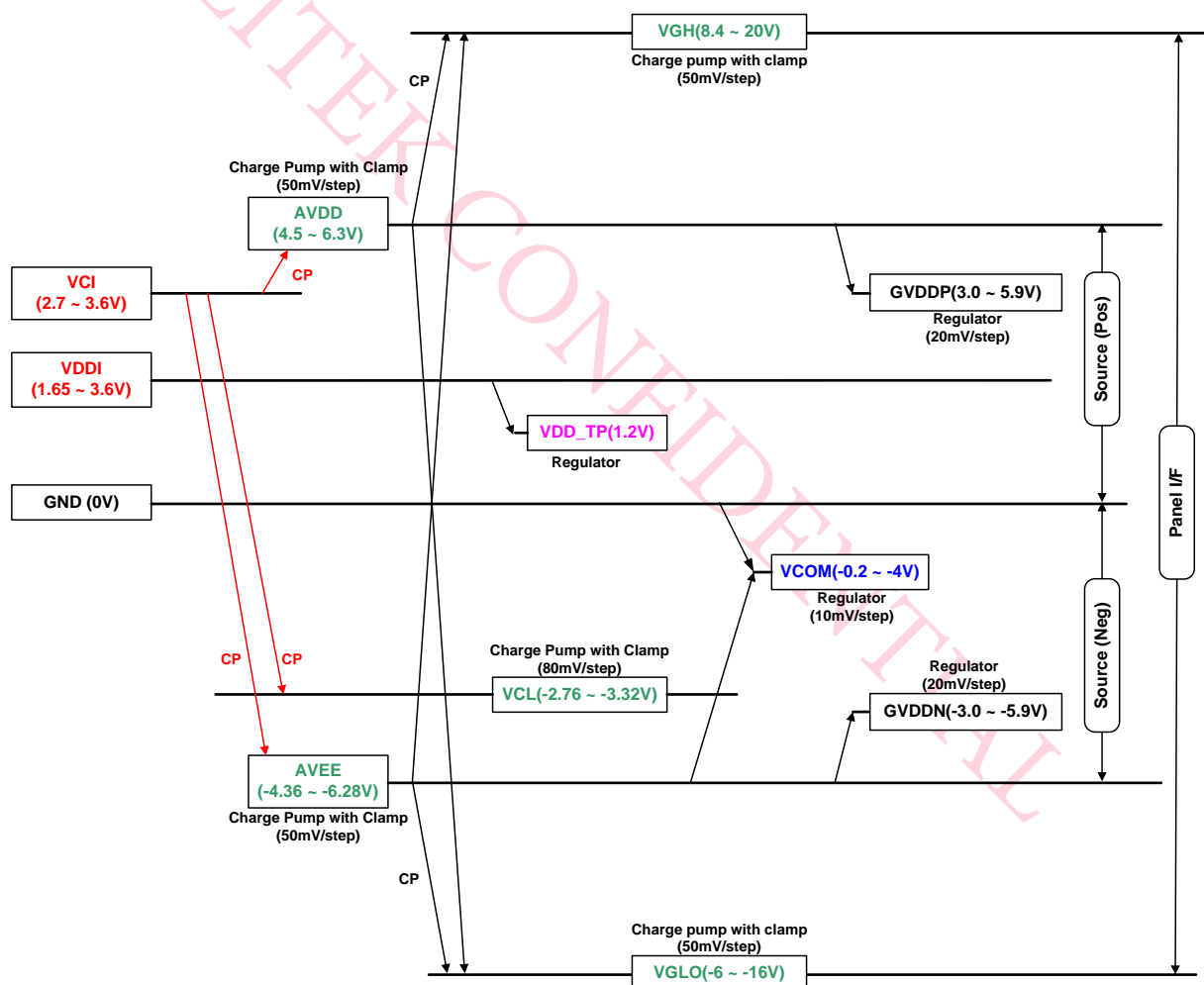


Figure 3. Voltage Generation diagram

4 Display Interface

4.1 MCU Interface

4.1.1 Write Cycle and Sequence

During a write cycle the host processor the parallel data to the display module via the interface. The MCU interface utilize CSX, DCX, SDI_RDX, WRX_SCL and D[7:0] signals. WRX_SCL is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module receives the host processor information on the rising edge of SCL.

During the write sequence the host processor writes one or more bytes of information to the display module via the interface. The write sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high.

4.1.1.1 The basic command format

The host should send 2 bytes command including 1 byte real command and 1 byte dummy command.

For example, sleep-out command (11h), host should send 0x1100, column address set command (2Ah), host should send 0x2A00 and 0x0000 0000 0001 008F (400RGB) sequentially.

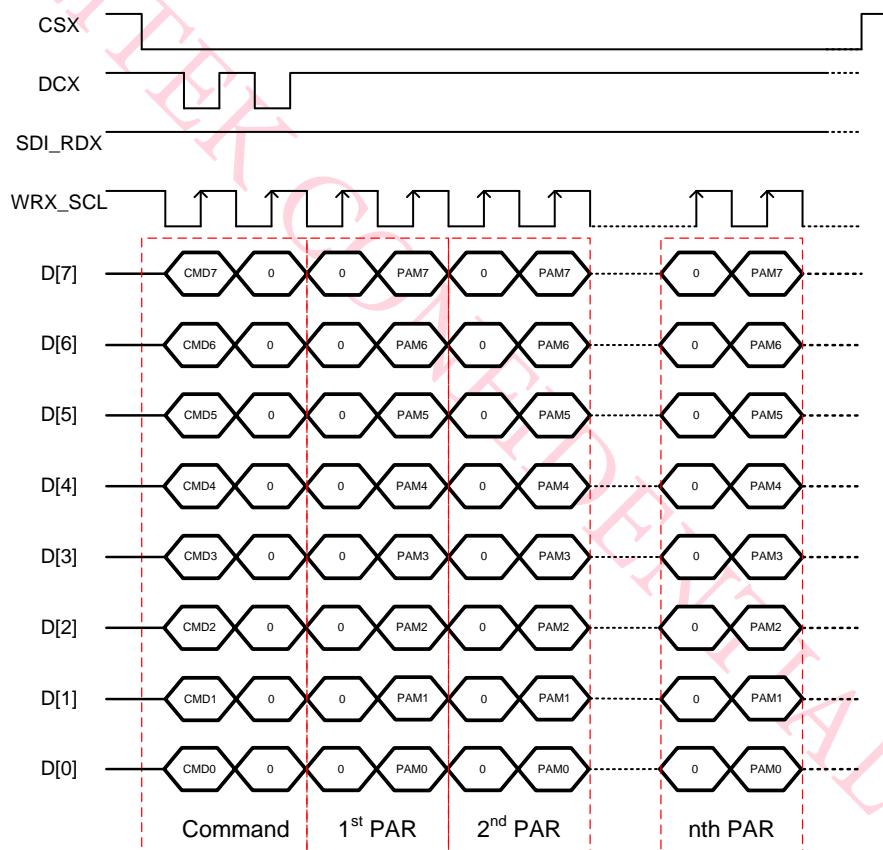


Figure 6. MCU interface basic command format

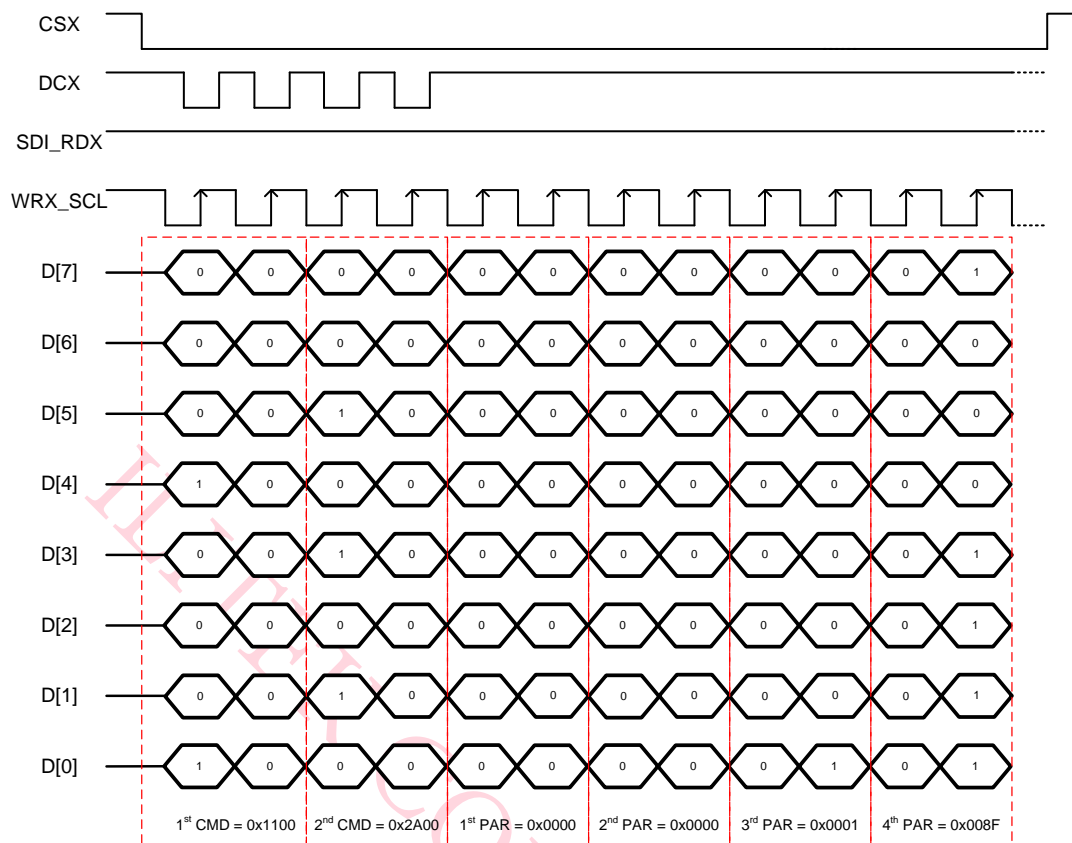


Figure 7. MCU interface command example

4.1.1.2 The pixel data format

When IFPF is equal to 7 (page 0, 3Ah=0x77):

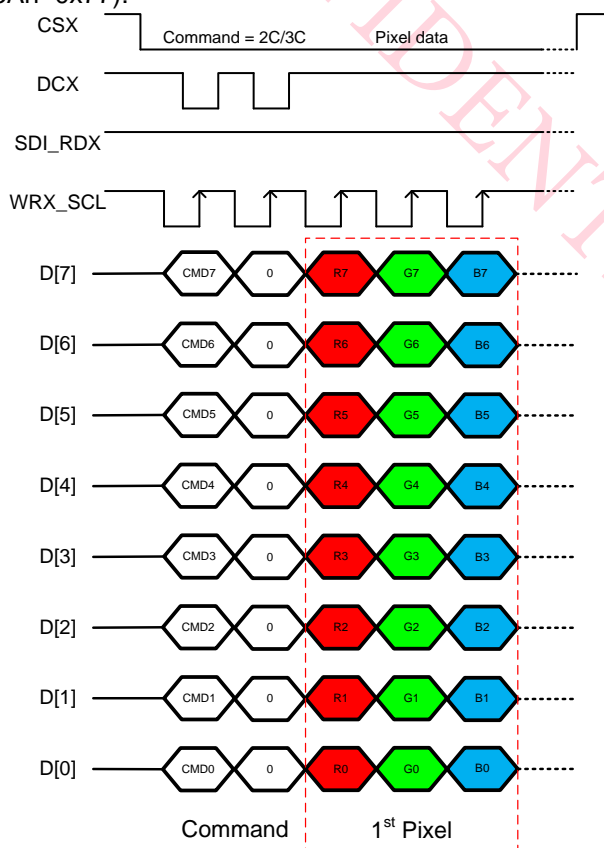


Figure 8. MCU Interface in 24-bit mode

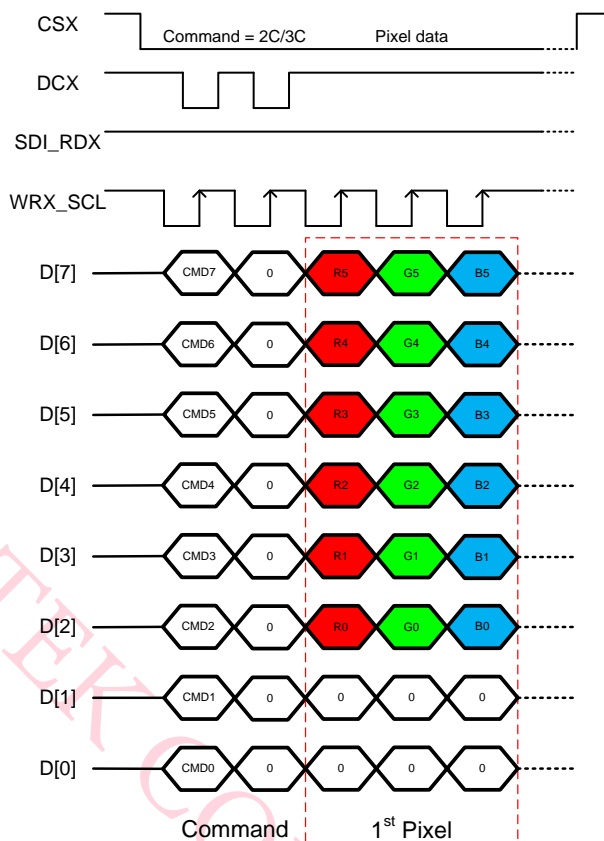


Figure 9. MCU Interface in 18-bit mode

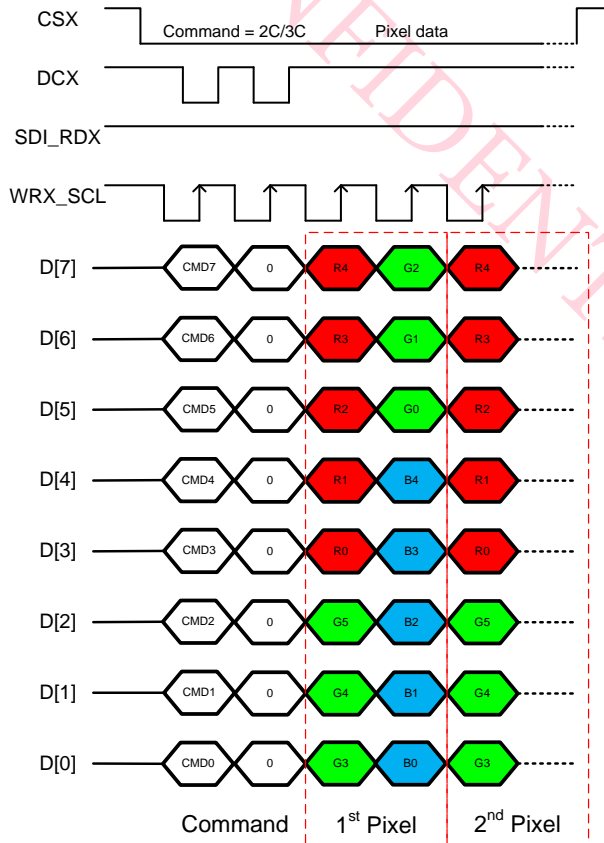


Figure 10. MCU Interface in 16-bit mode

4.1.2 Read Cycle and Sequence

When the host reads register's parameter or display data from IL79400A-XX, the host has to send a command and then the following byte is transmitted in the opposite direction. The host should send 2 bytes command including 1 byte real command and 1 byte dummy command, and IL79400A-XX will transmit 2 bytes parameters including 1 byte dummy parameter and 1 byte real parameter to host.

The register's parameter or display data is latch when CSX keeps low and SDI_RDX status is changed from low to high.

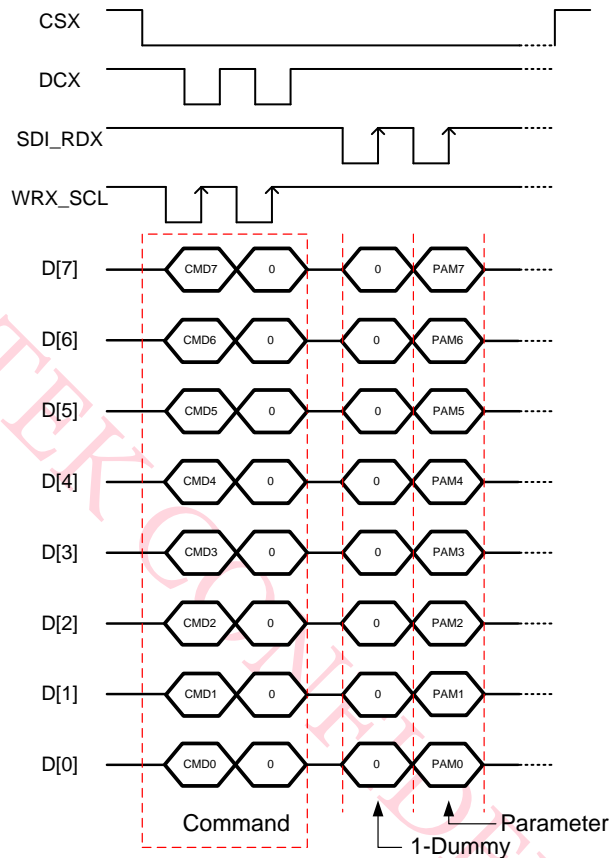


Figure 11. MCU Interface Read Operation

4.2 3-wire/ 4-wire SPI Interface

4.2.1 Write Cycle and Sequence

The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA). The 4-line serial mode consists of the Data/Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA) for data transmission. The data bus (D[7:0]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

The write mode of the interface means that host writes commands or data to IL79400A-XX. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is "low", the transmission byte is interpreted as a command byte. If the D/CX bit is "high", the transmission byte is stored as the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to IL79400A-XX and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.

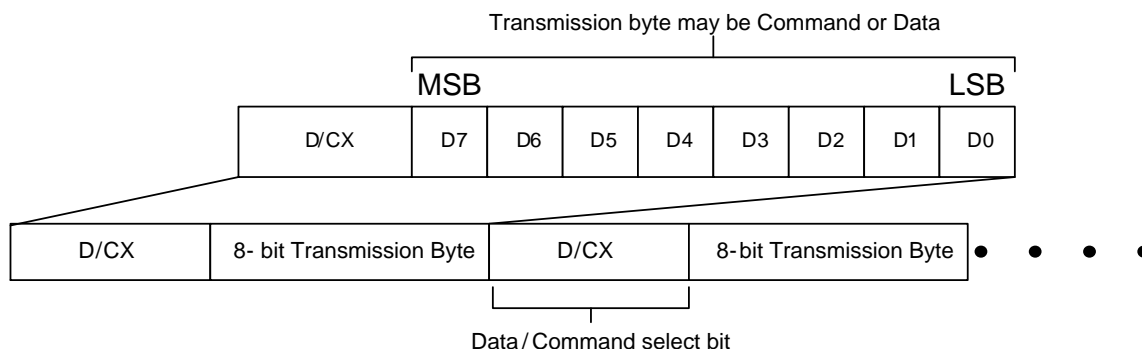


Figure 12. 3-line Serial Interface Data Format

Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by IL79400A-XX on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width.

The 3/4-line serial interface writes command sequences described in the figure as below.

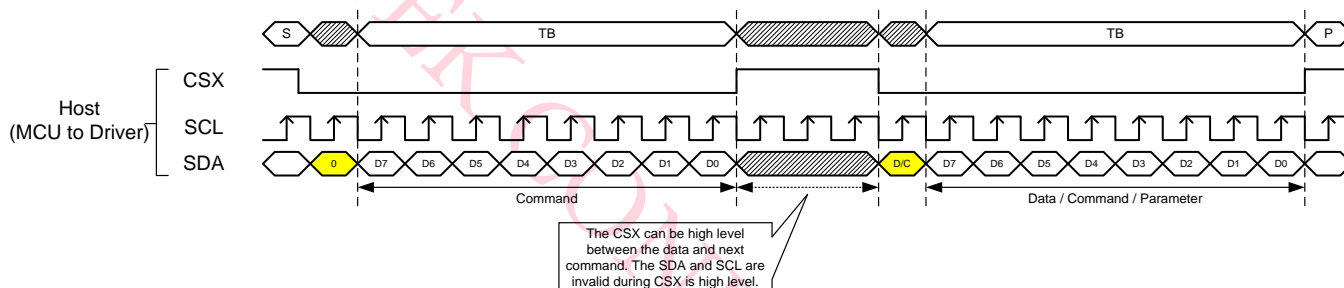


Figure 13. 3-line SPI Write Interface Protocol

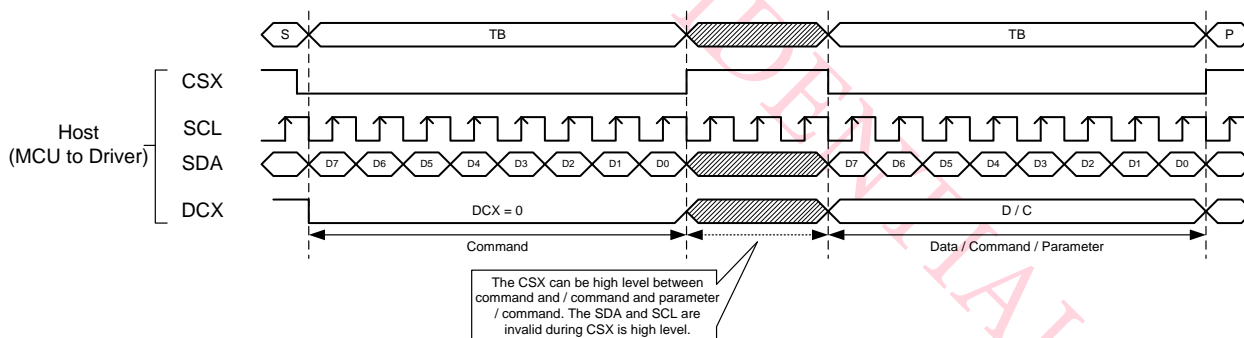


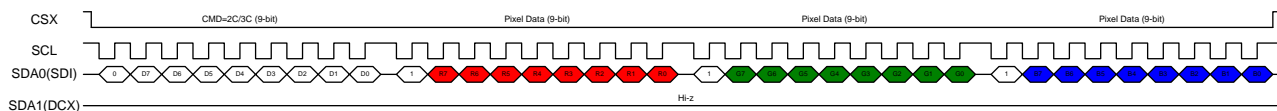
Figure 14. 4-line SPI Write Interface Protocol

The 3/4-line serial interface writes display data sequences described in the figure as below.

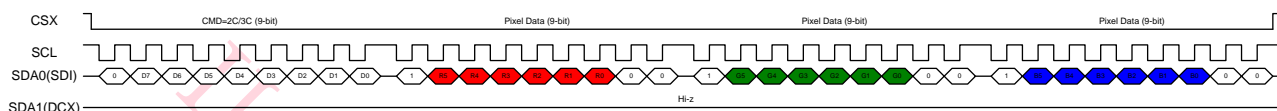
4.2.1.1 Single SPI

When DSPI_EN is equal to 0 (page 0, C4h_[0]=0), the host sends data by SDA only :

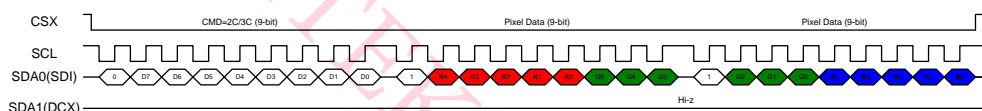
SPI3, RGB888 (IFPF[2:0]=3'b111), DSPI_EN[0]=1'b0



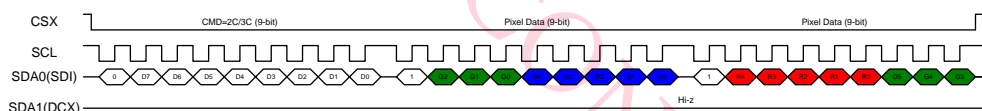
SPI3, RGB666 (IFPF[2:0]=3'b110), DSPI_EN[0]=1'b0



SPI3, RGB565 (IFPF[2:0]=3'b101), DSPI_EN[0]=1'b0



SPI3, RGB3553 (IFPF[2:0]=3'b101), DSPI_EN[0]=1'b0, 3553_EN=1



SPI3, RGB332 (IFPF[2:0]=3'b010), DSPI_EN[0]=1'b0

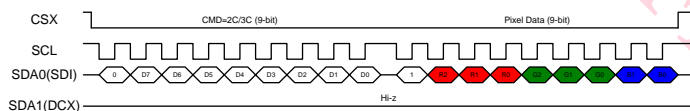
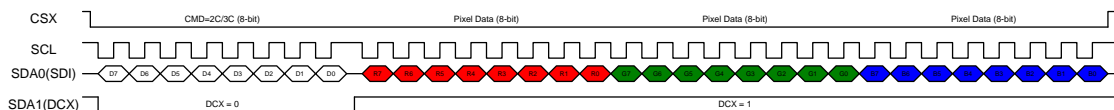
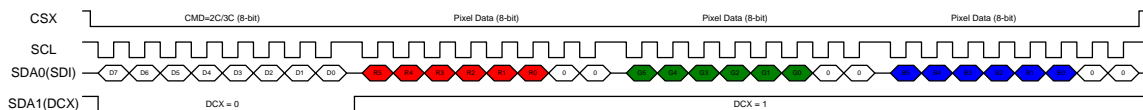


Figure 15. SPI-3 Mode in Single SPI

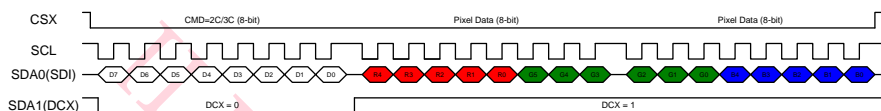
SPI4, RGB888 (IFPF[2:0]=3'b111), DSPI_EN[0]=1'b0



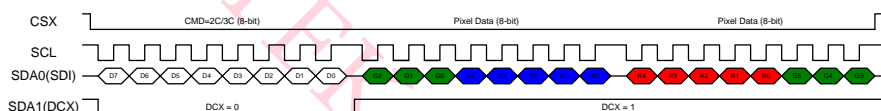
SPI4, RGB666 (IFPF[2:0]=3'b110), DSPI_EN[0]=1'b0



SPI4, RGB565 (IFPF[2:0]=3'b101), DSPI_EN[0]=1'b0



SPI4, RGB3553 (IFPF[2:0]=3'b101), DSPI_EN[0]=1'b0, 3553_EN=1



SPI4, RGB332 (IFPF[2:0]=3'b010), DSPI_EN[0]=1'b0

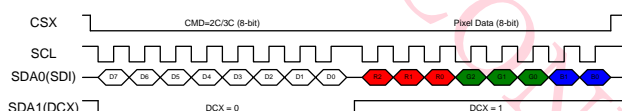
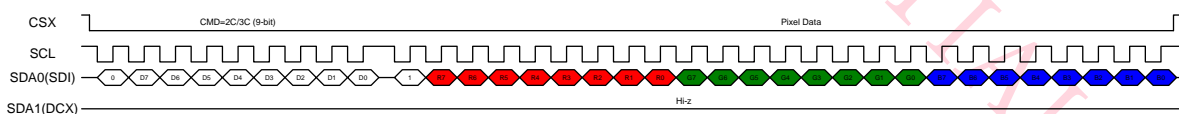


Figure 16. SPI-4 Mode in Single SPI

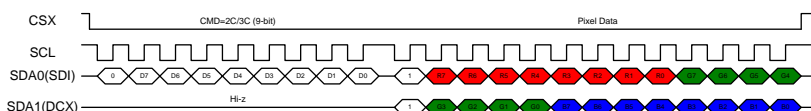
4.2.1.2 Dual SPI

When DSPI_EN is equal to 1 (page 0, C4h_[0]=1), the host sends data by SDA and DCX:

SPI3-1wire RGB888 (IFPF[2:0]=3'b111), DSPI_EN[0]=1'b1, DSPI_CFG[5:4]=2'b00



SPI3-1P1T-2wire, RGB888 (IFPF[2:0]=3'b111), DSPI_EN[0]=1'b1, DSPI_CFG[5:4]=2'b10



SPI3-2P3T-2wire, RGB888 (IFPF[2:0]=3'b111), DSPI_EN[0]=1'b1, DSPI_CFG[5:4]=2'b11

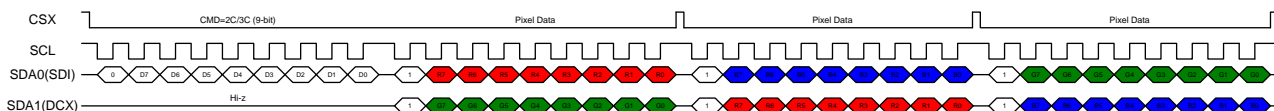
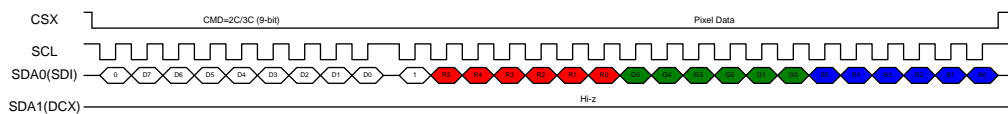
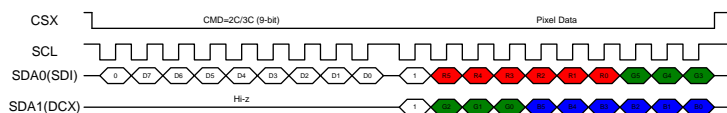


Figure 17. SPI-3 Mode in Dual SPI

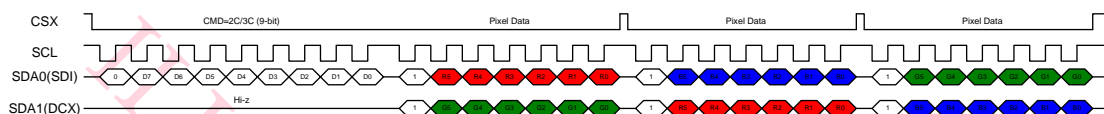
SPI3-1Wire RGB666 (IFPF[2:0]=3'b110), DSPI_EN[0]=1'b1, DSPI_CFG[5:4]=2'b00



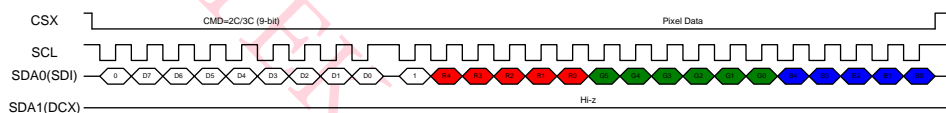
SPI3-1P1T-2wire, RGB666 (IFPF[2:0]=3'b110), DSPI_EN[0]=1'b1, DSPI_CFG[5:4]=2'b10



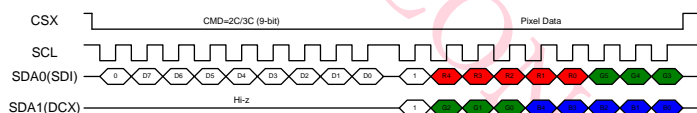
SPI3-2P3T-2wire, RGB666 (IFPF[2:0]=3'b110), DSPI_EN[0]=1'b1, DSPI_CFG[5:4]=2'b11



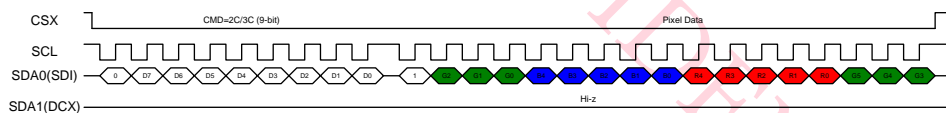
SPI3-1wire RGB565 (IFPF[2:0]=3'b101), DSPI_EN[0]=1'b1, DSPI_CFG[5:4]=2'b00



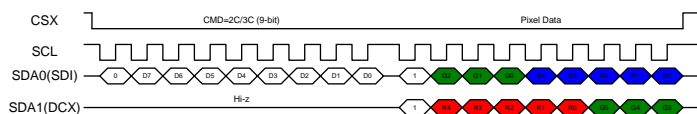
SPI3-1P1T-2wire, RGB565 (IFPF[2:0]=3'b101), DSPI_EN[0]=1'b1, DSPI_CFG[5:4]=2'b10



SPI3-1wire RGB3553 (IFPF[2:0]=3'b101), DSPI_EN[0]=1'b1, DSPI_CFG[5:4]=2'b00, 3553_EN=1



SPI3-1P1T-2wire, RGB3553 (IFPF[2:0]=3'b101), DSPI_EN[0]=1'b1, DSPI_CFG[5:4]=2'b10, 3553_EN=1



SPI3-1wire RGB332 (IFPF[2:0]=3'b010), DSPI_EN[0]=1'b1, DSPI_CFG[5:4]=2'b00

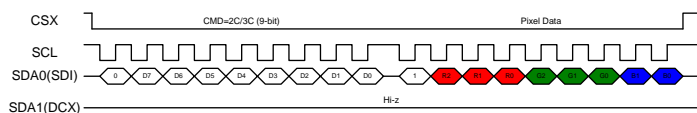
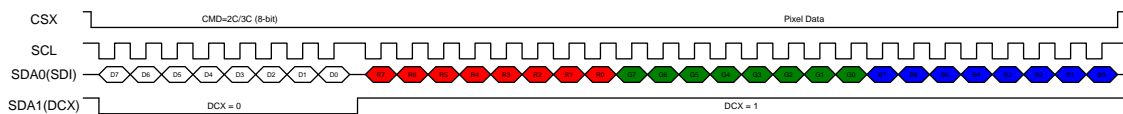
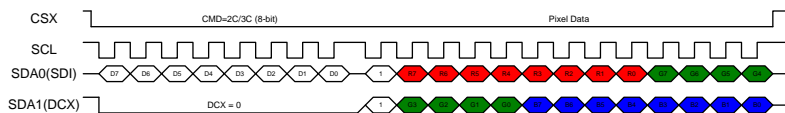


Figure 18. SPI-3 Mode in Dual SPI (continued)

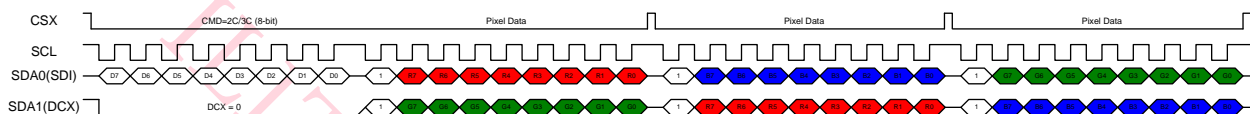
SPI4-1wire RGB888 (IFPF[2:0]=3'b111), DSPI_EN[0]=1'b1, DSPI_CFG[5:4]=2'b00



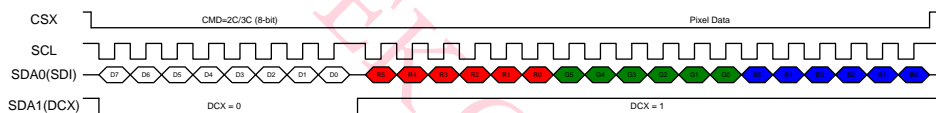
SPI4-1P1T-2wire, RGB888 (IFPF[2:0]=3'b111), DSPI_EN[0]=1'b1, DSPI_CFG[5:4]=2'b10



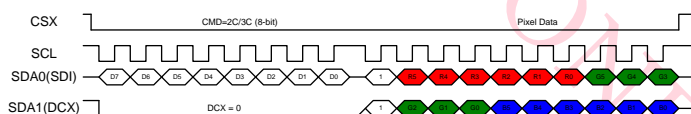
SPI4-2P3T-2wire, RGB888 (IFPF[2:0]=3'b111), DSPI_EN[0]=1'b1, DSPI_CFG[5:4]=2'b11



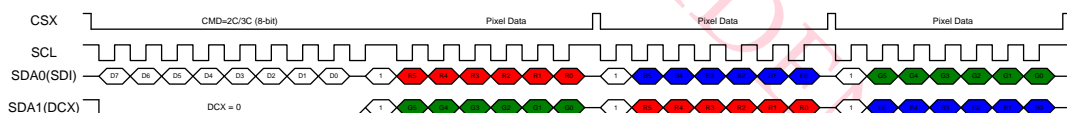
SPI4-1wire RGB666 (IFPF[2:0]=3'b110), DSPI_EN[0]=1'b1, DSPI_CFG[5:4]=2'b00



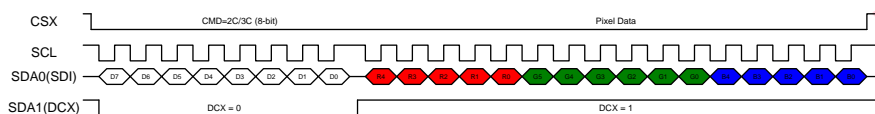
SPI4-1P1T-2wire, RGB666 (IFPF[2:0]=3'b110), DSPI_EN[0]=1'b1, DSPI_CFG[5:4]=2'b10



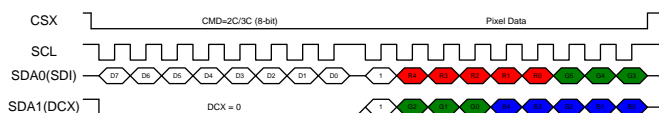
SPI4-2P3T-2wire, RGB666 (IFPF[2:0]=3'b110), DSPI_EN[0]=1'b1, DSPI_CFG[5:4]=2'b11



SPI4-1wire RGB565 (IFPF[2:0]=3'b101), DSPI_EN[0]=1'b1, DSPI_CFG[5:4]=2'b00



SPI4-1P1T-2wire, RGB565 (IFPF[2:0]=3'b101), DSPI_EN[0]=1'b1, DSPI_CFG[5:4]=2'b10



SPI4-1wire RGB3553 (IFPF[2:0]=3'b101), DSPI_EN[0]=1'b1, DSPI_CFG[5:4]=2'b00, 3553_EN=1

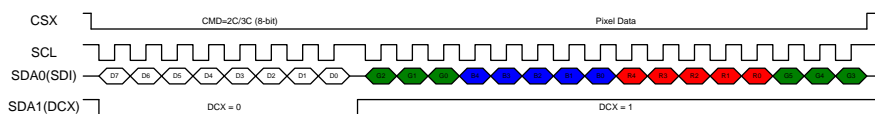
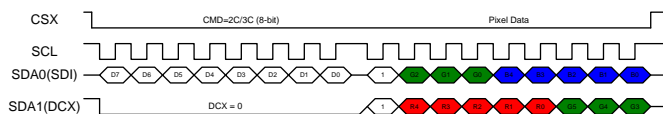


Figure 19. SPI-4 Mode in Dual SPI

SPI4-1P1T-2wire, RGB3553 (IFPF[2:0]=3'b101), DSPI_EN[0]=1'b1, DSPI_CFG[5:4]=2'b10, 3553_EN=1



SPI4-1wire RGB332 (IFPF[2:0]=3'b010), DSPI_EN[0]=1'b1, DSPI_CFG[5:4]=2'b00

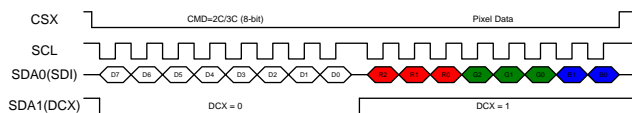


Figure 20. SPI-4 Mode in Dual SPI (continued)

4.2.2 Read Cycle and Sequence

The read mode of interface means that the host reads register's parameter or display data from IL79400A-XX. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. IL79400A-XX latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit.

The host read the n-th parameter of the level 2 command by SPI interface need set additional command RD9h at first. Only the first 8-bit parameter will be read out by the serial interface protocol at a time and it will be necessary set RD9h command again for another ordinal number parameter.

The 3/4-line serial interface reads command sequences described in the figure as below.

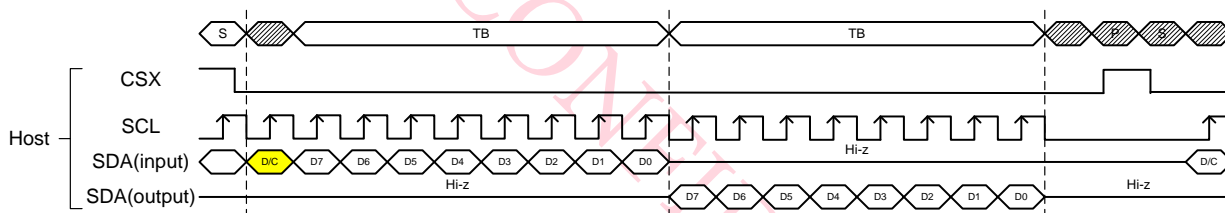


Figure 21. 3-line SPI Interface 8-bit read

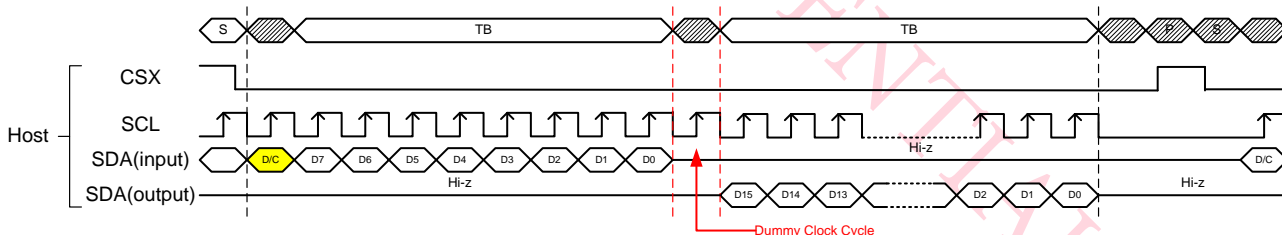


Figure 22. 3-line SPI Interface 16-bit read

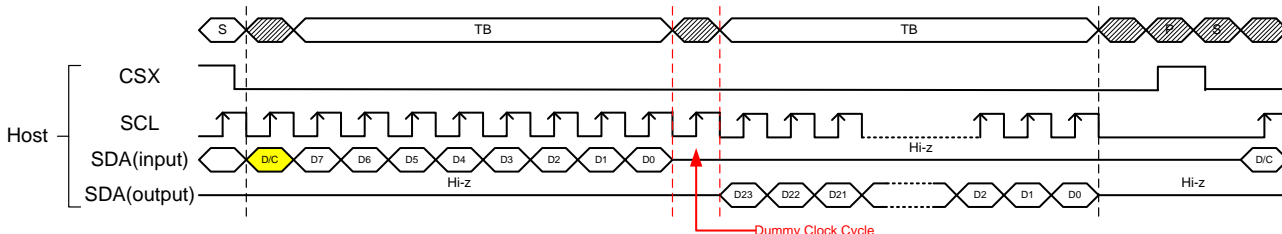


Figure 23. 3-line SPI Interface 24-bit read

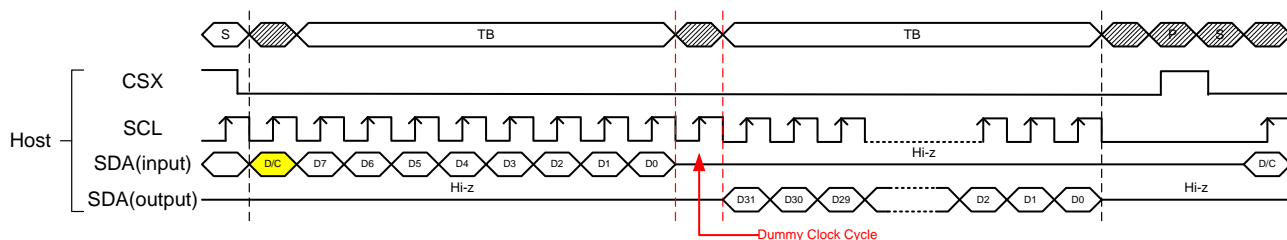


Figure 24. 3-line SPI Interface 32-bit read

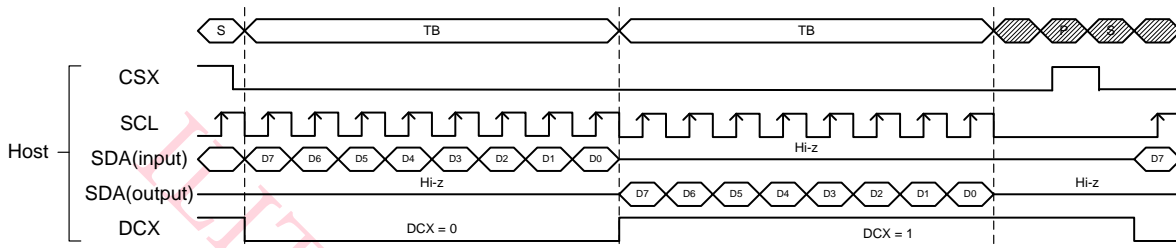


Figure 25. 4-line SPI Interface 8-bit read

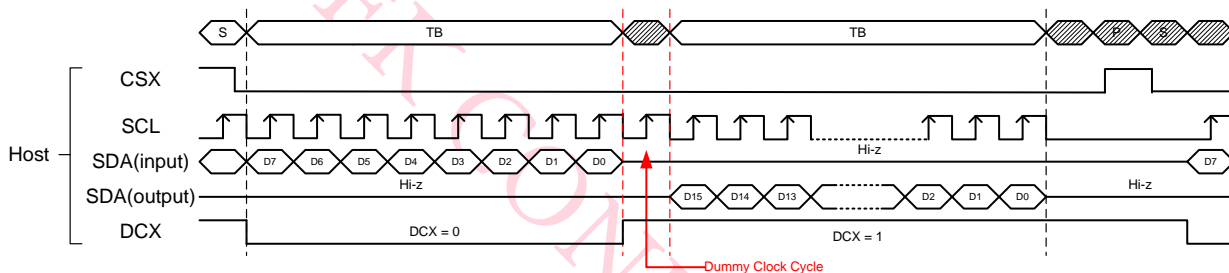


Figure 26. 4-line SPI Interface 16-bit read

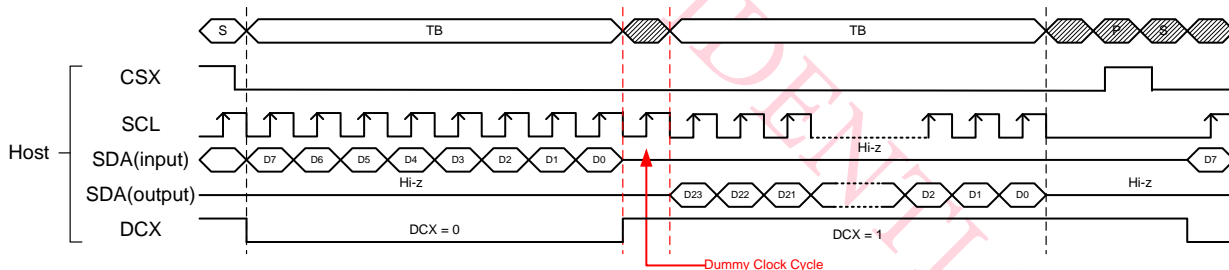


Figure 27. 4-line SPI Interface 24-bit read

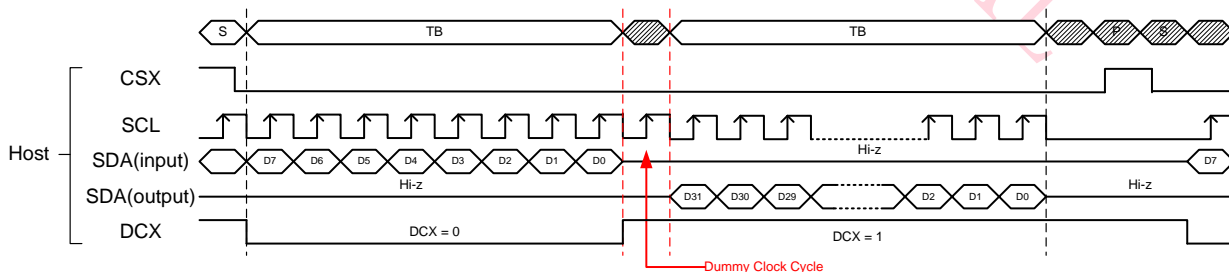


Figure 28. 4-line SPI Interface 32-bit read

4.3 Quad SPI Interface

The IL79400A-XX supports quad SPI interface and consists of the chip enable input (CSX), the serial clock input (SCL) and the serial data (SDA) for 1-wire mode write / read command and write pixel data, and the CSX, SCL, SDA, and data bus D[1:0] for 4-wire mode write pixel data.

4.3.1 White Cycle and Sequence

The quad SPI interface writes command for 1-wire mode sequence described in the figure as below. The head packet is equal to 02h for 1-wire mode command writing. The CMD_ADDR is the command address and is 24bits format, and it has to be set to "8'h00, CMD[7:0], 8'h00". For example, the sleep-out command (Page0, 11h) can be executed by writing head packet = 0x02, CMD_ADDR = 0x001100, and command parameter = 0x00.

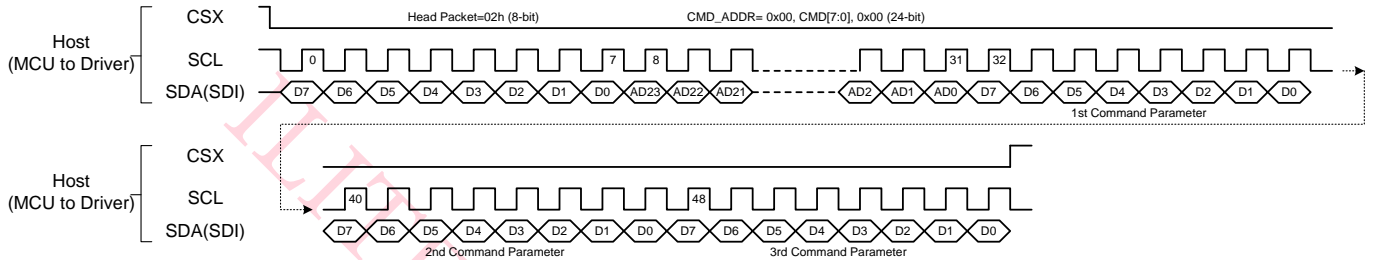


Figure 29. Quad SPI Write sequence

The quad SPI interface writes display data sequences described in the figure as below.

4.3.1.1 1-wire Mode

When the 1-wire mode quad SPI interface is adopted, the host sends data by SDA only. The head packet is equal to 02h for 1-wire mode pixel data writing. The CMD_ADDR is the command address and is 24bits format, and it has to be set to "0x002C00" or "0x003C00".

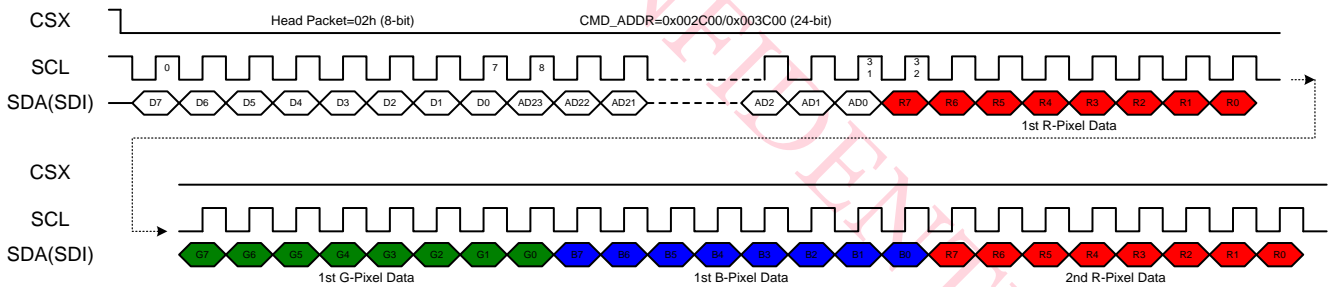


Figure 30. 1-wire RGB888 (IFPF[2:0]=3'b111)

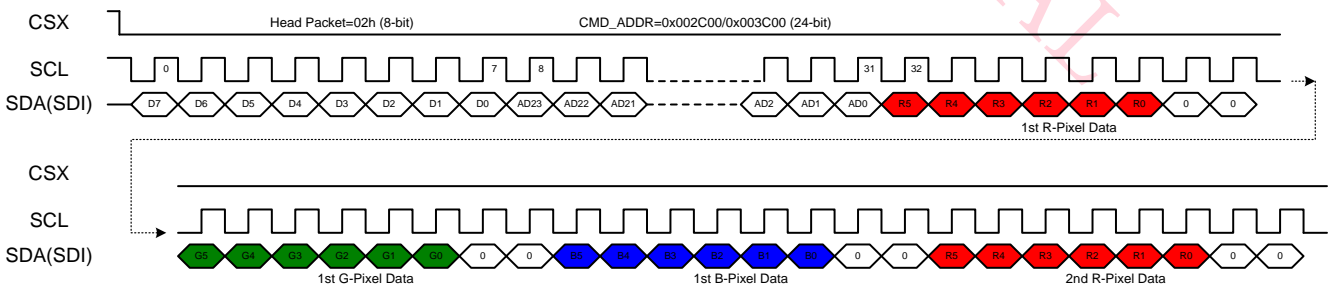


Figure 31. 1-wire RGB666 (IFPF[2:0]=3'b111)

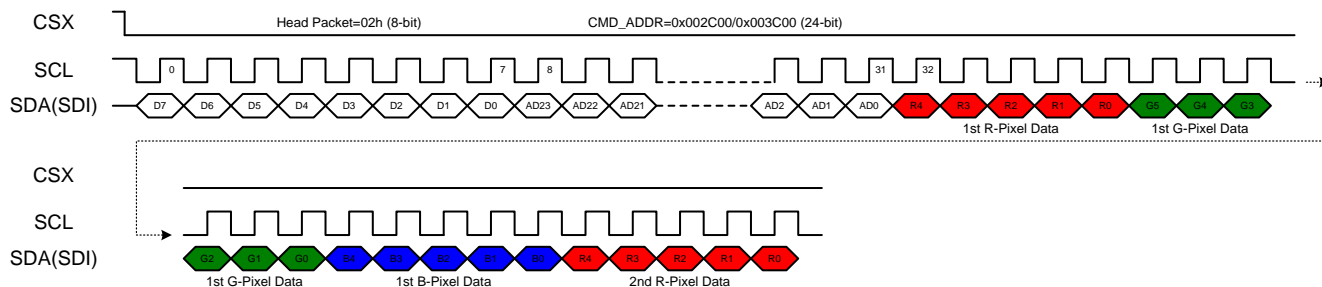


Figure 32. 1-wire RGB565 (IFPF[2:0]=3'b101)

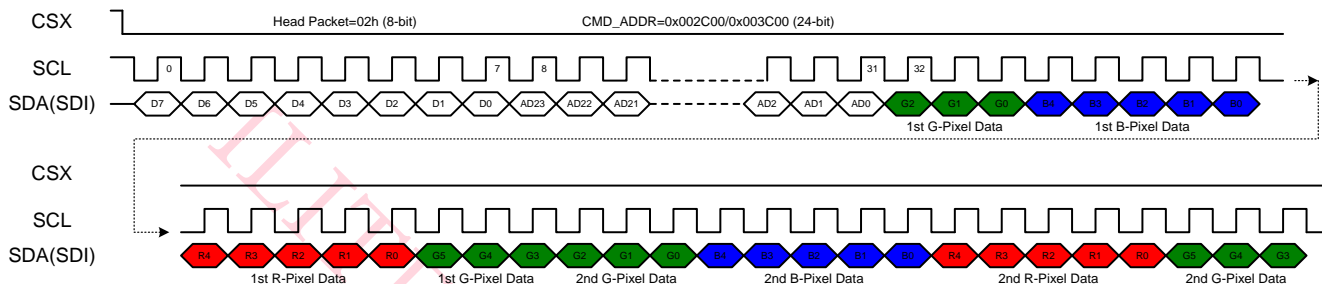


Figure 33. 1-wire RGB3553 (IFPF[2:0]=3'b101), 3553_EN=1

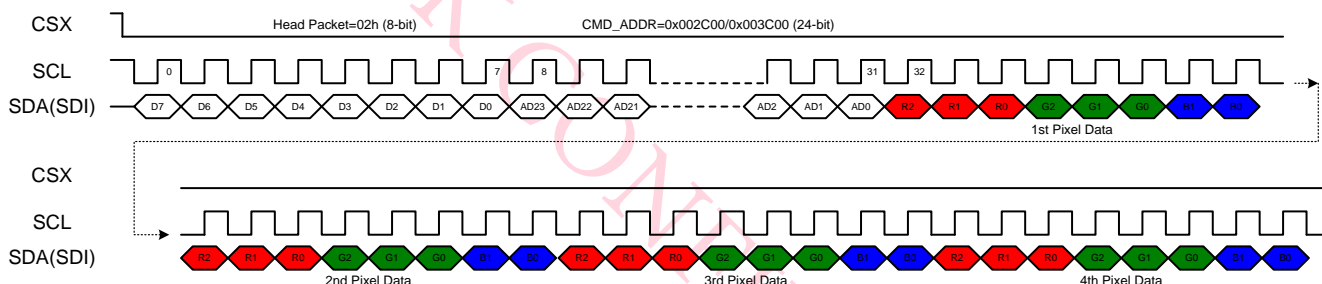


Figure 34. 1-wire RGB332 (IFPF[2:0]=3'b010)

4.3.1.2 4-wire Mode

When the 4-wire mode quad SPI interface is adopted, the host sends data by SDA, DCX, D[0] and D[1]. The head packet is equal to 12h and 32h for 24bits and 8bits command address (CMD_ADDR) writing, respectively.

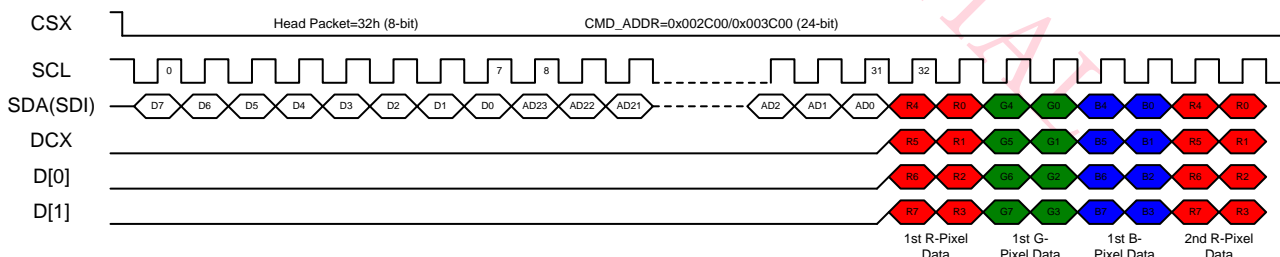


Figure 35. 4-wire RGB888 (IFPF[2:0]=3'b111), ADDR=24bits

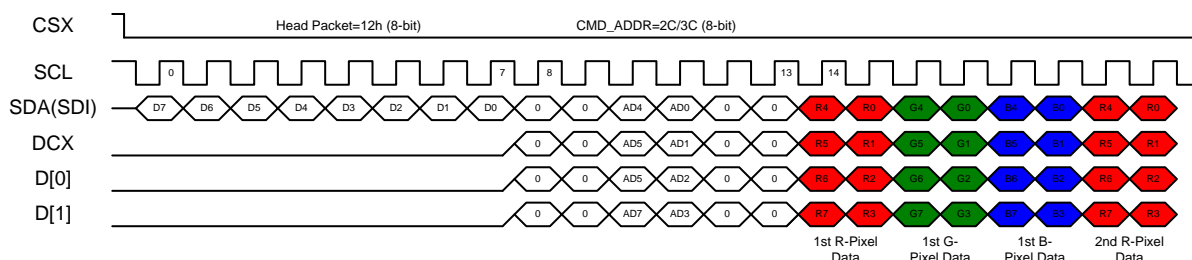


Figure 36. 4-wire RGB888 (IFPF[2:0]=3'b111), ADDR=8bits

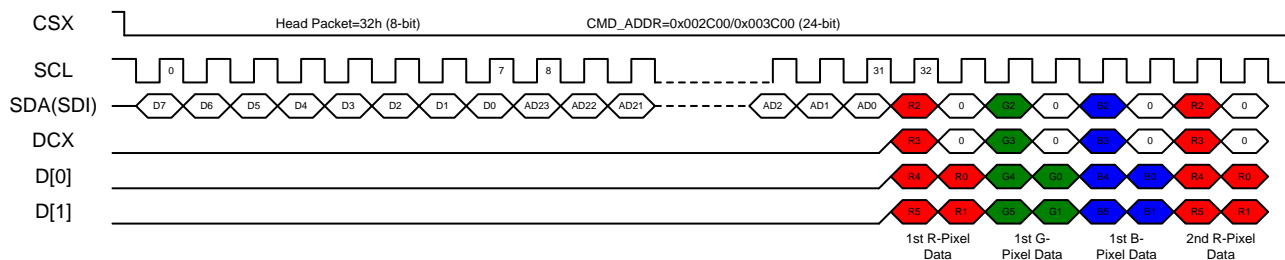


Figure 37. 4-wire RGB666 (IFPF[2:0]=3'b110), ADDR=24bits

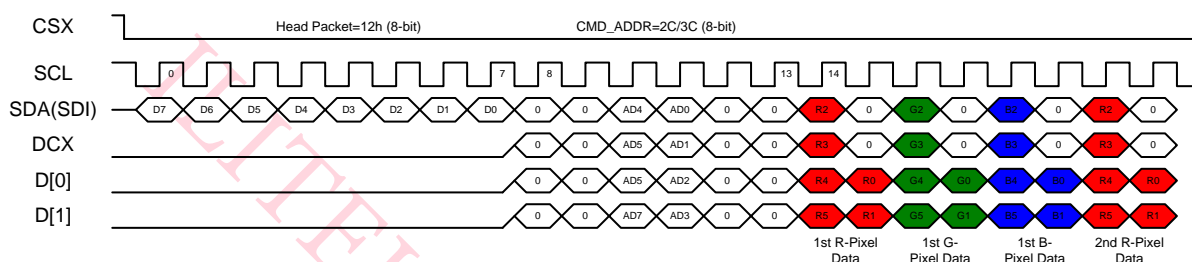


Figure 38. 4-wire RGB666 (IFPF[2:0]=3'b110), ADDR=8bits

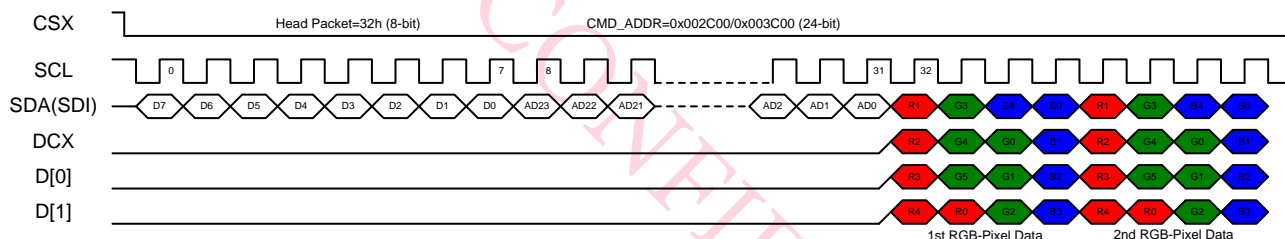


Figure 39. 4-wire RGB565 (IFPF[2:0]=3'b101), ADDR=24bits

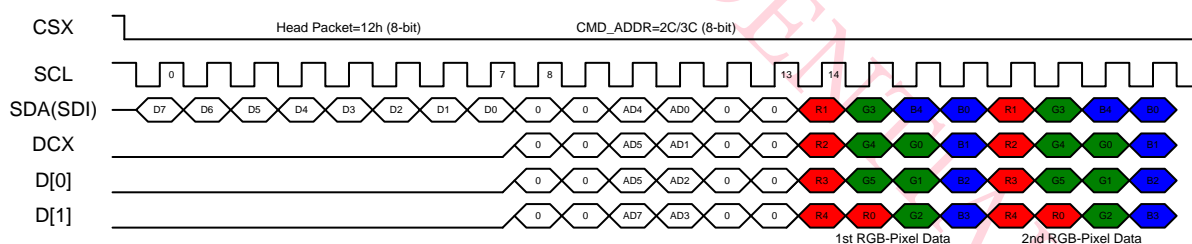


Figure 40. 4-wire RGB565 (IFPF[2:0]=3'b101), ADDR=8bits

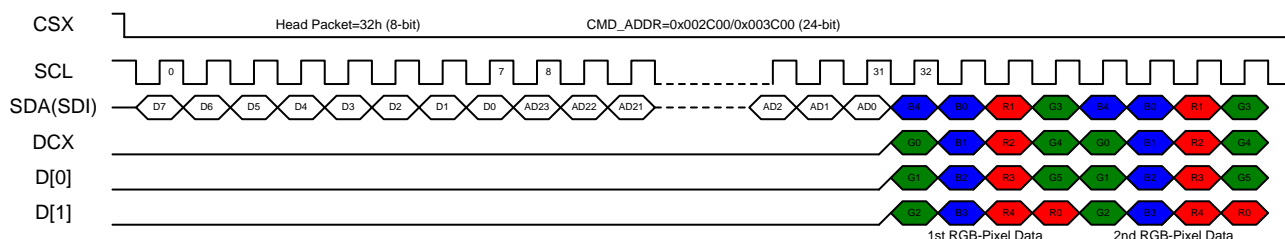


Figure 41. 4-wire RGB3553 (IFPF[2:0]=3'b101), ADDR=24bits, 3553_EN=1

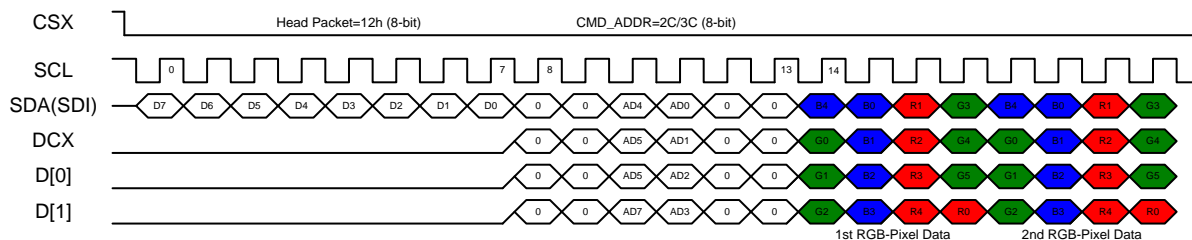


Figure 42. 4-wire RGB3553 (IFPF[2:0]=3'b101), ADDR=8bits, 3553_EN=1

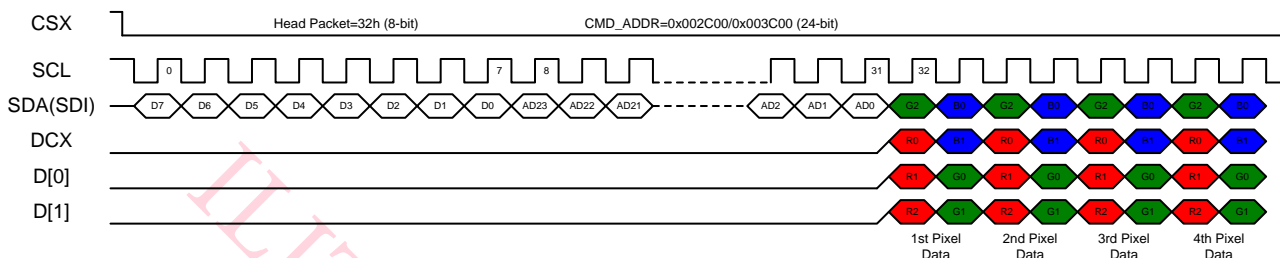


Figure 43. 4-wire RGB332 (IFPF[2:0]=3'b010), ADDR=24bits

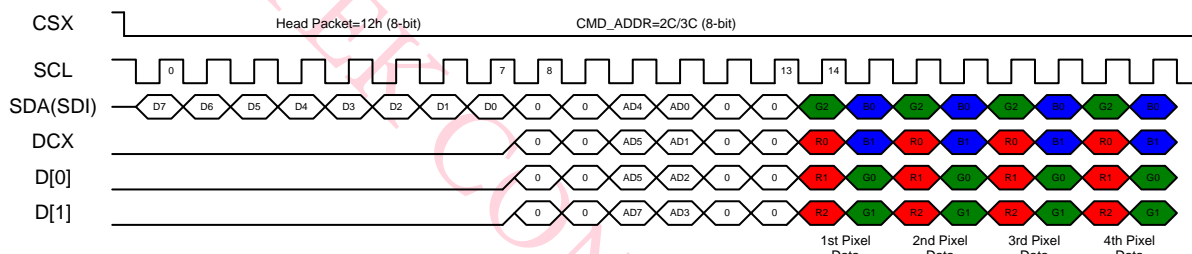


Figure 44. 4-wire RGB332 (IFPF[2:0]=3'b010), ADDR=8bits

4.3.2 Read Cycle and Sequence

The read mode of quad SPI interface means that the host reads register's parameter or display data from IL79400A-XX. The host has to send a head packet (03h) and a 24bits command address (CMD_ADDR), and then the following byte is transmitted in the opposite direction. IL79400A-XX latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The quad SPI interface reads command sequences described in the figure as below.

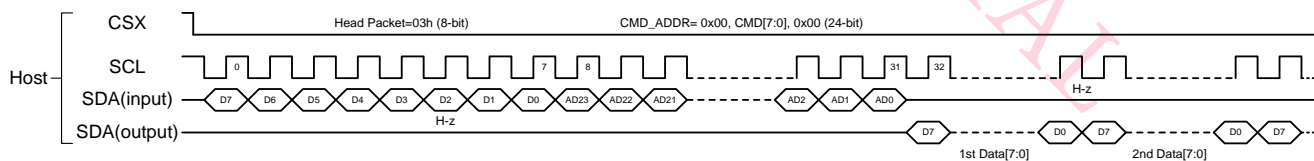


Figure 45. Quad SPI Read Cycle and Sequence

4.4 DSI System Interface

4.4.1 General Description

The MIPI DSI is enabled or disabled, control by external IM[1:0] pin.

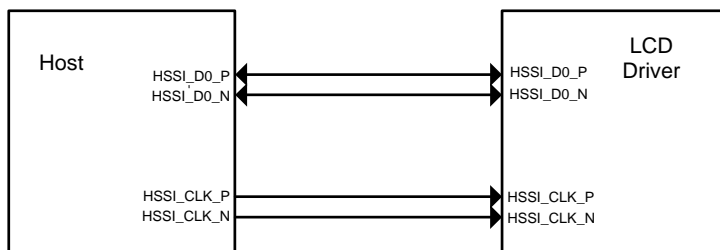


Figure 46. DSI Interface Connection

The IL79400A-XX supports MIPI DSI interface for high-speed serial data transfer. The pad mapping of MIPI DSI interface is set by PSWAP pin, as below table.

Table 12. The configuration of MIPI DSI

PSWAP	HSSI_CLK_P	HSSI_CLK_N	HSSI_D0_P	HSSI_D0_N
0	CLK+	CLK-	D0+	D0-
1	CLK-	CLK+	D0-	D0+

4.4.2 Interface Level Communication

4.4.2.1 General

The display module uses data and clock lane differential pairs for DSI (DSI-2M). Both differential lane pairs can be driven to Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in the single ended mode, a differential receiver is disable (a termination resistor of the receiver is disable), and it can be driven into a low power mode.

High Speed mode means that differential pairs (the termination resistor of the receiver is enable) are not used in the single ended mode.

Different modes and protocols are used in each mode when transferring information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Table 13. High Speed and Low-Power Lane Pair State Codes

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low Power	
	DATA_P	DATA_N	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential – 0	Note1	Note1
HS-1	High (HS)	Low (HS)	Differential – 1	Note1	Note1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS – Request	Mark - 0
LP-10	High (LP)	Low (LP)	Not Defined	LP - Request	Mark - 1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note2

Note:

- Low-Power Receivers (LP-Rx) of the lane pair will check the LP-00 state code when the Lane Pair is in the High Speed (HS) mode.
- If Low-Power Receivers (LP-Rx) of the lane pair recognizes the LP-11 state code, then the lane pair will return to LP-11 of the Control Mode.
- n = 0 (D0 P/N lane only for HS-0 and HS-1)

4.4.2.2 DSI CLK Lanes

CLKP/N lanes can be driven into three different power modes: Low Power Mode (LPM), Ultra-Low Power Mode (ULPM) and High Speed Clock Mode (HSCM). Clock lane are in the single ended mode (LP = Low Power) when entering or leaving Low Power Mode (LPM) or Ultra-Low Power Mode (ULPM). Clock lane is in the single ended mode (LP = Low Power) when entering in or leaving High Speed Clock Mode (HSCM). These entering and leaving protocols use Clock lane in the single ended mode to generate an entering or leaving sequence. The principal flow chart of the different Clock lane power modes is illustrated below.

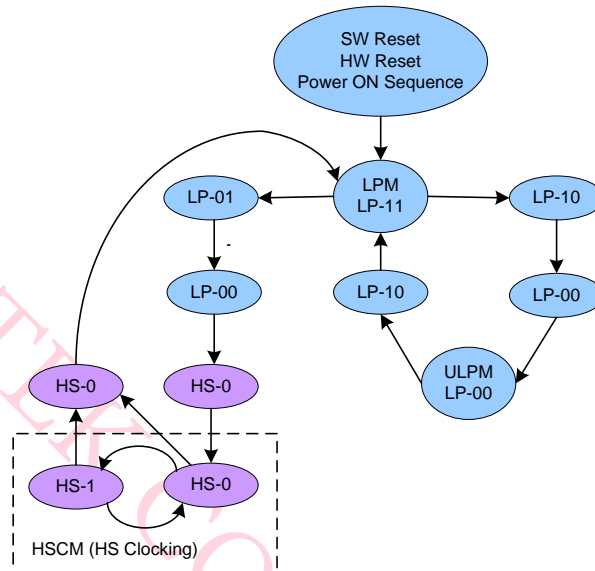


Figure 47. Clock lane Power Modes

4.4.2.2.1 Low Power Mode (LPM)

CLKP/N lanes can be driven to the Low Power Mode (LPM), when CLKP/N lanes enter LP-11 State Code, in three different ways:

- 1) After SW Reset, HW Reset or Power On Sequence => LP-11
- 2) After CLKP/N lanes leave Ultra-Low Power Mode (ULPM, LP-00 State Code) => LP-10 => LP-11 (LPM). This sequence is illustrated below.

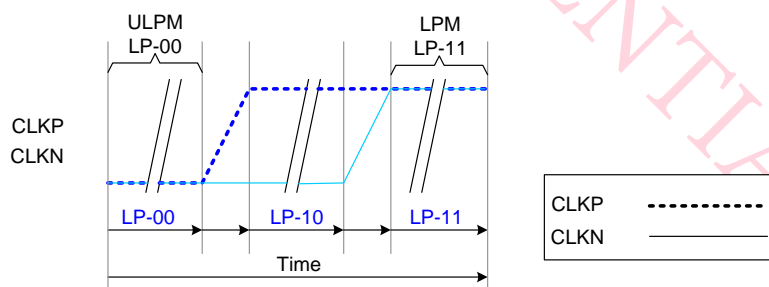


Figure 48. From ULPM to LPM

- 3) After CLKP/N lanes leave High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) => HS-0=> LP-11 (LPM). This sequence is illustrated below.

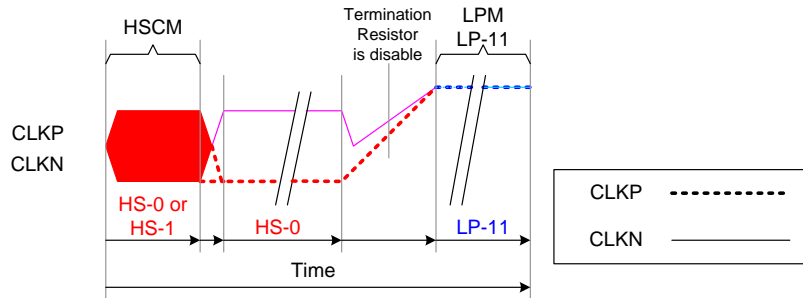


Figure 49. From High Speed Clock Mode (HSCM) to LPM

The changes of all the three modes are illustrated in the flow chart below.

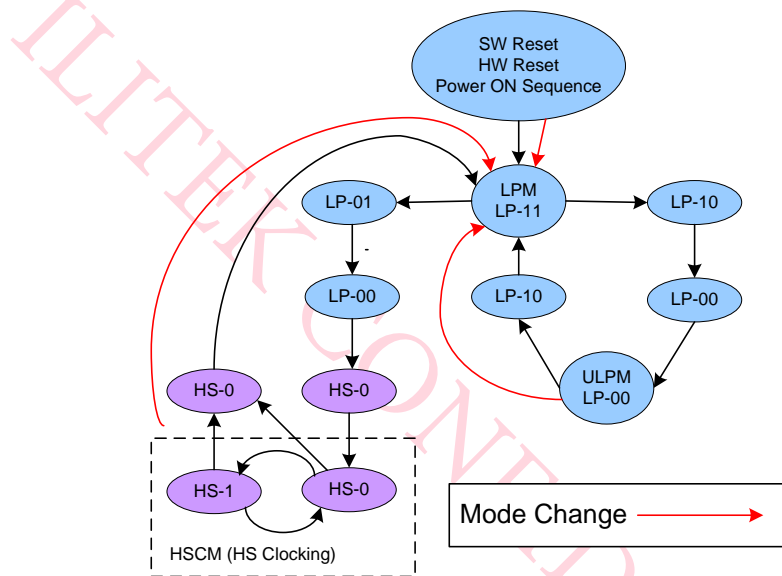


Figure 50. All Three Mode Changes to LPM

4.4.2.2.2 Ultra-Low Power Mode (ULPM)

CLKP/N lanes can be driven to the Ultra-Low power Mode (ULPM) when CLK lanes enter the LP-00 State Code. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) => LP-10 => LP-00 (ULPM). This sequence is illustrated below.

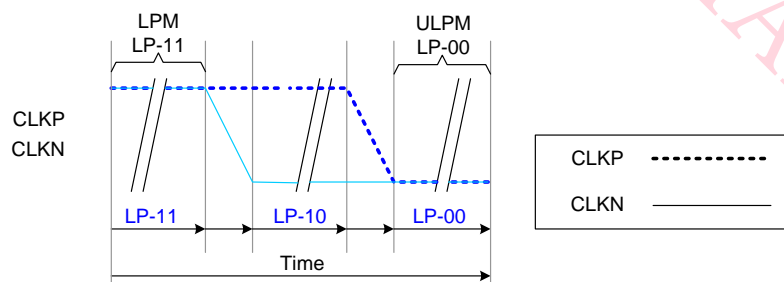


Figure 51. From LPM to ULPM

The mode change is also illustrated below.

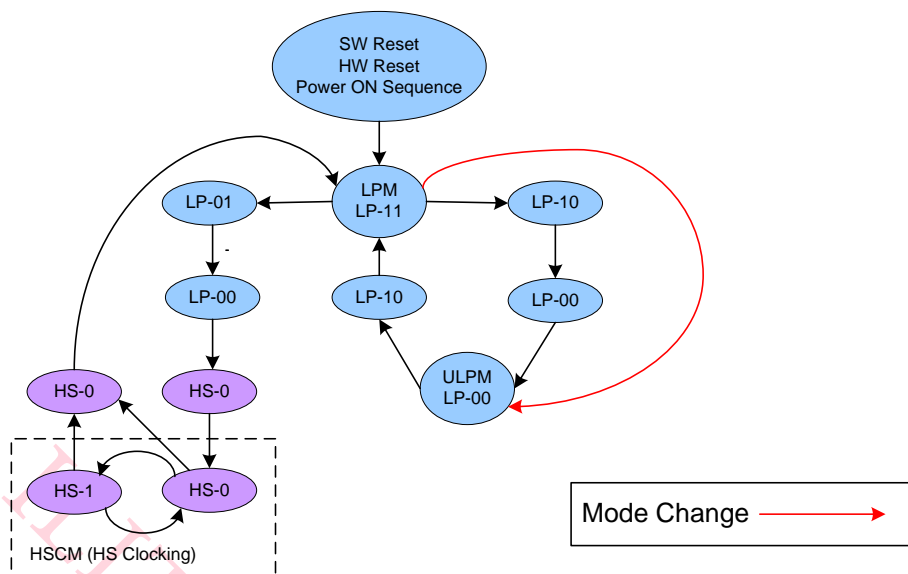


Figure 52. Mode Change from LPM to ULPM

4.4.2.2.3 High-Speed Clock Mode (HSCM)

CLKP/N lanes can be driven to the High Speed Clock Mode (HSCM) when CLK lanes start to function between HS-0 and HS-1 State Codes. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) => LP-01 => LP-00 => HS-0 => HS-0/1 (HSCM). This sequence is illustrated below.

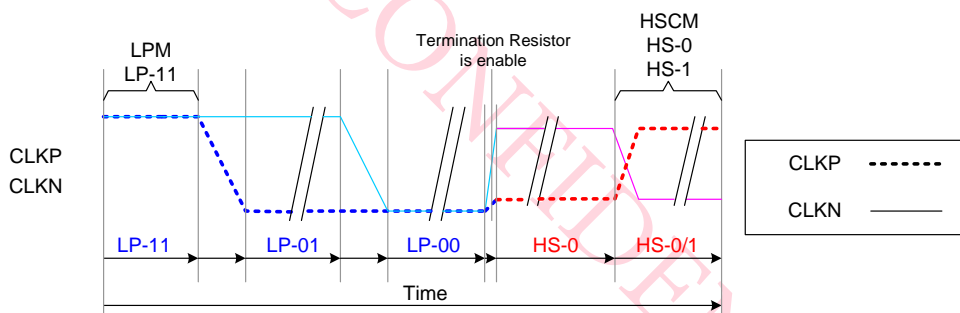


Figure 53. From LPM to HSCM

The mode change is also illustrated below.

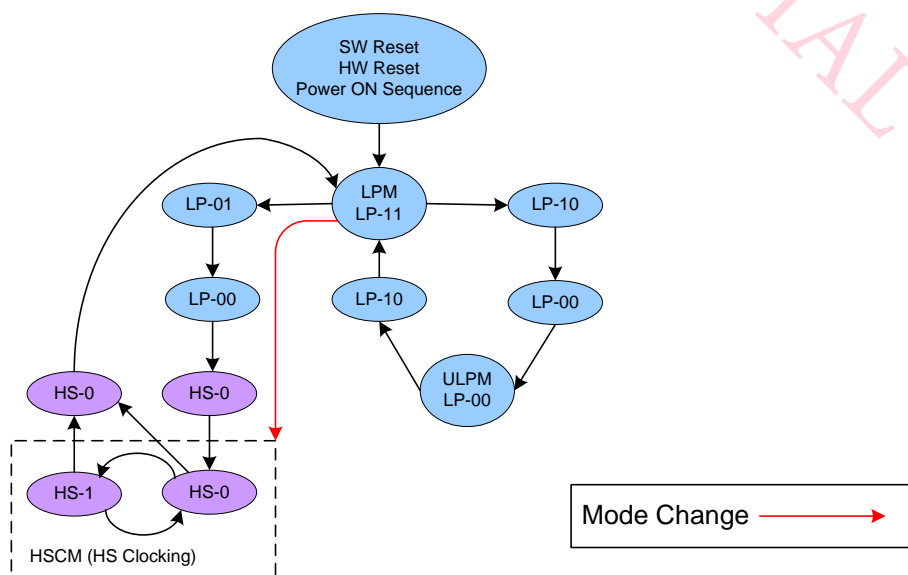


Figure 54. Mode Change from LPM to HSCM

The high speed clock (CLKP/N) starts before high speed data is sent via data lanes. The high speed clock continues clocking after the high speed data sending is stopped.

The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0

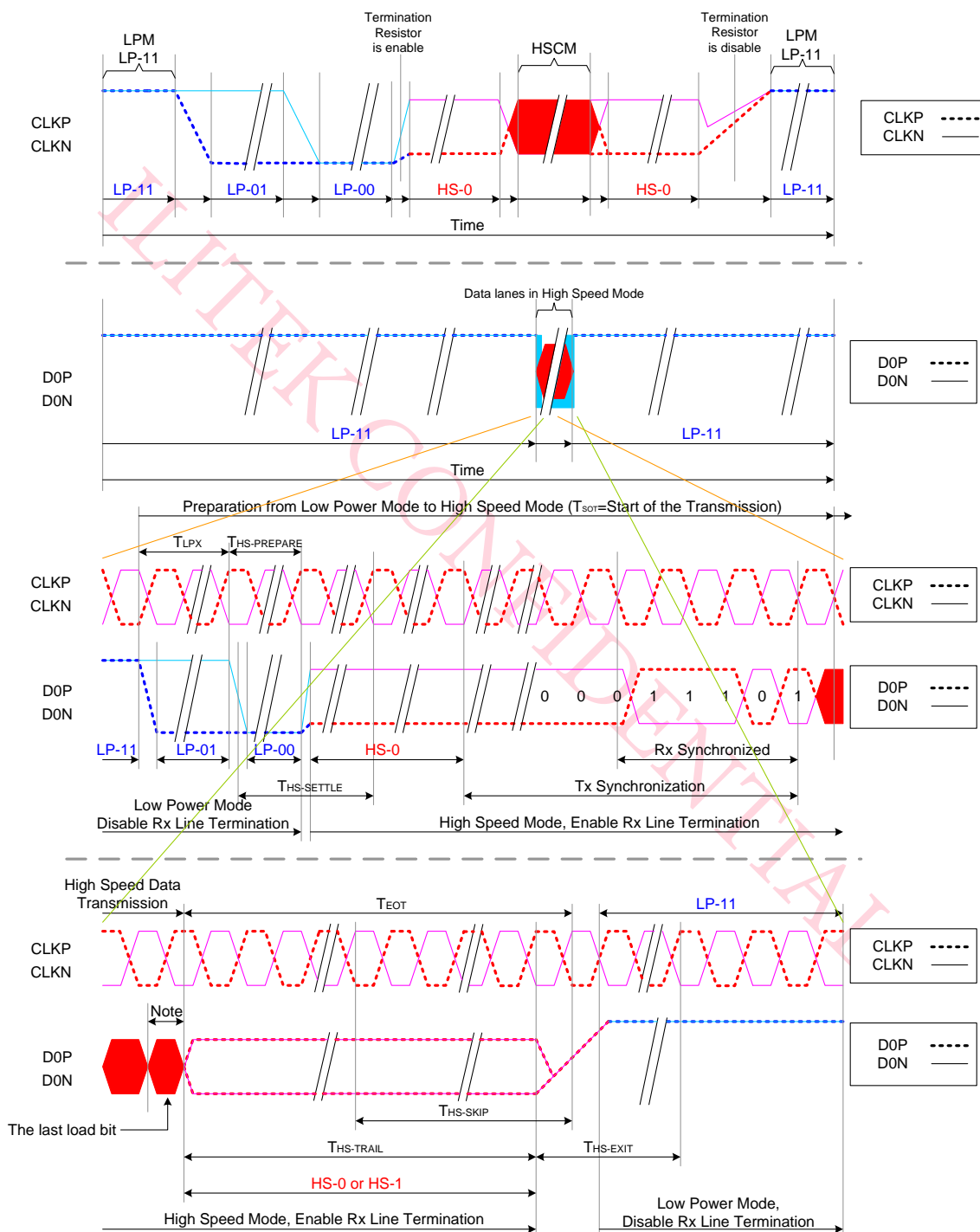


Figure 55. High Speed Clock Burst

Notes:

1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

4.4.2.3 DSI Data Lanes

4.4.2.3.1 General

D0P/N Data Lane can be driven into different modes:

- Escape Mode
- High-Speed Data Transmission
- Bus Turnaround Request

These modes and their entering codes are defined in the following table.

Table 14. Entering and Leaving Sequences

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode1	LP-11 → LP-10 → LP-00 → LP-01 → LP-00	LP-00 → LP-10 → LP-11 (Mark-1)
High-Speed Data Transmission2	LP-11 → LP-01 → LP-00 → HS-0	(HS-0 or HS-1) → LP-11
Bus Turnaround Request3	LP-11 → LP-10 → LP-00 → LP-10 → LP-00	Hi-Z

4.4.2.3.2 Escape Modes

HSSI_D0_P/N data lanes can be used in different Escape Modes when data lanes are in the Low Power (LP) mode. These Escape Modes are used to:

- Send “Low-Power Data Transmission” (LPDT) from the MCU to the display module,
- Drive data lanes to “Ultra-Low Power State” (ULPS),
- Indicate “Remote Application Reset” (RAR), which can reset the display module,
- Indicate “Acknowledge” (ACK), which is used to transmit a non-error event from the display module to the MCU.

The basic sequence of the Escape Mode is as follows:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Escape Command (EC), which is coded, when one of the data lanes changes from low-to-high-to-low then this changed data lane presents the value of the current data bit (D0P = 1, D0N= 0). When DSI-D0 changes from low-to-high-to-low, the receiver will latch a data bit, which value is logical 0. The receiver will use this low-to-high-to-low transition as its internal clock.
- A load if it is needed
- Exit Escape (Mark-1) LP-00 => LP-10 => LP-11
- End: LP-11

This basic construction is illustrated below:

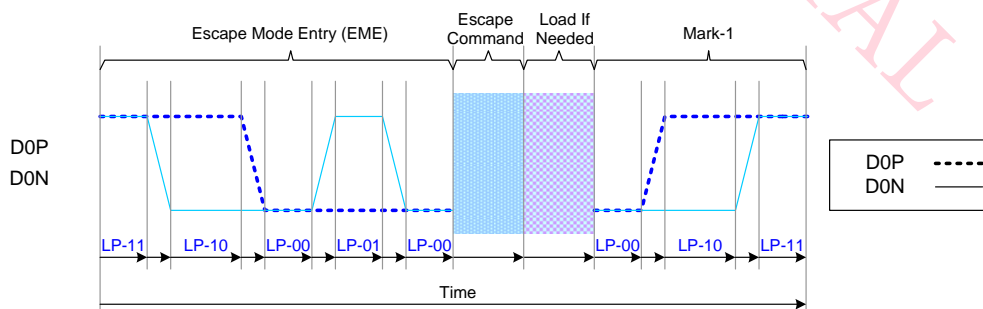


Figure 56. General Escape Mode Sequence

The Escape Commands (EC) are divided into two types: Mode and Trigger, as shown in Table 15. Escape Commands. An example of the Mode type Escape Command is ‘Ultra-Low Power Mode’, where the MCU instructs the display module to enter its Ultra-Low Power Mode.

Escape commands are defined in the following table.

Table 15. Escape Commands

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Escape command	Command Type Mode/Trigger	Entry command Pattern (First Bit → Last Bit Transmitted)	D0
Low-Power Data Transmission	Mode	1110 0001 b	X
Ultra-Low Power Mode	Mode	0001 1110 b	X
Undefined-1, ^{Note 1}	Mode	1001 1111 b	-
Undefined-2, ^{Note 1}	Mode	1101 1110 b	-
Remote Application Reset	Trigger	0110 0010 b	X
Tearing Effect	Trigger	0101 1101 b	-
Acknowledge	Trigger	0010 0001 b	X
Unknown-5, ^{Note 1}	Trigger	1010 0000 b	-

Notes:

1. This Escape command support is not implemented on the display module.

2. X = Supported

3. - = Not Supported

4.4.2.3.2.1 Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in the Low-Power Data Transmission (LPDT) mode when data lanes enter the Escape Mode and Low-Power Data Transmission (LPDT) command is sent to the display module. The display module also uses the same sequence when it sends data to the MCU. The Low Power Data Transmission (LPDT) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Low-Power Data Transmission (LPDT) command in the Escape Mode: 1110 0001 (first to last bit)
- Load (Data):
- One or more bytes (one byte = 8 bit)
- Data lanes are in pause mode when data lanes are stopped (both lanes are low) between bytes
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

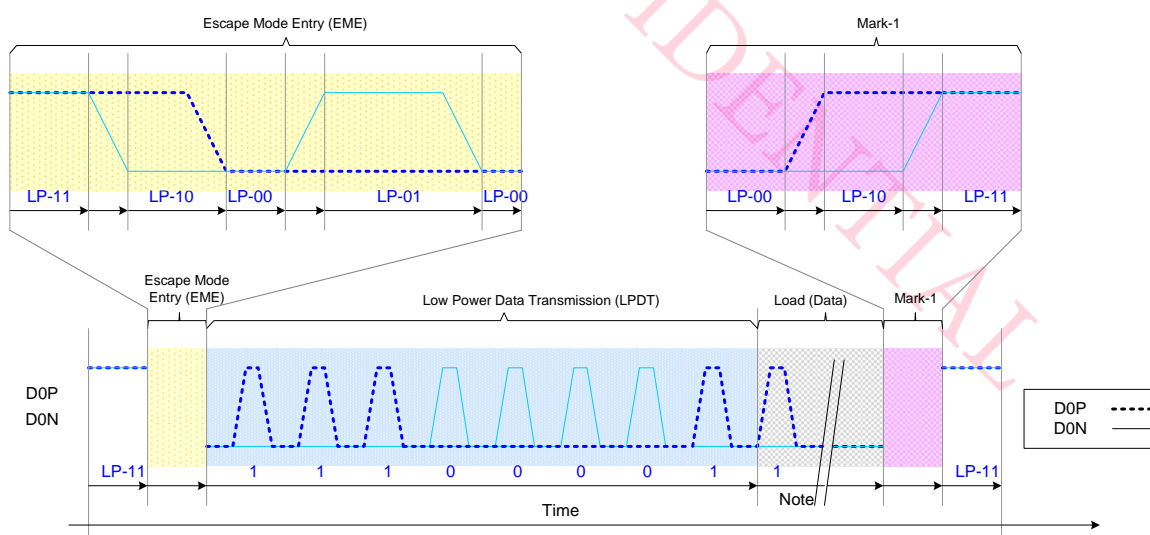


Figure 57. Low-Power Data Transmission (LPDT)

Note:

Load (Data) presents that the first bit is the logical 1 in this example.

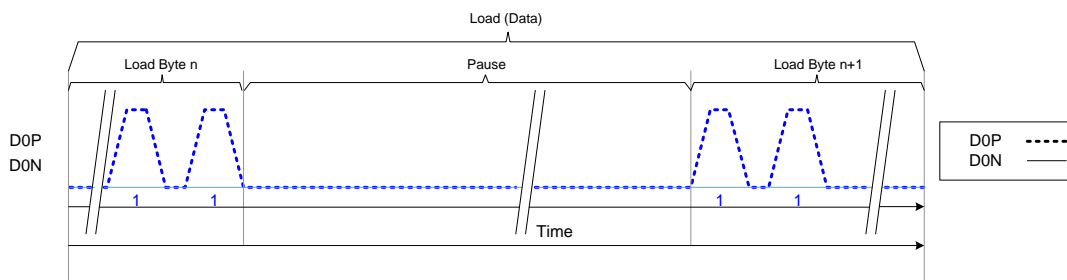


Figure 58. Pause (Example)

4.4.2.3.2.2 Ultra-Low Power State (ULPS)

The MCU can force data lanes get into the Ultra-Low Power State (ULPS) mode when data lanes enter the Escape Mode. The Ultra-Low Power State (ULPS) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Ultra-Low Power State (ULPS) command in the Escape Mode: 0001 1110 (first to last bit)
- Ultra-Low Power State (ULPS) when the MCU keeps data lanes low
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11 (Next command must wait 100us after data lanes leave ULPS)

This sequence is illustrated for reference purposes below:

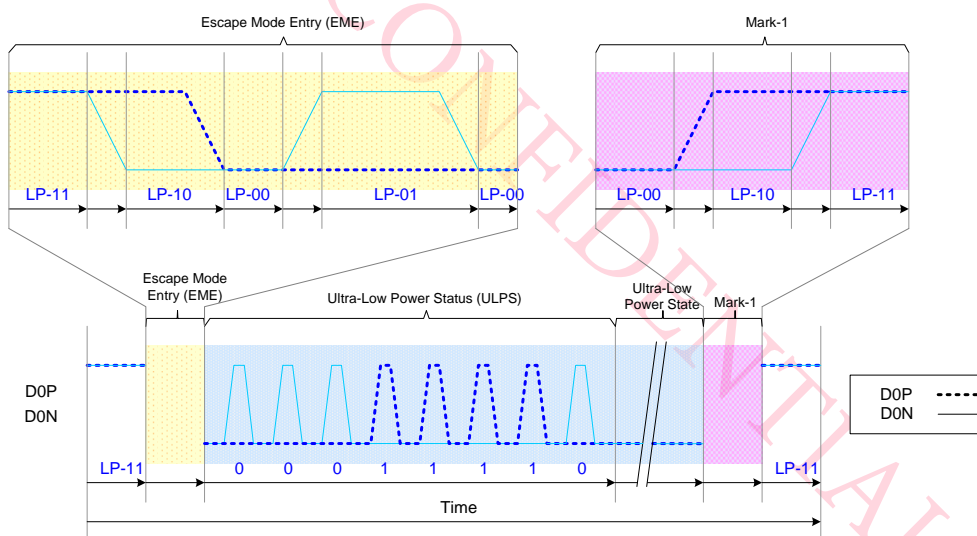


Figure 59. Ultra-Low Power State (ULPS)

4.4.2.3.2.3 Remote Application Reset (RAR)

The MCU can inform the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes enter the Escape Mode. The Remote Application Reset (RAR) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (first to last bit)
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

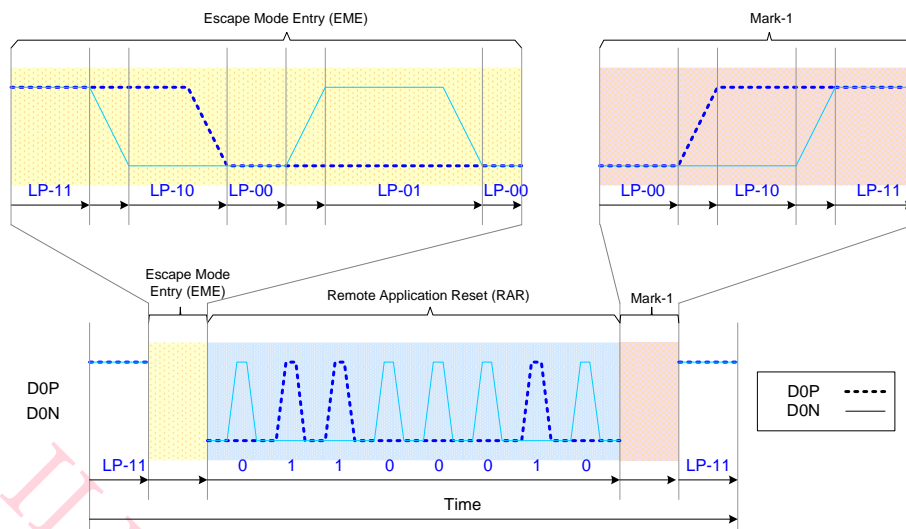


Figure 60. Remote Application Reset (RAR)

4.4.2.3.2.4 Acknowledge (ACK)

The display module can inform the MCU an error is not recognized by Acknowledge (ACK). The display module sends the Acknowledge (ACK) with the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Acknowledge (ACK) command in the Escape Mode: 0010 0001 (first to last bit)
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

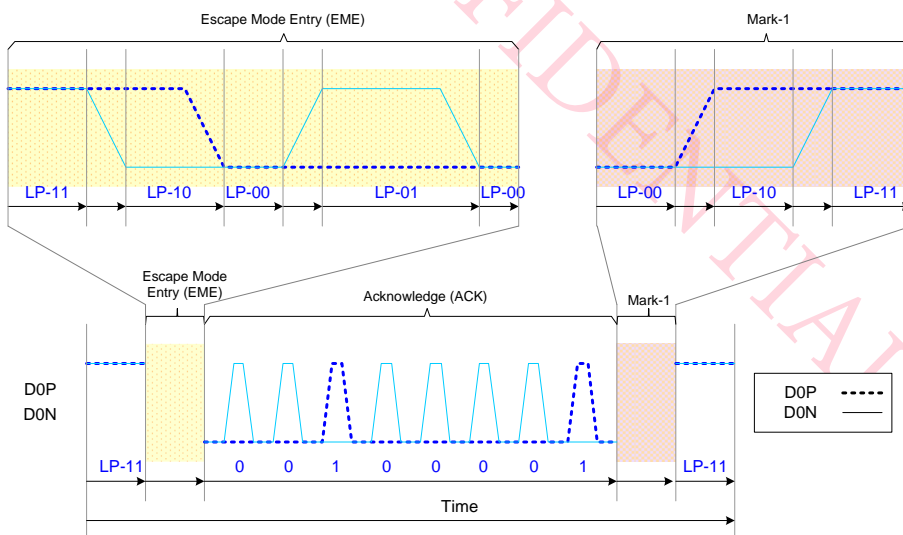


Figure 61. Acknowledge (ACK)

4.4.2.3.3 High-Speed Data Transmission (HSDT)

4.4.2.3.3.1 Entering High-Speed Data Transmission (TSOT of HSDT)

The display module enters High-Speed Data Transmission (HSDT) when Clock lane CLKP/N have already entered the High-Speed Clock Mode (HSCM) by the MCU. See more information in the section “4.4.2.2.3 High-Speed Clock Mode (HSCM)”.

Data lane D0P/N of the display module enter the High-Speed Data Transmission (TSOT of HSDT) as follows:

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

The sequence of entering High-Speed Data Transmission (TSOT of HSDT) is illustrated below:

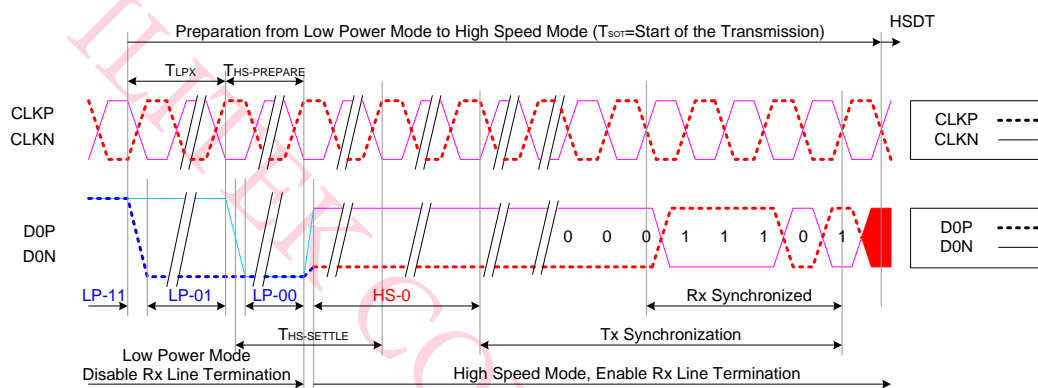


Figure 62. Entering High-Speed Data Transmission (TSOT of HSDT)

4.4.2.3.3.2 Leaving High-Speed Data Transmission (TEOT of HSDT)

The display module leaves the High-Speed Data Transmission (TEOT of HSDT) when Clock lane DSICLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU, and this HSCM is kept until data lane D0P/N are in the LP-11 mode. See more information in the section “4.4.2.2.3 High-Speed Clock Mode (HSCM)”. Data lane D0P/N of the display module leave the High-Speed Data Transmission (TEOT of HSDT) as follows:

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
- MCU changes to HS-1, if the last load bit is HS-0
- MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

The sequence of leaving High-Speed Data Transmission (TEOT of HSDT) is illustrated below:

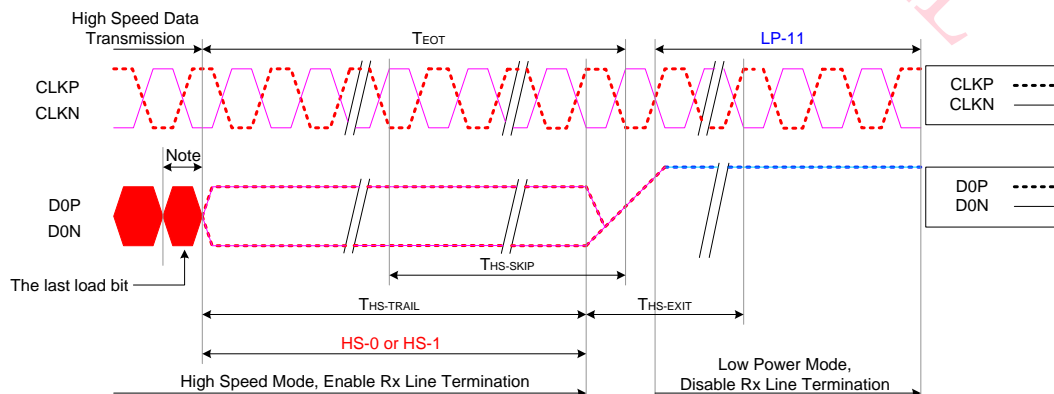


Figure 63. Leaving High-Speed Data Transmission (TEOT of HSDT)

Notes:

1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

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4.4.2.3.3 Burst of the High-Speed Data Transmission (HSDT)

The burst of the “High-Speed Data Transmission” (HSDT) can consist of one or several data packet(s). These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined in the section “4.4.3.1 Short Packet (SPa) and Long Packet (LPa) Structures”. These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

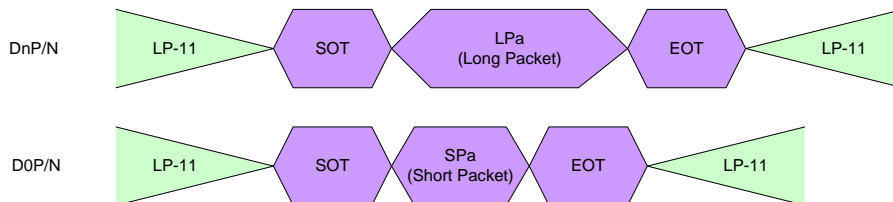


Figure 64. Single Packet in High-Speed Data Transmissions

The multiple packets in High-Speed Data Transmission are illustrated for reference purposes below:

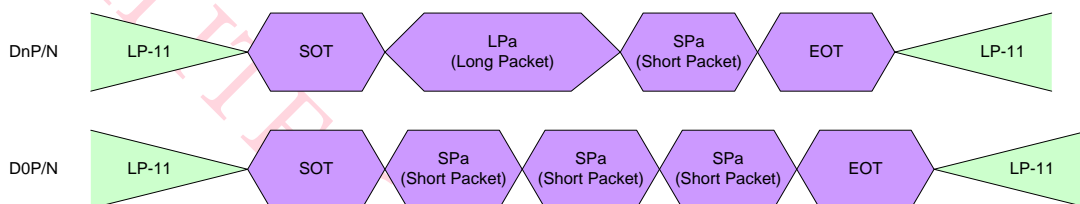


Figure 65. Multiple Packets in High-Speed Data Transmission – Examples

Table 16. Abbreviations

Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Both of Data lanes are '1's (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

4.4.2.3.4 Bus Turnaround (BTA)

The MCU or display module, which controls D0P/N Data Lanes, can start a bus turnaround procedure when it requires information from a receiver, which can be the MCU or display module.

The MCU and display module use the same sequence when this bus turnaround procedure is used. The sequence, when the MCU wants to do the bus turnaround procedure to the display module, is described for reference purposes as follows:

- Start (MCU): LP-11
- Turnaround Request (MCU): LP-11 => LP-10 => LP-00 => LP-10 => LP-00
- The MCU waits until the display module starts to control D0P/N data lanes and the MCU stops to control D0P/N data lanes (= High-Z)
- The display module changes to the stop mode: LP-00 => LP-10 => LP-11

The bus turnaround procedure (from the MCU to the display module) is illustrated below:

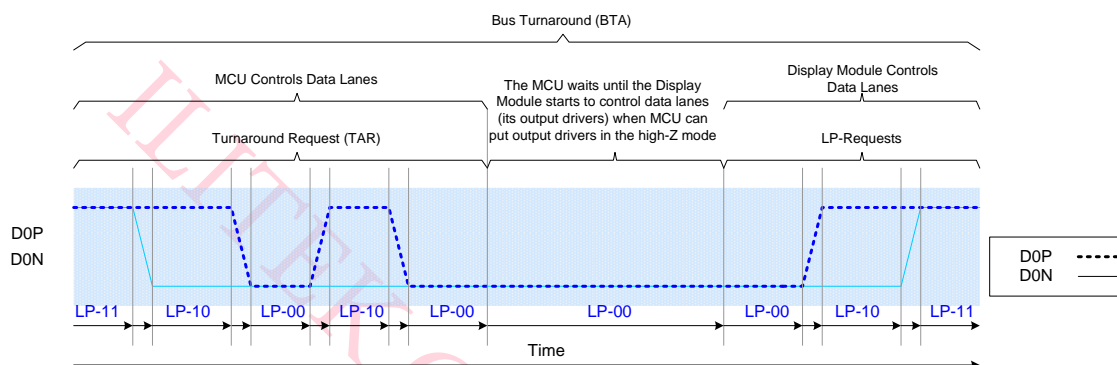


Figure 66. Bus Turnaround Procedure

MCU and display module terms can be switched in Figure 29 if the Bus Turnaround (BTA) is from the display module to the MCU.

4.4.3 Packet Level Communication

4.4.3.1 Short Packet (SPa) and Long Packet (LPa) Structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes. The lengths of the packets are:

- Short Packet (SPa): 4 bytes
- Long Packet (LPa): 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

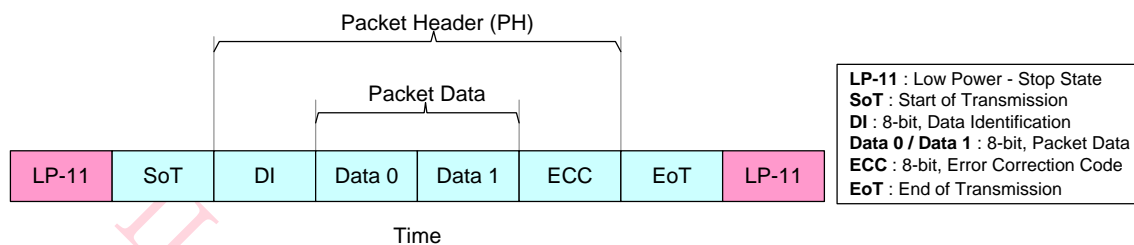


Figure 67. Short Packet (SPa) Structure

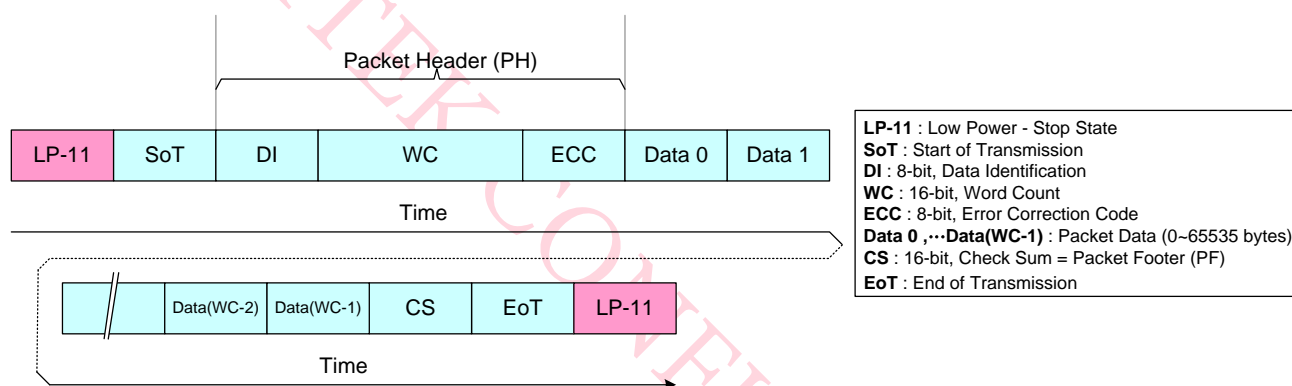


Figure 68. Long Packet (LPa) Structure

- Notes:
- Figure 30 and Figure 31 present a single packet sending (= Includes LP-11, SoT and EoT for each packet sending).
 - The other possibility is that SoT, EoT and LP-11 are not needed between packets if packets are sent in multiple packet format, e.g.
 - LP-11 => SoT => SPa => LPa => SPa => SPa => EoT => LP-11
 - LP-11 => SoT => SPa => SPa => SPa => EoT => LP-11
 - LP-11 => SoT => LPa => LPa => LPa => EoT => LP-11

4.4.3.1.1 Bit Order of the Byte on Packets

The bit order of the byte, what is used in packets, is that the Least Significant Bit (LSB) of the byte is sent first, and the Most Significant Bit (MSB) is sent last. The order is illustrated for reference purposes below.

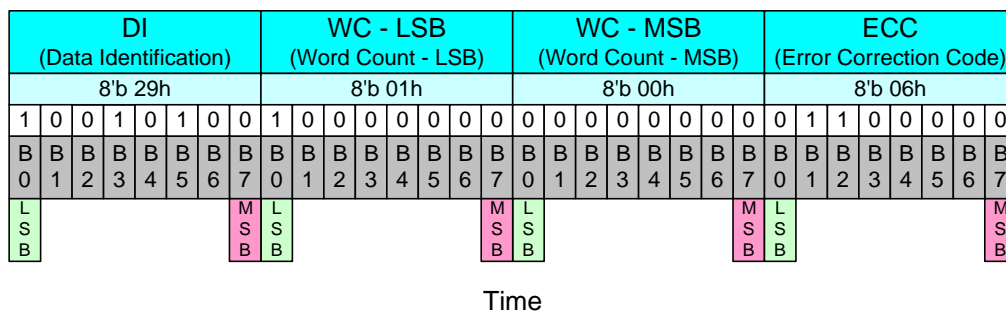


Figure 69. Bit Order of the Byte on Packets

4.4.3.1.2 Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used in packets, is that the Least Significant (LS) Byte of the information is sent first and the Most Significant (MS) Byte is sent last. For example, Word Count (WC) consists of 2 bytes (= 16 bits); while the LS byte is sent first and the MS byte is sent last. The order is illustrated for reference purposes below.

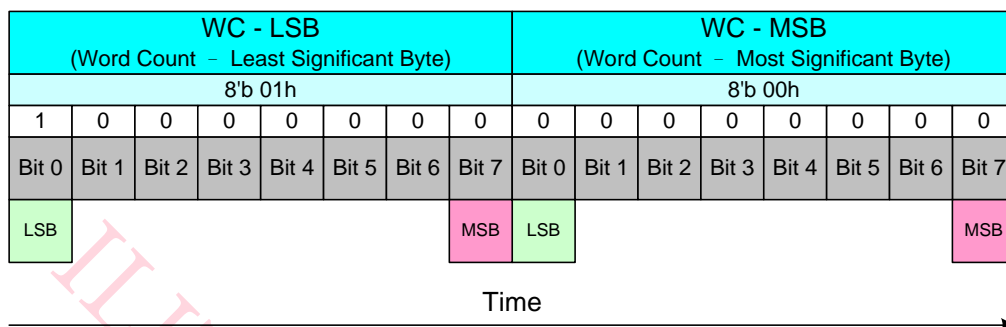


Figure 70. Byte Order of the Multiple Byte Information on Packets

4.4.3.1.3 Packet Header (PH)

The packet header always consists of 4 bytes. The content of these 4 bytes are different for Short Packet (SPa) and Long Packet (LPa).

Short Packet (SPa):

- 1st byte: Data Identification (DI) => Identify that this is a Short Packet (SPa)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
- 4th byte: Error Correction Code (ECC)

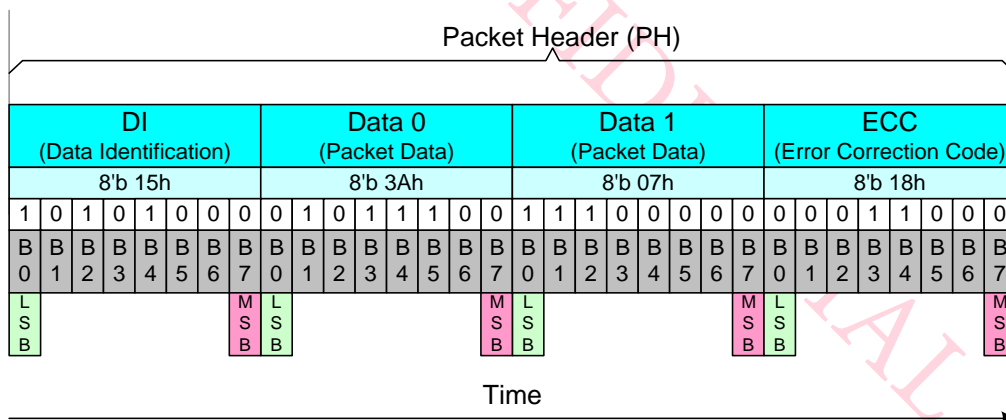


Figure 71. Packet Header (PH) in a Short Packet (SPa)

Long Packet (LPa):

- 1st byte: Data Identification (DI) => Identify that this is a Long Packet (LPa)
- 2nd and 3rd bytes: Word Count (WC)
- 4th byte: Error Correction Code (ECC)

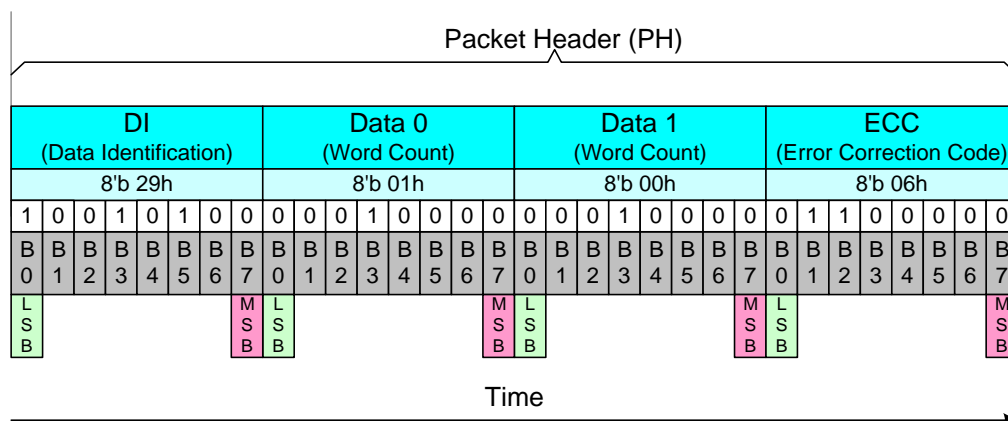


Figure 72. Packet Header (PH) in a Long Packet (LPa)

4.4.3.1.3.1 Data Identification (DI)

Data Identification (DI) is a part of the Packet Header (PH), and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI[7...6]
- Data Type (DT), 6 bits, DI[5...0]

The Data Identification (DI) structure is illustrated, see the figure below.

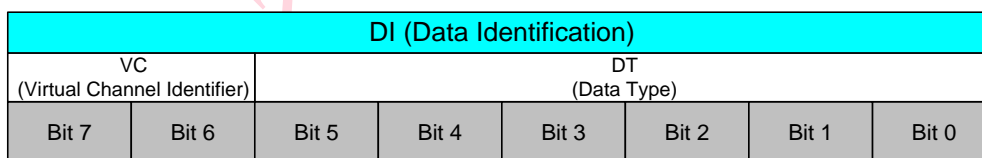


Figure 73. Data Identification (DI) Structure

Data Identification (DI) in the Packet Header (PH) is illustrated for reference purposes below.

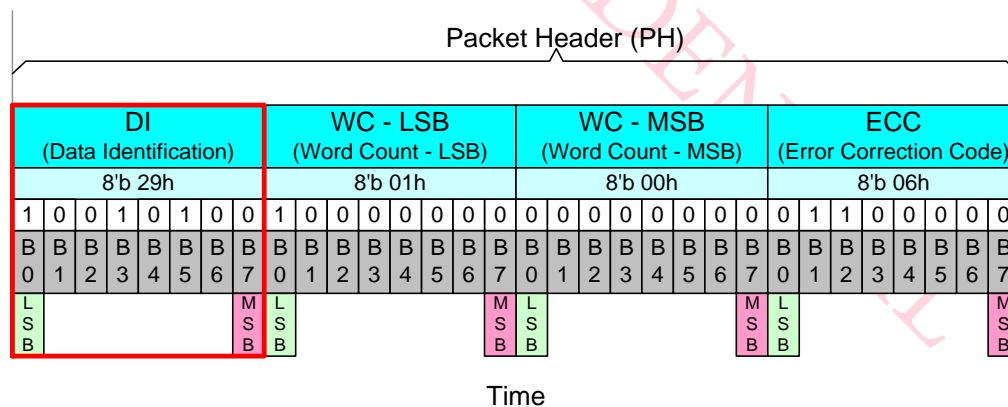


Figure 74. Data Identification (DI) on the Packet Header (PH)

4.4.3.1.3.1.1 Virtual Channel (VC)

Virtual Channel (VC) is a part of Data Identification (DI[7...6]) structure, and it is used to address where a packet is to be sent from the MCU. Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

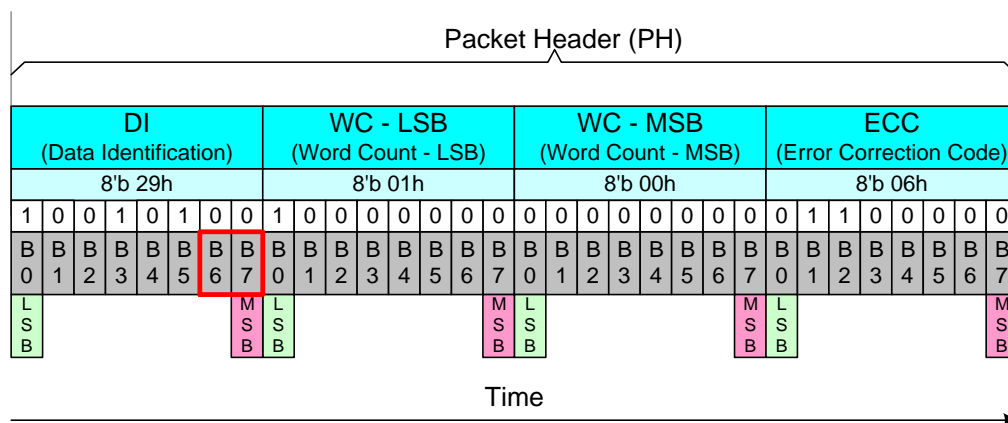


Figure 75. Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can assign 4 different channels for 4 different display modules. Devices will use the same virtual channel as which the MCU uses to send packets to them, e.g.

- The MCU uses the virtual channel 0 when it sends packets to the IL79400A-XX
- The IL79400A-XX also uses the virtual channel 0 when it sends packets to the MCU

This functionality is illustrated below.

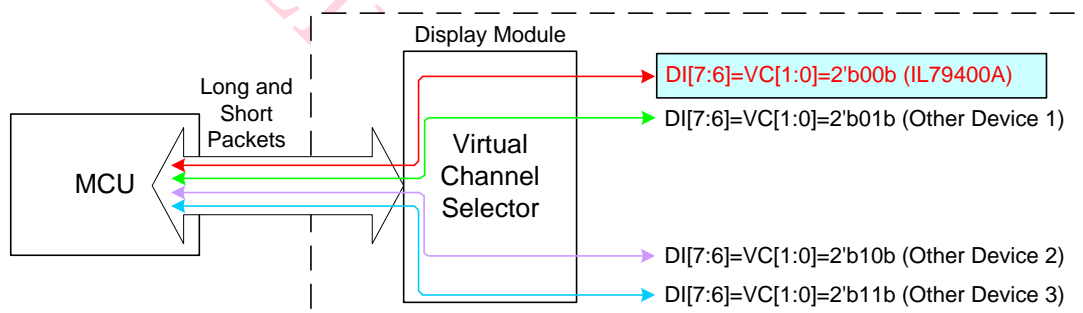


Figure 76. Virtual Channel (VC) Configuration

Virtual Channel (VC) is always 0 (DI[7:6] = VC[1:0] = 00b) when the MCU sends "End of Transmission Packet" to the display module. See the section "4.4.3.2.1.7 End of Transmission Packet (EoTP)".

This display module does not support the virtual channel selector for other devices (1 to 3) when the only possible virtual channel (VC[1..0]) is 00b for the IL79400A-XX.

4.4.3.1.3.1.2 Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5...0]) structure, and it is used to define the type of the used data in a packet. Bits of the Data Type (DT) are illustrated for reference purposes below.

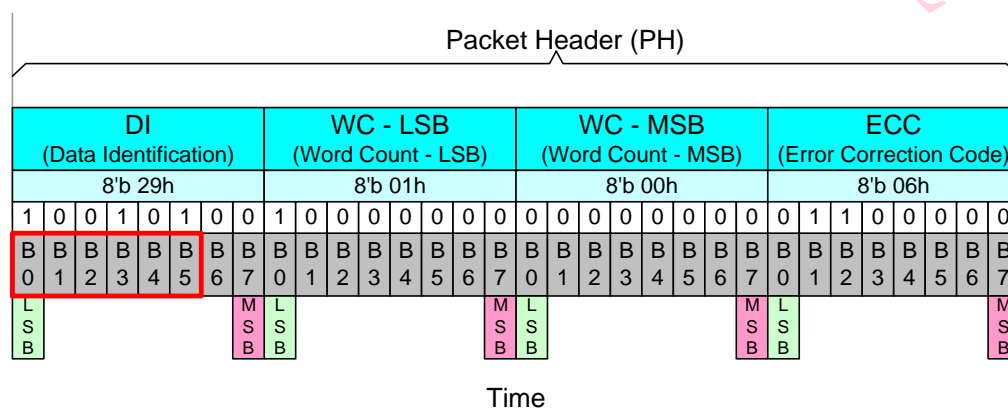


Figure 77. Data Type (DT) on the Packet Header (PH)

This Data Type (DT) also defines the used packet is a Short Packet (SPa) or a Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa. These Data Types (DT) are defined in the tables below.

Table 17. Data Type (DT) from the MCU to the Display Module

From the MCU to the Display Module							Description	Short/Long Packet
Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex		
0	0	0	0	0	1	01h	Sync Event, V Sync Start	SPa (Short Packet)
0	1	0	0	0	1	11h	Sync Event, V Sync End	SPa (Short Packet)
1	0	0	0	0	1	21h	Sync Event, H Sync Start	SPa (Short Packet)
1	1	0	0	0	1	31h	Sync Event, H Sync End	SPa (Short Packet)
0	0	0	1	1	1	07h	Compression Mode Command	SPa (Short Packet)
0	0	1	0	0	0	08h	End of Transmission Packet (EoTP) ^{Note1}	SPa (Short Packet)
0	0	0	0	1	0	02h	Color Mode Off Command	SPa (Short Packet)
0	1	0	0	1	0	12h	Color Mode On Command	SPa (Short Packet)
1	0	0	0	1	0	22h	Shut Down Peripheral Command	SPa (Short Packet)
1	1	0	0	1	0	32h	Turn On Peripheral Command	SPa (Short Packet)
0	0	0	0	1	1	03h	Generic Short WRITE, no parameters	SPa (Short Packet)
0	1	0	0	1	1	13h	Generic Short WRITE, 1 parameters	SPa (Short Packet)
1	0	0	0	1	1	23h	Generic Short WRITE, 2 parameters	SPa (Short Packet)
0	0	0	1	0	0	04h	Generic Short READ, no parameters	SPa (Short Packet)
0	1	0	1	0	0	14h	Generic Short READ, 1 parameters	SPa (Short Packet)
1	0	0	1	0	0	24h	Generic Short READ, 2 parameters	SPa (Short Packet)
0	0	0	1	0	1	05h	DCS Write, No Parameter	SPa (Short Packet)
0	1	0	1	0	1	15h	DCS Write, 1 Parameter	SPa (Short Packet)
0	0	0	1	1	0	06h	DCS Read, No Parameter	SPa (Short Packet)
1	1	0	1	1	1	37h	Set Maximum Return Packet Size	SPa (Short Packet)
0	0	1	0	0	1	09h	Null Packet, No Data, ^{Note2}	LPa (Long Packet)
0	1	1	0	0	1	19h	Blanking Packet, no data	LPa (Long Packet)
1	0	1	0	0	1	29h	Generic Long Write	LPa (Long Packet)
1	1	1	0	0	1	39h	DCS Write Long	LPa (Long Packet)
0	0	1	0	1	0	0Ah	Picture Parameter Set	LPa (Long Packet)
0	0	1	0	1	1	0Bh	Compressed Pixel Stream	LPa (Long Packet)
0	0	1	1	0	1	0Dh	Packed Pixel Stream, 30-bit RGB, 10-10-10 Format	LPa (Long Packet)
0	0	1	1	1	0	0Eh	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	LPa (Long Packet)
0	1	1	1	1	0	1Eh	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	LPa (Long Packet)
1	0	1	1	1	0	2Eh	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	LPa (Long Packet)
1	1	1	1	1	0	3Eh	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	LPa (Long Packet)
x	x	0	0	0	0	x0h	DO NOT USE	
x	x	1	1	1	1	xFh	All unspecified codes are reserved	

Notes:

1. This can be used when the MCU wants to make sure that it is the end of the transmission in High Speed Data Transferring (HSDT) mode.
2. This can be used when data lanes are to be kept in High Speed Data Transferring (HSDT) Mode.

Table 18. Data Type (DT) from the Display Module to the MCU

From the Display Module to the MCU							Description	Short/Long Packet
Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex		
0	0	0	0	1	0	02h	Acknowledge with Error Report	SPa (Short Packet)
0	0	1	0	0	0	08h	End of Transmission Packet (EoTP)	SPa (Short Packet)
0	1	0	0	0	1	11h	Generic Short READ Response, 1 byte returned	SPa (Short Packet)
0	1	0	0	1	0	12h	Generic Short READ Response, 2 byte returned	SPa (Short Packet)
0	1	1	0	1	0	1Ah	Generic Long READ Response	LPa (Long Packet)
0	1	1	1	0	0	1Ch	DCS Read Long Response	LPa (Long Packet)
1	0	0	0	0	1	21h	DCS Read Short Response, 1 byte returned	SPa (Short Packet)
1	0	0	0	1	0	22h	DCS Read Short Response, 2 byte returned	SPa (Short Packet)

Note:

The receiver will ignore other Data Types (DT) if they are not defined in Table 17 and Table 18.

4.4.3.1.3.2 Packet Data (PD) in a Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is placed after Data Type (DT) of the Data Identification (DI) and indicates a Short Packet (SPa) is to be sent. Packet Data (PD) of a Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1. The sending order of the Packet Data (PD) is that Data 0 is sent first and the Data 1 is sent last. Bits of Data 1 are set to 0 if the information length is 1 byte. Packet Data (PD) of a Short Packet (SPa), when the length of the information is 1 or 2 bytes and Virtual Channel (VC) is 0, are illustrated for reference purposes below.

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Packet Data (PD) information:

- Data 0: 26h (Display Command Set (DCS) with 1 Parameter => DI (Data Type (DT)) = 15h)
- Data 1: 01h (DCS's parameter)

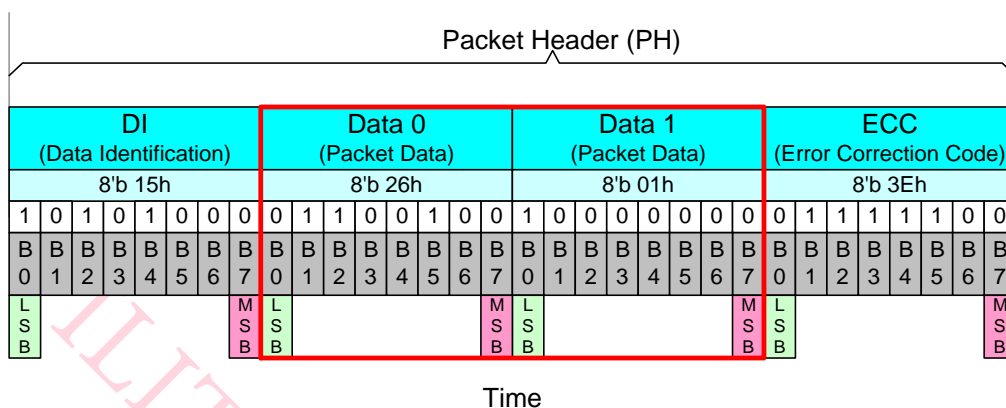


Figure 78. Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

Packet Data (PD) information:

- Data 0: 10h (DCS without parameter => DI (Data Type (DT)) = 05h)
- Data 1: 00h (Null)

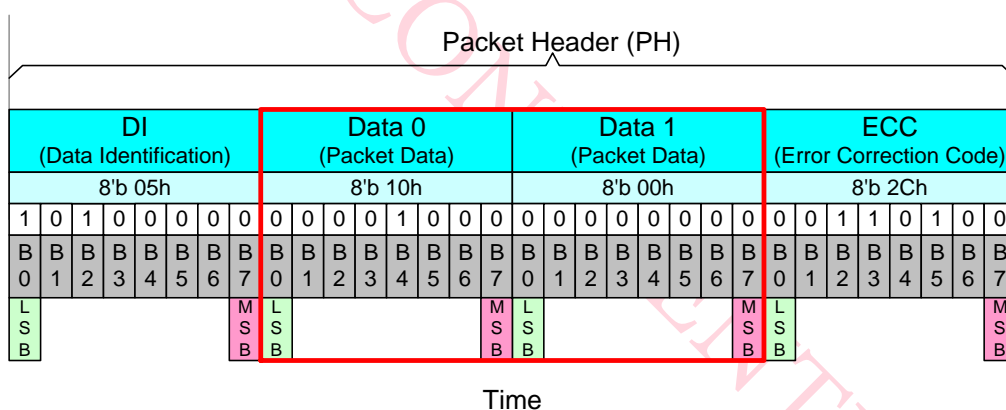


Figure 79. Packet Data (PD) for Short Packet (SPa), 1 Byte Information

4.4.3.1.3.3 Word Count (WC) in a Long Packet (LPa)

Word Count (WC) of the Long Packet (LPa) is placed after Data Type (DT) of the Data Identification (DI) and indicates that a Long Packet (LPa) is to be sent. Word Count (WC) indicates the amount of data bytes of the Packet Data (PD) that is to be sent after the Packet Header (PH). The location of the Word Count (WC) in a Long Packet is the same as which of the Packet Data (PD) in a Short Packet (SPa), as shown in Figure 44. Word Count (WC) of the Long Packet (LPa) consists of 2 bytes. The sending order of these 2 bytes of the Word Count (WC) is that the Least Significant (LS) Byte is sent first, and the Most Significant (MS) Byte is sent last. Word Count (WC) of a Long Packet (LPa) is illustrated for reference purposes below.

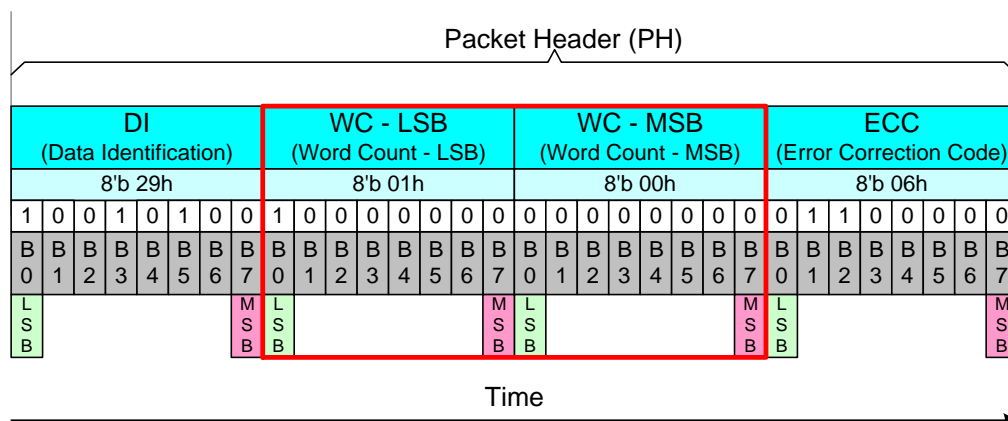


Figure 80. Word Count (WC) in a Long Packet (LPa)

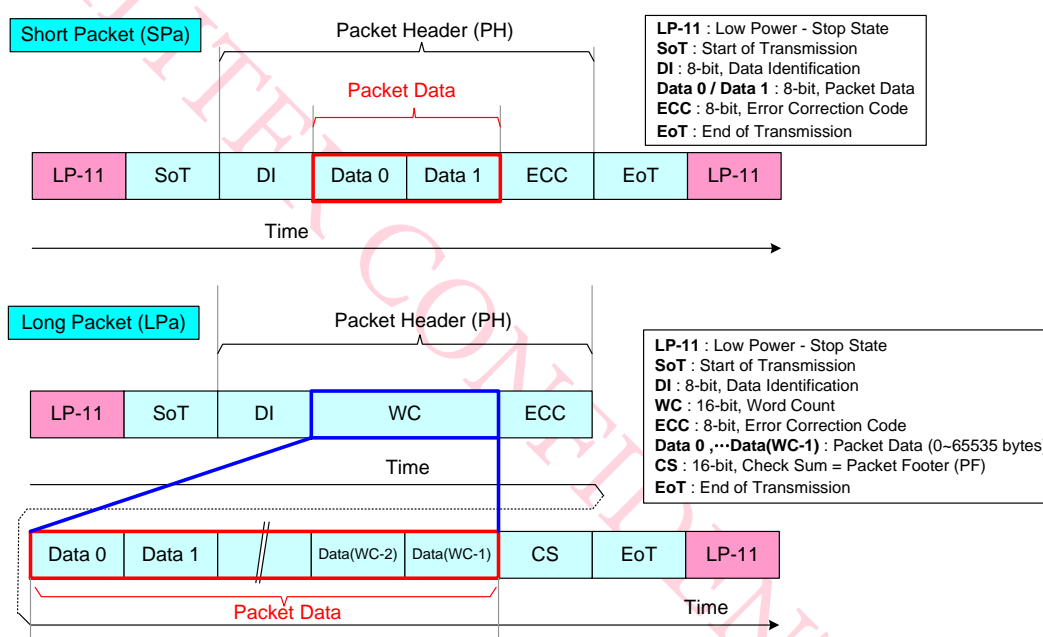


Figure 81. Packet Data in Short and Long Packets

4.4.3.1.3.4 Error Correction Code (ECC)

The Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors. The ECC protects the following fields:

- Short Packet (SPa): Data Identification (DI) byte (8 bits: D[0...7]), Packet Data (PD) bytes (16 bits: D[8...23]) and ECC (8 bits: P[0...7])
- Long Packet (LPa): Data Identification (DI) byte (8 bits: D[0...7]), Word Count (WC) bytes (16 bits: D[8...23]) and ECC (8 bits: P[0...7])

D[23...0] and P[7...0] are illustrated for reference purposes below.

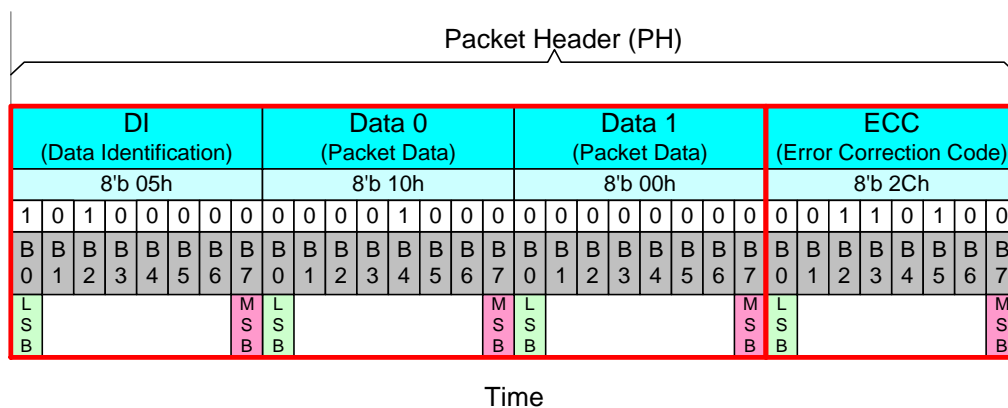


Figure 82. D[23...0] and P[7...0] in a Short Packet (SPa)

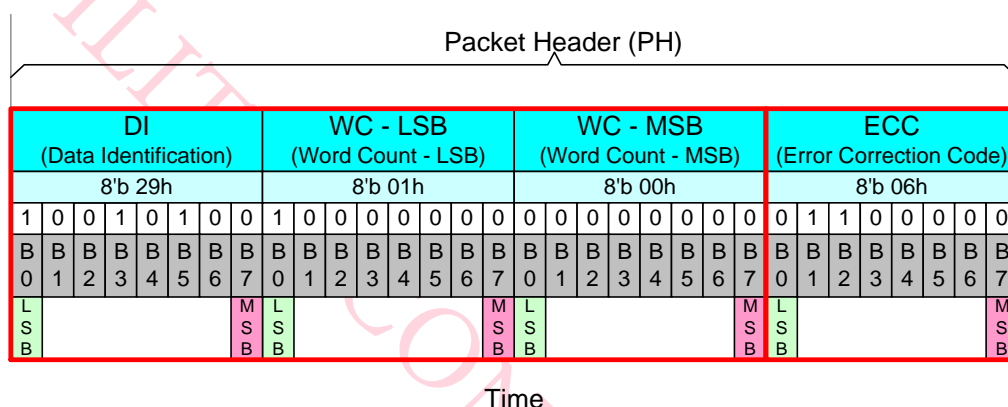


Figure 83. D[23...0] and P[7...0] in a Long Packet (LPa)

Error Correction Code (ECC) can recognize one or several error(s) and can only correct one-bit error. Bits (P[7...0]) of the Error Correction Code (ECC) are defined, where the symbol '∧' presents the XOR function (Pn is 1 if there is odd number of 1, and Pn is 0 if there is even number of 1), as follows.

- P7 = 0
- P6 = 0
- P5 = D10∧D11∧D12∧D13∧D14∧D15∧D16∧D17∧D18∧D19∧D21∧D22∧D23
- P4 = D4∧D5∧D6∧D7∧D8∧D9∧D16∧D17∧D18∧D19∧D20∧D22∧D23
- P3 = D1∧D2∧D3∧D7∧D8∧D9∧D13∧D14∧D15∧D19∧D20∧D21∧D23
- P2 = D0∧D2∧D3∧D5∧D6∧D9∧D11∧D12∧D15∧D18∧D20∧D21∧D22
- P1 = D0∧D1∧D3∧D4∧D6∧D8∧D10∧D12∧D14∧D17∧D20∧D21∧D22∧D23
- P0 = D0∧D1∧D2∧D4∧D5∧D7∧D10∧D11∧D13∧D16∧D20∧D21∧D22∧D23

P7 and P6 are set to 0 because Error Correction Code (ECC) is based on 64 bit value (D[63...0]), but this implementation is based on 24 bit value (D[23...0]). Therefore, only 6 bits are needed (P[5...0]) for Error Correction Code (ECC).

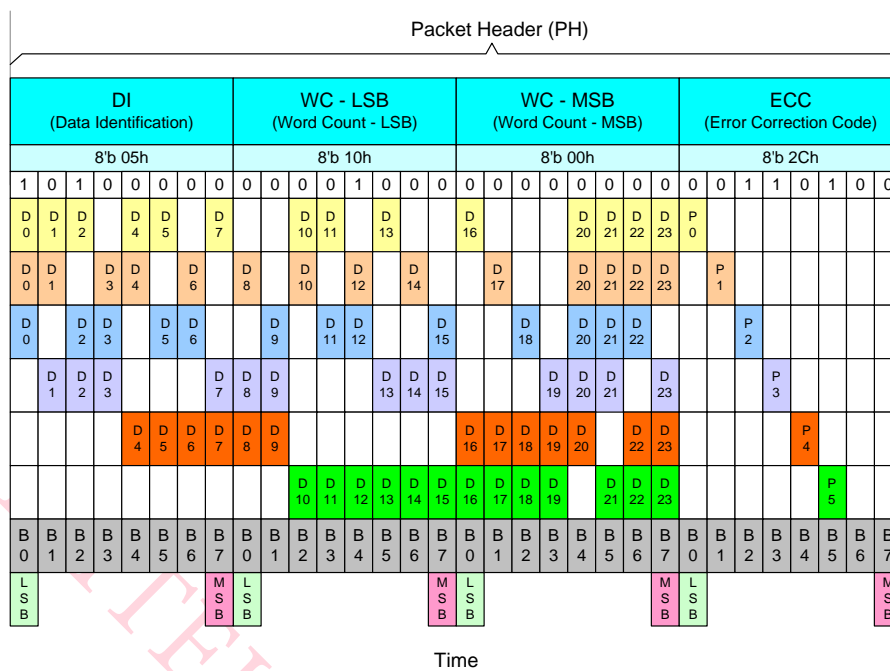


Figure 84. XOR Function on a Short Packet (SPa)

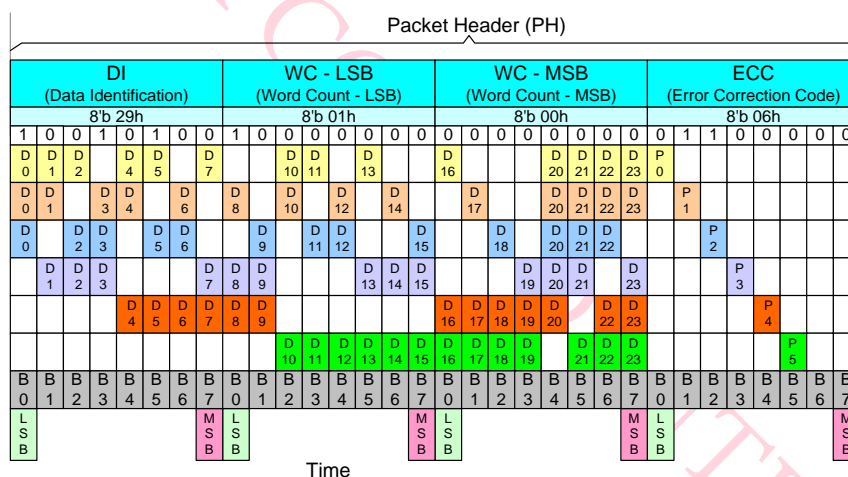


Figure 85. XOR Function on a Long Packet (LPa)

The transmitter (= the MCU or the Display Module) will send data bits D[23...0] and Error Correction Code (ECC) P[7...0]. The receiver (= the Display module or the MCU) will calculate the Internal Error Correction Code (IECC) and compare the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have performed the XOR function. The result of this function is PO[7...0]. This functionality, where the transmitter is the MCU and the receiver is the display module, is illustrated for reference purposes below.

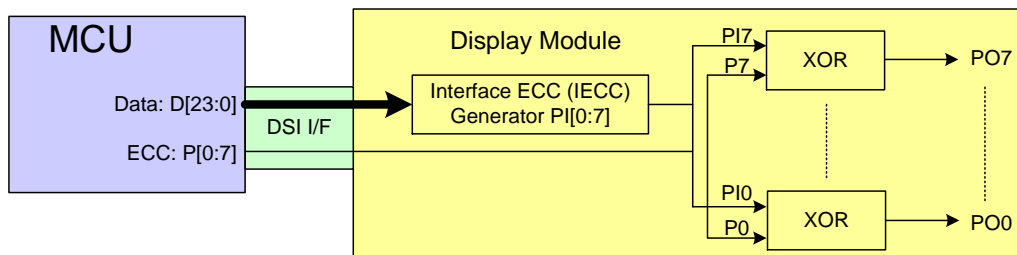


Figure 86. Internal Error Correction Code (IECC) on the Display Module (= the Receiver)

The sent data bits (D[23...0]) and ECC (P[7...0]) are correctly received if the value of the PO[7...0] is 00h.
 The sent data bits (D[23...0]) and ECC (P[7...0]) are not correctly received if the value of the PO[7...0] is not 00h.

ECC P[7...0]	1 1 0 0 0 0 0 0	03h
IECC PI[7...0]	1 1 0 0 0 0 0 0	03h
XOR(ECC,IECC) => PO[7...0]	0 0 0 0 0 0 0 0	=> 00h => No Error
	L M	
	S S	
	B B	

Figure 87. Internal XOR Calculation between ECC and IECC Values – No Error

ECC P[7...0]	1 1 0 0 0 0 0 0	03h
IECC PI[7...0]	1 1 1 1 0 0 0 0	0Fh
XOR(ECC,IECC) => PO[7...0]	0 0 1 1 0 0 0 0	=> 0Ch => Error
	L M	
	S S	
	B B	

Figure 88. Internal XOR Calculation between ECC and IECC Values - Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) function is not used for data values D[23...0] on the transmitter side. The number of the errors (one or more) can be defined when the value of the PO[7...0] is compared to the values in the following table.

Table 19. One Bit Error Value of the Error Correction Code (ECC)

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah
D[9]	0	0	0	1	1	1	0	0	1Ch
D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h
D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

An error is detected if the value of the PO[7...0] is in Table 19, and the receiver can correct this one bit error because this found value also defines the location of the corrupt bit, e.g.

- PO[7...0] = 0Eh
- The bit of the data (D[23...0]), that is not correct, is D[3]

More than one error is detected if the value of the PO[7...0] is not in Table 19, for example, PO[7...0] = 0Ch.

4.4.3.1.4 Packet Data (PD) in a Long Packet (LPa)

Packet Data (PD) of a Long Packet (LPa) is placed after the Packet Header (PH) of a Long Packet (LPa). The amount of the data bytes is defined in the section “4.4.3.1.3.3 Word Count (WC) in a Long Packet (LPa)”.

4.4.3.1.5 Packet Footer (PF) in a Long Packet (LPa)

Packet Footer (PF) of a Long Packet (LPa) is placed after the Packet Data (PD) of a Long Packet (LPa). The Packet Footer (PF) is a checksum value that is calculated from the Packet Data of the Long Packet (LPa). The checksum uses a 16-bit Cyclic Redundancy Check (CRC) value which is generated by a polynomial $x^{16}+x^{12}+x^5+x^0$, as illustrated below.

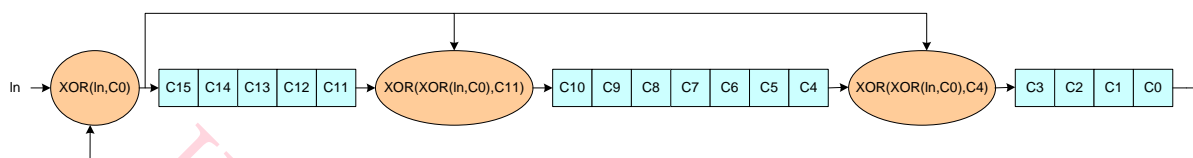


Figure 89. 16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit which is inputted into the 16-bit Cyclic Redundancy Check (CRC). An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of a Long Packet (LPa) is 01h, is illustrated (step-by-step) below.

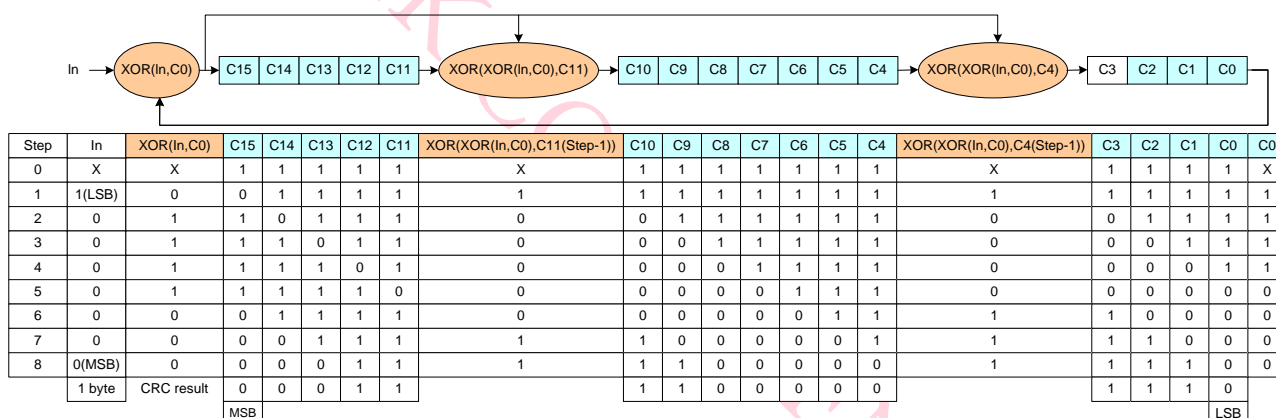


Figure 90. CRC Calculation – Packet Data (PD) is 01h

The value of the Packet Footer (PF) is 1E0Eh in this example (Command 01h has been sent), and is illustrated below.

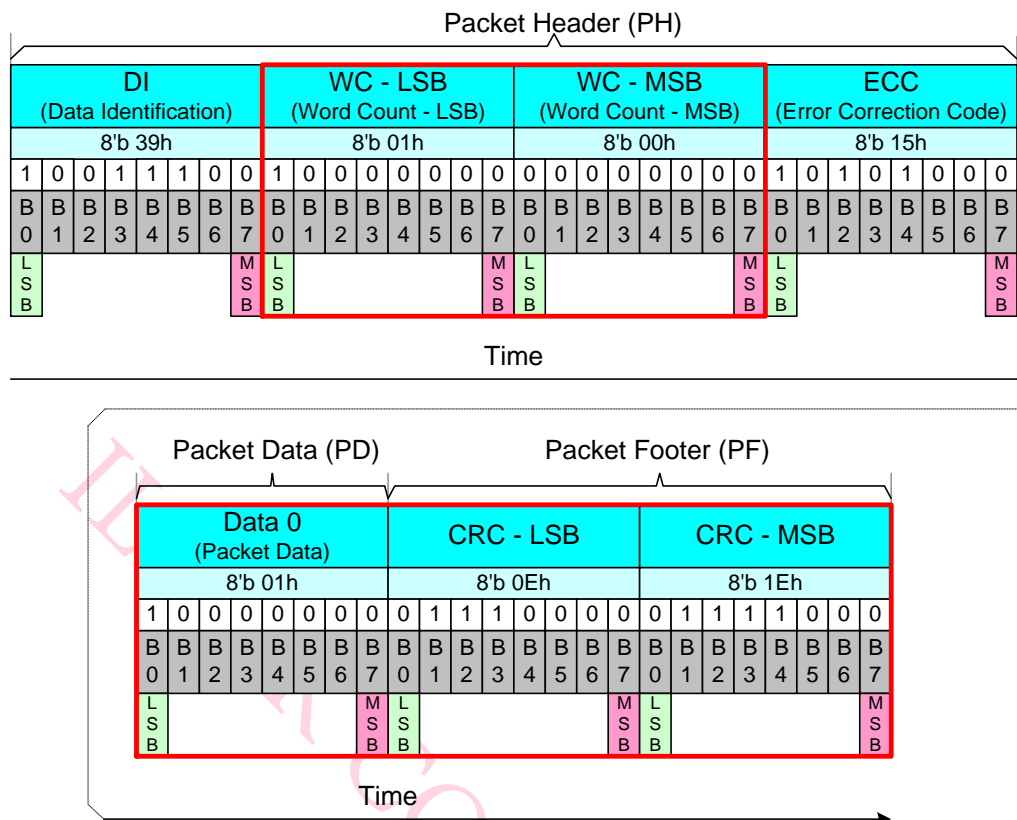


Figure 91. Packet Footer (PF) Example

The receiver calculates its checksum value from the received Packet Data (PD). The receiver compares its checksum and the Packet Footer (PF) that the transmitter has sent. The received Packet Data (PD) and Packet Footer (PF) are correct if the checksum of the receiver and Packet Footer (PF) are equal. The received Packet Data (PD) and Packet Footer (PF) are not correct if the checksum of the receiver and Packet Footer (PF) are not equal.

4.4.3.2 Packet Transmissions

4.4.3.2.1 Packet from the MCU to the Display Module

4.4.3.2.1.1 Display Command Set (DCS)

Display Command Set (DCS), defined in the section "Page 0 Command Description", is used from the MCU to the display module. This Display Command Set (DCS) is always defined in the Data 0 of the Packet Data (PD), and is included in Short Packet (SPa) and Long packet (LPa), as illustrated below.

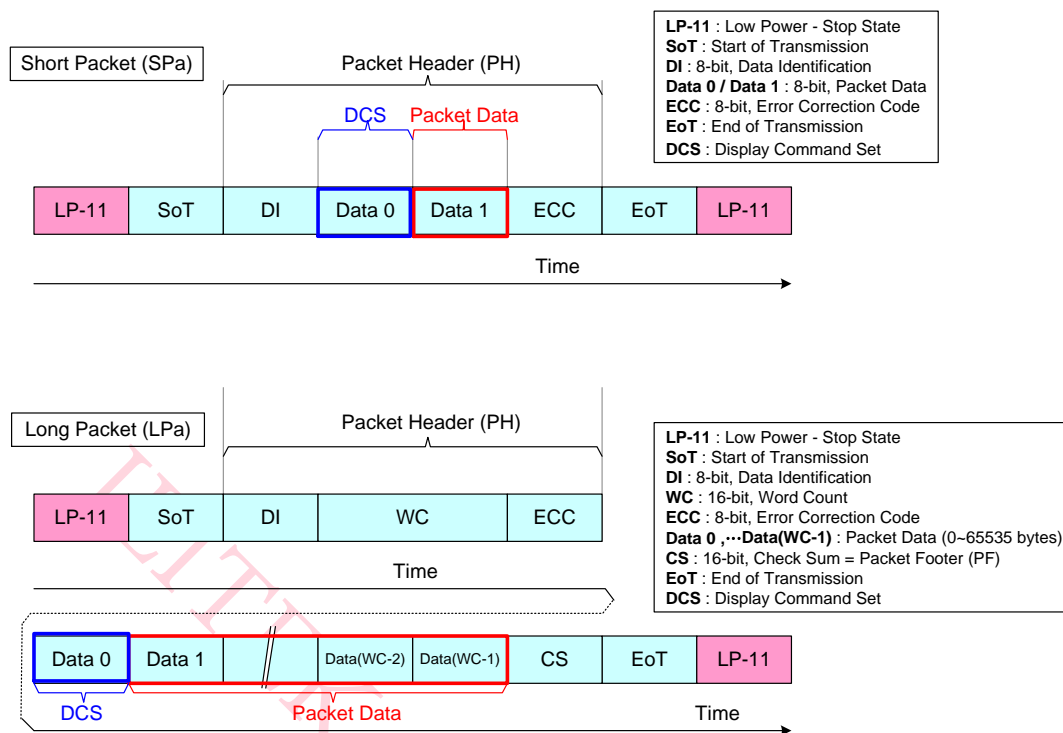


Figure 92. Display Command Set (DCS) in Short Packet (SPa) and Long Packet (LPa)

4.4.3.2.1.2 Display Command Set (DCS) Write, No Parameter (DCSWN-S)

“Display Command Set (DCS) Write, No Parameter”, which is defined in Data Type (DT, 00 0101b), is always used in a Short Packet (SPa) from the MCU to the display module. These commands are defined in a table below.

Table 20. Display Command Set (DCS) Write, No Parameters (DCSWN-S)

Command
NOP (00h)
Software Reset (01h)
Sleep In(10h)
Sleep Out (11h)
Normal Display Mode On (13h)
Display Inversion Off (20h)
Display Inversion On (21h)
All Pixel Off (22h)
All Pixel On (23h)
Display Off (28h)
Display ON (29h)
Tearing Effect Line Off (34h)
Idle Mode Off (38h)
Idle Mode On (39h)

A Short Packet (SPa) is defined as:

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 00 0101b
- Packet Data (PD)
 - Data 0: “Sleep In (10h)”, Display Command Set (DCS)
 - Data 1: Always 00h
- Error Correction Code (ECC)



“Display Command Set (DCS) Write, 1 Parameter” (DCSW1-S), which is defined in the Data Type (DT, 01 0101b), is always used in a Short Packet (SPa) from the MCU to the display module. These commands are defined in the table below.

Command
Tearing Effect Line On (35h)
Memory Access Control (36h)
Interface Pixel Format (3Ah)
Write CTRL Display (53h)
Write Power Save (55h)

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 01 0101b
- Packet Data (PD)
 - Data 0: "Tearing Effect Line On (35h)", Display Command Set (DCS)
 - Data 1: 01h, Parameter of the DCS
- Error Correction Code (ECC)



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“Display Command Set (DCS) Write Long” (DCSW-L), which is defined in Data Type (DT, 11 1001b), is always used in a Long Packet (LPa) from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters) are defined in a table below.

Table 22. Display Command Set (DCS) Write Long (DCSW-L)

Command
NOP (00h), ^{Note 1}
Software Reset (01h), ^{Note 1}
Sleep In(10h), ^{Note 1}
Sleep Out (11h), ^{Note 1}
Normal Display Mode On (13h), ^{Note 1}
Display Inversion Off (20h), ^{Note 1}
Display Inversion On (21h), ^{Note 1}
All Pixel Off (22h), ^{Note 1}
All Pixel On (23h), ^{Note 1}
Display Off (28h), ^{Note 1}
Display ON (29h), ^{Note 1}
Memory Write (2Ch)
Tearing Effect Line Off (34h), ^{Note 1}
Tearing Effect Line On (35h), ^{Note 2}
Memory Access Control (36h), ^{Note 2}
Idle Mode Off (38h), ^{Note 1}
Idle Mode On (39h), ^{Note 1}
Interface Pixel Format (3Ah), ^{Note 2}
Memory Write Continue (3Ch)
Set Tear Scan Line (44h)
Write Display Brightness (51h)
Write CTRL Display (53h), ^{Note 2}
Write Power Save (55h), ^{Note 2}

Notes:

1. Short Packet (SPa) can also be used; See the section “4.4.3.2.1.2 Display Command Set (DCS) Write, No Parameter (DCSWN-S)”.
2. Short Packet (SPa) can also be used; See the section “4.4.3.2.1.3 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)”.

A Long Packet (LPa) with one command (No Parameter) is defined as:

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 11 1001b
- Word Count (WC)
 - Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0: “Sleep In (10h)”, Display Command Set (DCS)
- Packet Footer (PF)

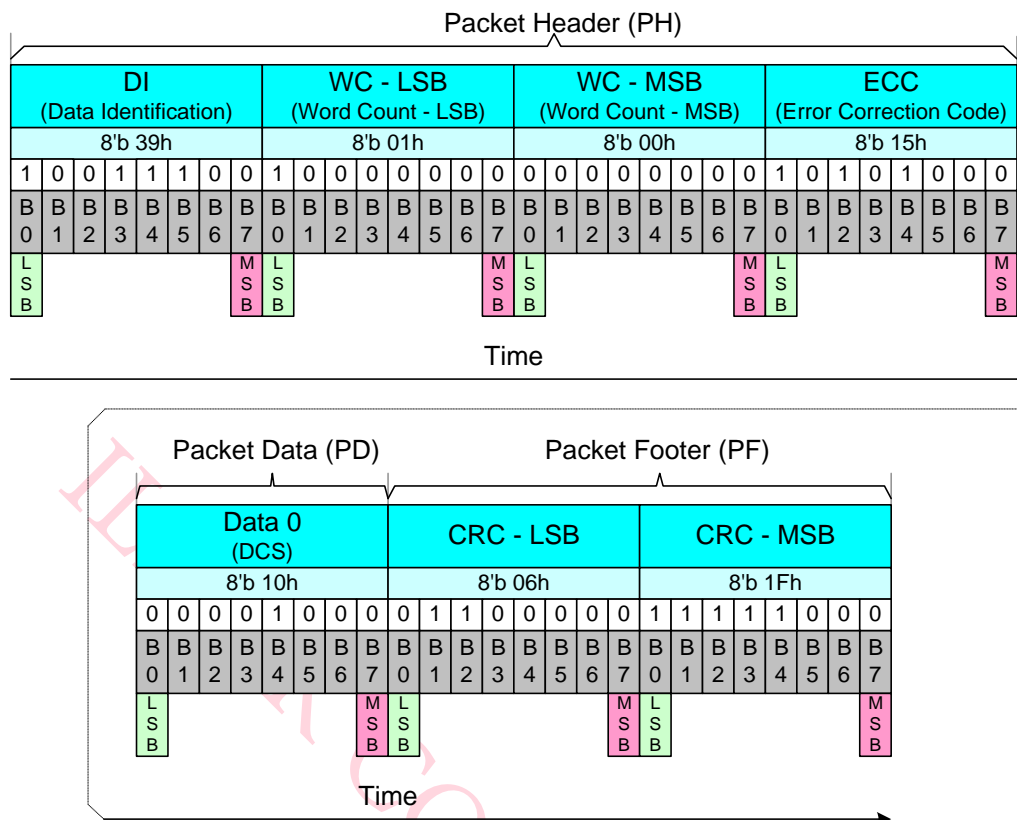


Figure 95. Display Command Set (DCS) Write Long (DCSW-L) with DCS Only - Example

A Long Packet (LPa) with one Write (1 parameter) is defined as:

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 11 1001b
- Word Count (WC)
 - Word Count (WC): 0002h
- Error Correction Code (ECC)
- Packet Data (PD):
 - Data 0: "Tearing Effect Line On (35h)", Display Command Set (DCS)
 - Data 1: 01h, Parameter of the DCS
- Packet Footer (PF)

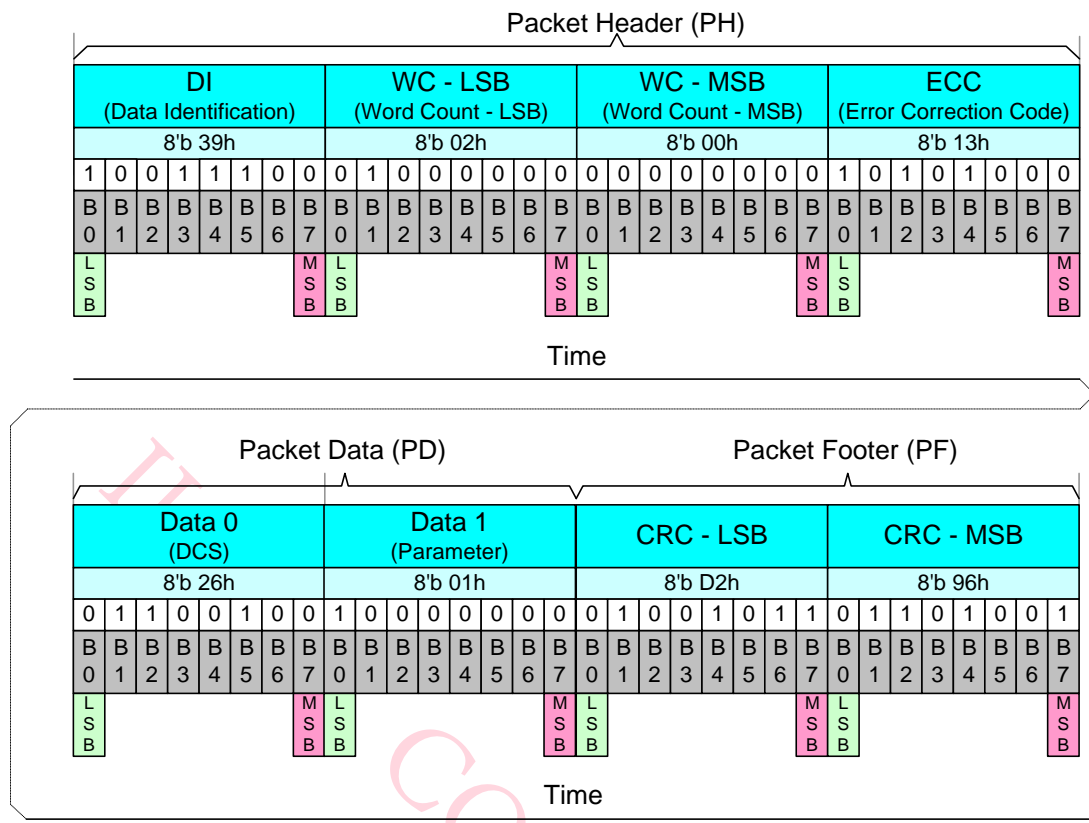


Figure 96. Display Command Set (DCS) Write Long with DCS and 1 Parameter - Example

A Long Packet (LPa) with one Write (4 parameters) is defined as:

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 11 1001b
- Word Count (WC)
 - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
 - Data 0: "Column Address Set (2Ah)" (For example only), Display Command Set (DCS)
 - Data 1: 00h, 1st Parameter of the DCS, Start Column SC[15...8]
 - Data 2: 12h, 2nd Parameter of the DCS, Start Column SC[7...0]
 - Data 3: 01h, 3rd Parameter of the DCS, End Column EC[15...8]
 - Data 4: EFh, 4th Parameter of the DCS, End Column EC[7...0]
- Packet Footer (PF)

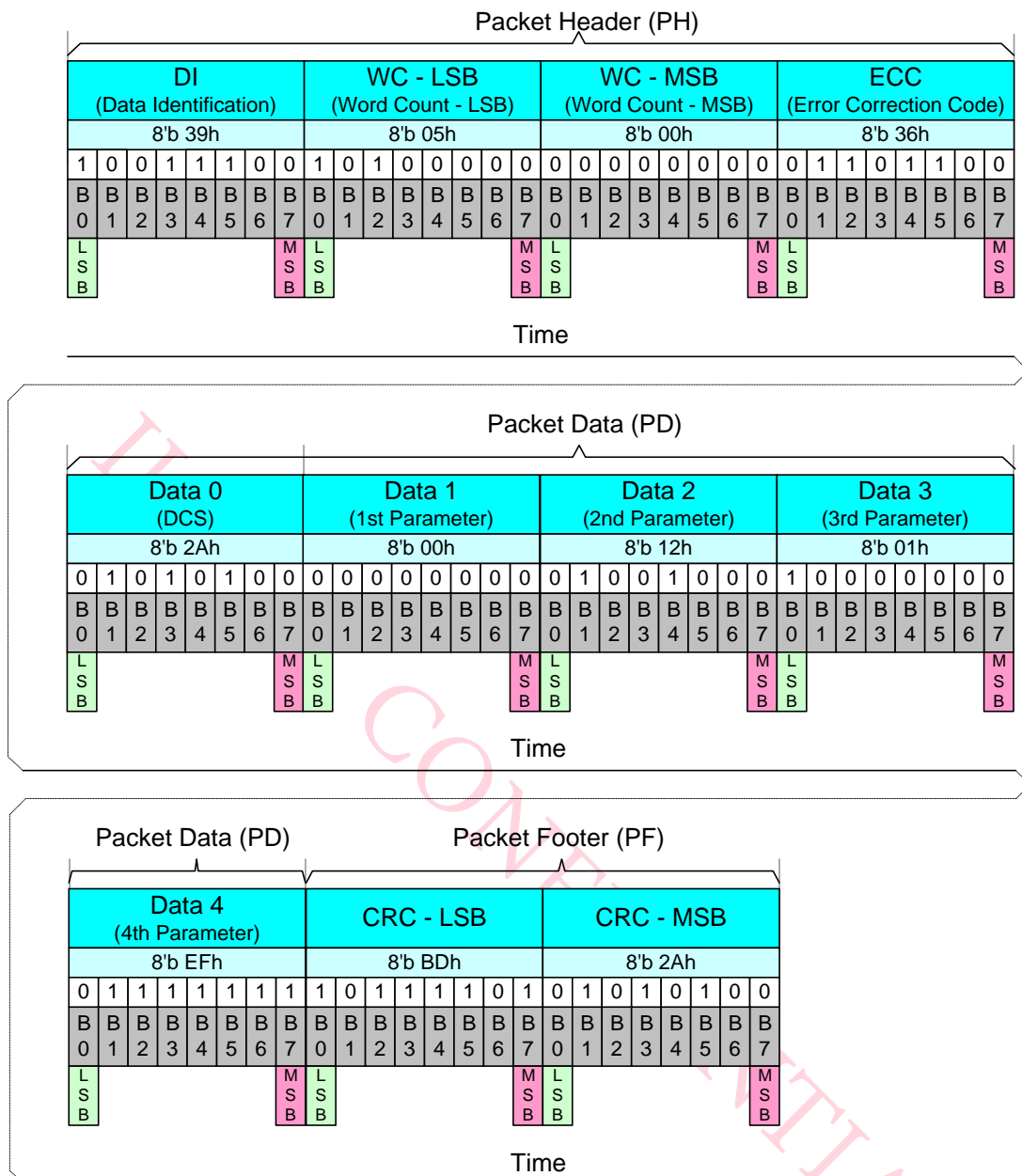


Figure 97. Display Command Set (DCS) Write Long with DCS and 4 Parameters - Example

4.4.3.2.1.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)

“Display Command Set (DCS) Read, No Parameter” (DCSRN-S), which is defined in Data Type (DT, 00 0110b), is always used in a Short Packet (SPa) from the MCU to the display module. These commands are defined in the table below.

Table 23. Display Command Set (DCS) Read, No Parameter (DCSRN-S)

Command
Read Number of the Errors on DSI (05h)
Read Display Power Mode (0Ah)
Read Display MADCTL (0Bh)
Read Display Pixel Format (0Ch)
Read Display Image Mode (0Dh)
Read Display Signal Mode (0Eh)
Read Display Self-Diagnostic Result (0Fh)
Get Tear Scan Line (45h)
Read Display Brightness Value (52h)
Read CTRL Value Display (54h)
Read Power Save (56h)
Read DDB Start (A1h)
Read DDB Continue (A8h)
Read First Checksum (AAh)
Read Continue Checksum (AFh)
Read ID1 (DAh)
Read ID2 (DBh)
Read ID3 (DCh)

The MCU has to define to the display module the maximum size of the returned packet. The command, which is used for this purpose, is “Set Maximum Return Packet Size” (SMRPS-S), which Data Type (DT) is 11 0111b and is used in a Short Packet (SPa) before the MCU can send “Display Command Set (DCS) Read, No Parameter” to the display module. This sequence is illustrated for reference purposes below.

Step 1:

The MCU sends “Set Maximum Return Packet Size” (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 11 0111b
- Maximum Return Packet Size (MRPS)
 - Data 0: 01h
 - Data 1: 00h
- Error Correction Code (ECC)

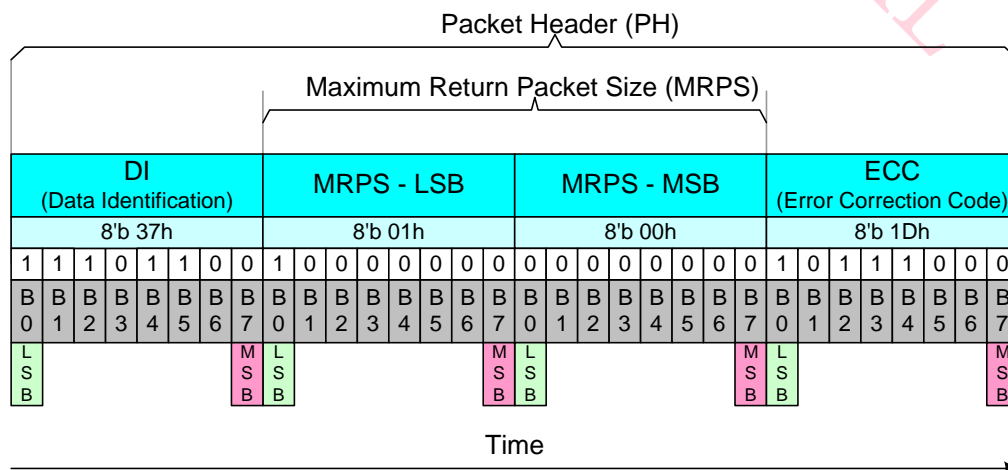


Figure 98. Set Maximum Return Packet Size (SMRPS-S) - Example

Step 2:

The MCU wants to receive the value of the “Read ID1 (DAh)” from the display module when the MCU sends “Display Command Set (DCS) Read, No Parameter” to the display module.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 00 0110b
- Packet Data (PD)
 - Data 0: “Read ID1 (DAh)”, Display Command Set (DCS)
 - Data 1: Always 00h
- Error Correction Code (ECC)

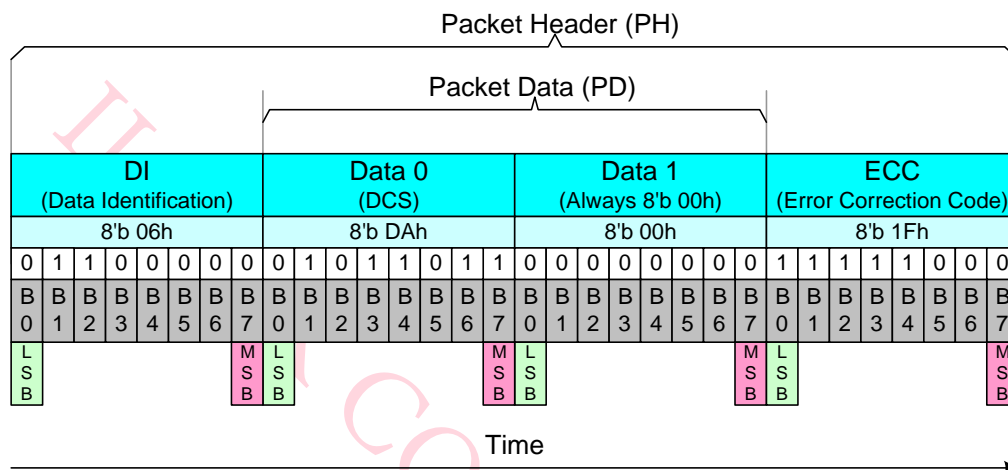


Figure 99. Display Command Set (DCS) Read, No Parameter (DCSRN-S) - Example

Step 3:

The display module can send 2 different information to the MCU after Bus Turnaround (BTA):

1. An acknowledge with Error Report (AwER), which is used in a Short Packet (SPa), if there is an error when receiving a command. See the section “4.4.3.2.2 Acknowledge with Error Report (AwER)”.
2. Information of the received command, which can be a Short Packet (SPa) or a Long Packet (LPa).

4.4.3.2.1.6 Null Packet, No Data (NP-L)

“Null Packet, No Data” (NP-L), which is defined in Data Type (DT, 001001b), is always used in a Long Packet (LPa) from the MCU to the display module. The purpose of this command is to keep data lanes in the high speed mode (HSDT) if necessary. The display module can ignore the Packet Data (PD) that the MCU sends.

A Long Packet (LPa) with 5 random data bytes of the Packet Data (PD) is defined as:

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 00 1001b
- Word Count (WC)
 - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
 - Data 0: 89h (Random data)
 - Data 1: 23h (Random data)
 - Data 2: 12h (Random data)
 - Data 3: A2h (Random data)
 - Data 4: E2h (Random data)
- Packet Footer (PF)

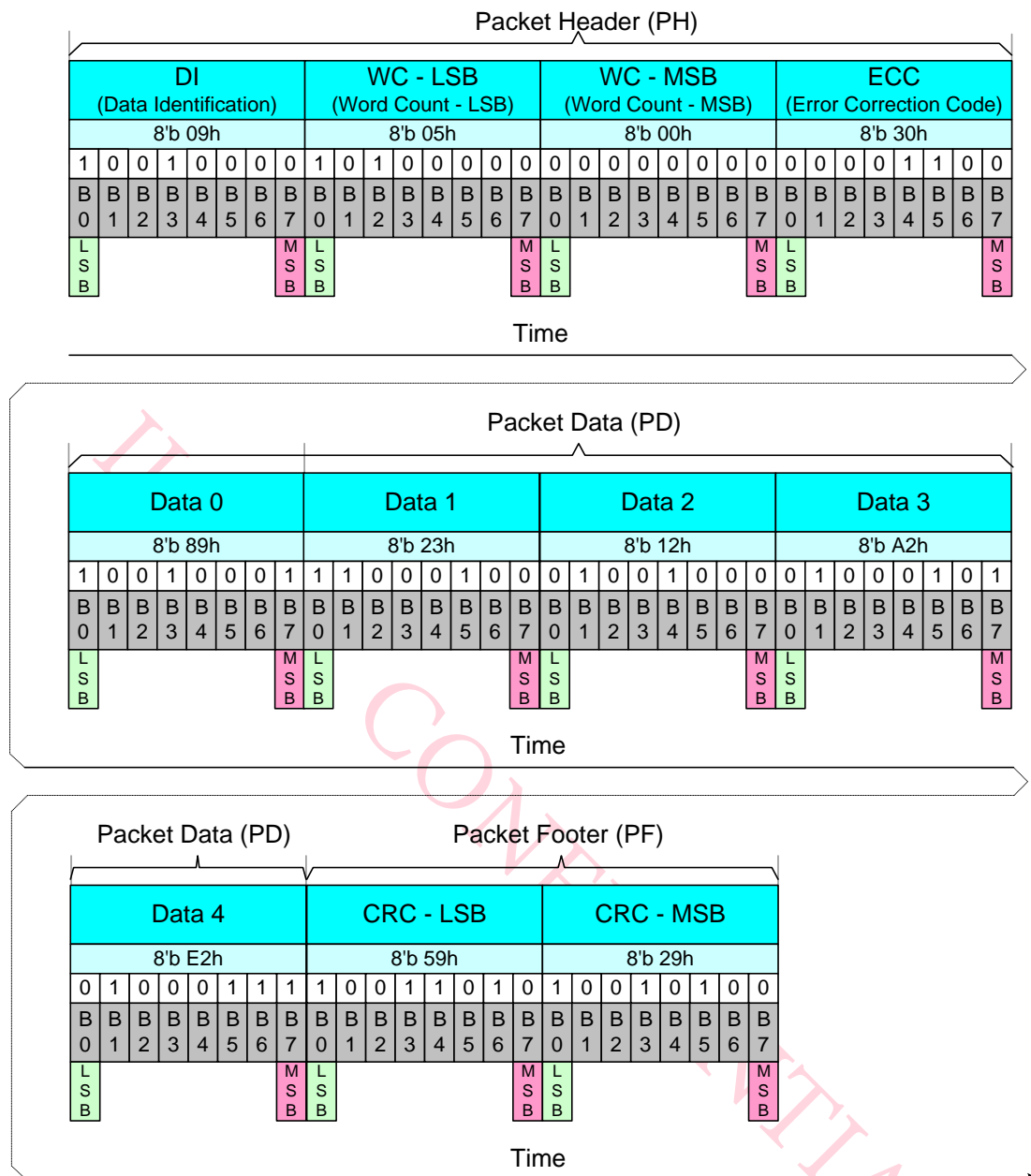


Figure 100. Null Packet, No Data (NP-L) - Example

4.4.3.2.1.7 End of Transmission Packet (EoTP)

“End of Transmission Packet” (EoTP), which is an interface level function and defined in Data Type (DT, 00 1000b), is always used in a Short Packet (SPa) from the MCU to the display module. The purpose of this command is to terminate the high Speed Data Transmission (HSDT) mode properly when EoTP is added after the last payload packet before “End of Transmission” (EoT).

The MCU can decide if it wants to use the “End of Transmission Packet” (EoTP) or not. The display shall have the capability to support both. That is, if the MCU applies the EoTP, it shall report the “DSI Protocol Violation Error” when the EoTP is not detected in the High-Speed (HS). The error report of display module shall be enabled or disabled statistically, according to the module application.

The display module does or does not receive “End of Transmission Packet” (EoTP) from the MCU during the Low Power Data Transmission (LPDT) mode before “Mark-1” (= leaving the Escape mode) which ends the Low Power Data Transmission (LPDT) mode. The display module is not allowed to send “End of Transmission Packet” (EoTP) to the MCU during the Low Power Data Transmission (LPDT) mode. The summary of the receiving and transmitting EoTP is listed below.

Table 24. Receiving and Transmitting EoTP during LPDT

Direction	Display Module (DM) in High Speed Data Transmission (HSDT)	Display Module (DM) in Low Power Data Transmission (LPDT)
MCU => Display Module	Support With and Without EoTP	Support With and Without EoTP
Display Module => MCU	HS Mode is not available (EoTP is not available)	EoTP cannot be sent by the Display Module (DM)

A Short Packet (SPa) using a fixed format is as follows:

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 00 1000b
- Packet Data (PD)
 - Data 0: 0Fh
 - Data 1: 0Fh
- Error Correction Code (ECC)
 - ECC: 01h

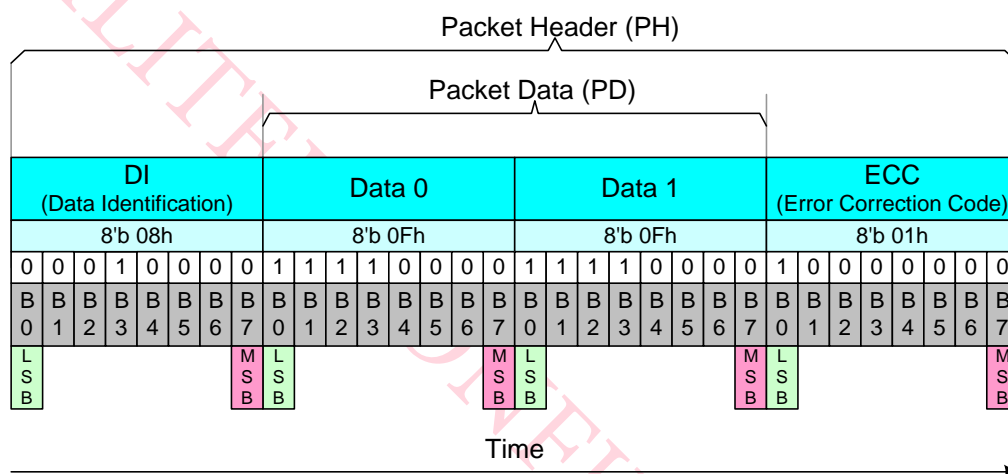


Figure 101. End of Transmission Packet (EoTP)

Some examples of the “End of Transmission Packet” (EoTP) are illustrated for reference purposes below.

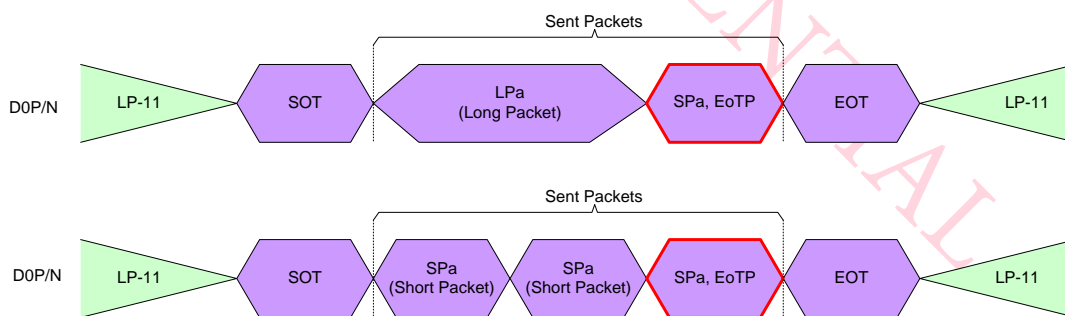


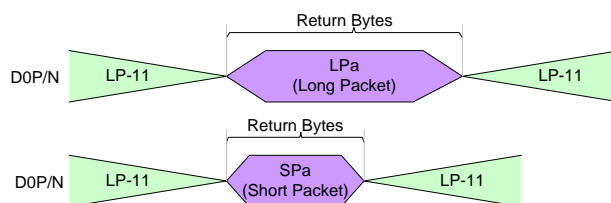
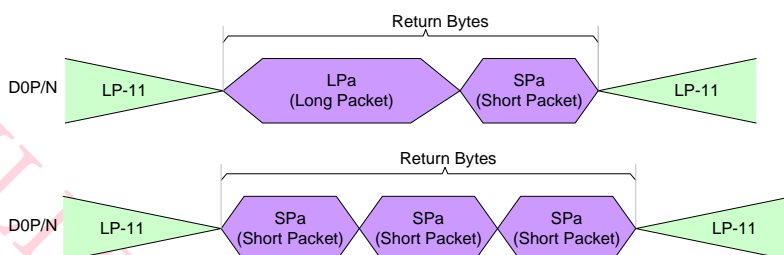
Figure 102. End of Transmission Packet (EoTP)-Examples

4.4.3.2.2 Packet from the Display Module to the MCU

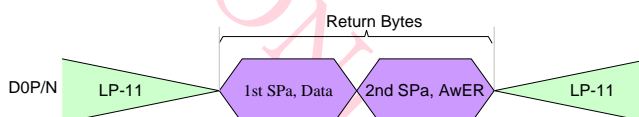
4.4.3.2.2.1 Used Packet types

The display module always uses Short Packets (SPa) or Longs Packet (LPa) when returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) (See the section “4.4.3.2.1.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)”) or an Acknowledge with Error Report (See the section “4.4.3.2.2.2 Acknowledge with Error Report (AwER)”).

The used packet type is defined on Data Type (DT). See the section “4.4.3.1.3.1.2 Data Type (DT)”. If the maximum size of the Packet Data (PD) could be sent in one packet, the display module should not send returned bytes in several packets. Both cases are illustrated for reference purposes below.


Figure 103. Return Bytes in Single Packet

Figure 104. Return Bytes in Several Packets – Not Allowed
EXCEPTION:

The display module will return 2 packets (1st packet: Data, 2nd Packet: Acknowledge with Error Report) to the MCU when the display module receives a read command (See section “4.4.3.2.1.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)”), which is detected and corrected a single bit error by the EEC (See bit 8 in Table 15). These returned packets are illustrated for reference purposes below.


Figure 105. Exception when Returned Bytes in Several Packets

AwER = Acknowledge with Error Report

4.4.3.2.2 Acknowledge with Error Report (AwER)

“Acknowledge with Error Report” (AwER), which is defined in Data Type (DT, 00 0010b), is always used in a Short Packet (SPa) from the display module to the MCU. The Packet Data (PD) can include bits, which define the current error, when the corresponding bit is set to 1, as defined in the following table.

Table 25. Error Report (AwER) Bit Definitions

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long Packet only)
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to 0 internally
15	DSI Protocol Violation

These errors are included in all packages that have been received from the MCU to the display module before the Bus Turnaround (BTA). The display module ignores the received packet which includes error or errors.

Acknowledge with Error Report (AwER) of a Short Packet (SPa) is defined as:

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 00 0010b
- Packet Data (PD)
 - Bit 8: ECC Error, single-bit (detected and corrected)
 - AwER: 0100h
- Error Correction Code (ECC)

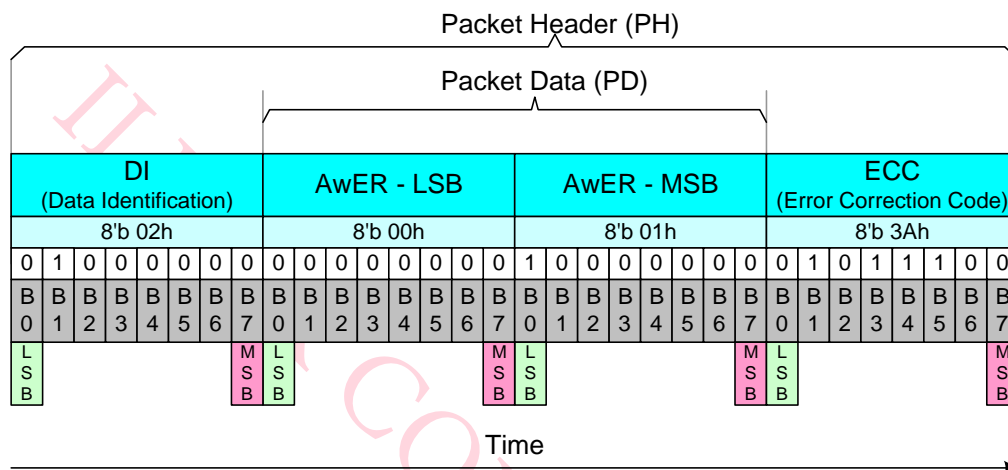


Figure 106. Acknowledge with Error Report (AwER) – Example

It is possible that the display module receives several packets, which include errors, from the MCU before the MCU performs the Bus Turnaround (BTA). Some examples are illustrated for reference purposes below.

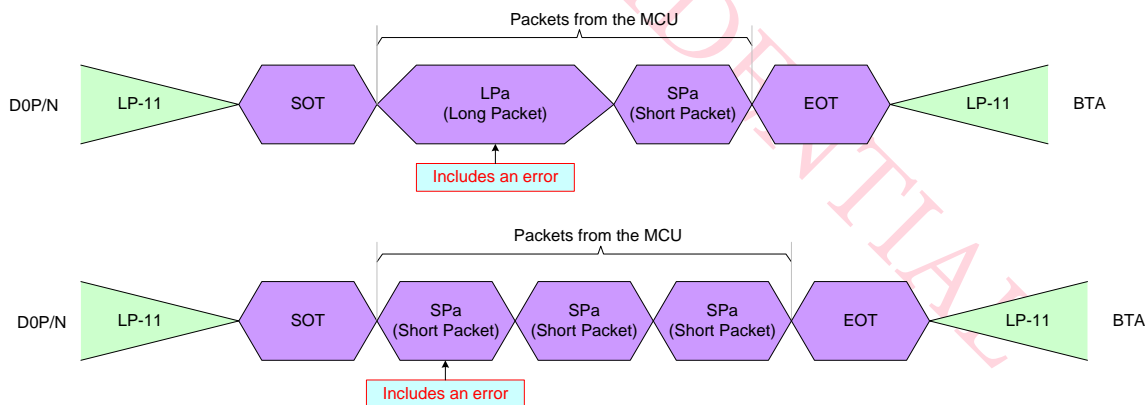


Figure 107. Errors Packets

Therefore, a method is needed to check if there are errors in the previous packets. These errors of the previous packets can be detected by “Read Display Signal Mode (0Eh)” and “Read Number of the Errors on DSI (05h)” commands. The bit D0 of the “Read Display Signal Mode (0Eh)” command will be set to 1 if a received packet includes an error. The amount of packets, which include an ECC or CRC error, is calculated in the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h and set the bit D0 of the “Read Display Signal Mode (0Eh)” command to 0 after the MCU has read the RDNUMED register from the display module. The functionality of the RDNUMED register is illustrated for reference purposes below.

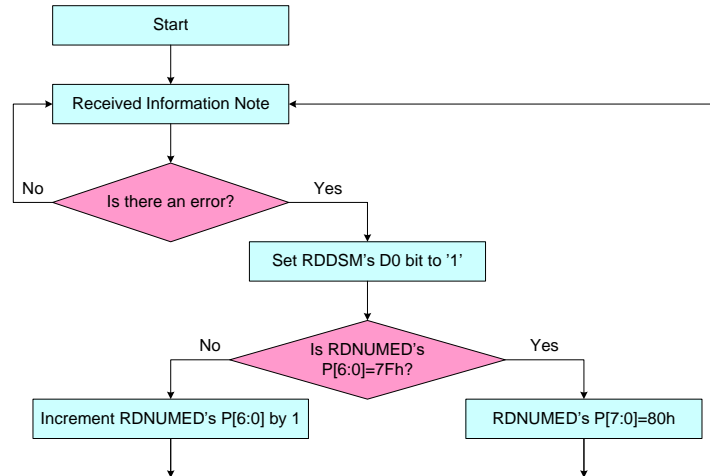


Figure 108. Flow Chart for Errors on DSI

Notes:

1. This information can be Interface or Packet Level Communication, but it is always from the MCU to the display module.
2. CRC or ECC error

4.4.3.2.2.3 DCS Read Long Response (DCSRR-L)

“DCS Read Long Response” (DCSRR-L), which is defined in Data Type (DT, 011100b), is always used in a Long Packet (LPa) from the display module to the MCU. “DCS Read Long Response” (DCSRR-L) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

A Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined as:

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 01 1100b
- Word Count (WC)
 - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
 - Data 0: 89h
 - Data 1: 23h
 - Data 2: 12h
 - Data 3: A2h
 - Data 4: E2h
- Packet Footer (PF)

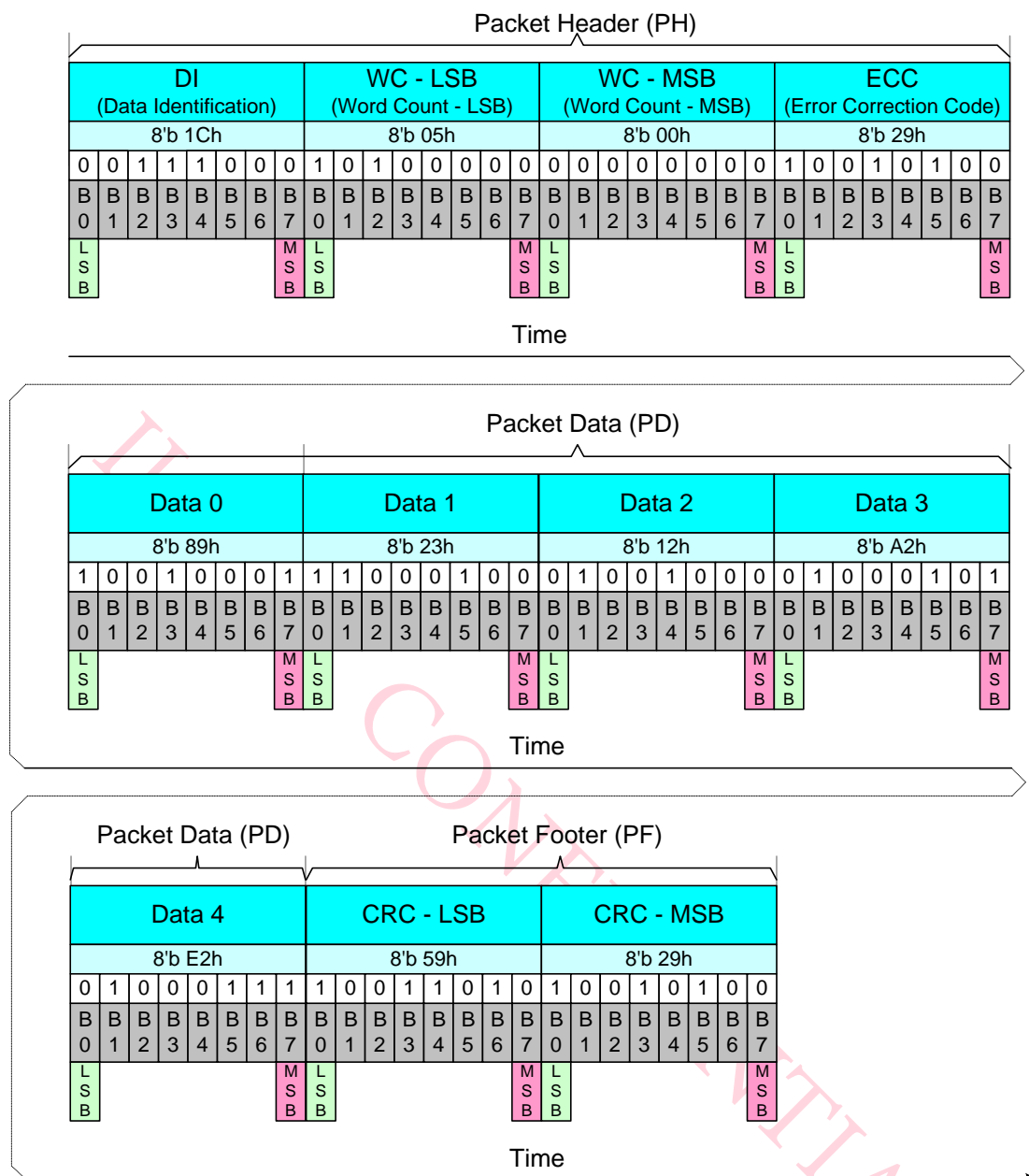


Figure 109. DCS Read Long Response (DCSRR-L) - Example

4.4.3.2.2.4 DCS Read Short Response, 1 Byte Returned (DCSRR1-S)

“DCS Read Short Response, 1 Byte Returned” (DCSRR1-S), which is defined in Data Type (DT, 10 0001b), is always used in a Short Packet (SPa) from the display module to the MCU. “DCS Read Short Response, 1 Byte Returned” (DCSRR1-S) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

A Short Packet (SPa) is defined as:

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 10 0001b
- Packet Data (PD)
 - Data 0: 45h
 - Data 1: 00h (Always)
- Error Correction Code (ECC)

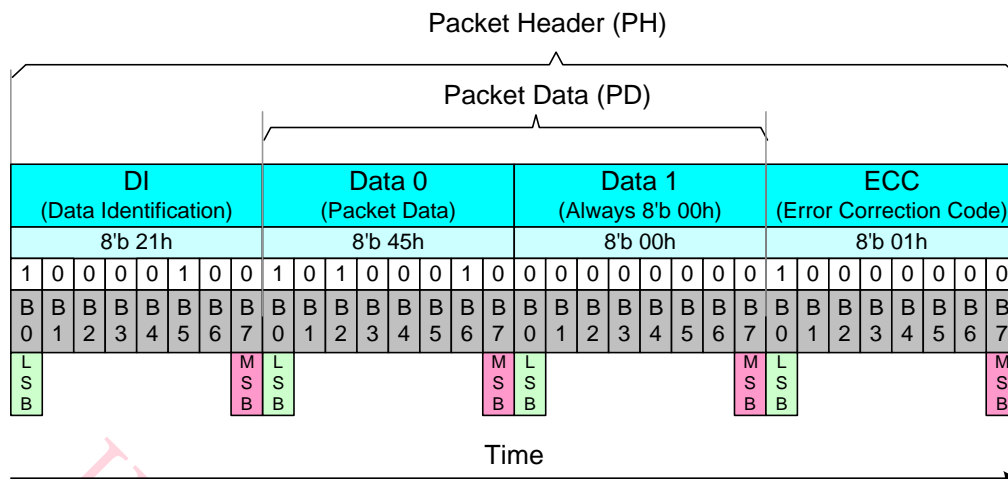


Figure 110. DCS Read Short Response, 1 Byte Returned (DCSRR1-S) - Example

4.4.3.2.5 DCS Read Short Response, 2 Bytes Returned (DCSRR2-S)

“DCS Read Short Response, 2 Bytes Returned” (DCSRR2-S), which is defined in Data Type (DT, 10 0010b), is always used in a Short Packet (SPa) from the display module to the MCU. “DCS Read Short Response, 2 Bytes Returned” (DCSRR2-S) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

A Short Packet (SPa) is defined as:

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 10 0010b
- Packet Data (PD)
 - Data 0: 45h
 - Data 1: 32h
- Error Correction Code (ECC)

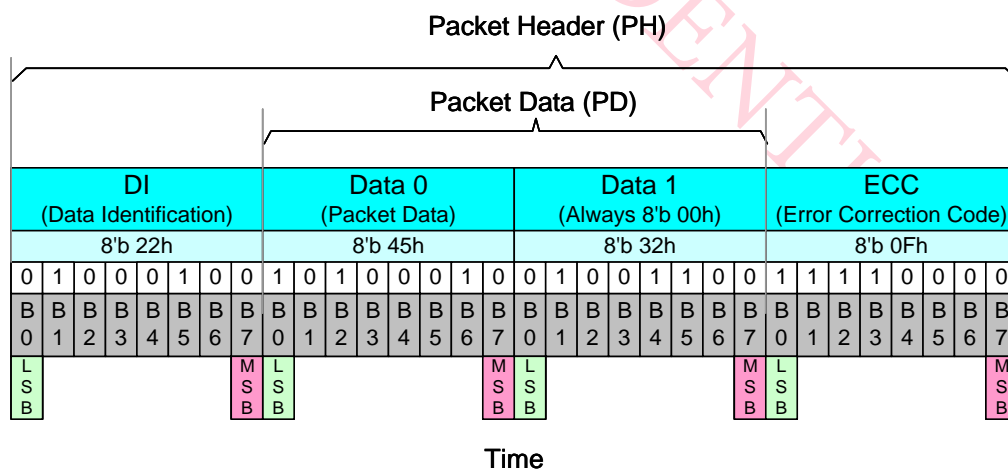


Figure 111. DCS Read Short Response, 2 Bytes Returned (DCSRR2-S) - Example

4.4.3.3 Communication Sequences

4.4.3.3.1 General

The communication sequences can be done on interface or packet levels between the MCU and the display module. See sections “4.4.2 Interface Level Communication” and “4.4.3 Packet Level Communication”. This communication sequence description is for DSI data lane (HSSI_D0_P/N), and it is assumed that the needed low level communication is done on DSI

Clock lane (HSSI_CLK_P/N) automatically. See the section “4.4.2.2 DSI CLK Lanes”. Functions of the interface level communication are described in the following table.

Table 26. Interface Level Communication

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop State
	LPDT	Low Power Data Transmission
	ULPS	Ultra-Low Power State
	RAR	Remote Application Reset
	ACK	Acknowledge (No Error)
	BTA	Bus Turnaround
High Speed	HSDT	High speed Data Transmission

Functions of the packet level communication are described in the following table.

Table 27. Packet Level Communication for MCU-sourced Packets

Interface Mode	Abbreviation	Packet Size	Interface Action Description
MCU	VSS	Short Packet	Sync Event, V Sync Start
	VSE	Short Packet	Sync Event, V Sync End
	HSS	Short Packet	Sync Event, H Sync Start
	HSE	Short Packet	Sync Event, H Sync End
	EoTP	Short Packet	End of Transmission Packet (EoTP)
	CMOFF	Short Packet	Color Mode Off Command
	CMON	Short Packet	Color Mode On Command
	SDNP	Short Packet	Shut Down Peripheral Command
	TONP	Short Packet	Turn On Peripheral Command
	GENWN-S	Short Packet	Generic Short WRITE, no parameters
	GENW1-S	Short Packet	Generic Short WRITE, 1 parameters
	GENW2-S	Short Packet	Generic Short WRITE, 2 parameters
	GENRN-S	Short Packet	Generic Short READ, no parameters
	GENR1-S	Short Packet	Generic Short READ, 1 parameters
	GENR2-S	Short Packet	Generic Short READ, 2 parameters
	DCSWN-S	Short Packet	DCS Write, No Parameter
	DCSW1-S	Short Packet	DCS Write, 1 Parameter
	DCSRN-S	Short Packet	DCS Read, No Parameter
	SMRPS-S	Short Packet	Set Maximum Return Packet Size
	NP-L	Long Packet	Null Packet, No Data.
	BLK-L	Long Packet	Blanking Packet, no data
	GENW-L	Long Packet	Generic Long Write
	DCSW-L	Long Packet	DCS Write Long
	PKPS16	Long Packet	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format
	PKPS18	Long Packet	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format
	LPKPS18	Long Packet	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format
	PKPS24	Long Packet	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format

Table 28. Packet Level Communication for Peripheral-sourced packets

Interface Mode	Abbreviation	Packet Size	Interface Action Description
Display Module (IL79400A-XX)	AwER	Short Packet	Acknowledge with Error Report
	EoTP	Short Packet	End of Transmission Packet
	GENRR1-S	Short Packet	Generic Short READ Response, 1 byte returned
	GENRR2-S	Short Packet	Generic Short READ Response, 2 byte returned
	GENRR-L	Long Packet	Generic Long READ Response
	DCSRR-L	Long Packet	DCS Read Long Response
	DCSRR1-S	Short Packet	DCS Read Short Response, 1 byte returned
	DCSRR2-S	Short Packet	DCS Read Short Response, 2 byte returned

4.4.3.3.2 Sequences

4.4.3.3.2.1 DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” is defined in the section “4.4.3.2.1.3 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” and example sequences on how this packet is used are described in following tables.

Table 29. DCS Write, 1 Parameter Sequence – Example 1

DCS Write, 1 Parameter Sequence – Example 1						
Line	MCU		Information Direction	Display Module (IL79400A-XX)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 30. DCS Write, 1 Parameter Sequence – Example 2

DCS Write, 1 Parameter Sequence – Example 2						
Line	MCU		Information Direction	Display Module (IL79400A-XX)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 31. DCS Write, 1 Parameter Sequence – Example 3

DCS Write, 1 Parameter Sequence – Example 3						
Line	MCU		Information Direction	Display Module (IL79400A-XX)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	↔	BTA	--	Interface Control Change from MCU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7	--	--				
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	↔	BTA	--	Interface Control Change from the display module to MCU
11	--	LP-11	→	--	--	End
12	--	--				
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	↔	BTA	--	
16	--	LP-11	→	--	--	End

4.4.3.3.2.2 DCS Write, No Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Write, No Parameter (DCSWN-S)" is defined in the section "4.4.3.2.1.2 Display Command Set (DCS) Write, No Parameter (DCSWN-S)" and example sequences on how this packet is used are described in following tables.

Table 32. DCS Write, No Parameter Sequence – Example 1

DCS Write, No Parameter Sequence – Example 1						
Line	MCU		Information Direction	Display Module (IL79400A-XX)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 33. DCS Write, No Parameter Sequence – Example 2

DCS Write, No Parameter Sequence – Example 2						
Line	MCU		Information Direction	Display Module (IL79400A-XX)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 34. DCS Write, No Parameter Sequence – Example 3

DCS Write, 1 Parameter Sequence – Example 3						
Line	MCU		Information Direction	Display Module (IL79400A-XX)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	↔	BTA	--	Interface Control Change from MCU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7	--	--				
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	↔	BTA	--	Interface Control Change from the display module to MCU
11	--	LP-11	→	--	--	End
12	--	--				
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	↔	BTA	--	
16	--	LP-11	→	--	--	End

4.4.3.3.2.3 DCS Write Long Sequence

A Long Packet (LPa) of "Display Command Set (DCS) Write Long (DCSW-L)" is defined in the section "4.4.3.2.1.4 Display Command Set (DCS) Write Long (DCSW-L)" and example sequences on how this packet is used are described in following tables.

Table 35. DCS Write Long Sequence – Example 1

DCS Write Long Sequence – Example 1						
Line	MCU		Information Direction	Display Module (IL79400A-XX)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 36. DCS Write Long Sequence – Example 2

DCS Write Long Sequence – Example 2						
Line	MCU		Information Direction	Display Module (IL79400A-XX)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 37. DCS Write Long Sequence – Example 3

DCS Write Long Sequence – Example 3						
Line	MCU		Information Direction	Display Module (IL79400A-XX)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	↔	BTA	--	Interface Control Change from MCU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	↔	BTA	--	Interface Control Change from the display module to MCU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	↔	BTA	--	
16	--	LP-11	→	--	--	End

4.4.3.2.4 DCS Read, No Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Read, No Parameter (DCSRN-S)" is defined in the section "4.4.3.2.1.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)" and example sequences on how this packet is used are described in following tables.

Table 38. DCS Read, No Parameter Sequence – Example 1

DCS Read, No Parameter Sequence – Example 1						
Line	MCU		Information Direction	Display Module (IL79400A-XX)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	SMRPS-S	HSDT	→	--	--	Defined how many data byte is wanted to read : 1 byte
3	DCSRN-S	HSDT	→	--	--	Wanted to get a response ID1 (DAh)
4	EoTP	HSDT	→	--	--	End of Transmission Packet
5	--	LP-11	→	--	--	
6	--	BTA	↔	BTA	--	Interface Control Change from MCU to the display module
7	--	--	←	LP-11	--	If No Error → Go to Line 9 If Error Occurs → Go to Line 14 If Error is Corrected by ECC → Go to Line 19
8	--	--	←	LPDT	DCSRR1-S	Response 1 byte return
9	--	--	←	LP-11	--	
10	--	BTA	↔	BTA	--	Interface Control Change from the display module to MCU
11	--	LP-11	→	--	--	End
12	--	--	←	LPDT	AwER	Error Report
13	--	--	←	LP-11	--	
14	--	BTA	↔	BTA	--	Interface Control Change from the display module to MCU
15	--	LP-11	→	--	--	End
16	--	--	←	LPDT	DCSRR1-S	Response 1 byte return
17	--	--	←	LPDT	AwER	Error Report (Error is corrected by ECC)
18	--	--	←	LP-11	--	
19	--	BTA	↔	BTA	--	Interface Control Change from the display module to MCU
20	--	LP-11	→	--	--	End
21	--	--	←	LPDT	AwER	Error Report
22	--	--	←	LP-11	--	
23	--	BTA	↔	BTA	--	Interface Control Change from the display module to MCU
24	--	LP-11	→	--	--	End

Table 39. DCS Read, No Parameter Sequence – Example 2

DCS Read, No Parameter Sequence – Example 2						
Line	MCU		Information Direction	Display Module (IL79400A-XX)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	SMRPS-S	HSDT	→	--	--	Defined how many data byte is wanted to read : 200 bytes
3	DCSRN-S	HSDT	→	--	--	Wanted to get a response
4	EoTP	HSDT	→	--	--	End of Transmission Packet
5	--	LP-11	→	--	--	
6	--	BTA	↔	BTA	--	Interface Control Change from MCU to the display module
7	--	--	←	LP-11	--	If No Error → Go to Line 9 If Error Occurs → Go to Line 14 If Error is Corrected by ECC → Go to Line 19
8	--	--	←	LPDT	DCSRR-L	Response 200 byte return
9	--	--	←	LP-11	--	
10	--	BTA	↔	BTA	--	Interface Control Change from the display module to MCU
11	--	LP-11	→	--	--	End
12	--	--	←	LPDT	AwER	Error Report

15	--	--	←	LP-11	--	
16	--	BTA	↔	BTA	--	Interface Control Change from the display module to MCU
17	--	LP-11	→	--	--	End
18						
19	--	--	←	LPDT	DCSRR-S	Response 200 byte return
20	--	--	←	LPDT	AwER	Error Report (Error is corrected by ECC)
21	--	--	←	LP-11	--	
22	--	BTA	↔	BTA	--	Interface Control Change from the display module to MCU
23	--	LP-11	→	--	--	End

4.4.3.3.2.5 Null Packet, No Data Sequence

A Long Packet (LPa) of "Null Packet, No Data (NP-L)" is defined in the section "4.4.3.2.1.6 Null Packet, No Data (NP-L)", and an example sequence on how this packet is used is described in the following table.

Table 40. Null Packet, No Data Sequence - Example

Line	MCU		Information Direction	Display Module (IL79400A-XX)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	NP-L	HSDT	→	--	--	Only High Speed Data Transmission is used
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

4.4.3.3.2.6 End of Transmission Packet

A Short Packet (SPa) of "End of Transmission (EoTP)" is defined in the section "4.4.3.2.1.7 End of Transmission Packet (EoTP)", and an example sequence on how this packet is used is described in the following table.

Table 41. End of Transmission Packet – Example

Line	MCU		Information Direction	Display Module (IL79400A-XX)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	NP-L	HSDT	→	--	--	Only High Speed Data Transmission is used
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

4.4.4 DSI Transmission Data Format

4.7.1.1. 24-bit per Pixel, Long Packet, Data Type = 11 1110 (3Eh)

Packed Pixel Stream 24-Bit Format is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed and non-displayed pixels) should be a multiple of three bytes.

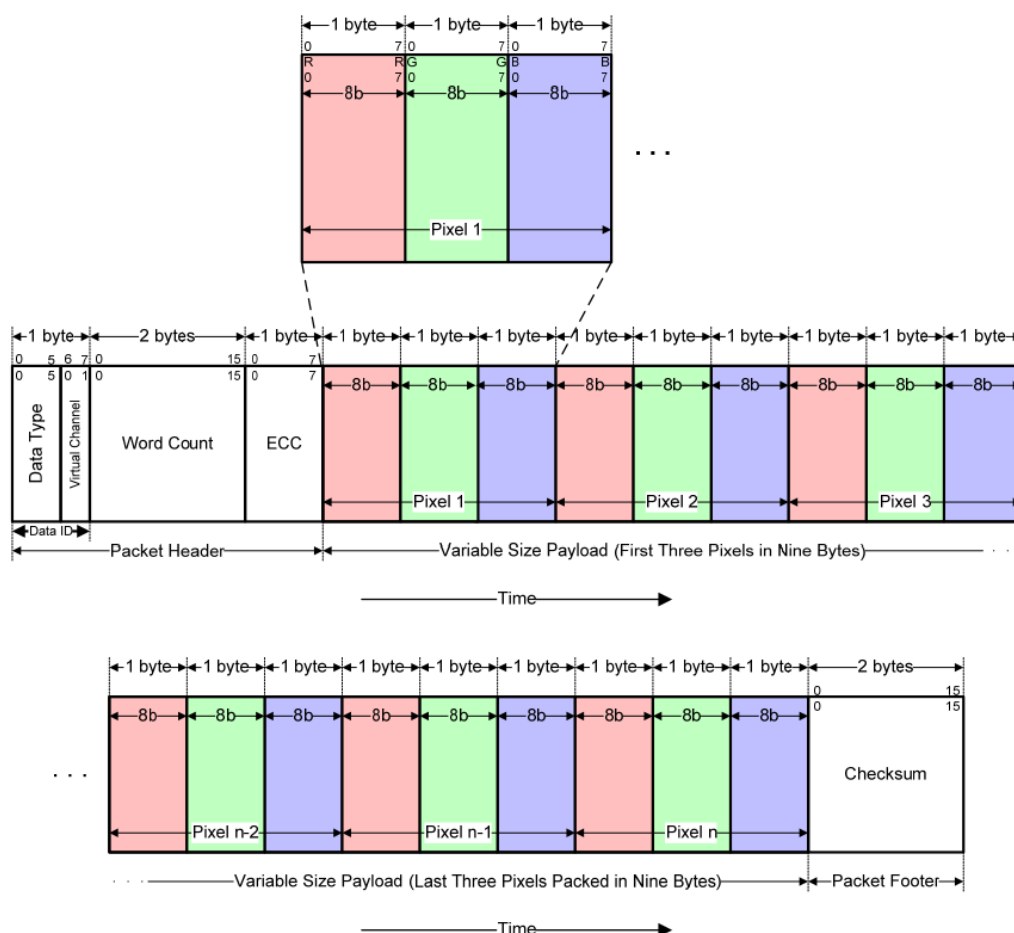


Figure 112. 24-bit per Pixel, Data Type = 11 1110 (3Eh)

5 Display Command

5.1 Command Flow

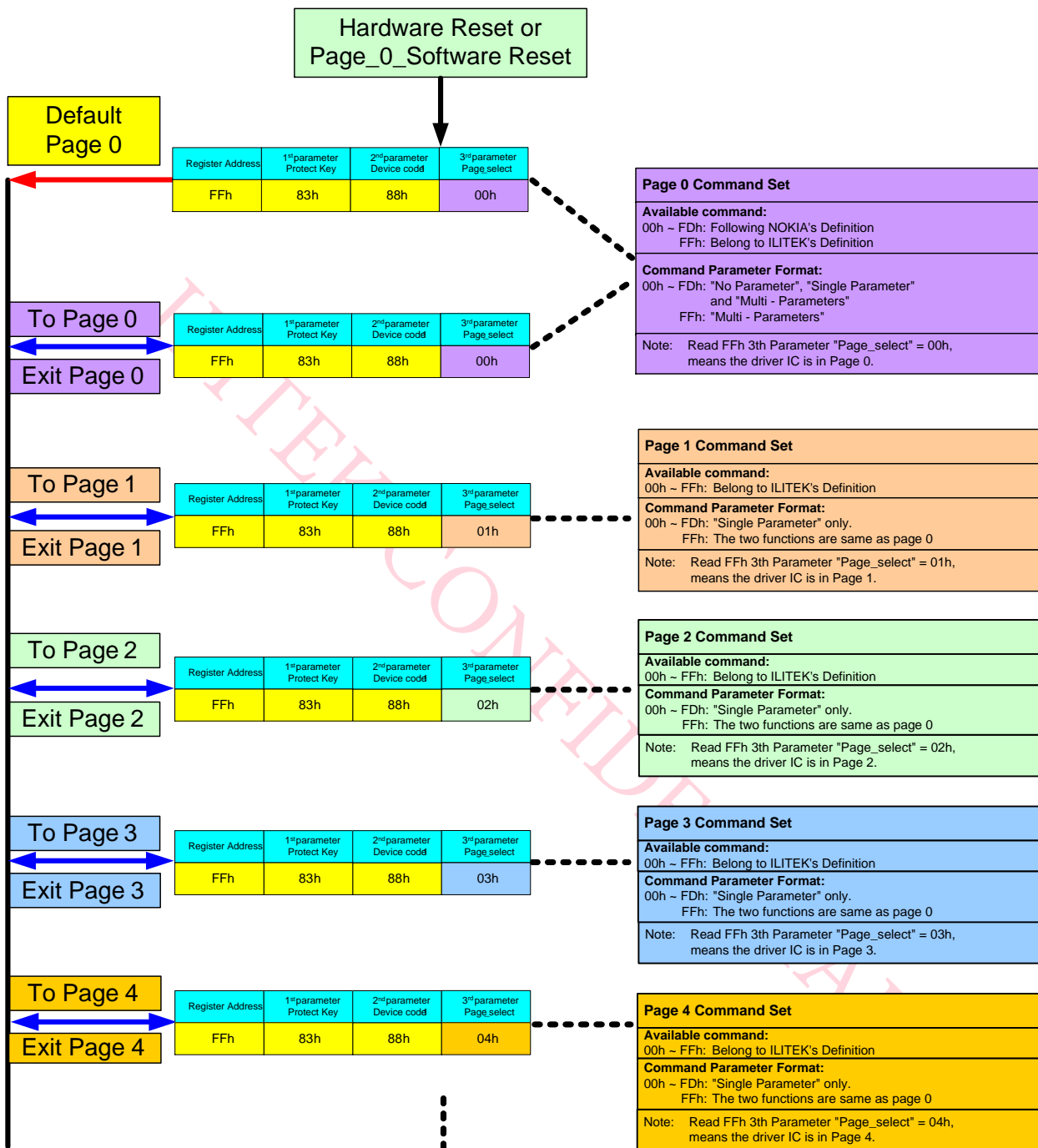


Figure 113. Command Flow

5.2 Command List

5.2.1 Page 0 Command Set

Table 42. Page 0 Command Set

Page	CMD	Para.	W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default
P0	00h	-	W	NOP	No Argument								-
P0	01h	-	W	Software Reset	No Argument								-
P0	05h	1st	R	Read Number of the Errors	P[7:0]								00h
P0	09h	1st	R	Read Display Status	D31	0	0	0	0	D26	0	D24	00h
		2nd	R		D23	IFPI[2:0]		D19	0	D17	D16	71h	
		3rd	R		0	0	D13	D12	D11	D10	D9	D8	00h
		4th	R		D7	D6	D5	0	0	0	0	D0	00h
P0	0Ah	1st	R	Read Display Power Mode	BVSTA	IDMON	0	SLPOUT	NORON	DSPON	0	0	08h
P0	0Bh	1st	R	Read Display MADCTL	MY	MX	0	0	RGB	0	SS	GS	00h
P0	0Ch	1st	R	Read Display Pixel Format	SPI_IFP_F_SEL	VIPF[2:0]			0	IFPI[2:0]			77h
P0	0Dh	1st	R	Read Display Image Mode	0	0	INVON	ALLPON	ALLPOFF	0	0	0	00h
P0	0Eh	1st	R	Read Display Signal Mode	TEON	TELOM	0	0	0	0	0	EODSI	00h
P0	0Fh	1st	R	Read Display Self-Diag. Result	REGLD	FUNDT	0	GLSBK	0	0	0	CHKSC	00h
P0	10h	-	W	Sleep In	No Argument								-
P0	11h	-	W	Sleep Out	No Argument								-
P0	13h	-	W	Normal Display Mode On	No Argument								-
P0	20h	-	W	Display Inversion Off	No Argument								-
P0	21h	-	W	Display Inversion On	No Argument								-
P0	22h	-	W	All Pixel Off	No Argument								-
P0	23h	-	W	All Pixel On	No Argument								-
P0	28h	-	W	Display Off	No Argument								-
P0	29h	-	W	Display On	No Argument								-
P0	2Ah	1st	W	Column Address Set	0	0	0	0	0	0	SC9	SC8	00h
		2nd	W		SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	00h
		3rd	W		0	0	0	0	0	0	EC9	EC9	1Fh
		4th	W		EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	8Fh
P0	2Bh	1st	W	Page Address Set	0	0	0	0	0	0	SP9	SP8	00h
		2nd	W		SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	00h
		3rd	W		0	0	0	0	0	0	EP9	EP9	1Fh
		4th	W		EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	8Fh
P0	2Ch	1st	W	Memory Write	D1[7:0]								XXh
		2nd	W		D2[7:0]								XXh
		:	:		:								XXh
		Nth	W		DN[7:0]								XXh
P0	34h	-	W	Tear Effect Line Off	No Argument								-
P0	35h	1st	W	Tear Effect Line On	0	0	0	0	0	0	0	M	00h
P0	36h	1st	W	Memory Access Control	0	0	0	0	0	0	SS	GS	00h
P0	38h	-	W	Idle Mode Off	No Argument								-
P0	39h	-	W	Idle Mode On	No Argument								-
P0	3Ah	1st	W	Interface Pixel Format	SPI_IFP_F_SEL	VIPF[2:0]			0	IFPF[2:0]			77h
P0	3Ch	1st	W	Memory Write Continue	D1[7:0]								XXh
		2nd	W		D2[7:0]								XXh
		:	:		:								XXh
		Nth	W		DN[7:0]								XXh
P0	44h	1st	W	Set Tear Scan Line	STS[15:8]								00h
		2nd	W		STS[7:0]								00h
P0	45h	1st	R	Get Tear Scan Line	GTS[15:8]								00h
		2nd	R		GTS[7:0]								00h
P0	51h	1st	W	Write Display Brightness	0	0	0	0	DBV[11:8]				00h
		2nd	W		DBV[7:0]								00h
P0	52h	1st	R	Read Display Brightness Value	0	0	0	0	DBV[11:8]				00h
		2nd	R		DBV[7:0]								00h
P0	53h	1st	W	Write Control Display	HBM[1:0]		BCTRL	0	DD	BL	0	0	00h
P0	54h	1st	R	Read Control Display value	HBM[1:0]		BCTRL	0	DD	BL	0	0	00h
P0	55h	1st	W	Write Power Save	0	0	0	0	0	0	PWRSV[1:0]		00h
P0	56h	1st	R	Read Power Save	0	0	0	0	BGR	0	PWRSV[1:0]		00h
P0	59h	-	W	Stop Transition	No Argument								-
P0	5Eh	1st	W	Write CABC Minimum Brightness	0	0	0	0	CMB[11:8]				00h
		2nd	W		CMB[7:0]								00h
P0	5Fh	1st	R	Read CABC Minimum Brightness	0	0	0	0	CMB[11:8]				00h
		2nd	R		CMB[7:0]								00h
P0	68h	1st	W	Set Transition	TT_STP[7:0]								00h
		2nd	W		ST_TIM[7:0]								00h
P0	69h	1st	R	Get Transition	TT_STP[7:0]								00h
		2nd	R		ST_TIM[7:0]								00h
P0	A1h	1st	R	Read DDB Start	SID[7:0]								00h
		2nd			SID[15:8]								00h
		3rd			MID[7:0]								00h
		4th			MID[15:8]								00h
		5th			RID[7:0]								00h
		6th			RID[15:8]								00h
		7th			1	1	1	1	1	1	1	1	FFh
P0	A8h	1st	R	Read DDB Continue	D1[7:0]								00h
		2nd			D2[7:0]								00h
		:			:								:
		Nth			DN[7:0]								00h

Table 43. Page 0 Command Set (Continued)

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Page	CMD	Para.	W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default
P0	AAh	1st	R	Read First Checksum	FCS[7:0]								00h
P0	AFh	1st	R	Read Continue Checksum	CCS[7:0]								00h
P0	C2h	1st	W/R	Set DISP Mode	0	0	0	0	0	0	DM[1:0]		00h
P0	C4h	1st	W/R	Set DISP Mode	SPI_WRA M	0	DSPI_C FG	DSP_C G0	0	0	0	DSPI_EN	00h
P0	DAh	1st	R	Read ID1	ID1[7:0]								00h
P0	DBh	1st	R	Read ID2	ID2[7:0]								00h
P0	DCh	1st	R	Read ID3	ID3[7:0]								00h
P0	FDh	1st	W	Read EXTC CMD In SPI Mode	0	0	0	0	0	0	0	0	00h
		2nd	W		EXT_SPI_ READ_EN	EXT_SPI_CNT[6:0]							00h
		3rd	W		0	0	0	0	0	0	0	0	00h
P0	FFh	1st	W	EXTC CMD Set Enable	1	0	0	0	0	0	1	1	83h
		2nd	W		8	0	0	0	1	0	0	0	88h
		3rd	W		PAGE[7:0]								00h

Notes:

- Undefined commands are treated as NOP (00h) command.
- Commands 10h, 12h, 13h, 28h, 29h, 30h, 36h, 38h, 39h, 44h, 45h, 51h, 53h and 55h, are updated during V-SYNC when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read Number of the Errors on DSI (05h), Read Display Power Mode (0Ah), Read Display MADCTL (0Bh), Read Display Pixel Format (0Ch), Read Display Signal Mode (0Eh), Read Display Self-Diagnostic Result (0Fh), Get Tear Scan Line (45h), Read Display Brightness Value (52h), Read CTRL Value Display (54h), Read Power Save (56h) of these commands is updated immediately both in Sleep In mode and Sleep Out mode.

5.3 Page 0 Command Description

5.3.1 NOP (00h)

Table 44. NOP (00h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	0	0	0	0	0	0	00h
1 st Para	-	No Argument								-
Description	This command is an empty command; it does not have any effect on this IC.									
Restriction	None									
Register Availability			Status				Availability			
			Normal Mode On, Idle Mode Off, Sleep Out				Yes			
			Normal Mode On, Idle Mode On, Sleep Out				Yes			
			Idle Mode Off, Sleep Out				Yes			
			Idle Mode On, Sleep Out				Yes			
			Sleep In				Yes			
Default			Status		Default Value					
			Power On Sequence		N/A					
			S/W Reset		N/A					
			H/W Reset		N/A					

5.3.2 Software Reset (01h)

Table 45. Software Reset (01h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	0	0	0	0	0	0	1	01h												
1 st Para	-	No Argument								-												
Description	When the Software Reset command (01h) is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description). The display is blank immediately.																					
Restriction	It is necessary to wait 10msec before sending a new command following software reset. The display module loads all display suppliers' factory default values to the registers during this 5msec. If Software Reset command (01h) is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command (11h). The Software Reset command (01h) cannot be sent during Sleep Out sequence.																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table>										Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A				
Status	Default Value																					
Power On Sequence	N/A																					
S/W Reset	N/A																					
H/W Reset	N/A																					
Flow Chart	<div><div><div>SWRESET (01h)</div><div>Display whole blank screen</div><div>Set Commands to S/W Default Value</div><div>Sleep In Mode</div></div><div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																					

5.3.3 Read Number of the Errors on DSI (05h)

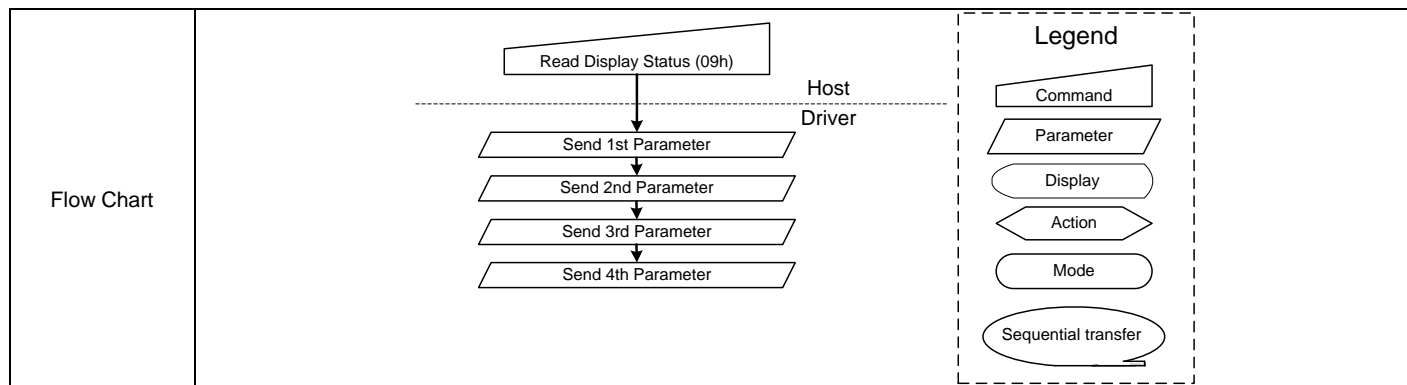
Table 46. Read Number of the Errors on DSI (05h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	0	0	0	0	1	0	1	05h												
1 st Para	Read	P[7:0]								00h												
Description	The 1st parameter tells the number of errors on DSI. The more detailed description of this parameter is below. P[6:0] tells the number of the errors. P[7] is set to '1' if there is overflow with P[6:0]. P[7:0] is set to '0's (as well as Read Display Signal Mode command (0Eh)'s D0 is set '0' at the same time) after the parameter information is sent (read cmd. 05h is completed).																					
Restriction	None																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>										Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value																					
Power On Sequence	00h																					
S/W Reset	00h																					
H/W Reset	00h																					
Flow Chart	<div><div><div>RDNUMED(05h)</div><div>↓</div><div>P[7:0] = 00h RDDSM(0Eh)'s D0 = '0'</div></div><div>Host ----- Driver</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																					

5.3.4 Read Display Status (09h)

Table 47. Read Display Status (09h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default													
Command	Write	0	0	0	0	1	0	0	1	09h													
1 st Para	Read	D31	D30	D29	0	0	D26	0	D24	00h													
2 nd Para	Read	D23	D22	D21	D20	D19	0	D17	D16	71h													
3 rd Para	Read	0	0	D13	D12	D11	D10	D9	0	00h													
4 th Para	Read	0	D6	D5	0	0	0	0	D0	00h													
Description	This command indicates the current status of the display, as described in the table below.																						
	Bit	Description	Value		Status																		
	D31	Sleep In/Out	0		Booster Off																		
			1		Booster On																		
	D30	MY	0		Top to Bottom (When MADCTL D7='0')																		
			1		Bottom to Top (When MADCTL D7='1')																		
	D29	MX	0		Left to Right (When MADCTL D6='0')																		
			1		Right to Left (When MADCTL D6='1')																		
	D26	BGR (RGB/BGR order)	0		RGB																		
			1		BGR																		
	D24	SS (Source Scan sequence)	0		Source output Left to Right																		
			1		Source output Right to Left																		
	D23	GS (Gate Scan sequence)	0		Gate output Top to Bottom																		
			1		Gate output Bottom to Top																		
	D22 ~ D20		IFPF[2:0]		Refer to CMD 3Ah																		
	D19	Idle Mode On/Off	0		Idle Mode Off																		
			1		Idle Mode On																		
	D17	Sleep In/Out	0		Sleep In Mode																		
			1		Sleep Out Mode																		
	D16	Display Normal Mode On/Off	0		Display Normal Mode Off (All Pixels Off or All Pixels On mode)																		
			1		Display Normal Mode On																		
	D13	Inversion On/Off	0		Inversion Off																		
			1		Inversion On																		
	D12	All Pixel On	0		Normal mode																		
			1		All Pixels On																		
	D11	All Pixel Off	0		Normal mode																		
			1		All Pixels Off																		
	D10	Display On/Off	0		Display is OFF																		
			1		Display is ON																		
	D9	TE On/Off	0		Tearing Effect Line OFF																		
			1		Tearing Effect Line ON																		
	D5	TE Mode	0		Tearing Effect Line Mode 1																		
			1		Tearing Effect Line Mode 2																		
	D0	Parity Error on DSI	0		No Parity Error																		
			1		Parity Error																		
Note: For D26, D24 and D23 definition refer to Memory Access Control command (36h).																							
Restriction	None																						
Register Availability	<table><tr><th colspan="2">Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status		Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
											Status		Availability										
											Normal Mode On, Idle Mode Off, Sleep Out	Yes											
											Normal Mode On, Idle Mode On, Sleep Out	Yes											
											Idle Mode Off, Sleep Out	Yes											
											Idle Mode On, Sleep Out	Yes											
Sleep In	Yes																						
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h, 71h, 00h, 00h</td></tr><tr><td>S/W Reset</td><td>00h, 71h, 00h, 00h</td></tr><tr><td>H/W Reset</td><td>00h, 71h, 00h, 00h</td></tr></table>										Status	Default Value	Power On Sequence	00h, 71h, 00h, 00h	S/W Reset	00h, 71h, 00h, 00h	H/W Reset	00h, 71h, 00h, 00h					
											Status	Default Value											
											Power On Sequence	00h, 71h, 00h, 00h											
											S/W Reset	00h, 71h, 00h, 00h											
H/W Reset	00h, 71h, 00h, 00h																						



5.3.5 Read Display Power Mode (0Ah)

Table 48. Read Display Power Mode (0Ah)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	0	0	0	1	0	1	0	0Ah												
1 st Para	Read	BVSTA	IDMON	0	SLPOUT	NORON	DSPON	0	0	08h												
Description	This command indicates the current status of the display as described in the table below.																					
	Bit	Description				Value	Status															
	D7	Booster Voltage Status				0	Booster Off or Has a fault															
						1	Booster On and Working OK															
	D6	Idle Mode On/Off				0	Idle Mode Off															
						1	Idle Mode On															
	D4	Sleep In/Out				0	Sleep In Mode															
						1	Sleep Out Mode															
	D3	Display Normal Mode On/Off				0	Display Normal Mode Off															
						1	Display Normal Mode On															
D2	Display On/Off				0	Display Off																
					1	Display On																
Restriction	None																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>08h</td></tr><tr><td>S/W Reset</td><td>08h</td></tr><tr><td>H/W Reset</td><td>08h</td></tr></table>										Status	Default Value	Power On Sequence	08h	S/W Reset	08h	H/W Reset	08h				
Status	Default Value																					
Power On Sequence	08h																					
S/W Reset	08h																					
H/W Reset	08h																					
Flow Chart	<div><div><div>Serial I/F Mode</div><div><div>RDDPM (0Ah)</div><div>Send D[7:0]</div></div></div><div><div>Parallel I/F Mode</div><div><div>RDDPM (0Ah)</div><div>Dummy Read</div><div>Send D[7:0]</div></div></div><div><div>Host Driver</div></div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																					

5.3.6 Read Display MADCTL (0Bh)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	0	0	0	1	0	1	1	0Bh												
1 st Para	Read	MY	MX	0	0	BGR	0	SS	GS	00h												
Description	This command depends on Memory Access Control command (36h) and indicates the current status of the display as described in the table below.																					
	Bit	Description	Value	Status																		
	D7	MY	0	Top to Bottom (When MADCTL D7='0')																		
			1	Bottom to Top (When MADCTL D7='1')																		
	D6	MX	0	Left to Right (When MADCTL D6='0')																		
			1	Right to Left (When MADCTL D6='1')																		
	D3	RGB	0	RGB (When MADCTL D3='0')																		
			1	BGR (When MADCTL D3='1')																		
	D1	SS	0	Source output Left to Right (When MADCTL D1='0')																		
			1	Source output Right to Left (When MADCTL D1='1')																		
	D0	GS	0	Gate output Top to Bottom (When MADCTL D0='0')																		
			1	Gate output Bottom to Top (When MADCTL D0='1')																		
Restriction	None																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>										Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value																					
Power On Sequence	00h																					
S/W Reset	00h																					
H/W Reset	00h																					
Flow Chart	<div><div><div>Serial I/F Mode</div><div><div>RDDMADCTL (0Bh)</div><div>↓</div><div>Send D[7:0]</div></div></div><div><div>Parallel I/F Mode</div><div><div>RDDMADCTL (0Bh)</div><div>↓</div><div>Dummy Read</div><div>↓</div><div>Send D[7:0]</div></div></div><div><div>Host Driver</div></div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																					

5.3.7 Read Display Pixel Format (0Ch)

Table 49. Read Display Pixel Format (0Ch)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default																																								
Command	Write	0	0	0	0	1	1	0	0	0Ch																																								
1 st Para	Read	SPI_IFPF_SEL	VIPF[2:0]			0	IFPF[2:0]			77h																																								
Description	<p>To return the status of Interface Pixel Format (3Ah).</p> <p>This command sets the pixel format for the RGB image data used by the interface.</p> <p>If SPI_IFPF_SEL(3Ah_D7) = 1: The VIPF[2:0] can be used to set pixel format by the SPI / Q-SPI interface, the IFPF[2:0] can be used to set pixel format by the MCU / MIPI interface.</p> <p>If SPI_IFPF_SEL(3Ah_D7) = 0: The IFPF[2:0] can be used to set pixel format by the SPI / Q-SPI / MCU / MIPI interface.</p> <p>VIPF[2:0]: Pixel format for SPI / Q-SPI interface(SPI_IFPF_SEL = 1)</p> <table><tr><th>Control Interface Color Format</th><th>VIPF[2]</th><th>VIPF[1]</th><th>VIPF[0]</th></tr><tr><td>8-bits / pixel (256 colors) (including SPI3 / SPI4 / Q-SPI)</td><td>0</td><td>1</td><td>0</td></tr><tr><td>16-bits / pixel (65,536 colors) (including SPI3 / SPI4 / Q-SPI)</td><td>1</td><td>0</td><td>1</td></tr><tr><td>18-bits / pixel (262,144 colors) (including SPI3 / SPI4 / Q-SPI)</td><td>1</td><td>1</td><td>0</td></tr><tr><td>24-bits / pixel (16.7M colors) (including SPI3 / SPI4 / Q-SPI)</td><td>1</td><td>1</td><td>1</td></tr></table> <p>IFPF[2:0]: Pixel format for SPI / Q-SPI / MCU / MIPI interface(SPI_IFPF_SEL = 0)</p> <table><tr><th>Control Interface Color Format</th><th>IFPF[2]</th><th>IFPF[1]</th><th>IFPF[0]</th></tr><tr><td>8-bits / pixel (256 colors) (including SPI3 / SPI4 / Q-SPI)</td><td>0</td><td>1</td><td>0</td></tr><tr><td>16-bits / pixel (65,536 colors) (including SPI3 / SPI4 / Q-SPI / MCU / MIPI)</td><td>1</td><td>0</td><td>1</td></tr><tr><td>18-bits / pixel (262,144 colors) (including SPI3 / SPI4 / Q-SPI / MCU / MIPI)</td><td>1</td><td>1</td><td>0</td></tr><tr><td>24-bits / pixel (16.7M colors) (including SPI3 / SPI4 / Q-SPI / MCU / MIPI)</td><td>1</td><td>1</td><td>1</td></tr></table>										Control Interface Color Format	VIPF[2]	VIPF[1]	VIPF[0]	8-bits / pixel (256 colors) (including SPI3 / SPI4 / Q-SPI)	0	1	0	16-bits / pixel (65,536 colors) (including SPI3 / SPI4 / Q-SPI)	1	0	1	18-bits / pixel (262,144 colors) (including SPI3 / SPI4 / Q-SPI)	1	1	0	24-bits / pixel (16.7M colors) (including SPI3 / SPI4 / Q-SPI)	1	1	1	Control Interface Color Format	IFPF[2]	IFPF[1]	IFPF[0]	8-bits / pixel (256 colors) (including SPI3 / SPI4 / Q-SPI)	0	1	0	16-bits / pixel (65,536 colors) (including SPI3 / SPI4 / Q-SPI / MCU / MIPI)	1	0	1	18-bits / pixel (262,144 colors) (including SPI3 / SPI4 / Q-SPI / MCU / MIPI)	1	1	0	24-bits / pixel (16.7M colors) (including SPI3 / SPI4 / Q-SPI / MCU / MIPI)	1	1	1
	Control Interface Color Format	VIPF[2]	VIPF[1]	VIPF[0]																																														
	8-bits / pixel (256 colors) (including SPI3 / SPI4 / Q-SPI)	0	1	0																																														
	16-bits / pixel (65,536 colors) (including SPI3 / SPI4 / Q-SPI)	1	0	1																																														
	18-bits / pixel (262,144 colors) (including SPI3 / SPI4 / Q-SPI)	1	1	0																																														
24-bits / pixel (16.7M colors) (including SPI3 / SPI4 / Q-SPI)	1	1	1																																															
Control Interface Color Format	IFPF[2]	IFPF[1]	IFPF[0]																																															
8-bits / pixel (256 colors) (including SPI3 / SPI4 / Q-SPI)	0	1	0																																															
16-bits / pixel (65,536 colors) (including SPI3 / SPI4 / Q-SPI / MCU / MIPI)	1	0	1																																															
18-bits / pixel (262,144 colors) (including SPI3 / SPI4 / Q-SPI / MCU / MIPI)	1	1	0																																															
24-bits / pixel (16.7M colors) (including SPI3 / SPI4 / Q-SPI / MCU / MIPI)	1	1	1																																															
Restriction	None																																																	
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes																												
Status	Availability																																																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																																																	
Idle Mode Off, Sleep Out	Yes																																																	
Idle Mode On, Sleep Out	Yes																																																	
Sleep In	Yes																																																	
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>77h</td></tr><tr><td>S/W Reset</td><td>77h</td></tr><tr><td>H/W Reset</td><td>77h</td></tr></table>										Status	Default Value	Power On Sequence	77h	S/W Reset	77h	H/W Reset	77h																																
Status	Default Value																																																	
Power On Sequence	77h																																																	
S/W Reset	77h																																																	
H/W Reset	77h																																																	
Flow Chart	<div><div><div><div>Serial I/F Mode</div><div><div>RDDCOLMOD (0Ch)</div><div>Send D[7:0]</div></div></div><div><div>Parallel I/F Mode</div><div><div>RDDCOLMOD (0Ch)</div><div>Dummy Read</div><div>Send D[7:0]</div></div></div></div><div><div>Host Driver</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																																																	

5.3.8 Read Display Image Mode (0Dh)

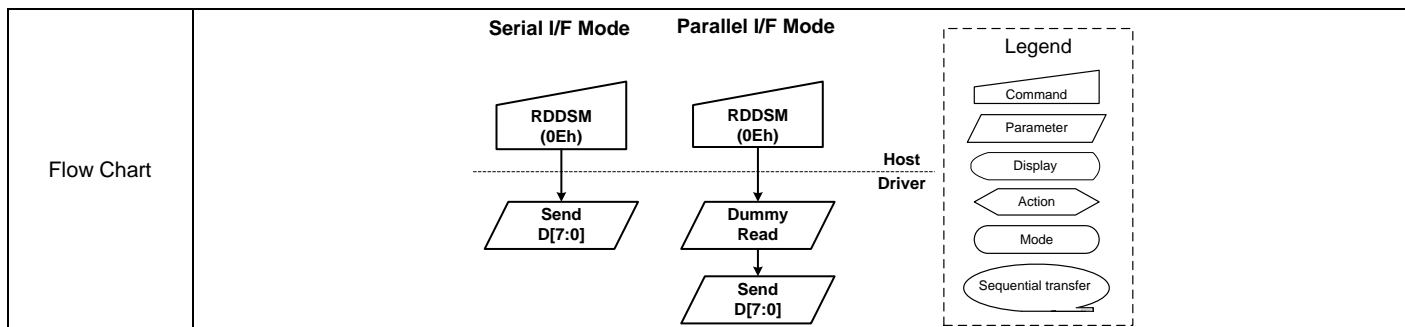
Table 50. Read Display Image Mode (0Dh)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	0	0	0	1	1	0	1	0Dh												
1 st Para	Read	0	0	INVON	ALLPON	ALLPOFF	0	0	0	00h												
Description	This command indicates the Image Mode status of the display as described in the table below :																					
	Bit	Description			Value		Status															
	D5	INVON			0		Inversion Off															
					1		Inversion On															
	D4	All Pixels On			0		Normal Display															
					1		White Display															
	D3	All Pixels Off			0		Normal Display															
					1		Black Display															
Restriction	None																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>										Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value																					
Power On Sequence	00h																					
S/W Reset	00h																					
H/W Reset	00h																					
Flow Chart	<div><div><div>Read RDDIM (0Dh)</div><div>↓</div><div>Send Parameter</div></div><div>Host Driver</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																					

5.3.9 Read Display Signal Mode (0Eh)

Table 51. Read Display Signal Mode (0Eh)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default																		
Command	Write	0	0	0	0	1	1	1	0	0Eh																		
1 st Para	Read	TEON	TELOM	0	0	0	0	0	EODSI	00h																		
Description	This command indicates the current status of the display as described in the table below.																											
	Bit	Description				Value		Status																				
	D7	Tearing Effect Line On/Off				0		Tearing Effect Line Off																				
						1		Tearing Effect Line On																				
	D6	Tearing Effect Line Output Mode				0		Tearing Effect Line Mode 1																				
						1		Tearing Effect Line Mode 2																				
	D0	Error on DSI				0		No Error on DSI																				
						1		Error on DSI																				
Restriction	None																											
Register Availability	<table><tr><th colspan="2">Status</th><th>Availability</th></tr><tr><td colspan="2">Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td colspan="2">Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td colspan="2">Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td colspan="2">Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td colspan="2">Sleep In</td><td>Yes</td></tr></table>										Status		Availability	Normal Mode On, Idle Mode Off, Sleep Out		Yes	Normal Mode On, Idle Mode On, Sleep Out		Yes	Idle Mode Off, Sleep Out		Yes	Idle Mode On, Sleep Out		Yes	Sleep In		Yes
											Status		Availability															
											Normal Mode On, Idle Mode Off, Sleep Out		Yes															
											Normal Mode On, Idle Mode On, Sleep Out		Yes															
											Idle Mode Off, Sleep Out		Yes															
											Idle Mode On, Sleep Out		Yes															
Sleep In		Yes																										
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>										Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h										
											Status	Default Value																
											Power On Sequence	00h																
											S/W Reset	00h																
H/W Reset	00h																											



5.3.10 Read Display Self-Diagnostic Result (0Fh)

Table 52. Read Display Self-Diagnostic Result (0Fh)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	0	0	0	1	1	1	1	0Fh												
1 st Para	Read	REGLD	FUNDT	0	0	0	0	0	CHKSC	00h												
Description	This command indicates the status of the display self-diagnostic results after Sleep Out command (11h) as described in the table below.																					
	Bit	Description				Action																
	D7	Register Loading Detection				Invert the D7 bit when the NVM and register values are same.																
	D6	Functionality Detection				Invert the D6 bit when the chip met User's functionality requirements																
	D0	Checksums Comparison				'0' = Checksums are same '1' = Checksums are not same																
Restriction	None																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability																				
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>										Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
	Status	Default Value																				
Power On Sequence	00h																					
S/W Reset	00h																					
H/W Reset	00h																					
Flow Chart	<div><div><div>Serial I/F Mode</div><div><div>RDDSDR (0Fh)</div><div>↓</div><div>Send D[7:0]</div></div></div><div><div>Parallel I/F Mode</div><div><div>RDDSDR (0Fh)</div><div>↓</div><div>Dummy Read</div><div>↓</div><div>Send D[7:0]</div></div></div><div><div>Host Driver</div></div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																					

5.3.11 Sleep In (10h)

Table 53. Sleep In (10h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	0	0	1	0	0	0	0	10h												
1 st Para	-	No Argument								-												
Description	<p>This command causes the IL79400A-XX to enter the minimum power consumption mode. In this mode, the DC/DC converter, Internal oscillator, and panel scanning are all stopped.</p> <div><div>OUT</div><div>Blank</div><div>STOP</div></div> <p>MIPI DSI and MCU interface and memory are still working and the memory can or cannot keep its contents. Ambient light based control is off. Backlights, display and keyboard, are off. Dimming function does not work when there is changing mode from Sleep Out to Sleep In.</p>																					
Restriction	<p>This command has no effect when the module is already in the Sleep In mode. To leave the Sleep In mode, only the Sleep Out Command (11h) is workable. It is necessary to wait 10msec before sending the next command; this is to allow time for the supply voltages and clock circuits to become stable. It is necessary to wait 200msec after sending the Sleep Out command (when in the Sleep In Mode) before the Sleep In command can be sent.</p>																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep In Mode</td></tr><tr><td>S/W Reset</td><td>Sleep In Mode</td></tr><tr><td>H/W Reset</td><td>Sleep In Mode</td></tr></table>										Status	Default Value	Power On Sequence	Sleep In Mode	S/W Reset	Sleep In Mode	H/W Reset	Sleep In Mode				
Status	Default Value																					
Power On Sequence	Sleep In Mode																					
S/W Reset	Sleep In Mode																					
H/W Reset	Sleep In Mode																					
Flow Chart	<div><div><div>SLPIN (10h)</div><div>Display whole blank screen (Automatic No effect to DISP ON/OFF commands)</div><div>Drain charge from LCD panel</div></div><div><div>Stop DC/DC Converter</div><div>Stop Internal Oscillator</div><div>Sleep In Mode</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																					

5.3.12 Sleep Out (11h)

Table 54. Sleep Out (11h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	0	0	1	0	0	0	1	11h												
1 st Para	-	No Argument								-												
Description	This command turns off sleep mode. In this mode e.g. the DC/DC converter is enabled, DDI's Internal oscillator is started, and panel scanning is started. <div><div>OUT</div><div>STOP</div><div>Blank</div><div>Memory Contents (DISPON 29h is set)</div></div>																					
Restriction	This command has no effect when module is already in Sleep Out mode. Sleep Out mode can be left by the Sleep In command (10h), S/W reset command (01h) or H/W reset. It is necessary to wait 10msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. The IL79400A-XX loads all display supplier's factory default values to the registers during this 10msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the IL79400A-XX is already Sleep Out mode. During this 10msec, IL79400A-XX is running self-diagnostic functions. It is necessary to wait 200msec after sending the Sleep In command (when in Sleep Out mode) before the Sleep Out command can be sent																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep In Mode</td></tr><tr><td>S/W Reset</td><td>Sleep In Mode</td></tr><tr><td>H/W Reset</td><td>Sleep In Mode</td></tr></table>										Status	Default Value	Power On Sequence	Sleep In Mode	S/W Reset	Sleep In Mode	H/W Reset	Sleep In Mode				
Status	Default Value																					
Power On Sequence	Sleep In Mode																					
S/W Reset	Sleep In Mode																					
H/W Reset	Sleep In Mode																					
Flow Chart	<div><div><div>SLPOUT (11h)</div><div>Start Internal Oscillator</div><div>Start up DC-DC Converter</div><div>Charge Offset Voltage for LCD Panel</div></div><div><div>Display whole blank screen for 2 frames (Automatic No effect to DISP ON/OFF Commands)</div><div>Display Memory contents in accordance with the current command table settings</div><div>Sleep Out Mode</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																					

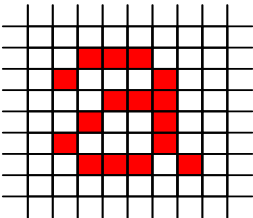
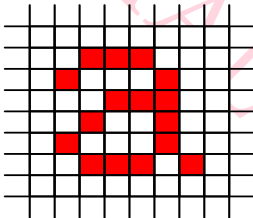
5.3.13 Normal Display Mode On (13h)

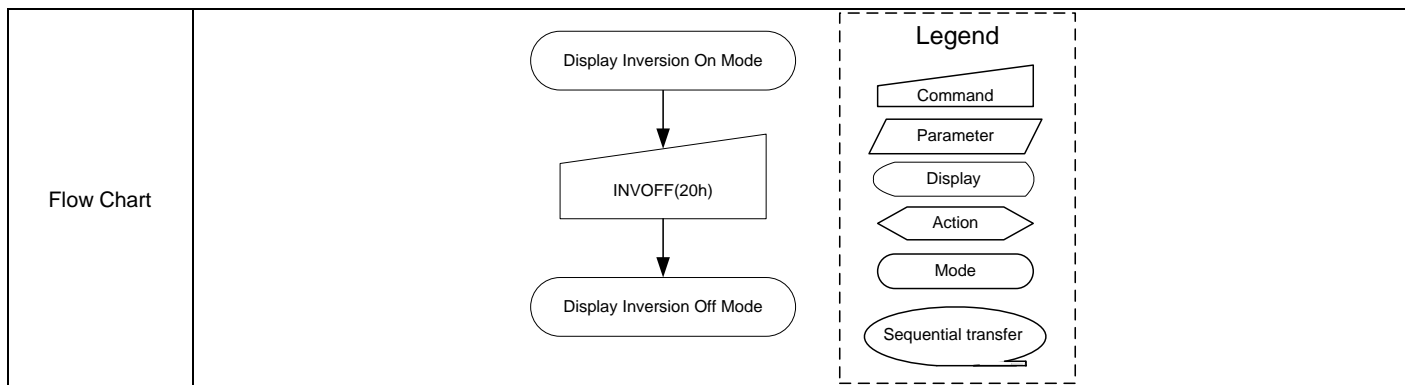
Table 55. Normal Display Mode On (13h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	0	0	1	0	0	1	1	13h												
1 st Para	-	No Argument								-												
Description	This command return the display to the Normal Display Mode. Using this command to exit All Pixel Off Mode (22h) and All Pixel On Mode (23h) into Normal Display Mode.																					
Restriction	This command has no effect when Normal Display Mode is active.																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode On</td></tr><tr><td>S/W Reset</td><td>Normal Display Mode On</td></tr><tr><td>H/W Reset</td><td>Normal Display Mode On</td></tr></table>										Status	Default Value	Power On Sequence	Normal Display Mode On	S/W Reset	Normal Display Mode On	H/W Reset	Normal Display Mode On				
Status	Default Value																					
Power On Sequence	Normal Display Mode On																					
S/W Reset	Normal Display Mode On																					
H/W Reset	Normal Display Mode On																					
Flow Chart	<div><div><div>All Pixel Off/On Mode</div><div>NORON(13h)</div><div>Normal Display Mode</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																					

5.3.14 Display Inversion Off (20h)

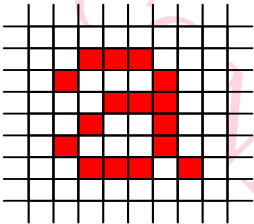
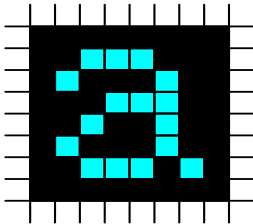
Table 56. Display Inversion Off (20h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	0	1	0	0	0	0	0	20h												
1 st Para	-	No Argument								-												
Description	This command is used to recover from Display Inversion On mode. This command doesn't change any other status.																					
	<div><div><div>Before</div></div><div>→</div><div><div>After</div></div></div>																					
Restriction	This command has no effect when module is already in Display Inversion Off mode.																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Off</td></tr><tr><td>S/W Reset</td><td>Display Off</td></tr><tr><td>H/W Reset</td><td>Display Off</td></tr></table>										Status	Default Value	Power On Sequence	Display Off	S/W Reset	Display Off	H/W Reset	Display Off				
Status	Default Value																					
Power On Sequence	Display Off																					
S/W Reset	Display Off																					
H/W Reset	Display Off																					



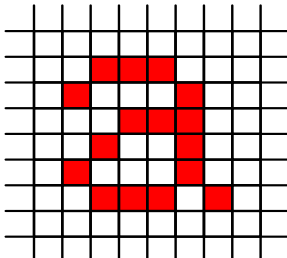
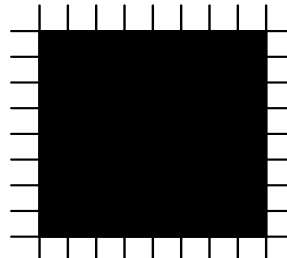
5.3.15 Display Inversion On (21h)

Table 57. Display Inversion On (21h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	0	1	0	0	0	0	1	21h												
1 st Para	-	No Argument								-												
Description	<p>This command is used to enter into Display Inversion On mode. This command doesn't change any other status. To exit Display Inversion On mode, the Display Inversion Off command (20h) should be written.</p> <div><div>Before</div><div></div><div>→</div><div><div>After</div><div></div></div></div>																					
Restriction	This command has no effect when module is already in Display Inversion Off mode.																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Off</td></tr><tr><td>S/W Reset</td><td>Display Off</td></tr><tr><td>H/W Reset</td><td>Display Off</td></tr></table>										Status	Default Value	Power On Sequence	Display Off	S/W Reset	Display Off	H/W Reset	Display Off				
Status	Default Value																					
Power On Sequence	Display Off																					
S/W Reset	Display Off																					
H/W Reset	Display Off																					
Flow Chart	<div><div><div>Display Inversion Off Mode</div><div>↓</div><div>INVON(21h)</div><div>↓</div><div>Display Inversion On Mode</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																					

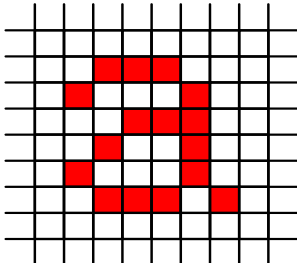
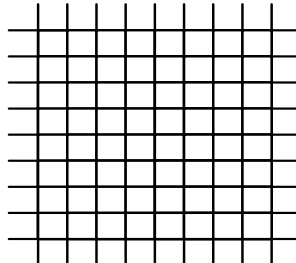
5.3.16 All Pixel Off (22h)

Table 58. All Pixel Off (22h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	0	1	0	0	0	1	0	22h												
1 st Para	-	No Argument								-												
Description	<p>This command turns the display panel black in Sleep Out Mode and a status bit of the Read Display Image Mode command (0Dh) can be read. This command does not change any other status.</p> <div><div>Before</div><div></div><div>→</div><div><div>After</div><div></div></div></div> <p>All Pixels On command (23h) and Normal Display Mode On command (13h) are used to leave All Pixel Off Mode.</p>																					
Restriction	This command has no effect when the module is already in the Display Off mode..																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Off</td></tr><tr><td>S/W Reset</td><td>Display Off</td></tr><tr><td>H/W Reset</td><td>Display Off</td></tr></table>										Status	Default Value	Power On Sequence	Display Off	S/W Reset	Display Off	H/W Reset	Display Off				
Status	Default Value																					
Power On Sequence	Display Off																					
S/W Reset	Display Off																					
H/W Reset	Display Off																					
Flow Chart	<div><div><div>Normal Display Mode On</div><div>↓</div><div>ALLPOFF (22h)</div><div>↓</div><div>Black Display</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																					

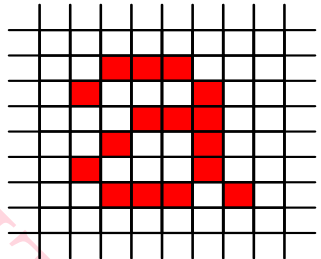
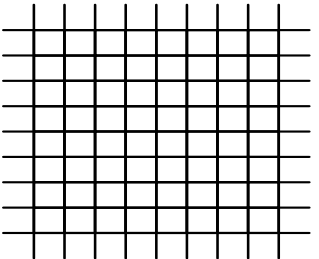
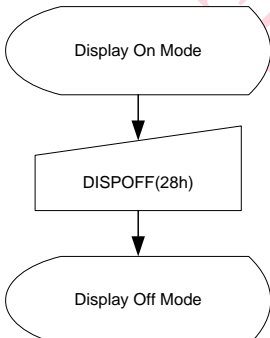
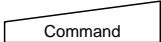
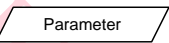

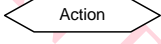
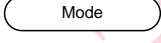
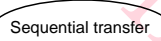
5.3.17 All Pixel On (23h)

Table 59. All Pixel On (23h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	0	1	0	0	0	1	1	23h												
1 st Para	-	No Argument								-												
Description	<p>This command turns the display panel white in Sleep Out Mode and a status bit of the Read Display Image Mode command (0Dh) can be read. This command does not change any other status.</p> <div><div>Before</div><div></div><div>→</div><div><div>After</div><div></div></div><p>All Pixels Off command (22h) and Normal Display Mode On command (13h) are used to leave All Pixel On Mode.</p></div>																					
Restriction	This command has no effect when the module is already in the Display Off mode.																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Off</td></tr><tr><td>S/W Reset</td><td>Display Off</td></tr><tr><td>H/W Reset</td><td>Display Off</td></tr></table>										Status	Default Value	Power On Sequence	Display Off	S/W Reset	Display Off	H/W Reset	Display Off				
Status	Default Value																					
Power On Sequence	Display Off																					
S/W Reset	Display Off																					
H/W Reset	Display Off																					
Flow Chart	<div><div><div>Normal Display Mode On</div><div>↓</div><div>ALLPON (23h)</div><div>↓</div><div>White Display</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																					

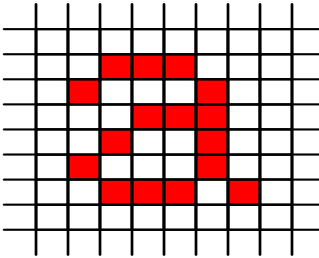
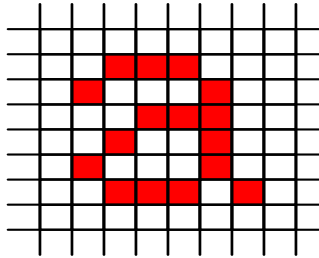
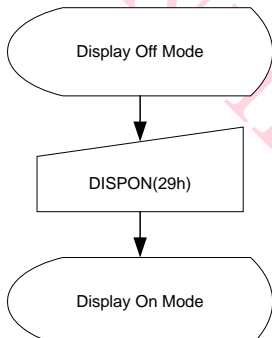
5.3.18 Display Off (28h)

Table 60. Display Off (28h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	0	1	0	1	0	0	0	28h												
1 st Para	-	No Argument								-												
Description	<p>This command is used to enter into Display Off mode. In this mode, the output data is disabled and blank page inserted. This command makes no change any other status. There will be no abnormal visible effect on the display.</p> <div><div><p>Before</p></div><div><p>After</p></div></div>																					
Restriction	This command has no effect when module is already in Display Off mode.																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Off</td></tr><tr><td>S/W Reset</td><td>Display Off</td></tr><tr><td>H/W Reset</td><td>Display Off</td></tr></table>										Status	Default Value	Power On Sequence	Display Off	S/W Reset	Display Off	H/W Reset	Display Off				
Status	Default Value																					
Power On Sequence	Display Off																					
S/W Reset	Display Off																					
H/W Reset	Display Off																					
Flow Chart	<div><div></div><div><p>Legend</p><ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer</div></div>																					

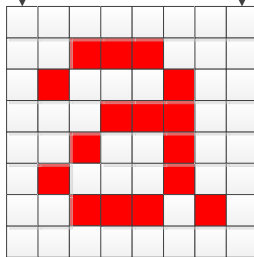
5.3.19 Display On (29h)

Table 61. Display On (29h)

Page 0	W / R	D6	D7	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	0	1	0	1	0	0	1	29h												
1 st Para	-	No Argument								-												
Description	<p>This command is used to recover from Display Off mode. Output data is enabled. This command does not change any other status.</p> <div><div><p>Before</p></div><div><p>After</p></div></div>																					
Restriction	This command has no effect when the Driver IC is already in Display On Mode.																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Off</td></tr><tr><td>S/W Reset</td><td>Display Off</td></tr><tr><td>H/W Reset</td><td>Display Off</td></tr></table>										Status	Default Value	Power On Sequence	Display Off	S/W Reset	Display Off	H/W Reset	Display Off				
Status	Default Value																					
Power On Sequence	Display Off																					
S/W Reset	Display Off																					
H/W Reset	Display Off																					
Flow Chart	<div><div><pre>graph TD; A([Display Off Mode]) --> B[/DISPON(29h)/]; B --> C([Display On Mode]);</pre></div><div><p>Legend</p><ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer</div></div>																					

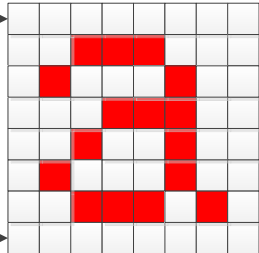
5.3.20 Column Address Set (2Ah)

Table 62. Column Address Set (2Ah)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	0	1	0	1	0	1	0	2Ah												
1 st Para	Read	0	0	0	0	0	0	SC9	SC8	00h												
2 nd Para	Read	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	00h												
3 rd Para	Read	0	0	0	0	0	0	EC9	EC8	01h												
4 th Para	Read	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	8Fh												
Description	<p>This command is used to define area of frame memory where MCU can access. This command makes no change on other driver status. The values of SC[9:0] and EC[9:0] are referred when memory write command comes. Each value represents one column line in the frame memory.</p> <div><div>SC[9:0]</div><div>EC[9:0]</div></div>																					
Restriction	<p>(1) The SC[9:0] always must be equal to or less than EC[9:0]. (2) The SC[9:0] and EC[9:0]-SC[9:0]+1 must be divisible by 2. (3) Minimum partial update area should ≥ 2x2</p>																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h, 00h, 01h, 8Fh</td></tr><tr><td>S/W Reset</td><td>00h, 00h, 01h, 8Fh</td></tr><tr><td>H/W Reset</td><td>00h, 00h, 01h, 8Fh</td></tr></table>										Status	Default Value	Power On Sequence	00h, 00h, 01h, 8Fh	S/W Reset	00h, 00h, 01h, 8Fh	H/W Reset	00h, 00h, 01h, 8Fh				
Status	Default Value																					
Power On Sequence	00h, 00h, 01h, 8Fh																					
S/W Reset	00h, 00h, 01h, 8Fh																					
H/W Reset	00h, 00h, 01h, 8Fh																					
Flow Chart	<div><div><div>CASET(2Ah)</div><div>1st&2nd Parameter: SC[9:0] 3rd &4th Parameter: EC[9:0]</div><div>PASET(2Bh)</div><div>1st&2nd Parameter: SP[9:0] 3rd &4th Parameter: EP[9:0]</div><div>RAMWR(2Ch)</div><div>Image Data D1[23:0], D2[23:0], ..., Dn[23:0]</div><div>Any Command</div></div><div>If needed</div><div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																					

5.3.21 Page Address Set (2Bh)

Table 63. Page Address Set (2Bh)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	0	1	0	1	0	1	1	2Bh												
1 st Para	Write	0	0	0	0	0	0	SP9	SP8	00h												
2 nd Para	Write	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	00h												
3 rd Para	Write	0	0	0	0	0	0	EP9	EP8	01h												
4 th Para	Write	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	8Fh												
Description	<p>This command is used to define area of frame memory where MCU can access. This command makes no change on other driver status. The values of SP[9:0] and EP[9:0] are referred when memory write command comes. Each value represents one page line in the frame memory.</p> <div><div>SP[9:0]→</div><div>EP[9:0]→</div></div>																					
Restriction	<p>(1) The SP[9:0] always must be equal to or less than EP[9:0] (2) The SP[9:0] and EP[9:0]-SP[9:0]+1 must be divisible by 2. (3) Minimum partial update area should ≥ 2x2</p>																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h, 00h, 01h, 8Fh</td></tr><tr><td>S/W Reset</td><td>00h, 00h, 01h, 8Fh</td></tr><tr><td>H/W Reset</td><td>00h, 00h, 01h, 8Fh</td></tr></table>										Status	Default Value	Power On Sequence	00h, 00h, 01h, 8Fh	S/W Reset	00h, 00h, 01h, 8Fh	H/W Reset	00h, 00h, 01h, 8Fh				
Status	Default Value																					
Power On Sequence	00h, 00h, 01h, 8Fh																					
S/W Reset	00h, 00h, 01h, 8Fh																					
H/W Reset	00h, 00h, 01h, 8Fh																					
Flow Chart	See “Column Address Set (2Ah)”																					

5.3.22 Memory Write (2Ch)

Table 64. Memory Write (2Ch)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	0	1	0	1	1	0	0	2Ch												
1 st Para	Write	D1[7:0]								XXh												
2 nd Para	Write	D1[7:0]								XXh												
:	:	:								:												
N th Para	Write	DN[7:0]								XXh												
Description	This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to zero. Then Dx[7:0] is stored in frame memory and the column register and the page register incremented at the same time. Sending any other command can stop frame Write.																					
Restriction	Data is compressed to 1/2 RAM, when two data-lines had been written Transmission sequences: LP_00=>HS for R2Ch=> LP_00=> HS for R3Ch=> LP_00=> HS for CMD=> LP_00																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>S/W Reset</td><td>Contents of memory is set randomly</td></tr><tr><td>H/W Reset</td><td>Contents of memory is set randomly</td></tr></table>										Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is set randomly	H/W Reset	Contents of memory is set randomly				
Status	Default Value																					
Power On Sequence	Contents of memory is set randomly																					
S/W Reset	Contents of memory is set randomly																					
H/W Reset	Contents of memory is set randomly																					
Flow Chart	<div><div><div>RAMWR(2Ch)</div><div>Image Data D1[23:0],D2[23:0], ...,Dn[23:0]</div><div>Any Command</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																					

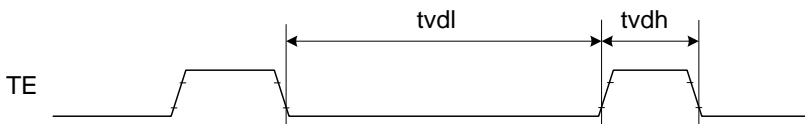
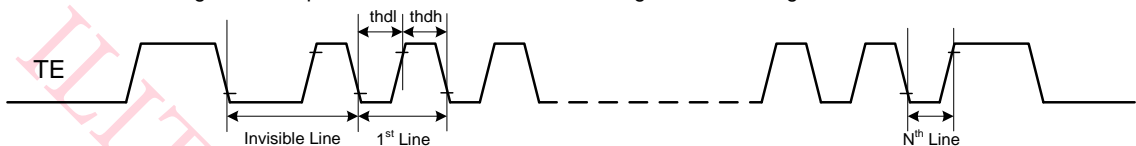
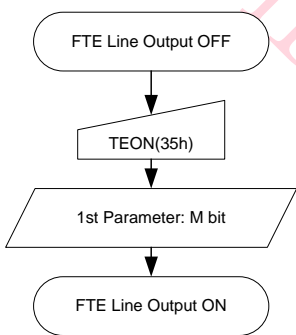
5.3.23 Tearing Effect Line Off (34h)

Table 65. Tearing Effect Line Off (34h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	1	1	0	1	0	0	34h
1 st Para	-	No Argument								-
Description	This command is used to turn off Display module's Tearing Effect output signal through TE pad.									
Restriction	This command has no effect when the Tearing Effect output is already off.									
Register Availability		Status					Availability			
		Normal Mode On, Idle Mode Off, Sleep Out					Yes			
		Normal Mode On, Idle Mode On, Sleep Out					Yes			
		Idle Mode Off, Sleep Out					Yes			
		Idle Mode On, Sleep Out					Yes			
		Sleep In					Yes			
Default		Status			Default Value					
		Power On Sequence			Tearing Effect output Off					
		S/W Reset			Tearing Effect output Off					
		H/W Reset			Tearing Effect output Off					
Flow Chart	<div><div><div>TE Line Output ON</div><div>↓</div><div>TEOFF(34h)</div><div>↓</div><div>TE Line Output OFF</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>									

5.3.24 Tearing Effect Line On (35h)

Table 66. Tearing Effect Line On (35h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	0	1	1	0	1	0	1	35h												
1 st Para	Write	0	0	0	0	0	0	0	M	-												
Description	<p>This command is used to turn ON the Tearing Effect output signal from the TE signal line. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.</p> <p>When M=0: The Tearing Effect Output line consists of V-Blanking information only: The Tearing Effect Output line shall be high during vertical blanking period.</p> 																					
	<p>When M=1: The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:</p> 																					
<p>Vertical blanking period: BP + FP Note: The Tearing Effect Output line shall be low when the display module is in Sleep mode</p>																						
Restriction	This command has no effect when the Tearing Effect output is already on.																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Tearing Effect output Off</td></tr><tr><td>S/W Reset</td><td>Tearing Effect output Off</td></tr><tr><td>H/W Reset</td><td>Tearing Effect output Off</td></tr></table>										Status	Default Value	Power On Sequence	Tearing Effect output Off	S/W Reset	Tearing Effect output Off	H/W Reset	Tearing Effect output Off				
Status	Default Value																					
Power On Sequence	Tearing Effect output Off																					
S/W Reset	Tearing Effect output Off																					
H/W Reset	Tearing Effect output Off																					
Flow Chart	<div></div> <div><p>Legend</p><ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer</div>																					

5.3.25 Memory Access Control (36h)

Table 67. Memory Access Control (36h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	1	1	0	1	1	0	36h
1 st Para	Write	MY	MX	0	0	BGR	0	SS	GS	00h

This command defines write scanning direction of frame memory. This command makes no change on the other driver status.

Symbol	Name	Description
MY ^{Note}	Row Address Order	These 2 bits control MCU to memory write direction.
MX	Column Address Order	
BGR	RGB-BGR Order	Color selector switch control (0=RGB, 1=BGR).
SS	Flip Horizontal	Select the source driver scan direction on panel module.
GS	Flip Vertical	Select the gate driver scan direction on panel module.

Note: The command MY="1" can be used to set row address write scanning in backward direction, please contact with ILITEK to obtain the application condition and detail.

Top-Left (0,0) means a physical display location

Row Address Order (MY) = "0"

Row Address Order (MY) = "1"

Column Address Order (MX) = "0"

Column Address Order (MX) = "1"

RGB-BGR Order control bit (RGB) = "0"

RGB-BGR Order control bit (BGR) = "1"

Top-Left (0,0) means a physical display location

	<div> <div>Vertical Scan Direction (SS) ="0"</div> <div> <div>Top Left Frame Memory</div> </div> <div>Top Left Display</div> </div> <div> <div>Vertical Scan Direction (SS) ="1"</div> <div> <div>Top Left Frame Memory</div> </div> <div>Top Left Display</div> </div> <div> <div>Horizontal Scan Direction (GS) ="0"</div> <div> <div>Top Left Frame Memory</div> </div> <div>Top Left Display</div> </div> <div> <div>Horizontal Scan Direction (GS) ="1"</div> <div> <div>Top Left Frame Memory</div> </div> <div>Top Left Display</div> </div>												
Restriction	None.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Idle Mode Off, Sleep Out	Yes												
Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>00h</td></tr> <tr> <td>S/W Reset</td><td>00h</td></tr> <tr> <td>H/W Reset</td><td>00h</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value												
Power On Sequence	00h												
S/W Reset	00h												
H/W Reset	00h												
Flow Chart	<div> <div> <div>MADCTR(36h)</div> <div>↓</div> <div>1st Parameter D[7:0]</div> </div> <div> <div>Legend</div> <div> <div>Command</div> <div>Parameter</div> <div>Display</div> <div>Action</div> <div>Mode</div> <div>Sequential transfer</div> </div> </div> </div>												

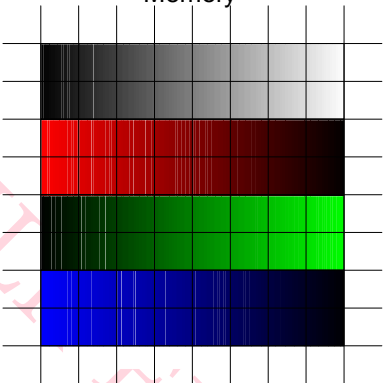
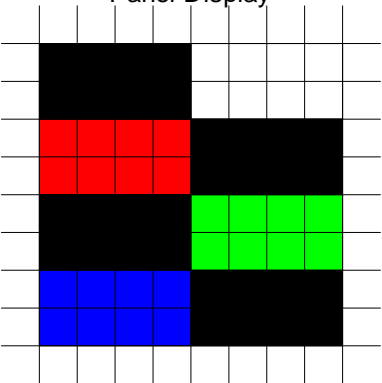
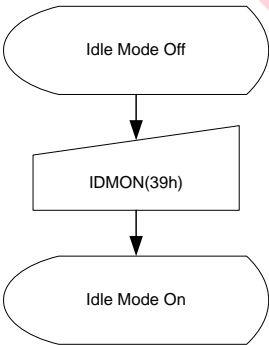
5.3.26 Idle Mode Off (38h)

Table 68. Idle Mode Off (38h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	0	1	1	1	0	0	0	38h												
1 st Para	Write	No Argument								-												
Description	This command causes the Display module to exit the Idle mode. In the Idle Mode Off, the display panel can display a maximum of 16.7M colors.																					
Restriction	This command has no effect when the module is already in the Idle Mode Off.																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle Mode Off</td></tr><tr><td>S/W Reset</td><td>Idle Mode Off</td></tr><tr><td>H/W Reset</td><td>Idle Mode Off</td></tr></table>										Status	Default Value	Power On Sequence	Idle Mode Off	S/W Reset	Idle Mode Off	H/W Reset	Idle Mode Off				
Status	Default Value																					
Power On Sequence	Idle Mode Off																					
S/W Reset	Idle Mode Off																					
H/W Reset	Idle Mode Off																					
Flow Chart	<div><div><div>Idle Mode On</div><div>↓</div><div>IDMOFF(38h)</div><div>↓</div><div>Idle Mode Off</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																					

5.3.27 Idle Mode On (39h)

Table 69. Idle Mode On (39h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	0	1	1	1	0	0	1	39h												
1 st Para	Write	No Argument								-												
Description	<p>This command is used to enter into Idle mode on.</p> <p>In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.</p> <div><div><p>Memory</p></div><div><p>Panel Display</p></div></div>																					
Restriction	This command has no effect when the module is already in the Idle Mode On.																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle Mode Off</td></tr><tr><td>S/W Reset</td><td>Idle Mode Off</td></tr><tr><td>H/W Reset</td><td>Idle Mode Off</td></tr></table>										Status	Default Value	Power On Sequence	Idle Mode Off	S/W Reset	Idle Mode Off	H/W Reset	Idle Mode Off				
Status	Default Value																					
Power On Sequence	Idle Mode Off																					
S/W Reset	Idle Mode Off																					
H/W Reset	Idle Mode Off																					
Flow Chart	<div><div></div><div><p>Legend</p><ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer</div></div>																					

5.3.28 Interface Pixel Format (3Ah)

Table 70. Interface Pixel Format (3Ah)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default																																																																													
Command	Write	0	0	1	1	1	0	1	0	3Ah																																																																													
1 st Para	Write	SPI_IFPF_SEL	VIPF[2:0]			0	IFPF[2:0]			77h																																																																													
Description	This command sets the pixel format for the RGB image data used by the interface.																																																																																						
	If SPI_IFPF_SEL(3Ah_D7) = 1: The VIPF[2:0] can be used to set pixel format by the SPI / Q-SPI interface, the IFPF[2:0] can be used to set pixel format by the MCU / MIPI interface.																																																																																						
	If SPI_IFPF_SEL(3Ah_D7) = 0: The IFPF[2:0] can be used to set pixel format by the SPI / Q-SPI / MCU / MIPI interface.																																																																																						
	VIPF[2:0]: Pixel format for SPI / Q-SPI interface(SPI_IFPF_SEL = 1)																																																																																						
	<table><tr><th>Control Interface Color Format</th><th>VIPF[2]</th><th>VIPF[1]</th><th>VIPF[0]</th></tr><tr><td>8-bits / pixel (256 colors) (including SPI3 / SPI4 / Q-SPI)</td><td>0</td><td>1</td><td>0</td></tr><tr><td>16-bits / pixel (65,536 colors) (including SPI3 / SPI4 / Q-SPI)</td><td>1</td><td>0</td><td>1</td></tr><tr><td>18-bits / pixel (262,144 colors) (including SPI3 / SPI4 / Q-SPI)</td><td>1</td><td>1</td><td>0</td></tr><tr><td>24-bits / pixel (16.7M colors) (including SPI3 / SPI4 / Q-SPI)</td><td>1</td><td>1</td><td>1</td></tr></table>				Control Interface Color Format	VIPF[2]	VIPF[1]	VIPF[0]	8-bits / pixel (256 colors) (including SPI3 / SPI4 / Q-SPI)	0	1	0	16-bits / pixel (65,536 colors) (including SPI3 / SPI4 / Q-SPI)	1	0	1	18-bits / pixel (262,144 colors) (including SPI3 / SPI4 / Q-SPI)	1	1	0	24-bits / pixel (16.7M colors) (including SPI3 / SPI4 / Q-SPI)	1	1	1																																																															
	Control Interface Color Format	VIPF[2]	VIPF[1]	VIPF[0]																																																																																			
	8-bits / pixel (256 colors) (including SPI3 / SPI4 / Q-SPI)	0	1	0																																																																																			
	16-bits / pixel (65,536 colors) (including SPI3 / SPI4 / Q-SPI)	1	0	1																																																																																			
	18-bits / pixel (262,144 colors) (including SPI3 / SPI4 / Q-SPI)	1	1	0																																																																																			
	24-bits / pixel (16.7M colors) (including SPI3 / SPI4 / Q-SPI)	1	1	1																																																																																			
IFPF[2:0]: Pixel format for SPI / Q-SPI / MCU / MIPI interface(SPI_IFPF_SEL = 0)																																																																																							
<table><tr><th>Control Interface Color Format</th><th>IFPF[2]</th><th>IFPF[1]</th><th>IFPF[0]</th></tr><tr><td>8-bits / pixel (256 colors) (including SPI3 / SPI4 / Q-SPI)</td><td>0</td><td>1</td><td>0</td></tr><tr><td>16-bits / pixel (65,536 colors) (including SPI3 / SPI4 / Q-SPI / MCU / MIPI)</td><td>1</td><td>0</td><td>1</td></tr><tr><td>18-bits / pixel (262,144 colors) (including SPI3 / SPI4 / Q-SPI / MCU / MIPI)</td><td>1</td><td>1</td><td>0</td></tr><tr><td>24-bits / pixel (16.7M colors) (including SPI3 / SPI4 / Q-SPI / MCU / MIPI)</td><td>1</td><td>1</td><td>1</td></tr></table>				Control Interface Color Format	IFPF[2]	IFPF[1]	IFPF[0]	8-bits / pixel (256 colors) (including SPI3 / SPI4 / Q-SPI)	0	1	0	16-bits / pixel (65,536 colors) (including SPI3 / SPI4 / Q-SPI / MCU / MIPI)	1	0	1	18-bits / pixel (262,144 colors) (including SPI3 / SPI4 / Q-SPI / MCU / MIPI)	1	1	0	24-bits / pixel (16.7M colors) (including SPI3 / SPI4 / Q-SPI / MCU / MIPI)	1	1	1																																																																
Control Interface Color Format	IFPF[2]	IFPF[1]	IFPF[0]																																																																																				
8-bits / pixel (256 colors) (including SPI3 / SPI4 / Q-SPI)	0	1	0																																																																																				
16-bits / pixel (65,536 colors) (including SPI3 / SPI4 / Q-SPI / MCU / MIPI)	1	0	1																																																																																				
18-bits / pixel (262,144 colors) (including SPI3 / SPI4 / Q-SPI / MCU / MIPI)	1	1	0																																																																																				
24-bits / pixel (16.7M colors) (including SPI3 / SPI4 / Q-SPI / MCU / MIPI)	1	1	1																																																																																				
SPI 3-3-2 8-bits / pixel (256 colors)																																																																																							
<table><tr><th>RGB 3-3-2 Bit</th><th>DCX</th><th>D[7]</th><th>D[6]</th><th>D[5]</th><th>D[4]</th><th>D[3]</th><th>D[2]</th><th>D[1]</th><th>D[0]</th><th>Note</th></tr><tr><td>CMDWR</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>2Ch for GRAM Write</td></tr><tr><td>1st RAM Data Write</td><td>1</td><td>R1[2]</td><td>R1[1]</td><td>R1[0]</td><td>G1[2]</td><td>G1[1]</td><td>G1[0]</td><td>B1[1]</td><td>B1[0]</td><td>1 Pixel Data Write</td></tr><tr><td>2nd RAM Data Write</td><td>1</td><td>R2[2]</td><td>R2[1]</td><td>R2[0]</td><td>G2[2]</td><td>G2[1]</td><td>G2[0]</td><td>B2[1]</td><td>B2[0]</td><td>2 Pixel Data Write</td></tr><tr><td>3rd RAM Data Write</td><td>1</td><td>R3[2]</td><td>R3[1]</td><td>R3[0]</td><td>G3[2]</td><td>G3[1]</td><td>G3[0]</td><td>B3[1]</td><td>B3[0]</td><td>3 Pixel Data Write</td></tr><tr><td>So on...</td><td>1</td><td>...</td><td>...</td><td>...</td><td>...</td><td>...</td><td>...</td><td>...</td><td>...</td><td>So on...</td></tr><tr><td>nth RAM Data Write</td><td>1</td><td>Rn[2]</td><td>Rn[1]</td><td>Rn[0]</td><td>Gn[2]</td><td>Gn[1]</td><td>Gn[0]</td><td>Bn[1]</td><td>Bn[0]</td><td>n Pixel Data Write</td></tr></table>											RGB 3-3-2 Bit	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note	CMDWR	0	0	0	1	0	1	1	0	0	2Ch for GRAM Write	1st RAM Data Write	1	R1[2]	R1[1]	R1[0]	G1[2]	G1[1]	G1[0]	B1[1]	B1[0]	1 Pixel Data Write	2nd RAM Data Write	1	R2[2]	R2[1]	R2[0]	G2[2]	G2[1]	G2[0]	B2[1]	B2[0]	2 Pixel Data Write	3rd RAM Data Write	1	R3[2]	R3[1]	R3[0]	G3[2]	G3[1]	G3[0]	B3[1]	B3[0]	3 Pixel Data Write	So on...	1	So on...	nth RAM Data Write	1	Rn[2]	Rn[1]	Rn[0]	Gn[2]	Gn[1]	Gn[0]	Bn[1]	Bn[0]	n Pixel Data Write
RGB 3-3-2 Bit	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note																																																																													
CMDWR	0	0	0	1	0	1	1	0	0	2Ch for GRAM Write																																																																													
1st RAM Data Write	1	R1[2]	R1[1]	R1[0]	G1[2]	G1[1]	G1[0]	B1[1]	B1[0]	1 Pixel Data Write																																																																													
2nd RAM Data Write	1	R2[2]	R2[1]	R2[0]	G2[2]	G2[1]	G2[0]	B2[1]	B2[0]	2 Pixel Data Write																																																																													
3rd RAM Data Write	1	R3[2]	R3[1]	R3[0]	G3[2]	G3[1]	G3[0]	B3[1]	B3[0]	3 Pixel Data Write																																																																													
So on...	1	So on...																																																																													
nth RAM Data Write	1	Rn[2]	Rn[1]	Rn[0]	Gn[2]	Gn[1]	Gn[0]	Bn[1]	Bn[0]	n Pixel Data Write																																																																													
Restriction	None																																																																																						
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes																																																																	
Status	Availability																																																																																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																																																																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																																																																																						
Idle Mode Off, Sleep Out	Yes																																																																																						
Idle Mode On, Sleep Out	Yes																																																																																						
Sleep In	Yes																																																																																						
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>77h</td></tr><tr><td>S/W Reset</td><td>77h</td></tr><tr><td>H/W Reset</td><td>77h</td></tr></table>										Status	Default Value	Power On Sequence	77h	S/W Reset	77h	H/W Reset	77h																																																																					
Status	Default Value																																																																																						
Power On Sequence	77h																																																																																						
S/W Reset	77h																																																																																						
H/W Reset	77h																																																																																						
Flow Chart	<div><div><div>16-bits/Pixel Mode</div><div>↓</div><div>COLMOD(3Ah)</div><div>↓</div><div>1st Parameter=06h</div><div>↓</div><div>18-bits/Pixel Mode</div></div><div><div>Legend</div><div>▭ Command</div><div>▱ Parameter</div><div>○ Display</div><div>◇ Action</div><div>▭ Mode</div><div>↻ Sequential transfer</div></div></div>																																																																																						


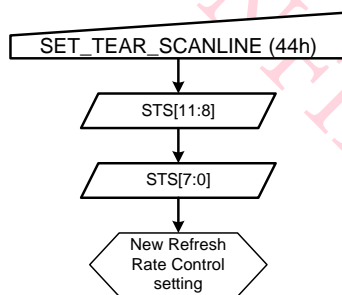
5.3.29 Memory Write Continue (3Ch)

Table 71. Memory Write (3Ch)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	0	1	1	1	1	0	0	3Ch												
1 st Para	Write	D1[7:0]								XXh												
2 nd Para	Write	D1[7:0]								XXh												
:	:	:								:												
N th Para	Write	DN[7:0]								XXh												
Description	This command is used to transfer data from the MCU to the Frame Memory, if want to continue the Frame Memory write after the “Memory Write (2Ch)” command. This command makes no change to the status of the other driver. When this command is accepted, the column register and the page register are not reset to zero since it has been done on “Memory Write (2Ch)” command. Sending any other command can stop frame Write.																					
Restriction	Data is compressed to 1/2 RAM, when two data-lines had been written Transmission sequences: LP_00=>HS for R2Ch=> LP_00=> HS for R3Ch=> LP_00=> HS for CMD=> LP_00																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>S/W Reset</td><td>Contents of memory is set randomly</td></tr><tr><td>H/W Reset</td><td>Contents of memory is set randomly</td></tr></table>										Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is set randomly	H/W Reset	Contents of memory is set randomly				
Status	Default Value																					
Power On Sequence	Contents of memory is set randomly																					
S/W Reset	Contents of memory is set randomly																					
H/W Reset	Contents of memory is set randomly																					
Flow Chart	<div><div><div>RAMWRC(3Ch)</div><div>Image Data D1[23:0],D2[23:0], ...,Dn[23:0]</div><div>Any Command</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																					

5.3.30 Set Tear Scan Line (44h)

Table 72. Set Tear Scan Line (44h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	1	0	0	0	1	0	0	44h												
1 st Para	Write	0	0	0	0	STS[11:8]				00h												
2 nd Para	Write	STS[7:0]								00h												
Description	<p>This command turns on the display module's Tearing Effect output signal on the FTE signal line when the display module reaches line N.</p> <p>The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode. After issuing a SET_TEAR_SCAN LINE command to the display module, the Tearing Effect output signal, e.g. as in DBI-2 systems, shall be a delayed version of V-Blanking information as illustrated by below figure.</p> <p>In other words, the TE pulse width needs to be identical with normal mode VSYNC related FTE pulse.</p> <div></div> <p>Note that SET_TEAR_SCAN LINE with N = 0 is equivalent to set_tear_on with M = 0. Please refer "Tearing Effect output signal".</p>																					
Restriction	None																					
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>00h, 00h</td></tr><tr><td>S/W Reset</td><td>00h, 00h</td></tr><tr><td>H/W Reset</td><td>00h, 00h</td></tr></tbody></table>										Status	Default Value	Power On Sequence	00h, 00h	S/W Reset	00h, 00h	H/W Reset	00h, 00h				
Status	Default Value																					
Power On Sequence	00h, 00h																					
S/W Reset	00h, 00h																					
H/W Reset	00h, 00h																					
Flow Chart	<div></div> <div><p>Legend</p><ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer</div>																					

5.3.31 Get Tear Scan Line (45h)

Table 73. Get Tear Scan Line (45h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	1	0	0	0	1	0	1	45h												
1 st Para	Read	0	0	0	0	GTS[11:8]				00h												
2 nd Para	Read	GTS[7:0]								00h												
Description	This readout returns the setting value of “Set Tear Scan Line (44h)” function.																					
Restriction	None																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability																				
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																				
	Normal Mode On, Idle Mode On, Sleep Out	Yes																				
	Idle Mode Off, Sleep Out	Yes																				
	Idle Mode On, Sleep Out	Yes																				
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h, 00h</td></tr><tr><td>S/W Reset</td><td>00h, 00h</td></tr><tr><td>H/W Reset</td><td>00h, 00h</td></tr></table>										Status	Default Value	Power On Sequence	00h, 00h	S/W Reset	00h, 00h	H/W Reset	00h, 00h				
	Status	Default Value																				
	Power On Sequence	00h, 00h																				
	S/W Reset	00h, 00h																				
H/W Reset	00h, 00h																					
Flow Chart	<div><div><div>Get Tear Scan Line (45h)</div><div>↓</div><div>1st Parameter : GTS[11:8]</div><div>↓</div><div>2nd Parameter : GTS[7:0]</div></div><div>Host ----- Driver</div></div>																					
	<div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																					

5.3.32 Write Display Brightness (51h)

Table 74. Write Display Brightness (51h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	1	0	1	0	0	0	1	51h												
1 st Para	Write	0	0	0	0	DBV[11:8]				00h												
2 nd Para	Write	DBV[7:0]								00h												
Description	This command is used to adjust the brightness value of the display. It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification. In principle relationship is that 0000h value means the lowest brightness and 0FFFh value means the highest brightness.																					
Restriction	None																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h, 00h</td></tr><tr><td>S/W Reset</td><td>00h, 00h</td></tr><tr><td>H/W Reset</td><td>00h, 00h</td></tr></table>										Status	Default Value	Power On Sequence	00h, 00h	S/W Reset	00h, 00h	H/W Reset	00h, 00h				
Status	Default Value																					
Power On Sequence	00h, 00h																					
S/W Reset	00h, 00h																					
H/W Reset	00h, 00h																					
Flow Chart	<div><div><div>WRDISBV(51h)</div><div>↓</div><div>DBV</div><div>↓</div><div>New Display Brightness Value Loaded</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																					

5.3.33 Read Display Brightness (52h)

Table 75. Read Display Brightness (52h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	1	0	1	0	0	1	0	52h												
1 st Para	Read	0	0	0	0	DBV[11:8]				00h												
2 nd Para	Read	DBV[7:0]								00h												
Description	<p>This command returns the brightness value of the display.</p> <p>It should be checked what the relationship between this returned value and output brightness of the display.</p> <p>This relationship is defined on the display module specification.</p> <p>In principle the relationship is that 0000h value means the lowest brightness and 0FFFh value means the highest brightness.</p> <p>DBV[11:0] is reset when display is in Sleep In mode.</p> <p>DBV[11:0] is '0', when bit BCTRL of Write CTRL Display Value command (53h) is '0'.</p> <p>DBV[11:0] is manual set brightness specified with Write CTRL Display Value command (53h), when bit BCTRL of Write CTRL Display Value command (53h) is '1'.</p> <p>When bit BCTRL of Write CTRL Display command (53h) is '1' and the setting value of Write Power Save command (55h) is '0', DBV[11:0] output is the brightness value specified with Write Display Brightness Value command (51h).</p>																					
Restriction	None																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h, 00h</td></tr><tr><td>S/W Reset</td><td>00h, 00h</td></tr><tr><td>H/W Reset</td><td>00h, 00h</td></tr></table>										Status	Default Value	Power On Sequence	00h, 00h	S/W Reset	00h, 00h	H/W Reset	00h, 00h				
Status	Default Value																					
Power On Sequence	00h, 00h																					
S/W Reset	00h, 00h																					
H/W Reset	00h, 00h																					
Flow Chart	<div><div><div>RDDISBV(52h)</div><div>↓</div><div>Send 1st Parameter</div></div><div>Host</div><div>Driver</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																					

5.3.34 Write CTRL Display (53h)

Table 76. Write CTRL Display (53h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default																		
Command	Write	0	1	0	1	0	0	1	1	53h																		
1 st Para	Write	HBM[1:0]		BCTRL	0	DD	BL	0	0	00h																		
Description	This command is used to control the display brightness. In SPI-4W/ Dual SPI-4W interface, please follow the step to write/read this register, (1) set RFDh_P1, P2=00, 01 to enable SPI write (2) set R53h value (3) set RFDh_P1, P2=00, 81 to enable SPI read bit and can read value																											
	HBM: High Brightness Mode																											
	<table><tr><td>HBM[1]</td><td>HBM[0]</td><td>Description</td></tr><tr><td>0</td><td>0</td><td>High brightness mode is off</td></tr><tr><td>0</td><td>1</td><td>High brightness mode is on. LCD: LED boost signal is ON. LEDPWM= 100% PWM.</td></tr><tr><td>1</td><td>0</td><td>High brightness mode is on. LCD: LED boost signal is ON. LEDPWM= 100% PWM.</td></tr><tr><td>1</td><td>1</td><td>High brightness mode is on. LCD: LED boost signal is ON. LEDPWM= 100% PWM.</td></tr></table>										HBM[1]	HBM[0]	Description	0	0	High brightness mode is off	0	1	High brightness mode is on. LCD: LED boost signal is ON. LEDPWM= 100% PWM.	1	0	High brightness mode is on. LCD: LED boost signal is ON. LEDPWM= 100% PWM.	1	1	High brightness mode is on. LCD: LED boost signal is ON. LEDPWM= 100% PWM.			
	HBM[1]	HBM[0]	Description																									
	0	0	High brightness mode is off																									
	0	1	High brightness mode is on. LCD: LED boost signal is ON. LEDPWM= 100% PWM.																									
	1	0	High brightness mode is on. LCD: LED boost signal is ON. LEDPWM= 100% PWM.																									
	1	1	High brightness mode is on. LCD: LED boost signal is ON. LEDPWM= 100% PWM.																									
	BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.																											
	<table><tr><td>BCTRL</td><td>Description</td></tr><tr><td>0</td><td>Brightness ControlBlock Off (DBV[11:0]=00h)</td></tr><tr><td>1</td><td>Brightness Control Block On (DBV[11:0] is active)</td></tr></table>										BCTRL	Description	0	Brightness ControlBlock Off (DBV[11:0]=00h)	1	Brightness Control Block On (DBV[11:0] is active)												
BCTRL	Description																											
0	Brightness ControlBlock Off (DBV[11:0]=00h)																											
1	Brightness Control Block On (DBV[11:0] is active)																											
DD: Display Dimming Control. This function is only for manual brightness setting.																												
<table><tr><td>DD</td><td>Description</td></tr><tr><td>0</td><td>Display Dimming Off</td></tr><tr><td>1</td><td>Display Dimming On</td></tr></table>										DD	Description	0	Display Dimming Off	1	Display Dimming On													
DD	Description																											
0	Display Dimming Off																											
1	Display Dimming On																											
BL: Backlight Control On/Off																												
<table><tr><td>BL</td><td>Description</td></tr><tr><td>0</td><td>Backlight Control Off</td></tr><tr><td>1</td><td>Backlight Control On</td></tr></table>										BL	Description	0	Backlight Control Off	1	Backlight Control On													
BL	Description																											
0	Backlight Control Off																											
1	Backlight Control On																											
Dimming function is adapted to the brightness registers for display, when bit BCTRL of Write CTRL Display Value command (53h) is changed at bit DD=1, e.g. bit BCTRL: 0 -> 1 or 1-> 0. When bit BL changes from “On” to “Off”, backlight is turned off without gradual dimming, even if Display Dimming On (bit DD=1) is selected.																												
Restriction	None																											
Register Availability	<table><tr><td colspan="2">Status</td><td>Availability</td></tr><tr><td colspan="2">Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td colspan="2">Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td colspan="2">Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td colspan="2">Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td colspan="2">Sleep In</td><td>Yes</td></tr></table>										Status		Availability	Normal Mode On, Idle Mode Off, Sleep Out		Yes	Normal Mode On, Idle Mode On, Sleep Out		Yes	Idle Mode Off, Sleep Out		Yes	Idle Mode On, Sleep Out		Yes	Sleep In		Yes
Status		Availability																										
Normal Mode On, Idle Mode Off, Sleep Out		Yes																										
Normal Mode On, Idle Mode On, Sleep Out		Yes																										
Idle Mode Off, Sleep Out		Yes																										
Idle Mode On, Sleep Out		Yes																										
Sleep In		Yes																										
Default	<table><tr><td>Status</td><td>Default Value</td></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>										Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h										
Status	Default Value																											
Power On Sequence	00h																											
S/W Reset	00h																											
H/W Reset	00h																											
Flow Chart	<div><div><div>WRCTRLD(53h)</div><div>HBM, BCTRL, DD, BL</div><div>New Control Value Loaded</div></div><div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																											

5.3.35 Read CTRL Display (54h)

Table 77. Read CTRL Display (54h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	1	0	1	0	1	0	0	54h												
1 st Para	Read	HBM[1:0]		BCTRL	0	DD	BL	0	0	00h												
Description	This command returns the display brightness control values.																					
	HBM: High Brightness Mode																					
	HBM[1]	HBM[0]	Description																			
	0	0	High brightness mode is off																			
	0	1	High brightness mode is on. LCD: LED boost signal is ON. LEDPWM= 100% PWM.																			
	1	0	High brightness mode is on. LCD: LED boost signal is ON. LEDPWM= 100% PWM.																			
	1	1	High brightness mode is on. LCD: LED boost signal is ON. LEDPWM= 100% PWM.																			
	BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.																					
	BCTRL	Description																				
	0	Brightness Control Block Off (DBV[11:0]=00h)																				
1	Brightness Control Block On (DBV[11:0] is active)																					
DD: Display Dimming Control. This function is only for manual brightness setting.																						
DD	Description																					
0	Display Dimming Off																					
1	Display Dimming On																					
BL: Backlight Control On/Off																						
BL	Description																					
0	Backlight Control Off																					
1	Backlight Control On																					
Dimming function is adapted to the brightness registers for display, when bit BCTRL of Write CTRL Display Value command (53h) is changed at bit DD=1, e.g. bit BCTRL: 0 -> 1 or 1-> 0. When bit BL changes from “On” to “Off”, backlight is turned off without gradual dimming, even if Display Dimming On (bit DD=1) is selected.																						
Restriction	None																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>										Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value																					
Power On Sequence	00h																					
S/W Reset	00h																					
H/W Reset	00h																					
Flow Chart	<div><div><div>RDCTRLD(54h)</div><div>↓</div><div>Send Parameter</div></div><div>Host ----- Driver</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																					

5.3.36 Write Power Save (55h)

Table 78. Write Power Save (55h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	1	0	1	0	1	0	1	55h
1 st Para	Write	0	0	0	0	0	0	PWRSAVE[1:0]		00h
Description	This command is used to write the setting for power save control functionalities.									
	D1	D0	Function				Note			
	0	0	Power Save Off				-			
	0	1	Power Save Low				Conservative Setting of CABC/DBLC			
	1	0	Power Save Medium				Medium Setting of CABC/DBLC			
	1	1	Power Save High				Aggressive Setting of CABC/DBLC			
CABC = Content Adaptive Brightness Control DBLC = Dynamic Backlight Control.										
Restriction	None									
Register Availability										
	Status							Availability		
	Normal Mode On, Idle Mode Off, Sleep Out							Yes		
	Normal Mode On, Idle Mode On, Sleep Out							Yes		
	Idle Mode Off, Sleep Out							Yes		
	Idle Mode On, Sleep Out							Yes		
Sleep In							Yes			
Default										
	Status					Default Value				
	Power On Sequence					00h				
	S/W Reset					00h				
H/W Reset					00h					
Flow Chart										

5.3.37 Read Power Save (56h)

Table 79. Read Power Save (56h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default																		
Command	Write	0	1	0	1	0	1	1	0	56h																		
1 st Para	Read	0	0	0	0	0	0	PWRSAVE[1:0]		00h																		
Description	This command is used to read the setting for power save control functionalities.																											
	D1	D0	Function				Note																					
	0	0	Power Save Off				-																					
	0	1	Power Save Low				Conservative Setting of CAB/DBLC																					
	1	0	Power Save Medium				Medium Setting of CAB/DBLC																					
	1	1	Power Save High				Aggressive Setting of CAB/DBLC																					
CABC = Content Adaptive Brightness Control DBLC = Dynamic Backlight Control (RGBW pixel structure, where is 2 sub pixels per pixel, is used on the display panel or a similar solution)																												
Restriction	None																											
Register Availability	<table><tr><th colspan="2">Status</th><th>Availability</th></tr><tr><td colspan="2">Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td colspan="2">Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td colspan="2">Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td colspan="2">Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td colspan="2">Sleep In</td><td>Yes</td></tr></table>										Status		Availability	Normal Mode On, Idle Mode Off, Sleep Out		Yes	Normal Mode On, Idle Mode On, Sleep Out		Yes	Idle Mode Off, Sleep Out		Yes	Idle Mode On, Sleep Out		Yes	Sleep In		Yes
Status		Availability																										
Normal Mode On, Idle Mode Off, Sleep Out		Yes																										
Normal Mode On, Idle Mode On, Sleep Out		Yes																										
Idle Mode Off, Sleep Out		Yes																										
Idle Mode On, Sleep Out		Yes																										
Sleep In		Yes																										
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>										Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h										
Status	Default Value																											
Power On Sequence	00h																											
S/W Reset	00h																											
H/W Reset	00h																											
Flow Chart	<div><div><div>RDPWRSAVE (56h)</div><div>↓</div><div>Send Parameter</div></div><div>Host ----- Driver</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																											

5.3.38 STOP_TR (59h)

Table 80. STOP_TR (59h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	1	0	1	1	0	0	1	59h												
1 st Para	-	No Argument								-												
Description	When DD bit status of “Write CTRL Display (53h)” register is ‘1’, applying this command instantly stops the ongoing transition of Display Dimming. When display module receives this command, the current output value stays active.																					
Restriction	None																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table>										Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A				
Status	Default Value																					
Power On Sequence	N/A																					
S/W Reset	N/A																					
H/W Reset	N/A																					
Flow Chart	<div><div><div>Display Dimming transition is active</div><div>↓</div><div>STOP_TR (59h)</div><div>↓</div><div>Stop ongoing transition</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																					

5.3.39 Write CABC Minimum Brightness (5Eh)

Table 81. Write CABC Minimum Brightness (5Eh)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	1	0	1	1	1	1	0	5Eh												
1 st Para	Write	0	0	0	0	CMB[11:8]				00h												
2 nd Para	Write	CMB[7:0]								00h												
Description	<p>In SPI-4W/ Dual SPI-4W interface, please follow the step to write/read this register, (1) set RFDh_P1, P2=00, 01 to enable SPI write (2) set R63h value (3) set RFDh_P1, P2=00, 81 to enable SPI read bit and can read value This command is used to set the minimum brightness value of the display for CABC function. CMB[11:0]: CABC minimum brightness control, this parameter is used to set a limit to the amount of brightness reduction allowed. When CABC is active, CABC cannot reduce the display brightness to less than CABC minimum brightness setting. Image processing function works as normal, even if the brightness cannot be changed. This function does not affect manual brightness setting. Manual brightness setting does not have a limit on allowable brightness reduction; display brightness can be set less than CABC minimum brightness. Smooth transition and dimming function work as normal. When display brightness is turned off (bit BCTRL of Write CTRL Display Value command (53h) is '0'), CABC minimum brightness setting is ignored. The principle relationship is such that 0000h value means the lowest brightness for CABC and 0FFFh value means the highest brightness for CABC.</p>																					
Restriction	None																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h, 00h</td></tr><tr><td>S/W Reset</td><td>00h, 00h</td></tr><tr><td>H/W Reset</td><td>00h, 00h</td></tr></table>										Status	Default Value	Power On Sequence	00h, 00h	S/W Reset	00h, 00h	H/W Reset	00h, 00h				
Status	Default Value																					
Power On Sequence	00h, 00h																					
S/W Reset	00h, 00h																					
H/W Reset	00h, 00h																					
Flow Chart	<div><div><div>WRCABCMB(5Eh)</div><div>CMB[11:0]</div><div>New Display Luminance Value Loaded</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																					

5.3.40 Read CABC Minimum Brightness (5Fh)

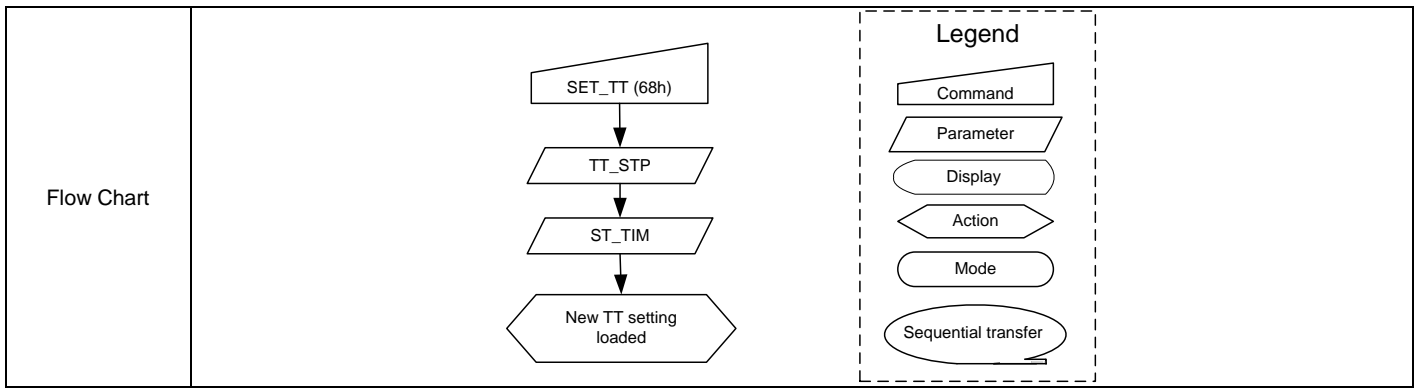
Table 82. Read CABC Minimum Brightness (5Fh)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	0	1	0	1	1	1	1	1	5Fh												
1 st Para	Read	0	0	0	0	CMB[11:8]				00h												
2 nd Para	Read	CMB[7:0]								00h												
Description	This command returns the minimum brightness value of CABC function. The principle relationship is such that 0000h value means the lowest brightness and 0FFFh value means the highest brightness. CMB[11:0] is CABC minimum brightness specified with Write CABC minimum brightness command (5Eh).																					
Restriction	None																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h, 00h</td></tr><tr><td>S/W Reset</td><td>00h, 00h</td></tr><tr><td>H/W Reset</td><td>00h, 00h</td></tr></table>										Status	Default Value	Power On Sequence	00h, 00h	S/W Reset	00h, 00h	H/W Reset	00h, 00h				
Status	Default Value																					
Power On Sequence	00h, 00h																					
S/W Reset	00h, 00h																					
H/W Reset	00h, 00h																					
Flow Chart	<div><div><div>RDCABCMB (5F)</div><div>↓</div><div>Send Parameter</div></div><div>Host ----- Driver</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																					

5.3.41 Set Transition Time (68h)

Table 83. Set Transition Time (68h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	1	1	0	1	0	0	0	68h
1 st Para	Write	TT_STP[7:0]								00h
2 nd Para	Write	ST_TIM[7:0]								00h
Description	This command controls the total transition time of Display Dimming function. Transition time is adjusted with two parameters, defining as follows: 1st Parameter TT_STP[7:0] defines the number of dimming steps for transition.									
	TT_STP[7:0]					Description				
	00h					1 step				
	01h					2 step				
	02h					4 step				
	03h					8 step				
	04h					16 step				
	05h					32 step				
	06h					64 step				
	07h					128 step				
08h					256 step					
09h					512 step					
0Ah					1024 step					
0Bh					2048 step					
0Ch					4096 step					
Others					Reserved					
Description	2nd Parameter ST_TIM[7:0] defines the step time as frame units for each dimming step.									
	ST_TIM[7:0]					Description				
	00h					1 frame				
	01h					1 frame				
	02h					2 frame				
	03h					3 frame				
	04h					4 frame				
	05h					5 frame				
	:					:				
	:					:				
FBh					251 frame					
FCh					252 frame					
FDh					253 frame					
FEh					254 frame					
FFh					255 frame					
Thereby, total transition time for dimming can be calculated as follows: TT_STP[7:0] * ST_TIM[7:0] = TT, where TT unit is frame. Value 0000h means the transition is instant. However, concerning relation with Display Brightness block, implementation should allow step selection between ranges from 0 to 4096. When bit DD of Write CTRL Display Value command (53h) is ‘1’, the transition time of dimming shall be the same when display brightness is increased or decreased.										
Restriction	None									
Register Availability						Status		Availability		
						Normal Mode On, Idle Mode Off, Sleep Out		Yes		
						Normal Mode On, Idle Mode On, Sleep Out		Yes		
						Idle Mode Off, Sleep Out		Yes		
						Idle Mode On, Sleep Out		Yes		
						Sleep In		Yes		
Default						Status		Default Value		
						Power On Sequence		00h, 00h		
						S/W Reset		00h, 00h		
						H/W Reset		00h, 00h		



5.3.42 Get Transition Time (69h)

Table 84. Get Transition Time (69h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default																														
Command	Write	0	1	1	0	1	0	0	1	69h																														
1 st Para	Read	TT_STP[7:0]								00h																														
2 nd Para	Read	ST_TIM[7:0]								00h																														
Description	This readout returns the Transition Time value of Display Dimming function, described in Set Transition Time command (68h). Transition time is adjusted with two parameters, defining as follows: 1st Parameter TT_STP[7:0] defines the number of dimming steps for transition.																																							
	<table><tr><th>TT_STP[7:0]</th><th>Description</th></tr><tr><td>00h</td><td>1 step</td></tr><tr><td>01h</td><td>2 step</td></tr><tr><td>02h</td><td>4 step</td></tr><tr><td>03h</td><td>8 step</td></tr><tr><td>04h</td><td>16 step</td></tr><tr><td>05h</td><td>32 step</td></tr><tr><td>06h</td><td>64 step</td></tr><tr><td>07h</td><td>128 step</td></tr><tr><td>08h</td><td>256 step</td></tr><tr><td>09h</td><td>512 step</td></tr><tr><td>0Ah</td><td>1024 step</td></tr><tr><td>0Bh</td><td>2048 step</td></tr><tr><td>0Ch</td><td>4096 step</td></tr><tr><td>Others</td><td>Reserved</td></tr></table>										TT_STP[7:0]	Description	00h	1 step	01h	2 step	02h	4 step	03h	8 step	04h	16 step	05h	32 step	06h	64 step	07h	128 step	08h	256 step	09h	512 step	0Ah	1024 step	0Bh	2048 step	0Ch	4096 step	Others	Reserved
	TT_STP[7:0]	Description																																						
	00h	1 step																																						
	01h	2 step																																						
	02h	4 step																																						
	03h	8 step																																						
	04h	16 step																																						
	05h	32 step																																						
	06h	64 step																																						
07h	128 step																																							
08h	256 step																																							
09h	512 step																																							
0Ah	1024 step																																							
0Bh	2048 step																																							
0Ch	4096 step																																							
Others	Reserved																																							
2nd Parameter ST_TIM[7:0] defines the step time as frame units for each dimming step.																																								
<table><tr><th>ST_TIM[7:0]</th><th>Description</th></tr><tr><td>00h</td><td>1 frame</td></tr><tr><td>01h</td><td>1 frame</td></tr><tr><td>02h</td><td>2 frame</td></tr><tr><td>03h</td><td>3 frame</td></tr><tr><td>04h</td><td>4 frame</td></tr><tr><td>05h</td><td>5 frame</td></tr><tr><td>:</td><td>:</td></tr><tr><td>:</td><td>:</td></tr><tr><td>FBh</td><td>251 frame</td></tr><tr><td>FCh</td><td>252 frame</td></tr><tr><td>FDh</td><td>253 frame</td></tr><tr><td>FEh</td><td>254 frame</td></tr><tr><td>FFh</td><td>255 frame</td></tr></table>										ST_TIM[7:0]	Description	00h	1 frame	01h	1 frame	02h	2 frame	03h	3 frame	04h	4 frame	05h	5 frame	:	:	:	:	FBh	251 frame	FCh	252 frame	FDh	253 frame	FEh	254 frame	FFh	255 frame			
ST_TIM[7:0]	Description																																							
00h	1 frame																																							
01h	1 frame																																							
02h	2 frame																																							
03h	3 frame																																							
04h	4 frame																																							
05h	5 frame																																							
:	:																																							
:	:																																							
FBh	251 frame																																							
FCh	252 frame																																							
FDh	253 frame																																							
FEh	254 frame																																							
FFh	255 frame																																							
Restriction	None																																							
Register Availability																																								

Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>00h, 00h</td></tr> <tr> <td>S/W Reset</td><td>00h, 00h</td></tr> <tr> <td>H/W Reset</td><td>00h, 00h</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h, 00h	S/W Reset	00h, 00h	H/W Reset	00h, 00h
Status	Default Value								
Power On Sequence	00h, 00h								
S/W Reset	00h, 00h								
H/W Reset	00h, 00h								
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;"> <pre> graph TD subgraph Host A[Read GET_TT (69h)] end subgraph Driver B[/Send 1st Parameter/] C[/Send 2nd Parameter/] end A --> B B --> C </pre> </div> <div style="flex: 0.5; border: 1px dashed black; padding: 5px; margin-left: 10px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>								

5.3.43 Read DDB Start (A1h)

Table 85. Read DDB Start (A1h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	1	0	1	0	0	0	0	1	A1h												
1 st Para	Read	SID[7:0]								00h												
2 nd Para	Read	SID[15:8]								00h												
3 rd Para	Read	MID[7:0]								00h												
4 th Para	Read	MID[15:8]								00h												
5 th Para	Read	RID[7:0]								00h												
6 th Para	Read	RID[15:8]								00h												
7 th Para	Read	1	1	1	1	1	1	1	1	FFh												
Description	<p>This command returns supplier identification and display module model/revision information.</p> <p>Note: This information is not the same what “Read ID1 (DAh)”, “Read ID2 (DBh)” and “Read ID3 (DCh)” commands are returning.</p> <p>SID[7:0]: LCD module’s manufacturer ID.</p> <p>SID[15:8]: LCD module/driver version ID.</p> <p>MID[7:0]: LCD module/driver ID.</p> <p>MID[15:8]: IC version code.</p> <p>RID[7:0]: Customer ID</p> <p>RID[15:8]: Customer ID</p> <p>FFh: - Exit code – there is no more data in the Descriptor Block</p> <p>This read sequence can be interrupted by any command and it can be continued by “Read DDB Continue (A8h)” command. For example, RDDDBS (A1h) => 1st parameter has been sent => 2nd parameter has been sent => interrupt => RDDDBC (A1h) => 3rd parameter of the RDDDBS has been sent.</p> <p>Note:</p> <p>These IDs information are not the same what “Read ID1 (DAh)”, “Read ID2 (DBh)” and “Read ID3 (DCh)” commands are returned value.</p> <p>Maximum DDB data length is 6 bytes with NVM program.</p>																					
Restriction	None																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h,00h,00h,00h,00h,00h,FFh</td></tr><tr><td>S/W Reset</td><td>00h,00h,00h,00h,00h,00h,FFh</td></tr><tr><td>H/W Reset</td><td>00h,00h,00h,00h,00h,00h,FFh</td></tr></table>										Status	Default Value	Power On Sequence	00h,00h,00h,00h,00h,00h,FFh	S/W Reset	00h,00h,00h,00h,00h,00h,FFh	H/W Reset	00h,00h,00h,00h,00h,00h,FFh				
Status	Default Value																					
Power On Sequence	00h,00h,00h,00h,00h,00h,FFh																					
S/W Reset	00h,00h,00h,00h,00h,00h,FFh																					
H/W Reset	00h,00h,00h,00h,00h,00h,FFh																					
Flow Chart	<div><div><div>RDDDBS(A1h)</div><div>Host</div><div>Driver</div><div>Send 1st Parameter</div><div>Send 2nd Parameter</div><div>...</div><div>Send 6th Parameter</div><div>Send 7th Parameter (FFh)</div></div><div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																					

5.3.44 Read DDB Continue (A8h)

Table 86. Read DDB Continue (A8h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	1	0	1	0	1	0	0	0	A8h												
1st Para	Read	D1[7:0]								00h												
2nd Para	Read	D2[7:0]								00h												
⋮	⋮	⋮								⋮												
Nth Para	Read	DN[7:0]								00h												
Description	This command is used to return the supplier's identification and revision information from the point where RDDDBS (A1h) was interrupted by another command. A Read DDB Start command (A1h) should be executed at least once before a Read DDB Continue command (A8h) to define the read location.																					
Restriction	None																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h,00h,...,00h</td></tr><tr><td>S/W Reset</td><td>00h,00h,...,00h</td></tr><tr><td>H/W Reset</td><td>00h,00h,...,00h</td></tr></table>										Status	Default Value	Power On Sequence	00h,00h,...,00h	S/W Reset	00h,00h,...,00h	H/W Reset	00h,00h,...,00h				
Status	Default Value																					
Power On Sequence	00h,00h,...,00h																					
S/W Reset	00h,00h,...,00h																					
H/W Reset	00h,00h,...,00h																					
Flow Chart	<div><div><div>RDDDBC(A8h)</div><div>Host</div></div><div><div>RDDDBS Data D1[7:0], D2[7:0],...Dn[7:0]</div><div>Driver</div></div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																					

5.3.45 Read First Checksum (AAh)

Table 87. Read First Checksum (AAh)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	1	0	1	0	1	0	1	0	AAh												
1 st Para	Read	FCS[7:0]								00h												
Description	This command returns the first checksum calculated from User's area registers and the Frame Memory after the write access to those registers and/or Frame Memory has been done.																					
Restriction	None																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>										Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value																					
Power On Sequence	00h																					
S/W Reset	00h																					
H/W Reset	00h																					
Flow Chart	<div><div><div><div>RDFCS (AAh)</div><div>↓</div><div>Send FCS[7:0]</div></div><div><div>Host</div><div>-----</div><div>Driver</div></div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																					

5.3.46 Read Continue Checksum (AFh)

Table 88. Read Continue Checksum (AFh)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	1	0	1	0	1	1	1	1	AFh												
1 st Para	Read	CCS[7:0]								00h												
Description	This command returns the continue checksum that has been calculated continuously after the first checksum has calculated from Page 0 area registers after the write access to those registers has been done.																					
Restriction	It will be necessary to wait 300ms after there is the last write access on Page 0 area registers before there can read this checksum value in the first time.																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>										Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value																					
Power On Sequence	00h																					
S/W Reset	00h																					
H/W Reset	00h																					
Flow Chart	<div><div><div>RDCCS (AFh)</div><div>↓</div><div>Send CCS[7:0]</div></div><div>Host ----- Driver</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																					

5.3.47 Set DISP Mode (C2h)

Table 89. Set DISP Mode (C2h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	1	1	0	0	0	0	1	0	C2h
1 st Para	Write	0	0	0	0	0	0	DM[1:0]		00h
Description	This command is used to select the display mode.									
	DM[1:0]		Description						Note	
	00b		Internal timing						Command mode	
	01b		reserved							
	10b		reserved							
	11b		External timing (VSYNC+HSYNC align mode)						Video mode ^{Note}	
NOTE:										
1. To enter Video mode, please set DM[1:0]=2'b11 and Page6_R09h=28h.										
2. In Video mode, the V-total and H-total of Host must match the V-total and H-total setting of DDIC. Please contact with ILITEK to obtain the application condition and details.										
Restriction	None									
Register Availability										
	Status								Availability	
	Normal Mode On, Idle Mode Off, Sleep Out								Yes	
	Normal Mode On, Idle Mode On, Sleep Out								Yes	
	Idle Mode Off, Sleep Out								Yes	
	Idle Mode On, Sleep Out								Yes	
Sleep In								Yes		
Default										
	Status					Default Value				
	Power On Sequence					00h				
	S/W Reset					00h				
H/W Reset					00h					
Flow Chart										
	<div><div>setDISPMode(C2h)</div><div>↓</div><div>1st Parameter</div><div>↓</div><div>New DISP mode loaded</div></div>									
	<div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>									

5.3.48 Get DISP Mode (C4h)

Table 90. Get DISP Mode (C4h)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	1	1	0	0	0	1	0	0	C4h												
1 st Para	Read	SPI_WRAM	0	DSPI_CFG[1:0]	0	0	0	0	DSPI_EN	00h												
Description	<table><tr><th>Parameter</th><th>Status</th><th>Availability</th></tr><tr><td>SPI_WRAM</td><td>This command is used in SPI interfaces. Making sure to set SPI_WRAM= 1 before host writes SRAM via SPI interfaces.</td><td>0b: disable 1b: SPI interface write RAM enable</td></tr><tr><td>DSPI_CFG[1:0]</td><td>DAUL SPI MODE Selection</td><td>00b: 1P1T for 1 wire 10b: 1P1T for 2 wire 11b: 2P3T for 2 wire 01b: reserve</td></tr><tr><td>DSPI_EN</td><td>DAUL SPI MODE Enable</td><td>0b: disable 1b: enable</td></tr></table>										Parameter	Status	Availability	SPI_WRAM	This command is used in SPI interfaces. Making sure to set SPI_WRAM= 1 before host writes SRAM via SPI interfaces.	0b: disable 1b: SPI interface write RAM enable	DSPI_CFG[1:0]	DAUL SPI MODE Selection	00b: 1P1T for 1 wire 10b: 1P1T for 2 wire 11b: 2P3T for 2 wire 01b: reserve	DSPI_EN	DAUL SPI MODE Enable	0b: disable 1b: enable
	Parameter	Status	Availability																			
	SPI_WRAM	This command is used in SPI interfaces. Making sure to set SPI_WRAM= 1 before host writes SRAM via SPI interfaces.	0b: disable 1b: SPI interface write RAM enable																			
	DSPI_CFG[1:0]	DAUL SPI MODE Selection	00b: 1P1T for 1 wire 10b: 1P1T for 2 wire 11b: 2P3T for 2 wire 01b: reserve																			
DSPI_EN	DAUL SPI MODE Enable	0b: disable 1b: enable																				
Restriction	None																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>										Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value																					
Power On Sequence	00h																					
S/W Reset	00h																					
H/W Reset	00h																					
Flow Chart	<div><div><div>setDSPIMode(C4h)</div><div>↓</div><div>1st Parameter</div><div>↓</div><div>New DSPI mode loaded</div></div><div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div></div>																					

5.3.49 Read ID1 (DAh)

Table 91. Read ID1 (DAh)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	1	1	0	1	1	0	1	0	DAh												
1 st Para	Read	ID1[7:0]								00h												
Description	This read byte is used to track the LCD module/driver version. It is defined by the display supplier and changes each time a revision is made to the display, material or construction specifications. The ID1 is programmed by NVM function.																					
Restriction	None																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>										Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value																					
Power On Sequence	00h																					
S/W Reset	00h																					
H/W Reset	00h																					
Flow Chart	<div><div><div>RDID1 (DAh)</div><div>↓</div><div>Send ID1[7:0]</div></div><div>Host ----- Driver</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																					

5.3.50 Read ID2 (DBh)

Table 92. Read ID2 (DBh)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	1	1	0	1	1	0	1	1	DBh												
1 st Para	Read	ID2[7:0]								80h												
Description	This read byte is used to track the LCD module/driver version. It is defined by the display supplier and changes each time a revision is made to the display, material or construction specifications. This ID parameter range is from 80h to FFh. The ID2 is programmed by NVM function.																					
Restriction	None																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>										Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value																					
Power On Sequence	00h																					
S/W Reset	00h																					
H/W Reset	00h																					
Flow Chart	<div><div><div>RDID2 (DBh)</div><div>Host</div><div>Driver</div><div>Send ID2[7:0]</div></div><div><div>Legend</div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																					

5.3.51 Read ID3 (DCh)

Table 93. Read ID3 (DCh)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	1	1	0	1	1	1	0	0	DCh												
1 st Para	Read	ID3[7:0]								00h												
Description	This read byte identifies the LCD module/driver. It is specified by User. The ID3 is programmed by NVM function.																					
Restriction	None																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>										Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value																					
Power On Sequence	00h																					
S/W Reset	00h																					
H/W Reset	00h																					
Flow Chart	<div><div><div>RDID3 (DCh)</div><div>↓</div><div>Send ID3[7:0]</div></div><div>Host Driver</div></div> <div><div>Legend</div><div><div>Command</div><div>Parameter</div><div>Display</div><div>Action</div><div>Mode</div><div>Sequential transfer</div></div></div>																					

5.3.52 CMD Read Write Control (FDh)

Table 94. CMD Read Write Control (FDh)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
Command	Write	1	1	1	1	1	1	0	1	FDh												
1 st Para	Write	0	0	0	0	0	0	0	0	00h												
2 nd Para	Write	EXT_SPI_READ_EN		EXT_SPI_CNT[6:0]						00h												
3 rd Para	Write	0	0	0	0	0	0	0	0	00h												
Description	EXT_SPI_Read_En: This command is used to read extend page (expect page0) register by -SPI Interface. EXT_SPI_CNT[6:0]: To set the read parameter count.																					
	<div><div><div>Read Extend Page Register</div><div><div>Set Page</div><div>↓</div><div>Set Register FDh=0x008100 to Enable Ext. Read</div><div>↓</div><div>Read Register</div><div>↓</div><div>Set Register FDh=0x000000 to Disable Ext. Read</div></div><div><div>Ex. Read Page1 CMD 00h</div><div><div>FF,03,83,88,01</div><div>↓</div><div>FD,03,00,81,00</div><div>↓</div><div>Read Register 00h=03h</div><div>↓</div><div>FD,03,00,00,00</div></div></div></div></div>																					
Restriction	None																					
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Idle Mode Off, Sleep Out	Yes	Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Idle Mode Off, Sleep Out	Yes																					
Idle Mode On, Sleep Out	Yes																					
Sleep In	Yes																					
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h, 00h, 00h</td></tr><tr><td>S/W Reset</td><td>00h, 00h, 00h</td></tr><tr><td>H/W Reset</td><td>00h, 00h, 00h</td></tr></table>										Status	Default Value	Power On Sequence	00h, 00h, 00h	S/W Reset	00h, 00h, 00h	H/W Reset	00h, 00h, 00h				
Status	Default Value																					
Power On Sequence	00h, 00h, 00h																					
S/W Reset	00h, 00h, 00h																					
H/W Reset	00h, 00h, 00h																					
Flow Chart																						

5.3.53 EXTC Command Set Enable (FFh)

Table 95. EXTC Command Set Enable (FFh)

Page 0	W / R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	1	1	1	1	1	1	1	1	FFh
1 st Para	Write	1	0	0	0	0	0	1	1	83h
2 nd Para	Write	1	0	0	0	1	0	0	0	88h
3 rd Para	Write	PAGE[7:0]								XXh
Description	PAGE[7:0]: Set the command page.									
	PAGE[7:0]		Command Page							
	00h		Page 0							
	01h		Page 1							
	02h		Page 2							
	03h		Page 3							
	04h		Page 4							
	05h		Page 5							
	06h		Page 6							
	07h		Page 7							
	08h		Page 8							
	09h		Page 9							
	0Fh		Page F							
	Set the register, 1st Parameter = 83h, 2nd Parameter = 88h, 3rd Parameter = Page value to enable “page command set” available.									
Restriction	None									
Register Availability	Status		Availability							
	Normal Mode On, Idle Mode Off, Sleep Out		Yes							
	Normal Mode On, Idle Mode On, Sleep Out		Yes							
	Idle Mode Off, Sleep Out		Yes							
	Idle Mode On, Sleep Out		Yes							
	Sleep In		Yes							
Default	Status		Default Value							
	Power On Sequence		83h, 88h, 00h							
	S/W Reset		83h, 88h, 00h							
	H/W Reset		83h, 88h, 00h							
Flow Chart	See “5.1 Command Flow”									

6 Display Functions

6.1 Sleep Out Command and Self-Diagnostic Functions

6.1.1 Register Loading Detection

Sleep Out command (See Sleep Out (11h)) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller works properly.

The display controller will compare factory values of the EEPROM and register values of the display controller (1st step: compare register and EEPROM values; 2nd step: load EEPROM value to the register). If those two values (EEPROM and register values) are the same, a bit is inverted (= increased by 1), which is defined in command Read Display Self-Diagnostic Result (0Fh) (= RDDSDR) (The used bit of this command is D7). If those values are not the same, this bit (D7) is not inverted (= not increased by 1). The flow chart for this internal function is as follows:

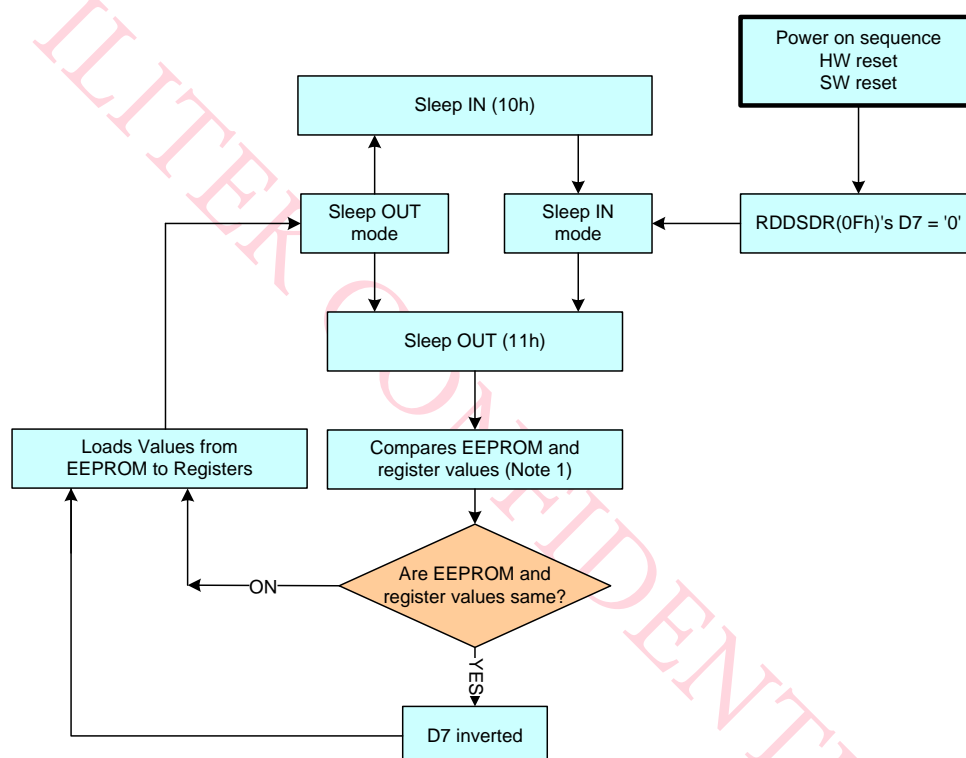


Figure 114. Register Loading Detection

Notes:

If the EEPROM and loaded register values are not compared, then they can be changed by 00h to AFh and DAh to DDh commands.

6.1.2 Functionality Detection

The Sleep Out command (See Sleep Out (11h)) is a trigger for an internal function of the display module. It indicates if the display module is still running and meets functionality requirements. The internal function (the display controller) is compared to check if the display module still meets functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirements are met, a bit is inverted (= increased by 1), defined in the command Read Display Self-Diagnostic Result (0Fh) (RDDSDR) (The used bit of this command is D6). If functionality requirement is not the same, this bit (D6) is not inverted (= not increased by 1). The flow chart for this internal function is as follows:

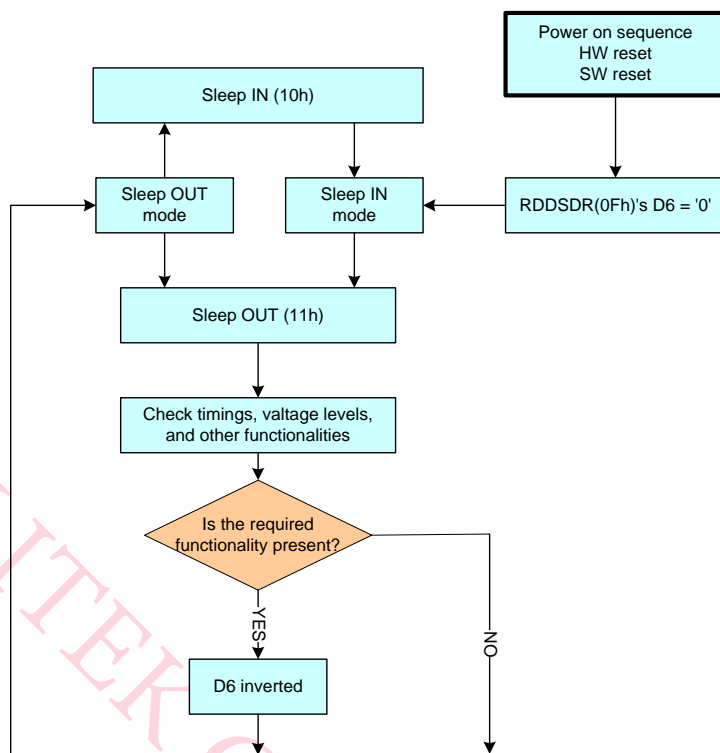


Figure 115. Functionality Detection

Notes:
When changing from the Sleep In mode to Sleep Out mode, 200msec are needed after the Sleep Out command before it is able to check if functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there will be 10msec delay for the D6's value to be valid when the Sleep Out command is sent in the Sleep Out mode.

6.2 TE Pin Output Signal

Tearing Effect Line signal can be output from TE pin as frame memory data transfer synchronous signals. TE signal is trigger for frame memory write operation to enable data transfer in synchronization with the scanning operation. Tearing Effect Output signal is turned on/off by Tearing Effect Line Off (34h) and Tearing Effect Line On (35h) commands.

Table 96. TE Pin Output

TEON (represents status of 35h command)	M (35h 1st parameter)	TE pin output
0	*	GND
1	0	TE (Mode1)
1	1	TE (Mode2)

Note :
1. Tearing Effect signal mode is defined by "M" of TEON (35h) command.
2. Write M=0 when using DSI TE report function.

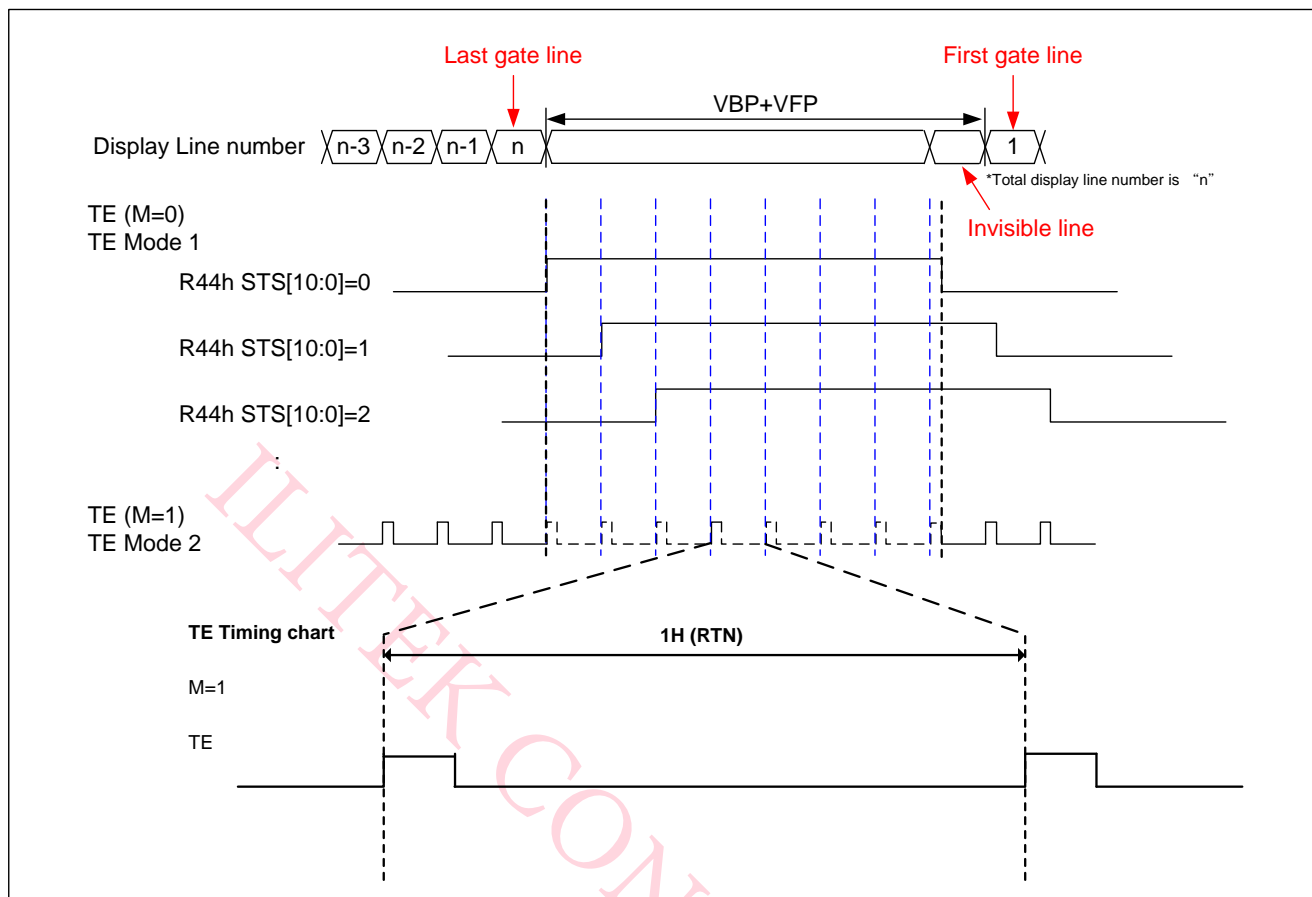


Figure 116. TE Pin Output Signal & Set Tear Scan Line Command (Page 0, R44h)

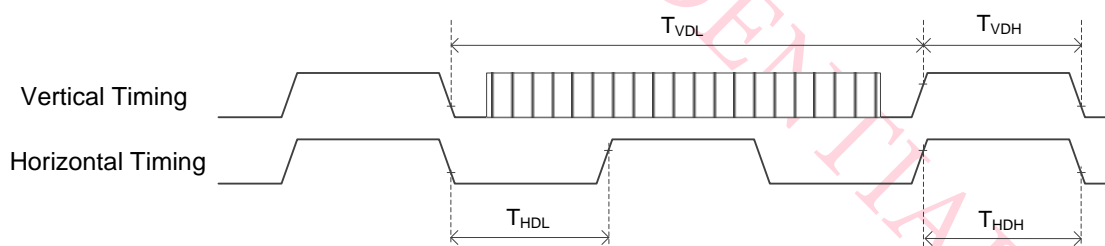


Figure 117. TE Timing Chart

Table 97. TE Pin Output timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Description
Vertical timing low duration	T_{VDL}	240	-	-	H	1*frame time- T_{VDH}
Vertical timing high duration	T_{VDH}	11	-	-	H	$T_{VDH} = V$ Porch time-1
Horizontal timing low duration	T_{HDL}	43.47	-	-	ns	
Horizontal timing high duration	T_{HDH}	43.47	-	-	ns	
Vertical Back Porch	VBP	8	8	-	Line	
Vertical Front Porch	VFP	8	8	-	Line	

6.3 CABC (Content Adaptive Brightness Control) function

The CABC, a dynamic backlight control function, drastically reduces power consumption of the luminance source. The IL79400A-XX will refer the gray scale content of the display image to output the LEDPWM pulse to the LED driver. The content of gray scale can be increased while simultaneously lowering the brightness of the backlight to achieve the same perceived brightness. The adjusted gray level scale and the power consumption reduction depend on the content of the image.

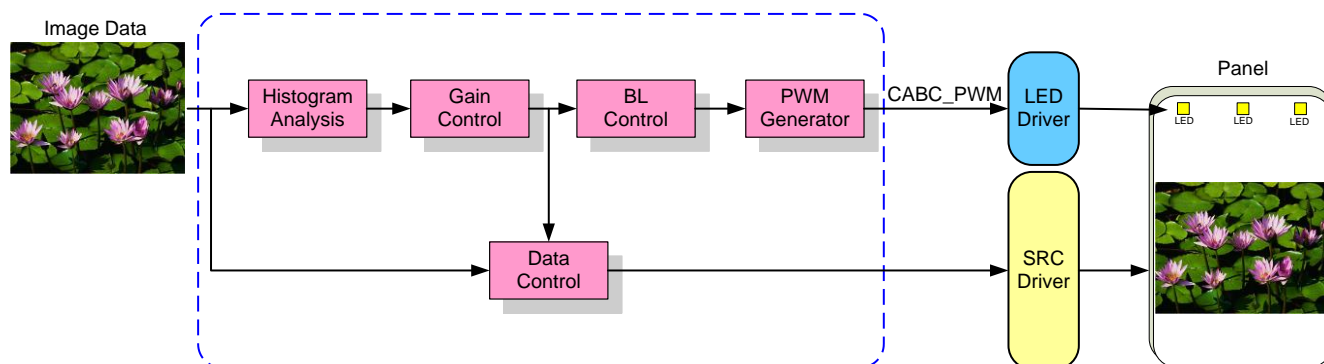


Figure 118. CABC Block Diagram

The IL79400A-XX can calculate the backlight brightness level and send a LEDPWM pulse to the LED driver via LEDPWM pad for backlight brightness control purposes. The PWM frequency can be adjusted by PWM_DIV parameters, and the calculating equation is shown below.

$$F_{\text{LEDPWM}} = \frac{25.5\text{MHz}}{(\text{PWM_DIV}[7:0]+1)} \times \text{PWM_DUTY_PRECISOIN}$$

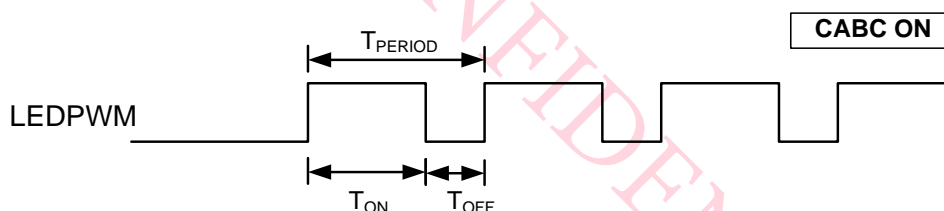


Figure 119. LEDPWM on/off period

6.4 Source Driver

The source driver uses 600 channels (S0~S601) which are used for driving the source line of the TFT LCD panel. The source driver converts the digital data into the analog voltage and generates the corresponding gray scale voltage output, enabling up to 16.7M colors to be displayed simultaneously. The output circuit of this source driver incorporates with an operational amplifier, so that a positive and a negative voltage can be alternately outputted from each channel.

6.5 Abnormal Power Off

The abnormal power off means a situation when e.g. there is removed a battery without the normal power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an abnormal power off event, IL79400A-XX will force the display to blank and will not be any abnormal visible effects within 1 second time on the display and remains blank until "Power On Sequence" powers it up.

6.6 Gamma Function

The Gamma structure of grayscale amplifier is shown as below. There are 16 voltage levels between GVDDP/GVDDN and VGS. It can be determined by the 16 adjustable registers.

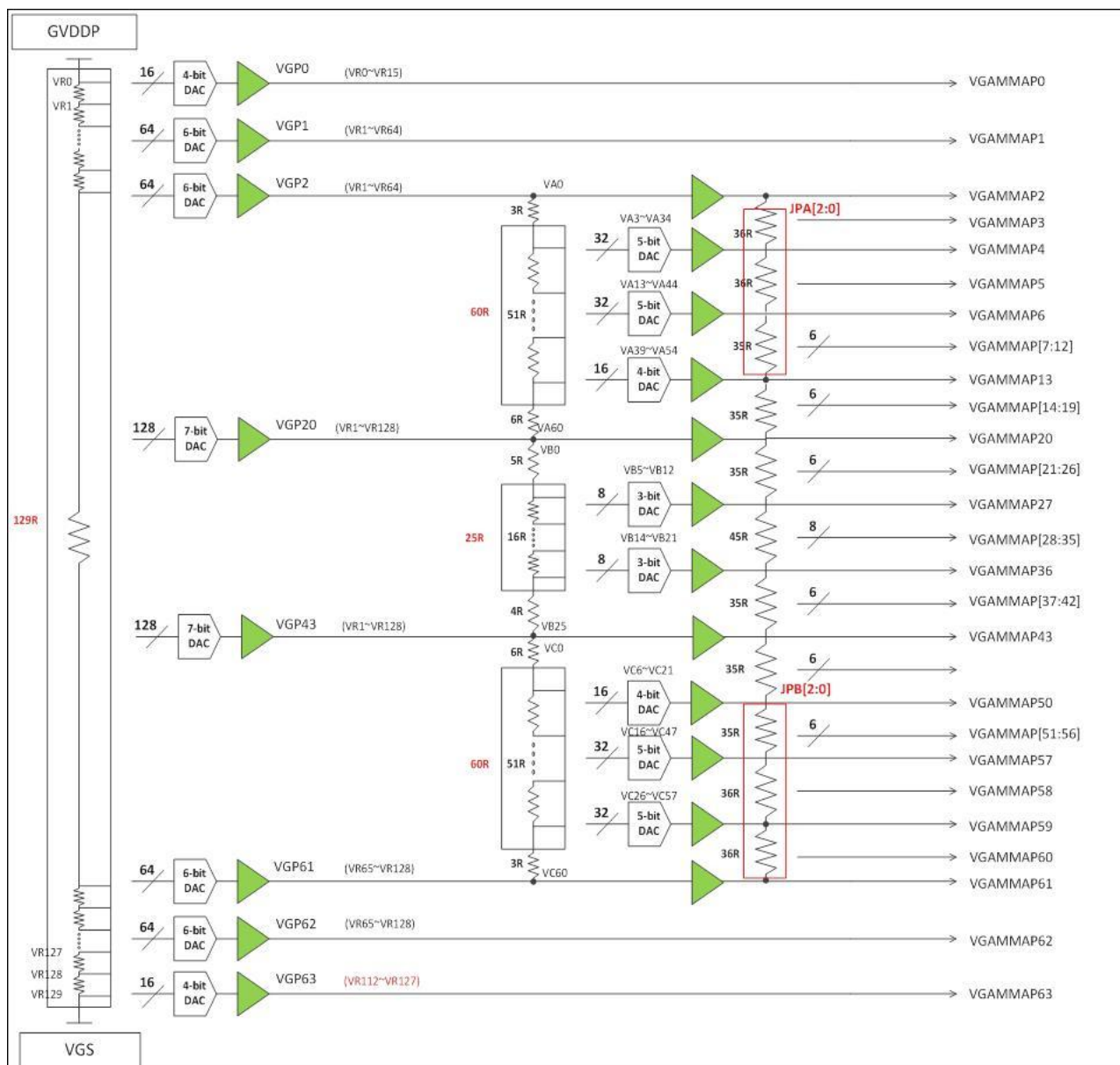


Figure 120. Positive Gamma Generation

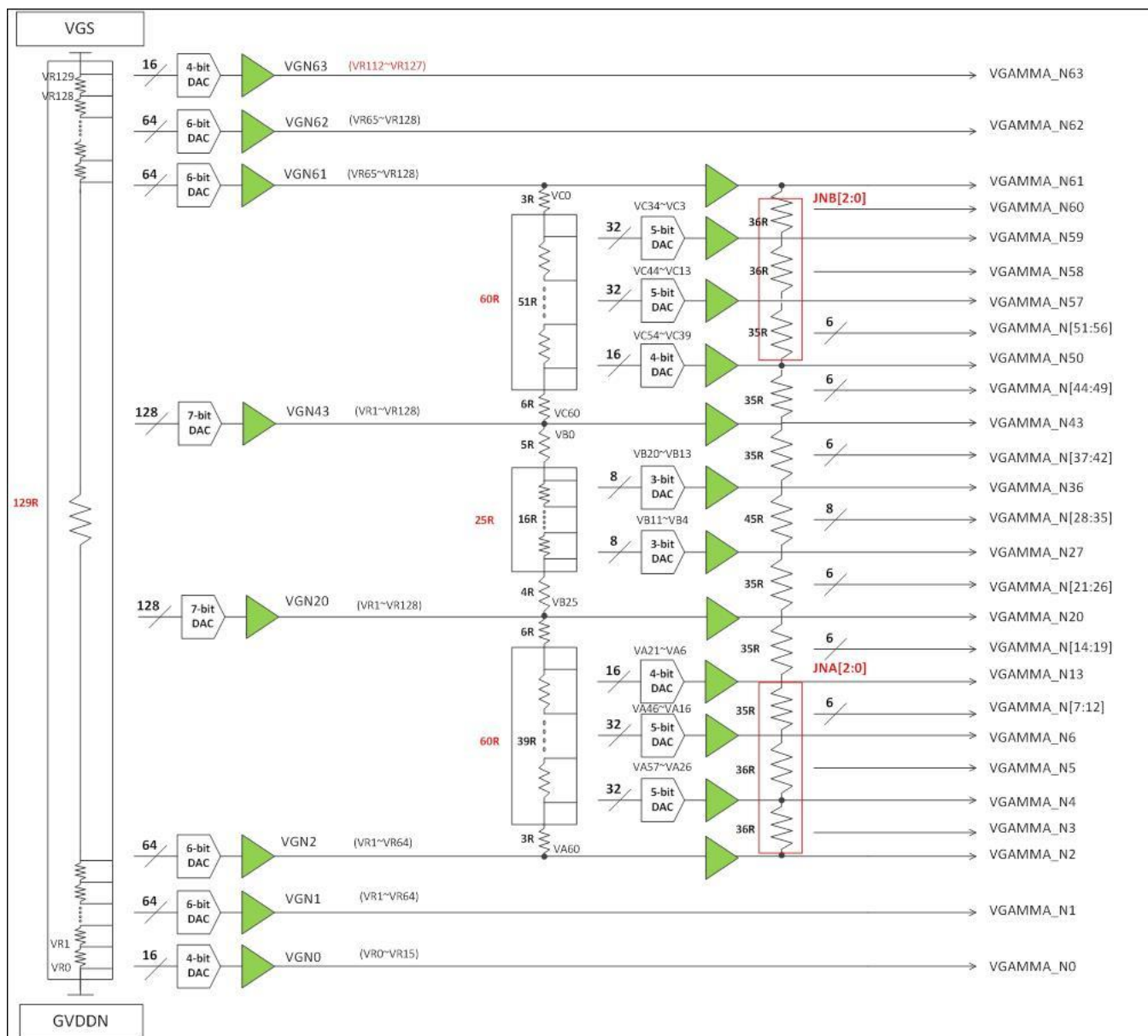


Figure 121. Negative Gamma Generation

6.7 NV Memory Programing Flow

- Auto Program
- One Byte Program
- Only Internal Program

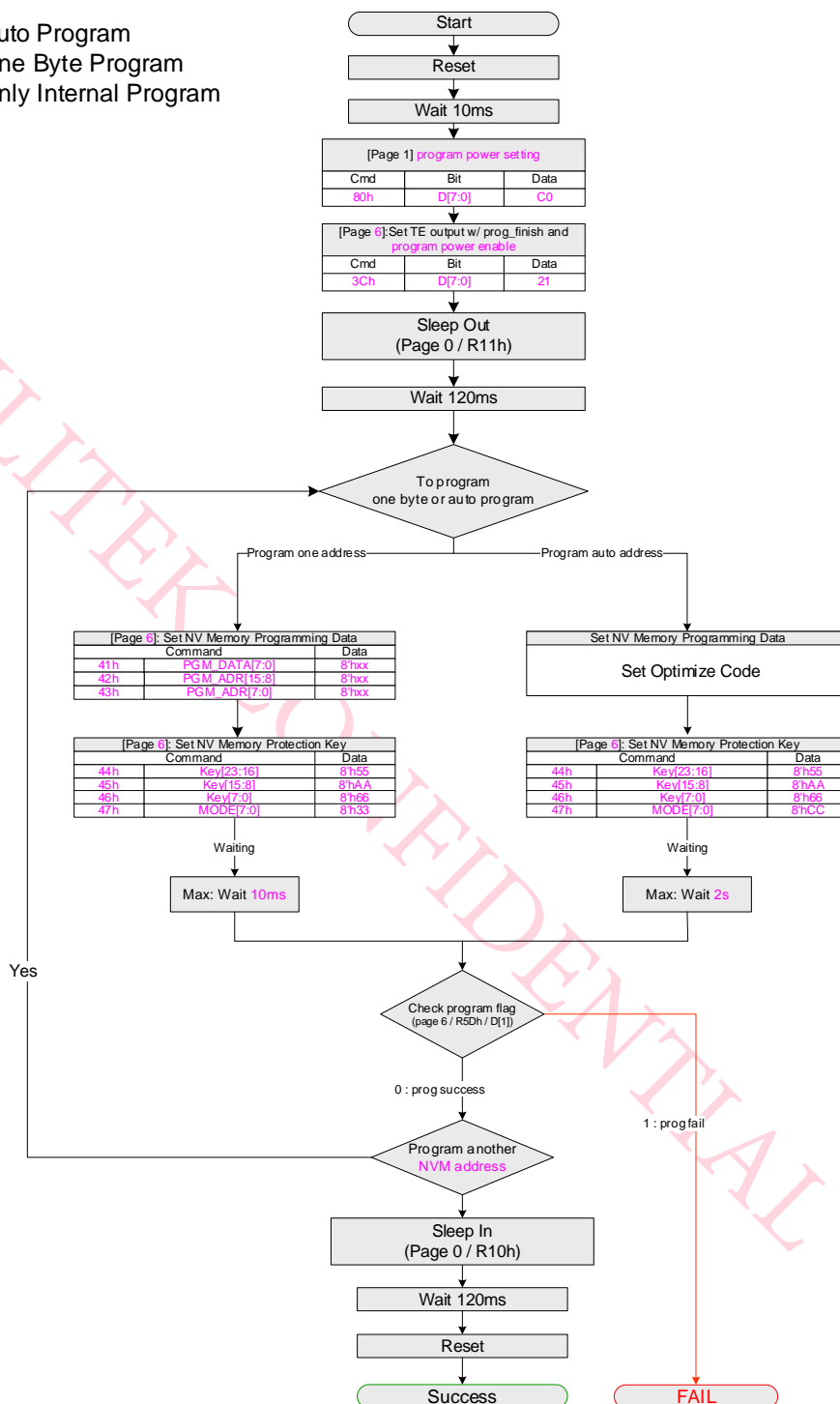


Figure 122. NV Memory Programing Flow Chart

6.8 VCOM NV Memory Programing Flow

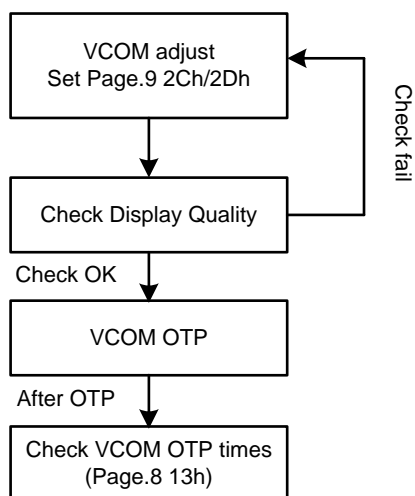


Figure 123. VCOM NV Memory Programing Flow Chart

7 Touch Panel Controller

7.1 Host Control Interface

7.1.1 Touch I2C Interface

The Slave end of I2C in IL79400A-XX is the one of interface for touch communication with HOST. Touch controller will send data transfer request to the HOST via I2C interface and complete the point report to the HOST. Once the TP_INT trigger signal is engaged, the HOST shall engage a data transfer to fetch the Touch Point information

The main features of the Touch I2C bus are:

- (1) Communication speed up to 400 kHz.
- (2) Support variableness of I2C Slave Address. (default:0x41)
- (3) External pull-up resistors are 4.7K Ω (suggested)

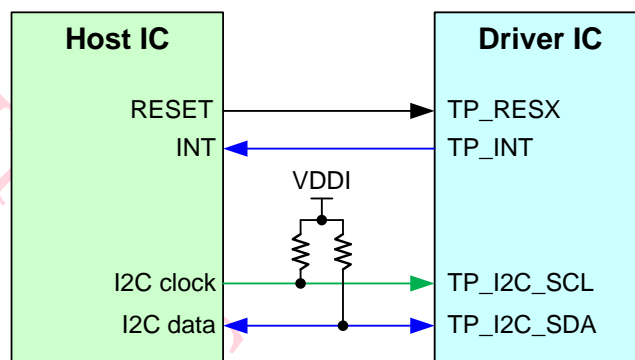


Figure 124. TP I2C System Interface Diagram

7.1.1.1 TP I2C Packet Format

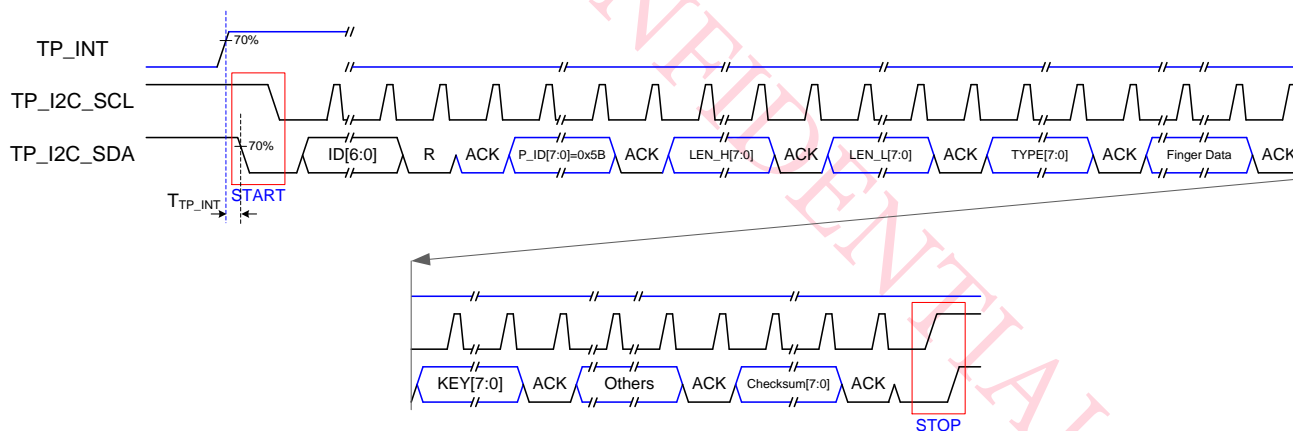


Figure 125. TP I2C Packet Format

Table 98. TP I2C Packet Content

Byte No.	Symbol	Function	Note
1	ID[6:0], WR	ID[6:0] = 0x41: Device ID, WR = 0b	
2	P_ID[7:0]	P_ID[7:0] = 0x5B: Demo Command	
3	LEN_H[7:0]	Packet Length High Byte	
4	LEN_L[7:0]	Packet Length Low Byte	
5	TYPE[7:0]	Finger pack, TYPE[2:0] = 01h: 5 bytes format.	
6~50	Finger Data	10 finger data, 5 bytes for each data	
51	KEY[7:0]	Not in used	
52~72	Others	Not in used	
73	Checksum[7:0]		

Note:

This packet format is for reference only, please contact ILITEK for more detail information.

7.1.2 Touch SPI Interface

The 4-Wire SPI interface is one of interface for touch communication with HOST.

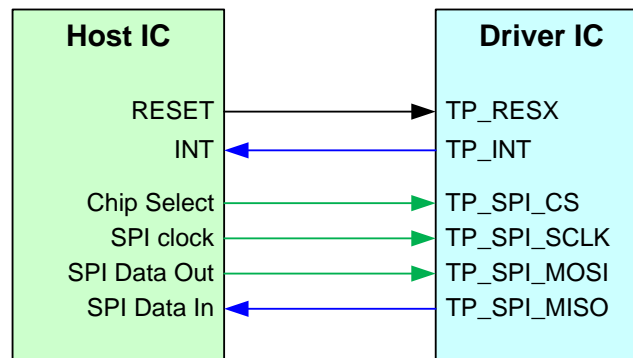


Figure 126. TP SPI 4-wire System Interface Diagram

7.1.2.1 TP SPI Packet Format

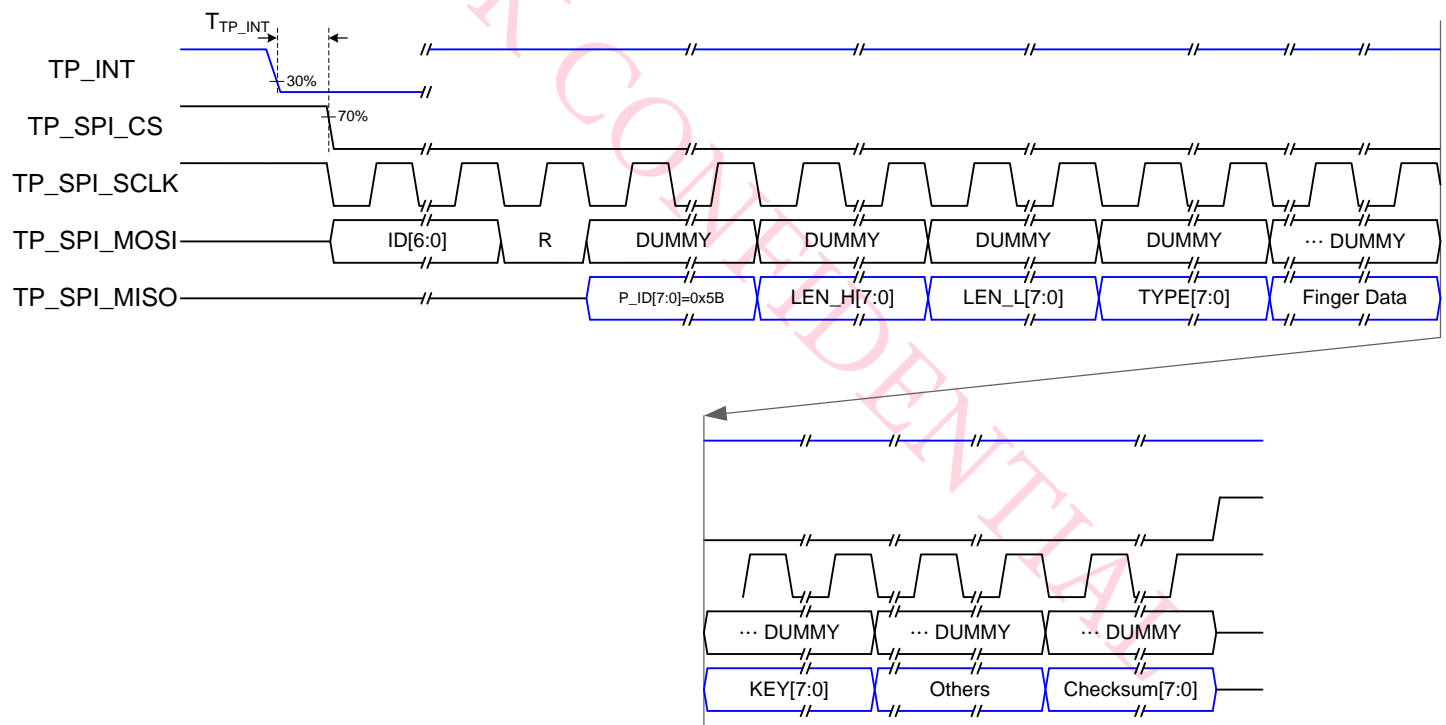


Figure 127. TP SPI Packet Format

Note:

1. The TP SPI Packet content is the same as "TP I2C Packet Content".
2. This packet format is for reference only, please contact ILITEK for more detail information.

7.1.3 General Purpose Input Output pins

The TP General Purpose Input Output (GPIO) pins is controllable by Embedded MCU at runtime. TP GPIO have no predefined purpose and are unused by default.

7.2 Flash Memory Interface

Flash Memory interface is used to communicate with external flash memory, which used to store the Firmware.

7.2.1 Flash Memory connection

The master mode Flash Serial Peripheral Interface (SPI) communicate with Flash Memory and fetch the Firmware for Embedded MCU to achieve the Touch function.

The main features of the Flash Memory interface are:

1. Communication speed up to 12 MHz
2. Master mode operation.
3. Configurable 8-bit length of a transfer word.
4. MSB first transfer.

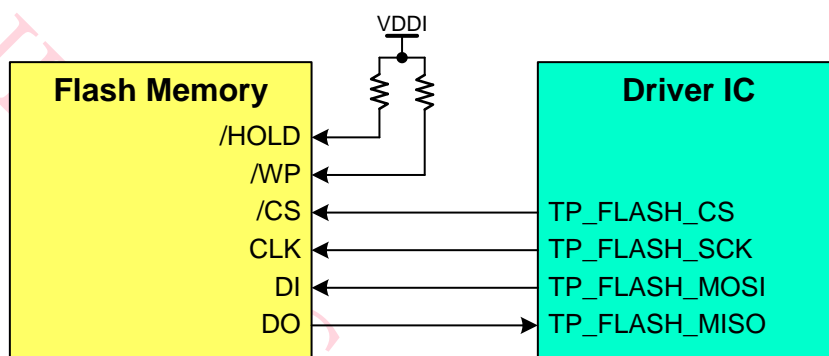


Figure 128. Flash SPI Interface Connection

Note: 0~100Kohm Pull-up resistor is suggested. (TBD)

8 Characteristics of I/O

8.1 Output or Bi-directional (I/O) Pins

Table 99. Status of Output or Bi-directional (I/O) Pins

Pin/Line	After Power On	After Hardware Reset	After Software Reset
HSSI_D0_P	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
HSSI_D0_N	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
TE	Low	Low	Low
LEDPWM	Low	Low	Low
SDI_RD_X	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
TP_I2C_SCL	High	High	High
TP_I2C_SDA	Hi-z	High	High
TP_INT	High/Low	High	High
TP_SPI_MISO	High/Low	Low	Low
TP_FLASH_CS	High	Low	Low
TP_FLASH_MISO	High/Low	Low	Low

Note:
 There will be no output from HSSI_D0_P, HSSI_D0_N, LEDPWM and TE during power on/off sequence and hardware reset.

8.2 Input Pins

Table 100. Status of Input Pins

Pin/Line	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power OFF Process
RESX	See Section 3.4.3	Input valid	Input valid	Input valid	See Section 3.4.3
TP_RESX	See Section 3.4.3	Input valid	Input valid	Input valid	See Section 3.4.3
IM[1:0]	Input invalid	Input valid	Input valid	Input valid	Input invalid
PSWAP	Input invalid	Input valid	Input valid	Input valid	Input invalid
FRM	Input invalid	Input valid	Input valid	Input valid	Input invalid
CS	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX_SCL	Input invalid	Input valid	Input valid	Input valid	Input invalid
HSSI_CLK_P	Input invalid	Input valid	Input valid	Input valid	Input invalid
HSSI_CLK_N	Input invalid	Input valid	Input valid	Input valid	Input invalid
HSSI_D0_P	Input invalid	Input valid	Input valid	Input valid	Input invalid
HSSI_D0_N	Input invalid	Input valid	Input valid	Input valid	Input invalid
TP_FLASH_MISO	Input invalid	Input valid	Input valid	Input valid	Input invalid
TP_SPI_CS	Input invalid	Input valid	Input valid	Input valid	Input invalid
TP_SPI_MOSI	Input invalid	Input valid	Input valid	Input valid	Input invalid
TP_SPI_SCLK	Input invalid	Input valid	Input valid	Input valid	Input invalid

9 Electrical Characteristics

9.1 Absolute Maximum Ratings

The absolute maximum rating is listed on the following table. When the IL79400A-XX is used out of the absolute maximum ratings, it may be permanently damaged. To use the IL79400A-XX within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the IL79400A-XX will malfunction and cause poor reliability.

Table 101. Absolute Maximum Ratings

Item	Symbol	Unit	Value
Analog Operating Voltage	VCI ~ GND	V	-0.3 ~ +3.6
Digital Operating Voltage	VDDI ~ GND	V	-0.3 ~ +3.6
Analog Operating Voltage	AVDD ~ GND	V	-0.3 ~ +6.3
Gate Driver High Voltage	VGH ~ GND	V	-0.3 ~ +20
Gate Driver Low Voltage	VGLO ~ GND	V	0.3 ~ -16.4
Driver Supply Voltage	VGH - VGL	V	≤ 32V
Driver Supply Voltage	VDDI - VCL	V	≤ 6.5V
Driver Supply Voltage	VDDI - VCOM	V	≤ 6.5V
Input Voltage	VIN	V	-0.3 ~ VDDI+ 0.3
MIPI differential input	HSSI_CLK_P / HSSI_CLK_N HSSI_D0_P / HSSI_D0_N	V	-0.3 ~ + 1.3
Operating Temperature	T _{OPER}	°C	Refer to Chapter 2 Note 2. Part_number_description
Storage Temperature	T _{STOR}	°C	-55 ~ +125

Note:

If one of the above parameters is exceeded the absolute maximum rating even momentarily, the quality of the product may be degraded or be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

9.2 DC Characteristics

Table 102. I/O and Input Power DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Analog operating voltage	VCI	2.7	3.3	3.6	V	
Digital operating voltage	VDDI	1.65	1.8	3.6	V	
Analog operating voltage	AVDD	4.5	5.5	6.3	V	
Logic High level input voltage	VIH	0.7*VDDI		VDDI	V	Note 1, 6
Logic Low level input voltage	VIL	0		0.3*VDDI	V	Note 1, 6
Logic High level output voltage	VOH	0.8*VDDI		VDDI	V	IOH = -1.0mA ^{Note 1, 7}
Logic Low level output voltage	VOL	0		0.2*VDDI	V	IOL = +1.0mA ^{Note 1, 7}
Gate Driver High Voltage	VGH	8.4	16	20	V	Note 4
Gate Driver Low Voltage	VGLO	-6.0	-10	-16	V	Note 4
Driver Supply Voltage	VSPLY	-	-	32	V	Note 5
Positive Source Output Range	VSOUT	0.2	-	GVDDP	V	Note3
Negative Source Output Range	VSOUT	GVDDN	-	-0.2	V	Note3
Positive Gamma Reference Voltage	GVDDP	3	-	5.9	V	Note4
Negative Gamma Reference Voltage	GVDDN	-5.9	-	-3	V	Note4
Source Output Setting Time	T _R	-	2.83	-	us	Below with 99% Precision. ^{Note2,3}
Output Deviation Voltage (Source Output channel)	V _{DEV}	-	-	±10	mV	S _{OUT} ≥ 4.2V
		-	-	±5	mV	S _{OUT} ≤ 0.8V ^{Note2} 4.2V > S _{OUT} > 0.8V
Output Offset Voltage	V _{OFFSET}	-	-	TBD	mV	Note2
DC VCOM Amplitude Voltage	VCOM	-4.0	-	-0.2	V	Note2
Sleep In mode	I(VCI SLP IN)	-	TBD	-	uA	Ta = 25°C VCI=3.3V VDDI=1.8V
	I(VDDI SLP IN)	-	TBD	-	uA	
Deep Standby mode	I(VCI DSTB)	-	TBD	-	uA	
	I(VDDI DSTB)	-	TBD	-	uA	

Note:

1. VCI = 2.7V to 3.6V , VDDI = 1.65V to 3.6V
2. Source channel loading = 5.2KΩ, 17pF/channel
3. The maximum value is between Note2 measure point and Gamma setting value
4. GVDDP ≤ AVDD-0.3V and GVDDN ≥ AVEE+0.3V.
5. Driver Supply Voltage is "VGH + TVCH - VGL(VGLO)".
6. Logic input pins include IM[1:0], PSWAP, RESX, FRM, CSX, WRX_SCL, SDI_RDX(input mode), DCX,D[7:0](input mode), TP_RESX, TP_I2C_SCL, TP_I2C_SDA(input mode), TP_FLASH_MISO, TP_SPI_CS, TP_SPI_SCLK, TP_SPI_MOSI.
7. Logic output pins include TE, LEDPWM, SDI_RDX(output mode), D[7:0](output mode), TP_I2C_SDA(output mode), TP_FLASH_CS, TP_FLASH_SCLK, TP_FLASH_MOSI, TP_SPI_MISO

9.3 DSI DC Characteristics

The DSI uses different state codes which depend on DC voltage levels of the clock and data lanes. The meaning of the state codes is defined in the following table.

Table 103. Line DC Voltage Levels

State Code	CLOCK_P or DATA_P	CLOCK_N or DATA_N
HS-0	Low (HS)	High (HS)
HS-1	High (HS)	Low (HS)
LP-00	Low (LP)	Low (LP)
LP-01	Low (LP)	High (LP)
LP-10	High (LP)	Low (LP)
LP-11	High (LP)	High (LP)

9.3.1 DC Characteristics for DSI LP Mode

DC levels of the LP-00, LP-01, LP-10 and LP-11 are defined in the table below: DC Characteristics for the DSI LP mode when LP-RX, LP-CD or LP-TX is mentioned in the condition column. Other logical levels in the table are for MCU interface.

Table 104. DSI LP Mode DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic 1 input voltage	V_{IHLPCD}	LP-CD	450	-	1320	mV
Logic 0 input voltage	V_{ILLPCD}	LP-CD	0.0	-	200	mV
Logic 1 input voltage	V_{IHLPRX}	LP-RX (CLK, D0)	880	-	1320	mV
Logic 0 input voltage	V_{ILLPRX}	LP-RX (CLK, D0)	0.0	-	550	mV
Logic 0 input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0.0	-	300	mV
Logic 1 output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic 0 output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic 1 input current	I_{IH}	LP-CD, LP-RX	-	-	10	uA
Logic 0 input current	I_{IL}	LP-CD, LP-RX	-10	-	-	uA

Notes:

- DSI High Speed mode is off.

9.3.2 Spike/Glitch Rejection

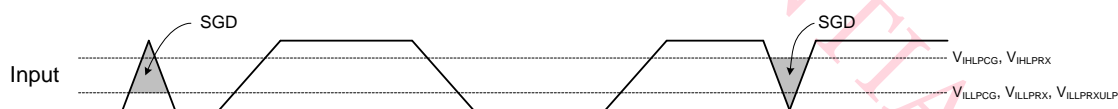


Figure 129. Spike/Glitch Rejection

Notes:

A spike/glitch can be rejected when the Peak Interference Amplitude is 200mV (at maximum) and Interference Frequency is 450MHz (at the very least).

Table 105. Spike/Glitch Rejection

Parameter	Symbol	Min	Max	Unit	Condition
Input pulse rejection for DSI	SGD	-	300	Vps	CLKP/N, D0P/N

9.3.3 DC Characteristics for DSI HS mode

Table 106. DC Characteristics for DSI HS mode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Common Mode Voltage for Clock	V_{CMCLK}	70	-	330	mV	CLKP/N Note 2,3
Input Common Mode Voltage for Data	V_{CMDATA}	70	-	330	mV	D0P/N Note 2,3
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	-50	-	50	mV	CLKP/N Note 4
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	-50	-	50	mV	D0P/N Note 4
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	-	-	100	mV	CLKP/N
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	-	-	100	mV	D0P/N
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	-70	-	-	mV	CLKP/N
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	-70	-	-	mV	D0P/N
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	-	-	70	mV	CLKP/N
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	-	-	70	mV	D0P/N
Single-ended Input Low Voltage	V_{ILHS}	-40	-	-	mV	CLKP/N, D0P/N Note 3
Single-ended Input High Voltage	V_{IHHS}	-	-	460	mV	CLKP/N, D0P/N Note 3
Differential Termination Resistor	R_{TERM}	80	100	125	Ω	CLKP/N, D0P/N Note 5
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	-	-	450	mV	CLKP/N, D0P/N
Termination Capacitor	C_{TERM}	-	-	60	pF	CLKP/N, D0P/N Note 5

Note:

1. $V_{CI} = 2.7V$ to $3.6V$, $V_{DDI} = 1.65V$ to $3.3V$.
2. Includes 50mV (-50mV to 50mV) ground difference
3. Without $V_{CMRCLKM450}/V_{CMRDATAM450}$
4. Without 50mV (-50mV to 50mV) ground difference
5. For higher bit rates, a 14pF capacitor will be needed to meet the common-mode return loss specification.

The DSI receiver (HS mode) understands that there is logical 1 (= HS-1) when a differential voltage is more than V_{THH} (CLKP/D0P). The DSI receiver (HS mode) understands that there is logical 0 (= HS-0) when a differential voltage is more than V_{THL} (CLKN/D0N). There is undefined state if the differential voltage is less than V_{THH} (CLKP/D0P) and less than V_{THL} (CLKN/D0N). A reference figure is below.

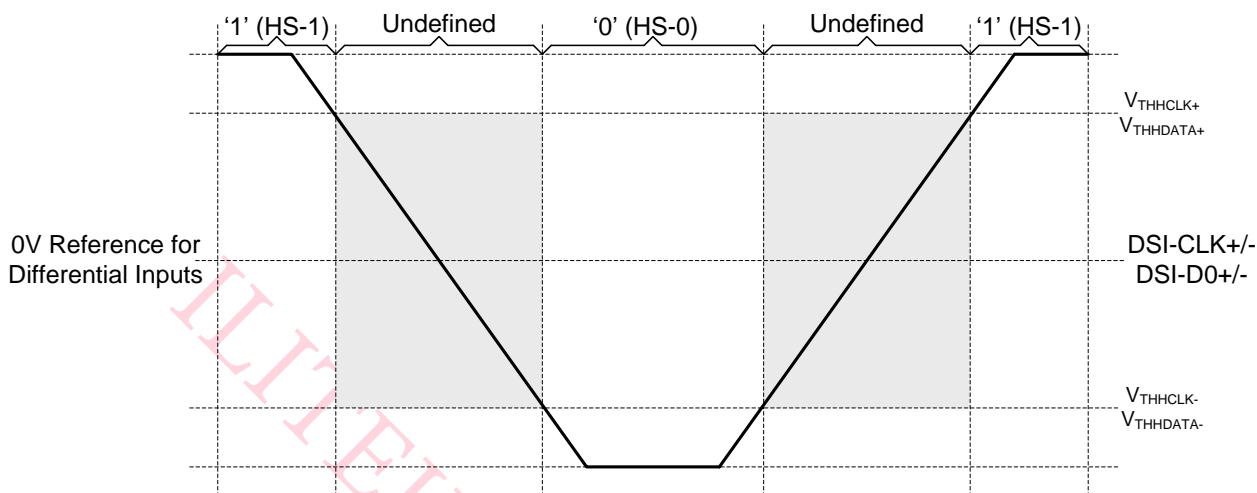


Figure 130. Differential Inputs Logical 0 and 1, Threshold High/Low, Differential Voltage Range

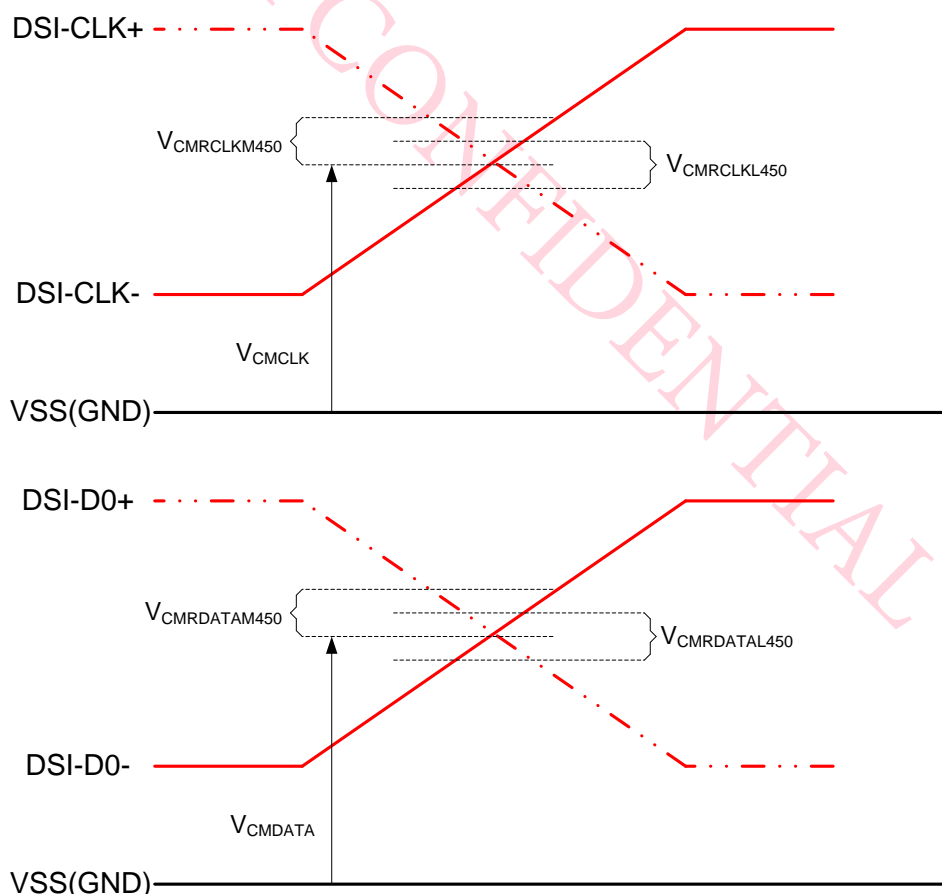


Figure 131. Common Mode Voltage on Clock and Data Channels

The termination resistor (R_{TERM}) of the differential DSI receiver can be driven to two different states by the receiver:
Low Power (LP) mode when the termination resistor is not connected between differential inputs (CLKP \Leftrightarrow CLKN or D0P \Leftrightarrow D0N)

High Speed (HS) mode when the termination resistor is connected between differential inputs (CLKP \Leftrightarrow CLKN or D0P \Leftrightarrow D0N)

The termination switch (HS/LP), when the termination resistor is not connected, is illustrated below.

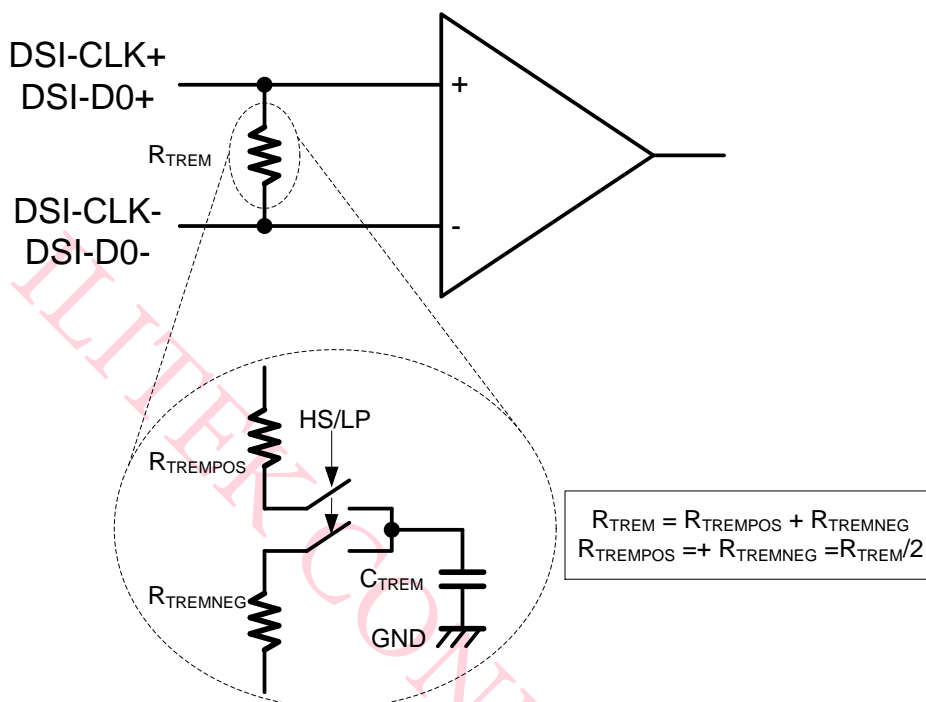


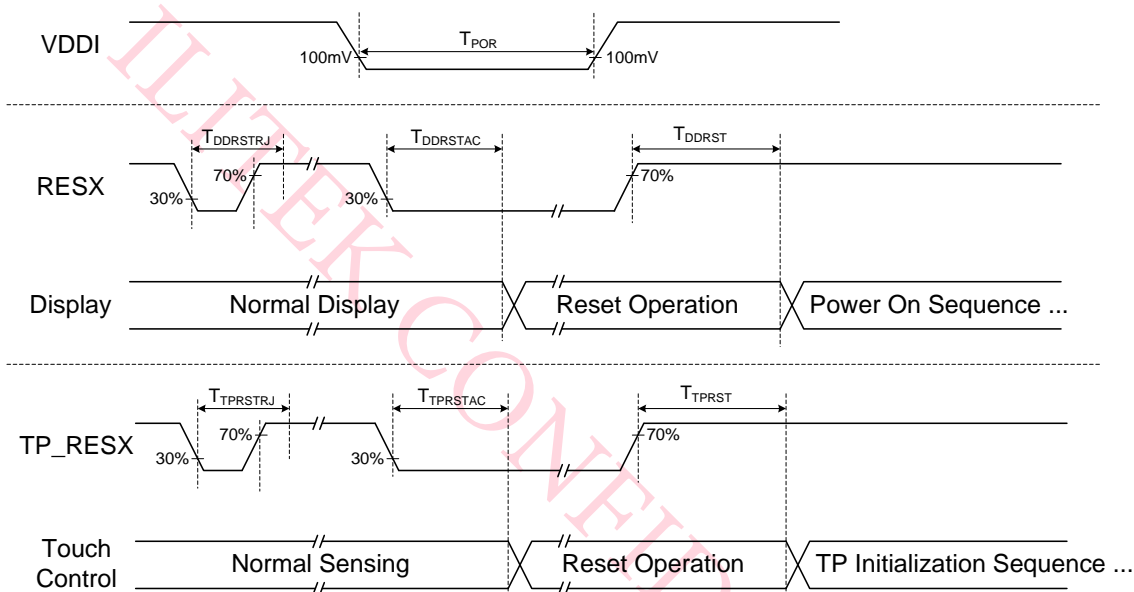
Figure 132. Differential Pair Termination Resistor on the Receiver Side

9.4 AC Characteristics

9.4.1 Reset Timing

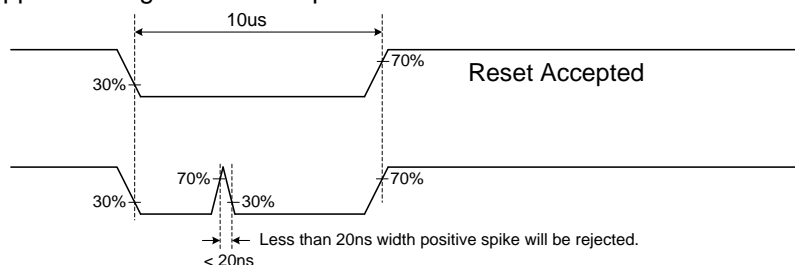
Table 107. Reset Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Power On Reset period	T_{POR}	100	-	-	ms	
RESX Reset rejection	$T_{DDRSTRJ}$	-	-	5	us	Note 1
RESX Reset pulse acceptance	$T_{DDRSTAC}$	10	-	-	us	
RESX Reset period	T_{DDRST}	35	-	-	ms	Sleep in Mode Note 1,5
		150	-	-	ms	Sleep Out mode Note 1,6,7
TP_RESX Reset rejection	$T_{TPRSTRJ}$	-	-	5	us	Note 1
TP_RESX Reset pulse acceptance	$T_{TPRSTAC}$	10	-	-	us	
TP_RESX Reset period	T_{TPRST}	100	-	-	ms	


Figure 133. Reset Timing

Note:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM to registers. This loading is done every time when there is H/W reset reject time ($T_{DDRSTRJ}$ & $T_{TPRSTRJ}$) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset.
3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 150 ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode.) and return to default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:

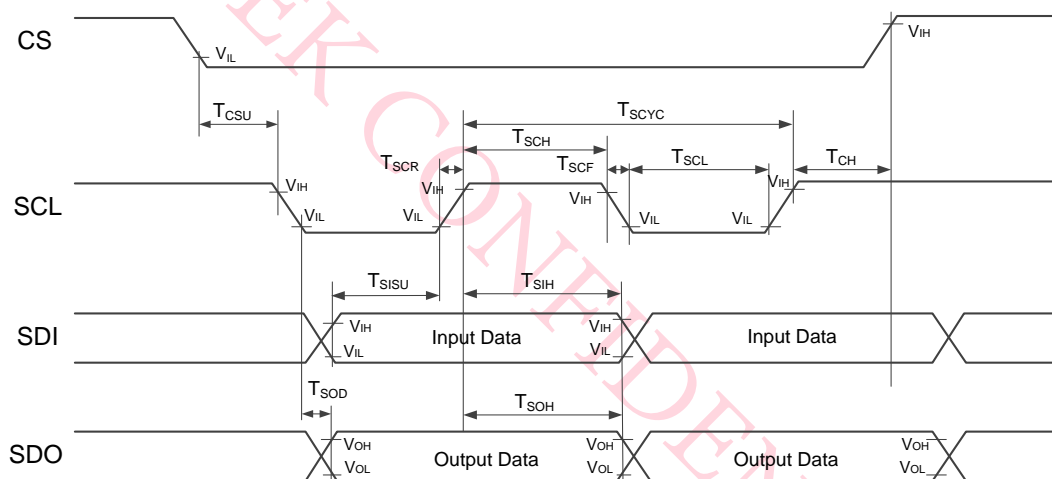
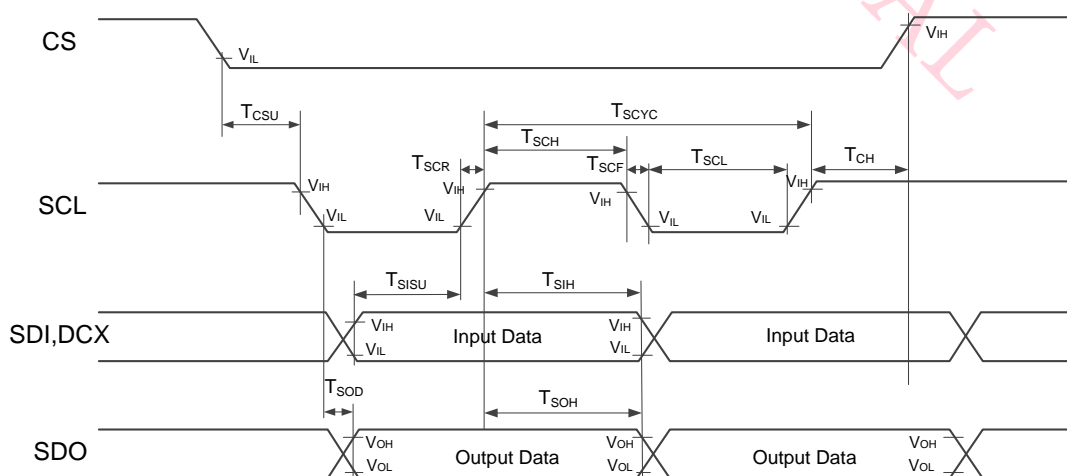

Figure 134. Spike Rejection

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 35ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 150ms.

9.4.2 Display SPI Interface Timing

Table 108. Display SPI Interface Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
SCL Clock cycle (write)	T_{SCYC}	16*	-	-	ns	
SCL Clock cycle (read)	T_{SCYC}	280	-	-	ns	
SCL Clock "H" pulse width (write)	T_{SCH}	7	-	-	ns	
SCL Clock "H" pulse width (read)	T_{SCH}	130	-	-	ns	
SCL Clock "L" pulse width (write)	T_{SCL}	7	-	-	ns	
SCL Clock "L" pulse width (read)	T_{SCL}	130	-	-	ns	
SCL Clock rise time	T_{SCR}	-	-	2.5	ns	
SCL Clock fall time	T_{SCF}	-	-	2.5	ns	
Chip select setup time	T_{CSU}	12	-	-	ns	
Chip select hold time	T_{CH}	12	-	-	ns	
Data input setup time	T_{SISU}	6	-	-	ns	
Data input hold time	T_{SIH}	6	-	-	ns	
Data output setup time	T_{SOD}	-	-	140	ns	
Data output hold time	T_{SOH}	6	-	-	ns	


Figure 135. SPI and Dual-SPI 3-wire Serial Interface Timing

Figure 136. SPI and Dual-SPI 4-wire Serial Interface Timing

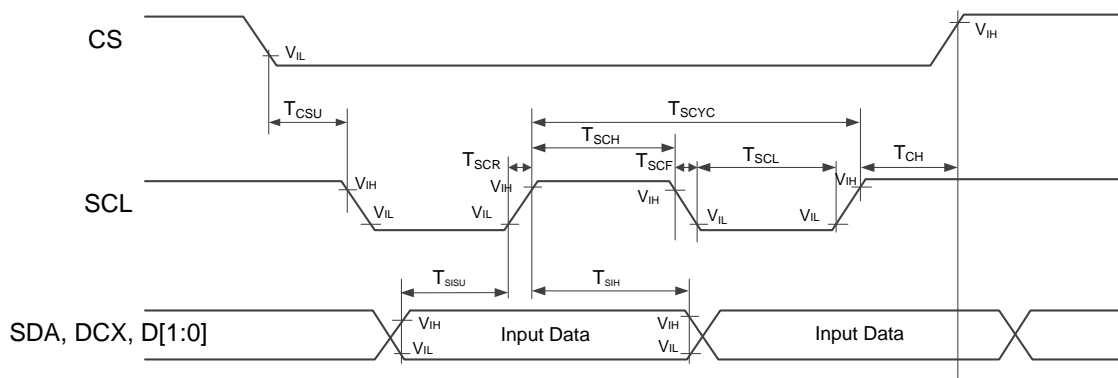


Figure 137. Quad-SPI Serial Interface Timing

Note:

1. Logic high and low levels are specified as 20% and 80% of VDDI for input signals.
2. To use QSPI in 63MHz condition, please contact ILITEK for more detail information.

9.4.3 Display Parallel 8-bit bus Timing

Table 109. Parallel 8-bit bus Read Mode Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
CSX hold time when read	T_{RCH}	15	-	-	ns	
Read cycle time	T_{RC}	180	-	-	ns	Command Read
		380	-	-	ns	RAM Read
Low pulse width of SCL	T_{RDL}	90	-	-	ns	Command Read
		190	-	-	ns	RAM Read
High Pulse width of SCL	T_{RDH}	90	-	-	ns	Command Read
		190	-	-	ns	RAM Read
Read data delay time	T_{RDD}	--	-	100	ns	
Output data hold time	T_{ODH}	5	-	--	ns	

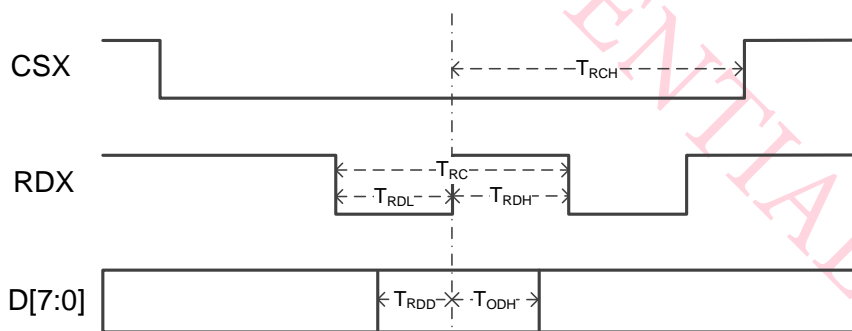
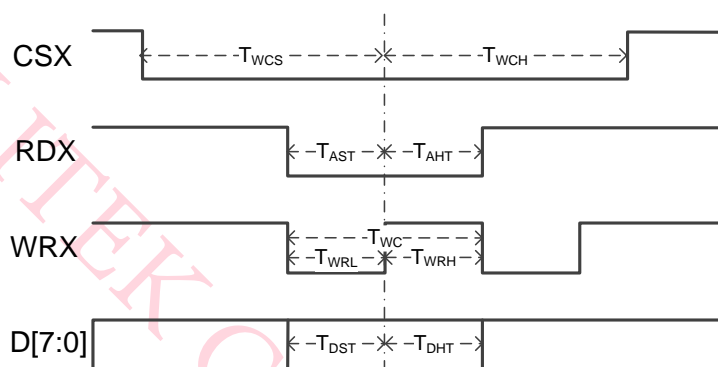


Figure 138. Parallel 8-bit bus Read Mode Timing

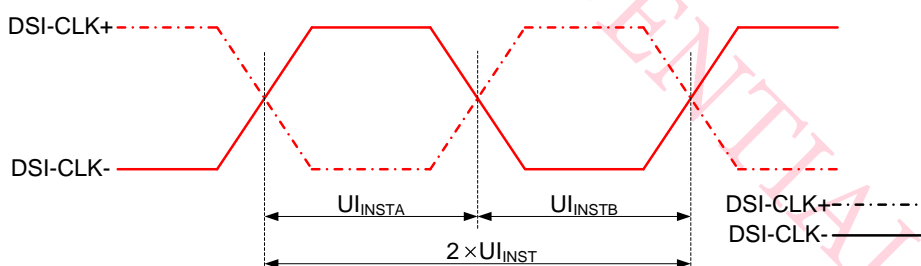
Table 110. Parallel 8-bit bus Write Mode Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
CSX setup time when write	T_{WCS}	15	-	-	ns	
CSX hold time when write	T_{WCH}	15	-	-	ns	
RDX setup time	T_{AST}	10	-	-	ns	
RDX hold time	T_{HAT}	10	-	-	ns	
WRX Write cycle	T_{WC}	20	-	-	ns	
WRX Write Control pulse L duration	T_{WRL}	12	-	-	ns	
WRX Write Control pulse H duration	T_{WRH}	12	-	-	ns	
Data Bus Write setup time	T_{DST}	10	-	-	ns	
Data Bus Write hold time	T_{DHT}	10	-	-	ns	


Figure 139. Parallel 8-bit bus Write Mode Timing

9.4.4 DSI Timing Characteristics

9.4.4.1 High Speed Mode – Clock Channel Timing


Figure 140. DSI Clock Channel Timing
Table 111. DSI Clock Channel Timing

Parameter	Symbol	Min	Max	Unit	Condition
Double UI instantaneous	$2 \times U_{IINST}$	4	13.2	ns	DSI-CLK+/-
UI instantaneous Half	U_{IINSTA}, U_{IINSTB}	2	6.6	ns	DSI-CLK+/-

Notes: $UI = U_{IINSTA} = U_{IINSTB}$

9.4.4.2 High Speed Mode – Data Clock Channel Timing

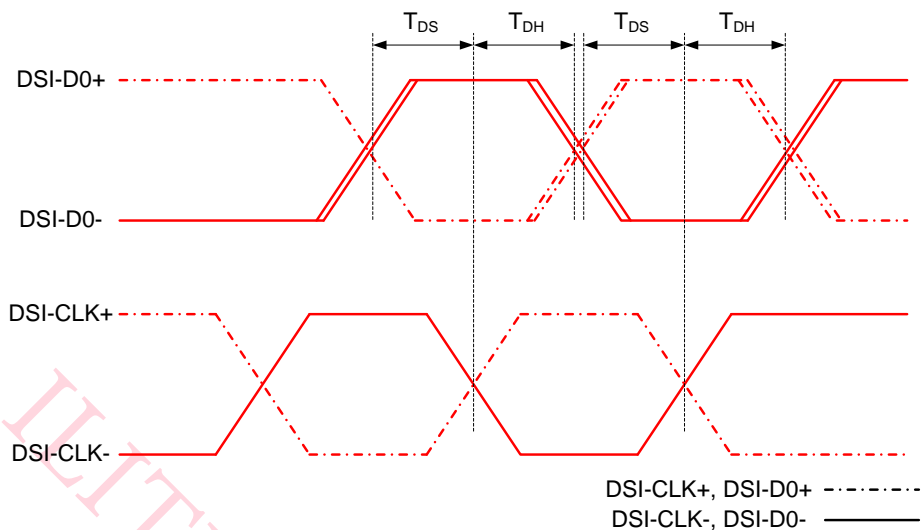


Figure 141. DSI Data to Clock Channel Timings

Table 112. DSI Data to Clock Channel Timings

Parameter	Symbol	Min.	Max.	Unit	Condition
Data to Clock Setup time	T_{DS}	0.15	-	UI	DSI-D0+/-
Clock to Data Hold Time	T_{DH}	0.15	-	UI	DSI-D0+/-

9.4.4.3 High Speed Mode – Rising and Falling Timings

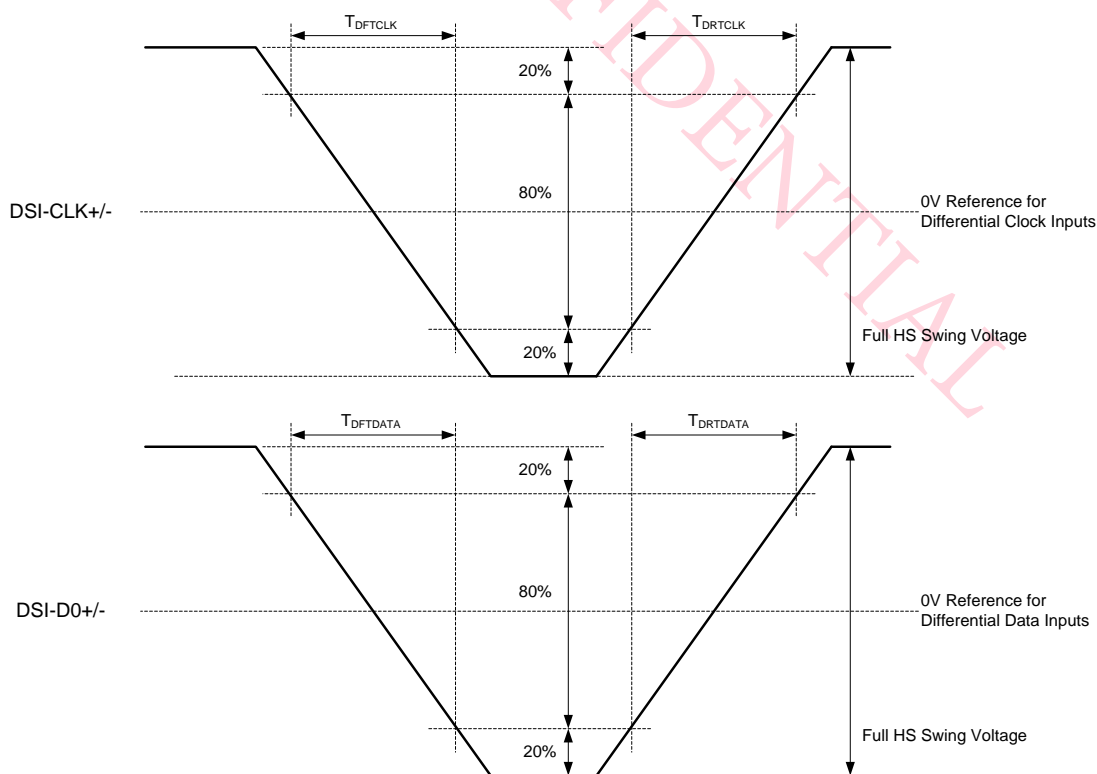


Figure 142. Rising and Falling Timings on Clock and Data Channels

Table 113. Rise and Fall Timings on Clock and Data Channels

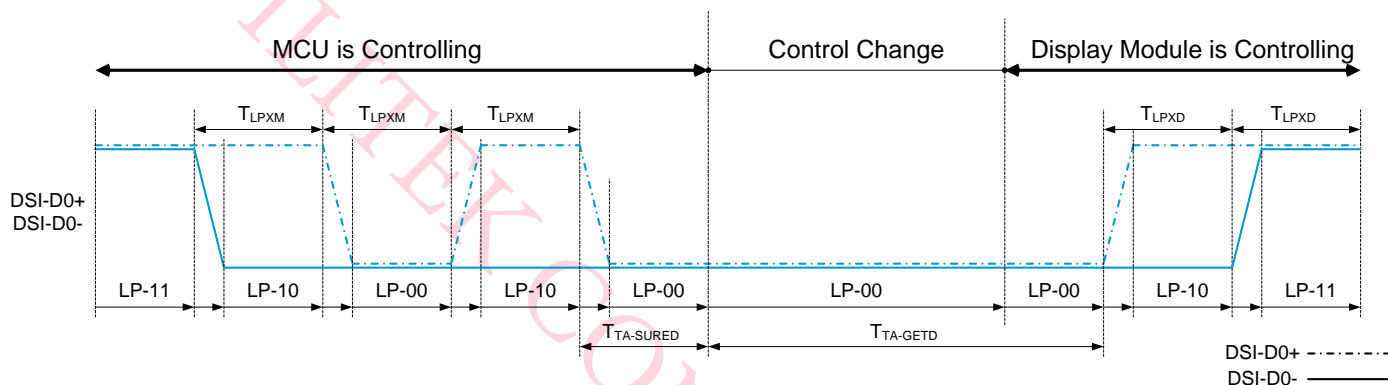
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Differential Rise Time for Clock	T_{DRTCLK}	150	-	$0.3 \times UI$	ps	DSI-CLK+/-
Differential Rise Time for Data	$T_{DRTDATA}$	150	-	$0.3 \times UI$	ps	DSI-D0+/-
Differential Fall Time for Clock	T_{DFTCLK}	150	-	$0.3 \times UI$	ps	DSI-CLK+/-
Differential Fall Time for Data	$T_{DFTDATA}$	150	-	$0.3 \times UI$	ps	DSI-D0+/-

Note:

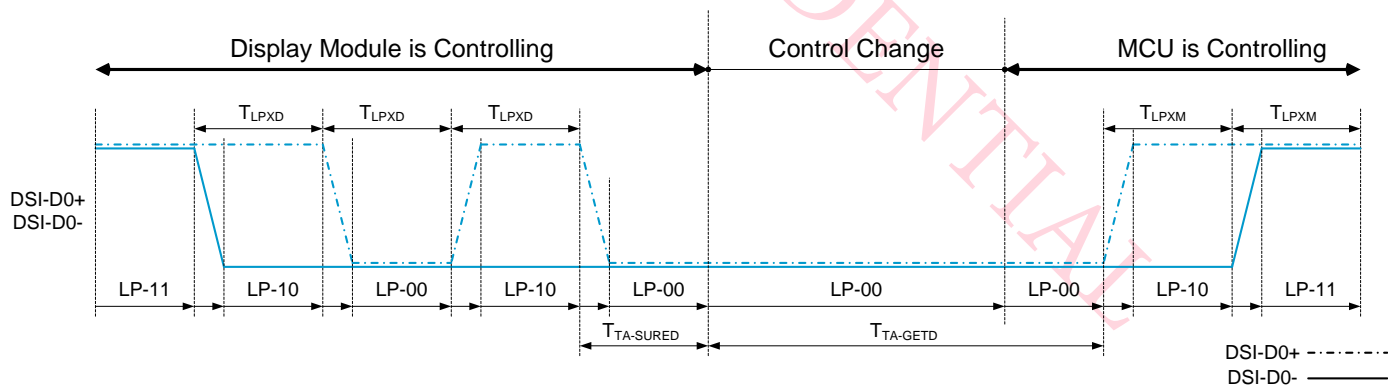
The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.

9.4.4.4 Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (IL79400A-XX) are illustrated for reference purposes below.


Figure 143. BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (IL79400A-XX) to the MCU are illustrated for reference purposes below.

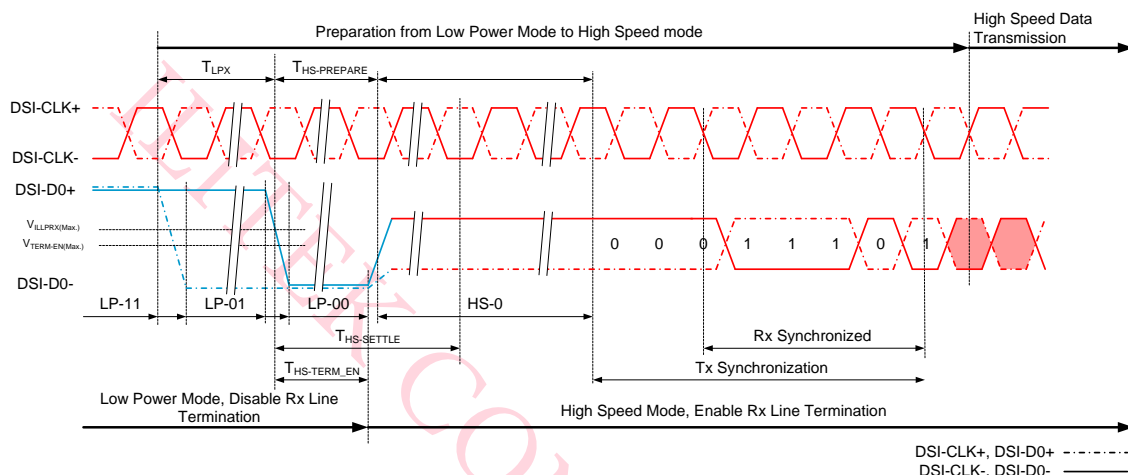

Figure 144. BTA from the Display Module to the MCU
Table 114. Low Power State Period Timings – A

Parameter	Symbol	Min.	Max.	Unit	Condition
Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → Display Module (IL79400A-XX)	T_{LPXM}	50	100	ns	D0P/N
Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (IL79400A-XX) → MCU	T_{LPXD}	50	100	ns	D0P/N
Time-out before the Display Module (IL79400A-XX) starts driving	$T_{TA-SURED}$	T_{LPXD}	$2 \times T_{LPXD}$	ns	D0P/N

Table 115. Low Power State Period Timings – B

Description	Symbol	Min.	Typ.	Max.	Unit	Condition
Time to drive LP-00 by Display Module (IL79400A-XX)	$T_{TA-GETD}$	-	5xTLPXD	-	ns	D0P/N
Time to drive LP-00 after turnaround request - MCU	T_{TA-GOD}	-	4xTLPXD	-	ns	D0P/N

9.4.4.5 Data Lanes from Low Power Mode to High Speed Mode


Figure 145. Data Lanes - Low Power Mode to High Speed Mode Timings
Table 116. Data Lanes - Low Power Mode to High Speed Mode Timings

Parameter	Symbol	Min	Max	Unit	Condition
Length of any Low Power State Period	T_{LPX}	50	-	ns	D0P/N
Time to drive LP-00 to prepare for HS Transmission	$T_{HS-PREPARE}$	40+4xUI	85+6xUI	ns	D0P/N
Time to enable Data Lane Receiver line termination measured from when D0 crosses V_{ILMAX}	$T_{HS-TERM-EN}$	-	35+4xUI	ns	D0P/N

9.4.4.6 Data Lanes from High Speed Mode to Low Power Mode

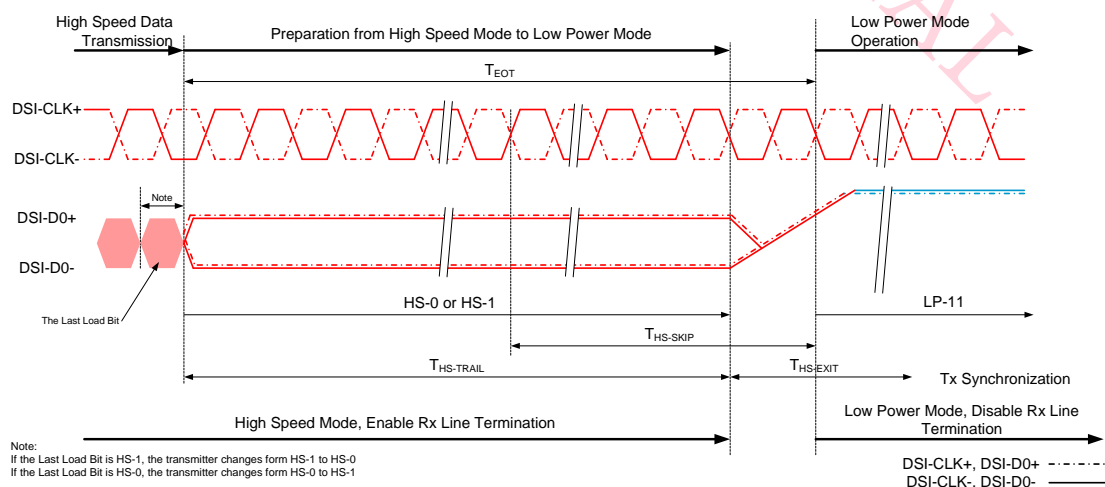

Figure 146. Data Lanes - High Speed Mode to Low Power Mode Timings

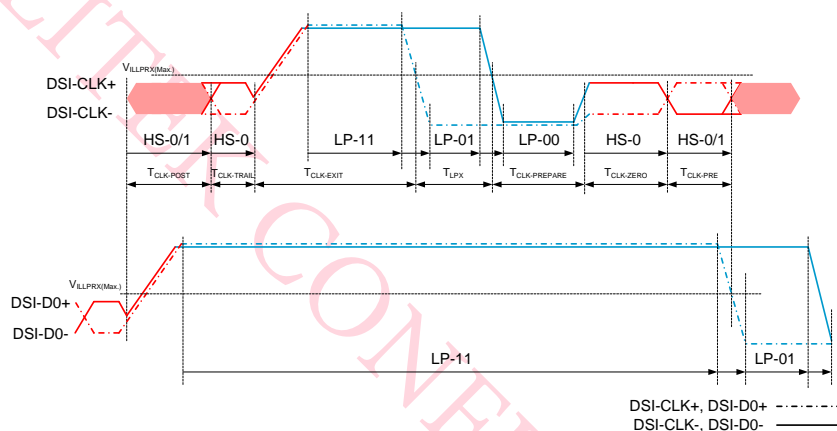
Table 117. Data Lanes - High Speed Mode to Low Power Mode Timings

Parameter	Symbol	Min	Max	Unit	Condition
Time-Out at Display Module (IL79400A-XX) to ignore transition period of EoT	$T_{HS-SKIP}$	40	$55+4 \times UI$	ns	D0P/N
Time to driver LP-11 after HS burst	$T_{HS-EXIT}$	100	-	ns	D0P/N
Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	$T_{HS-TRAIL}$	$\max(8 \times UI, 60ns+4 \times UI)^{Note}$	-	ns	D0P/N

Note:

Compare “8×UI” and “60ns+4×UI”, the larger one would be the min. value.

9.4.4.7 DSI Clock Burst – High Speed Mode to/from Low Power Mode


Figure 147. Clock Lanes - High Speed Mode to/from Low Power Mode Timings
Table 118. Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Parameter	Symbol	Min	Max	Unit	Condition
Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	$T_{CLK-POST}$	$60+52 \times UI$	-	ns	CLKP/N
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	ns	CLKP/N
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	ns	CLKP/N
Time to drive LP-00 to prepare for HS transmission	$T_{CLK-PREPARE}$	38	95	ns	CLKP/N
Time-out at Clock Lane to enable HS termination	$T_{CLK-TERM-EN}$	-	38	ns	CLKP/N
Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	300	-	ns	CLKP/N
Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	$8 \times UI$	-	ns	CLKP/N

9.4.4.8 Timing for DSI Video Mode

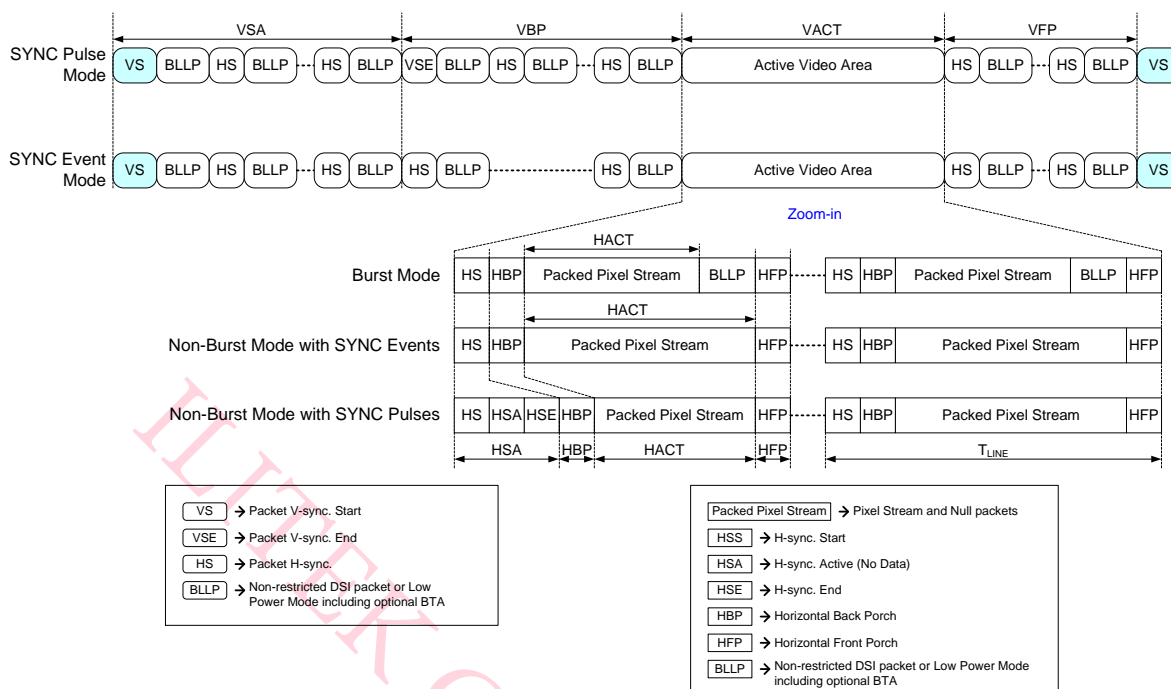


Figure 148. DSI Packet

Table 119. Timing for DSI Video Mode

Parameters	Symbol	Min.	Typ.	Max.	Units	Condition
Vertical sync. active	VSA	2	-	-	Line	Note 4,5
Vertical Back Porch	VBP	4	-	-	Line	Note 4,5
Vertical Front Porch	VFP	38	-	-	Line	Note 4,5,6
Active lines per frame	VACT	-	400	-	Line	
Horizontal sync. active	HSA	2	-	-	Pixel	
Horizontal Porch	HSA + HBP+ HFP	2	-	-	us	
Active pixels per line	HACT	-	400	-	Pixel	
Bit Rate	BR _{bps}	-	-	750	Mbps	

Note:

1. Pixel Format: Please reference to "4.4 DSI System Interface".
2. The formula exists slightly error because of the host-transmission way.
3. The best frame rate setting is 60Hz.
4. The minimum values of this table mean the limitation of IC without considering the panel GIP.
5. The actual values of VSA, VBP and VFP will be changed by different panel GIP setting.
6. Touch Controller operation time was considered.

1 UI = 1/Bit rate

HAS(pixel) = (HSA) / (UI × pixel format)

HBP(pixel) = (HBP) / (UI × pixel format)

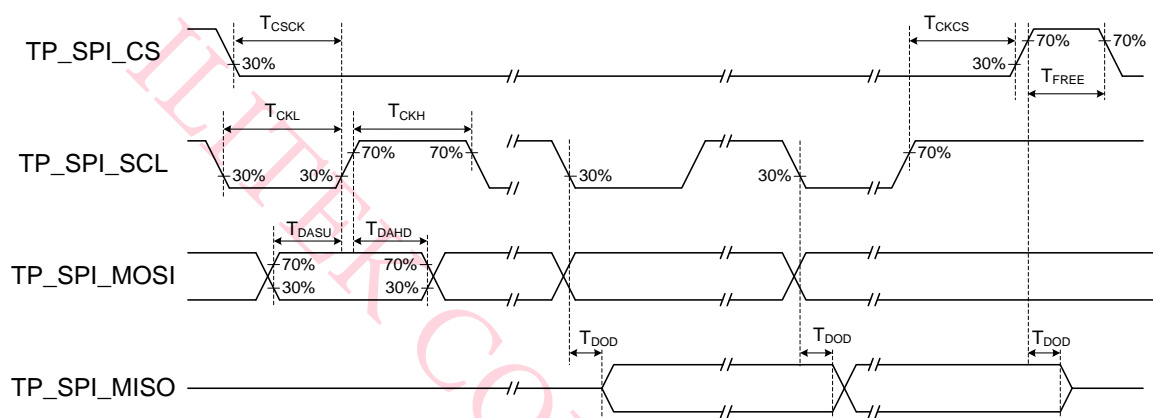
HFP(pixel) = (HFP) / (UI × pixel format)

$$\text{Frame Rate} = \frac{\text{BR}_{\text{bps}}}{(\text{VACT} + \text{VSA} + \text{VBP} + \text{VFP}) \times (\text{HACT} + \text{HAS} + \text{HBP} + \text{HFP}) \times \text{Pixel Format}}$$

9.4.5 TP SPI Interface

Table 120. TP SPI Interface AC Characteristic

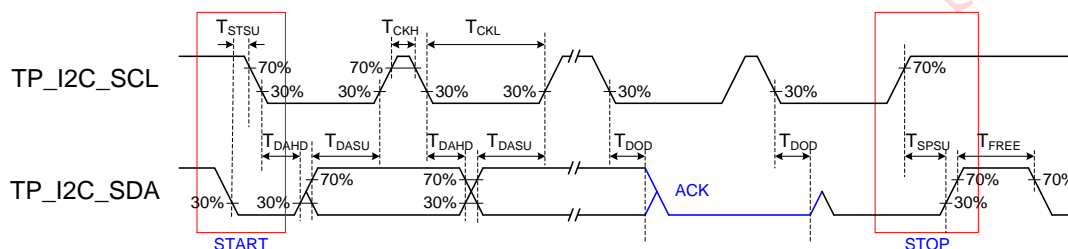
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Data Frequency	F_{SPI}	-	4	10	MHz	
SPI CS low to Clock high	T_{CSCK}	50	-	-	ns	
SPI Clock High to CS high	T_{CKCS}	50	-	-	ns	
SPI Clock Low	T_{CKL}	40	-	-	ns	
SPI Clock High	T_{CKH}	40	-	-	ns	
SPI Data hold time	T_{DAHD}	40	-	-	ns	
SPI Data setup time	T_{DASU}	40	-	-	ns	
SPI Data Output Delay time	T_{DOD}	25	-	-	ns	
SPI Bus free time	T_{FREE}	1	-	-	us	


Figure 149. TP SPI AC Timing Diagram

9.4.6 TP I2C Interface

Table 121. TP I2C Interface AC Characteristic

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Data Frequency	F_{I2C}	-	-	400	KHz	
I2C Clock Low	T_{CKL}	1.3	-	-	us	
I2C Clock High	T_{CKH}	0.6	-	-	us	
I2C Data Output Delay time	T_{DOD}	-	-	0.9	us	
I2C Data hold time	T_{DAHD}	0	-	-	us	
I2C Data setup time	T_{DASU}	0.1	-	-	us	
I2C START setup time	T_{STSU}	0.6	-	-	us	
I2C STOP setup time	T_{SPSU}	0.6	-	-	us	
I2C Bus free time	T_{FREE}	1.3	-	-	us	


Figure 150. TP I2C AC Timing Diagram

10 Pad Information

10.1 Bump Arrangement

Input Pad	<p>Diagram illustrating the layout of Input Pads. The pads are arranged in groups, with dimensions specified for each group. The groups shown are No.1, No.2, No.3, No.15, No.16, No.17, No.18, No.206, No.207, No.208, No.209, No.221, No.222, and No.223. Dimensions include 39um, 24um, 50um, and 75um.</p>															
Output Pad	<p>Diagram illustrating the layout of Output Pads. The pads are arranged in a grid, with dimensions specified for each group. The dimensions include 34um, 40um, 99um, 21um, 50um, and 44um.</p>															
Alignment Mark	<div><div><p>Left</p><p>12.5um, 25um, 25um, 25um, 12.5um</p></div><div><p>Right</p><p>12.5um, 25um, 25um, 25um, 12.5um</p></div></div> <table><tr><th>Index</th><th>X-Position</th><th>Y-Position</th><th>Width</th><th>Height</th></tr><tr><td>Alignment Mark Left</td><td>-5333.4</td><td>-253.4</td><td>100</td><td>100</td></tr><tr><td>Alignment Mark Right</td><td>5333.4</td><td>-253.4</td><td>100</td><td>100</td></tr></table>	Index	X-Position	Y-Position	Width	Height	Alignment Mark Left	-5333.4	-253.4	100	100	Alignment Mark Right	5333.4	-253.4	100	100
Index	X-Position	Y-Position	Width	Height												
Alignment Mark Left	-5333.4	-253.4	100	100												
Alignment Mark Right	5333.4	-253.4	100	100												
IC Dimension	<table><tr><th>Index</th><th>X (um)</th><th>Y (um)</th></tr><tr><td>Chip Size (with scribe line)</td><td>11000</td><td>998</td></tr></table>	Index	X (um)	Y (um)	Chip Size (with scribe line)	11000	998									
Index	X (um)	Y (um)														
Chip Size (with scribe line)	11000	998														

Unit: um.

10.2 Pad Coordination

No.	Pad Name	X-axis	Y-axis	Width	Height
1	GOUTL[1]	-4329	-417.5	24	50
2	GOUTL[2]	-4290	-417.5	24	50
3	GOUTL[3]	-4251	-417.5	24	50
4	GOUTL[4]	-4212	-417.5	24	50
5	GOUTL[5]	-4173	-417.5	24	50
6	GOUTL[6]	-4134	-417.5	24	50
7	GOUTL[7]	-4095	-417.5	24	50
8	GOUTL[8]	-4056	-417.5	24	50
9	GOUTL[9]	-4017	-417.5	24	50
10	GOUTL[10]	-3978	-417.5	24	50
11	GOUTL[11]	-3939	-417.5	24	50
12	GOUTL[12]	-3900	-417.5	24	50
13	GOUTL[13]	-3861	-417.5	24	50
14	GOUTL[14]	-3822	-417.5	24	50
15	GOUTL[15]	-3783	-417.5	24	50
16	GOUTL[16]	-3744	-417.5	24	50
17	VGLO	-3705	-405	24	75
18	VGLO	-3666	-405	24	75
19	DUMMY	-3627	-405	24	75
20	DUMMY	-3588	-405	24	75
21	DUMMY	-3549	-405	24	75
22	DUMMY	-3510	-405	24	75
23	IM[1]	-3471	-405	24	75
24	IM[0]	-3432	-405	24	75
25	D[7]	-3393	-405	24	75
26	D[6]	-3354	-405	24	75
27	D[5]	-3315	-405	24	75
28	D[4]	-3276	-405	24	75
29	D[3]	-3237	-405	24	75
30	D[2]	-3198	-405	24	75
31	TEST[2]	-3159	-405	24	75
32	TEST[1]	-3120	-405	24	75
33	TEST[0]	-3081	-405	24	75
34	EXTCLK	-3042	-405	24	75
35	TESTEN	-3003	-405	24	75
36	FRM	-2964	-405	24	75
37	PSWAP	-2925	-405	24	75
38	VSS	-2886	-405	24	75
39	VSS	-2847	-405	24	75
40	VDDI	-2808	-405	24	75
41	VDDI	-2769	-405	24	75
42	D[1]	-2730	-405	24	75
43	D[0]	-2691	-405	24	75
44	SDI_RD_X	-2652	-405	24	75
45	WRX_SCL	-2613	-405	24	75
46	DCX	-2574	-405	24	75
47	CSX	-2535	-405	24	75
48	LEDPWM	-2496	-405	24	75
49	TE	-2457	-405	24	75
50	RESX	-2418	-405	24	75
51	DUMMY	-2379	-405	24	75
52	DUMMY	-2340	-405	24	75
53	DUMMY	-2301	-405	24	75
54	DUMMY	-2262	-405	24	75
55	DUMMY	-2223	-405	24	75
56	DUMMY	-2184	-405	24	75
57	DUMMY	-2145	-405	24	75
58	DUMMY	-2106	-405	24	75
59	VG_HSSI	-2067	-405	24	75
60	HSSI_CLK_N	-2028	-405	24	75
61	HSSI_CLK_N	-1989	-405	24	75
62	HSSI_CLK_N	-1950	-405	24	75
63	HSSI_CLK_P	-1911	-405	24	75
64	HSSI_CLK_P	-1872	-405	24	75
65	HSSI_CLK_P	-1833	-405	24	75
66	VG_HSSI	-1794	-405	24	75
67	HSSI_D0_N	-1755	-405	24	75
68	HSSI_D0_N	-1716	-405	24	75
69	HSSI_D0_N	-1677	-405	24	75
70	HSSI_D0_P	-1638	-405	24	75
71	HSSI_D0_P	-1599	-405	24	75
72	HSSI_D0_P	-1560	-405	24	75
73	VG_HSSI	-1521	-405	24	75
74	VG_HSSI	-1482	-405	24	75
75	VG_HSSI	-1443	-405	24	75
76	VG_HSSI	-1404	-405	24	75
77	VG_HSSI	-1365	-405	24	75
78	VG_HSSI	-1326	-405	24	75
79	VG_HSSI	-1287	-405	24	75
80	VG_HSSI	-1248	-405	24	75
81	VSS	-1209	-405	24	75
82	VSS	-1170	-405	24	75
83	VSS	-1131	-405	24	75
84	VSS	-1092	-405	24	75
85	VDD_TP	-1053	-405	24	75
86	VDD_TP	-1014	-405	24	75
87	VDD_TP	-975	-405	24	75
88	VDD_TP	-936	-405	24	75
89	VDDI	-897	-405	24	75
90	VDDI	-858	-405	24	75

No.	Pad Name	X-axis	Y-axis	Width	Height
91	VDDI	-819	-405	24	75
92	TP_RESX	-780	-405	24	75
93	TP_INT	-741	-405	24	75
94	TP_I2C_SCL	-702	-405	24	75
95	TP_I2C_SDA	-663	-405	24	75
96	TP_FLASH_SCK	-624	-405	24	75
97	TP_FLASH_MOSI	-585	-405	24	75
98	TP_FLASH_MISO	-546	-405	24	75
99	TP_FLASH_CS	-507	-405	24	75
100	TP_SPI_SCLK	-468	-405	24	75
101	TP_SPI_MOSI	-429	-405	24	75
102	TP_SPI_MISO	-390	-405	24	75
103	TP_SPI_CS	-351	-405	24	75
104	TP_TMCS	-312	-405	24	75
105	TP_TCKC	-273	-405	24	75
106	TP_GPIO[0]	-234	-405	24	75
107	TP_GPIO[1]	-195	-405	24	75
108	TP_GPIO[2]	-156	-405	24	75
109	TP_GPIO[3]	-117	-405	24	75
110	TP_GPIO[4]	-78	-405	24	75
111	TP_GPIO[5]	-39	-405	24	75
112	TP_GPIO[6]	0	-405	24	75
113	TP_GPIO[7]	39	-405	24	75
114	TP_UART_TX	78	-405	24	75
115	TP_EXTCLK	117	-405	24	75
116	TP_TEST_EN	156	-405	24	75
117	GVDDN	195	-405	24	75
118	VCL	234	-405	24	75
119	VCL	273	-405	24	75
120	VCL	312	-405	24	75
121	AVEE	351	-405	24	75
122	AVEE	390	-405	24	75
123	AVEE	429	-405	24	75
124	AVEE	468	-405	24	75
125	AVSS	507	-405	24	75
126	AVSS	546	-405	24	75
127	AVSS	585	-405	24	75
128	AVSS	624	-405	24	75
129	AVSS	663	-405	24	75
130	AVSS	702	-405	24	75
131	AVSS	741	-405	24	75
132	AVSS	780	-405	24	75
133	AVSS	819	-405	24	75
134	C22N	858	-405	24	75
135	C22N	897	-405	24	75
136	C22N	936	-405	24	75
137	C22N	975	-405	24	75
138	C22P	1014	-405	24	75
139	C22P	1053	-405	24	75
140	C22P	1092	-405	24	75
141	C22P	1131	-405	24	75
142	C21N	1170	-405	24	75
143	C21N	1209	-405	24	75
144	C21N	1248	-405	24	75
145	C21N	1287	-405	24	75
146	C21P	1326	-405	24	75
147	C21P	1365	-405	24	75
148	C21P	1404	-405	24	75
149	C21P	1443	-405	24	75
150	VCI	1482	-405	24	75
151	VCI	1521	-405	24	75
152	VCI	1560	-405	24	75
153	VCI	1599	-405	24	75
154	VCI	1638	-405	24	75
155	VCI	1677	-405	24	75
156	VCI	1716	-405	24	75
157	VCI	1755	-405	24	75
158	VCI	1794	-405	24	75
159	C11P	1833	-405	24	75
160	C11P	1872	-405	24	75
161	C11P	1911	-405	24	75
162	C11N	1950	-405	24	75
163	C11N	1989	-405	24	75
164	C11N	2028	-405	24	75
165	C12N	2067	-405	24	75
166	C12N	2106	-405	24	75
167	C12N	2145	-405	24	75
168	C12P	2184	-405	24	75
169	C12P	2223	-405	24	75
170	C12P	2262	-405	24	75
171	AVDD	2301	-405	24	75
172	AVDD	2340	-405	24	75
173	AVDD	2379	-405	24	75
174	AVDD	2418	-405	24	75
175	GVDDP	2457	-405	24	75
176	TAVDD	2496	-405	24	75
177	TAVDD	2535	-405	24	75
178	TAVDD	2574	-405	24	75
179	TAVDD	2613	-405	24	75
180	AVSS	2652	-405	24	75

No.	Pad Name	X-axis	Y-axis	Width	Height
181	AVSS	2691	-405	24	75
182	AVSS	2730	-405	24	75
183	AVSS	2769	-405	24	75
184	AVSS	2808	-405	24	75
185	AVSS_BG	2847	-405	24	75
186	TAVSS	2886	-405	24	75
187	TAVSS	2925	-405	24	75
188	TAVSS	2964	-405	24	75
189	TAVSS	3003	-405	24	75
190	VMOD_GATE	3042	-405	24	75
191	VMOD_GATE	3081	-405	24	75
192	VCOM	3120	-405	24	75
193	VCOM	3159	-405	24	75
194	VCOM_OPT	3198	-405	24	75
195	VCOM_PASS	3237	-405	24	75
196	RX_OD[4]	3276	-405	24	75
197	RX_OD[3]	3315	-405	24	75
198	RX_OD[2]	3354	-405	24	75
199	RX_OD[1]	3393	-405	24	75
200	C31N	3432	-405	24	75
201	C31P	3471	-405	24	75
202	VGL	3510	-405	24	75
203	VGL	3549	-405	24	75
204	VGH	3588	-405	24	75
205	VGH	3627	-405	24	75
206	VGLO	3666	-405	24	75
207	VGLO	3705	-405	24	75
208	GOUTR[16]	3744	-417.5	24	50
209	GOUTR[15]	3783	-417.5	24	50
210	GOUTR[14]	3822	-417.5	24	50
211	GOUTR[13]	3861	-417.5	24	50
212	GOUTR[12]	3900	-417.5	24	50
213	GOUTR[11]	3939	-417.5	24	50
214	GOUTR[10]	3978	-417.5	24	50
215	GOUTR[9]	4017	-417.5	24	50
216	GOUTR[8]	4056	-417.5	24	50
217	GOUTR[7]	4095	-417.5	24	50
218	GOUTR[6]	4134	-417.5	24	50
219	GOUTR[5]	4173	-417.5	24	50
220	GOUTR[4]	4212	-417.5	24	50
221	GOUTR[3]	4251	-417.5	24	50
222	GOUTR[2]	4290	-417.5	24	50
223	GOUTR[1]	4329	-417.5	24	50
224	VCOM_PASS	5318.5	-77.2	21	50
225	VCOM_PASS	5307.5	-7.2	21	50
226	VCOM_PASS	5296.5	65.8	21	50
227	VCOM_PASS	5285.5	132.8	21	50
228	DUMMY	5274.5	-74.3	21	50
229	DUMMY	5263.5	-4.3	21	50
230	S[0]	5252.5	68.7	21	50
231	GRID	5241.5	135.7	21	50
232	S[1]	5230.5	-71.4	21	50
233	S[2]	5219.5	-1.4	21	50
234	S[3]	5208.5	71.6	21	50
235	SX[1]	5197.5	138.6	21	50
236	S[4]	5186.5	-68.5	21	50
237	S[5]	5175.5	1.5	21	50
238	S[6]	5164.5	74.5	21	50
239	DUMMY	5153.5	141.5	21	50
240	S[7]	5142.5	-65.6	21	50
241	S[8]	5131.5	4.4	21	50
242	S[9]	5120.5	77.4	21	50
243	DUMMY	5109.5	144.4	21	50
244	S[10]	5098.5	-62.7	21	50
245	S[11]	5087.5	7.3	21	50
246	S[12]	5076.5	80.3	21	50
247	SX[2]	5065.5	147.3	21	50
248	S[13]	5054.5	-59.8	21	50
249	S[14]	5043.5	10.2	21	50
250	S[15]	5032.5	83.2	21	50
251	DUMMY	5021.5	150.2	21	50
252	S[16]	5010.5	-56.9	21	50
253	S[17]	4999.5	13.1	21	50
254	S[18]	4988.5	86.1	21	50
255	DUMMY	4977.5	153.1	21	50
256	S[19]	4966.5	-54	21	50
257	S[20]	4955.5	16	21	50
258	S[21]	4944.5	89	21	50
259	SX[3]	4933.5	156	21	50
260	S[22]	4922.5	-51.1	21	50
261	S[23]	4911.5	18.9	21	50
262	S[24]	4900.5	91.9	21	50
263	DUMMY	4889.5	158.9	21	50
264	S[25]	4878.5	-48.2	21	50
265	S[26]	4867.5	21.8	21	50
266	S[27]	4856.5	94.8	21	50
267	DUMMY	4845.5	161.8	21	50
268	S[28]	4834.5	-45.3	21	50
269	S[29]	4823.5	24.7	21	50
270	S[30]	4812.5	97.7	21	50
271	SX[4]	4801.5	164.7	21	50
272	S[31]	4790.5	-42.4	21	50

No.	Pad Name	X-axis	Y-axis	Width	Height
273	S[32]	4779.5	27.6	21	50
274	S[33]	4768.5	100.6	21	50
275	DUMMY	4757.5	167.6	21	50
276	S[34]	4746.5	-39.5	21	50
277	S[35]	4735.5	30.5	21	50
278	S[36]	4724.5	103.5	21	50
279	DUMMY	4713.5	170.5	21	50
280	S[37]	4702.5	-36.6	21	50
281	S[38]	4691.5	33.4	21	50
282	S[39]	4680.5	106.4	21	50
283	SX[5]	4669.5	173.4	21	50
284	S[40]	4658.5	-33.7	21	50
285	S[41]	4647.5	36.3	21	50
286	S[42]	4636.5	109.3	21	50
287	DUMMY	4625.5	176.3	21	50
288	S[43]	4614.5	-30.8	21	50
289	S[44]	4603.5	39.2	21	50
290	S[45]	4592.5	112.2	21	50
291	DUMMY	4581.5	179.2	21	50
292	S[46]	4570.5	-27.9	21	50
293	S[47]	4559.5	42.1	21	50
294	S[48]	4548.5	115.1	21	50
295	SX[6]	4537.5	182.1	21	50
296	S[49]	4526.5	-25	21	50
297	S[50]	4515.5	45	21	50
298	S[51]	4504.5	118	21	50
299	DUMMY	4493.5	185	21	50
300	S[52]	4482.5	-22.1	21	50
301	S[53]	4471.5	47.9	21	50
302	S[54]	4460.5	120.9	21	50
303	DUMMY	4449.5	187.9	21	50
304	S[55]	4438.5	-19.2	21	50
305	S[56]	4427.5	50.8	21	50
306	S[57]	4416.5	123.8	21	50
307	SX[7]	4405.5	190.8	21	50
308	S[58]	4394.5	-16.3	21	50
309	S[59]	4383.5	53.7	21	50
310	S[60]	4372.5	126.7	21	50
311	DUMMY	4361.5	193.7	21	50
312	S[61]	4350.5	-13.4	21	50
313	S[62]	4339.5	56.6	21	50
314	S[63]	4328.5	129.6	21	50
315	DUMMY	4317.5	196.6	21	50
316	S[64]	4306.5	-10.5	21	50
317	S[65]	4295.5	59.5	21	50
318	S[66]	4284.5	132.5	21	50
319	SX[8]	4273.5	199.5	21	50
320	S[67]	4262.5	-7.6	21	50
321	S[68]	4251.5	62.4	21	50
322	S[69]	4240.5	135.4	21	50
323	DUMMY	4229.5	202.4	21	50
324	S[70]	4218.5	-4.7	21	50
325	S[71]	4207.5	65.3	21	50
326	S[72]	4196.5	138.3	21	50
327	DUMMY	4185.5	205.3	21	50
328	S[73]	4174.5	-1.8	21	50
329	S[74]	4163.5	68.2	21	50
330	S[75]	4152.5	141.2	21	50
331	SX[9]	4141.5	208.2	21	50
332	S[76]	4130.5	1.1	21	50
333	S[77]	4119.5	71.1	21	50
334	S[78]	4108.5	144.1	21	50
335	DUMMY	4097.5	211.1	21	50
336	S[79]	4086.5	4	21	50
337	S[80]	4075.5	74	21	50
338	S[81]	4064.5	147	21	50
339	DUMMY	4053.5	214	21	50
340	S[82]	4042.5	6.9	21	50
341	S[83]	4031.5	76.9	21	50
342	S[84]	4020.5	149.9	21	50
343	SX[10]	4009.5	216.9	21	50
344	S[85]	3998.5	9.8	21	50
345	S[86]	3987.5	79.8	21	50
346	S[87]	3976.5	152.8	21	50
347	DUMMY	3965.5	219.8	21	50
348	S[88]	3954.5	12.7	21	50
349	S[89]	3943.5	82.7	21	50
350	S[90]	3932.5	155.7	21	50
351	DUMMY	3921.5	222.7	21	50
352	S[91]	3910.5	15.6	21	50
353	S[92]	3899.5	85.6	21	50
354	S[93]	3888.5	158.6	21	50
355	SX[11]	3877.5	225.6	21	50
356	S[94]	3866.5	18.5	21	50
357	S[95]	3855.5	88.5	21	50
358	S[96]	3844.5	161.5	21	50
359	DUMMY	3833.5	228.5	21	50
360	S[97]	3822.5	21.4	21	50
361	S[98]	3811.5	91.4	21	50
362	S[99]	3800.5	164.4	21	50
363	DUMMY	3789.5	231.4	21	50
364	S[100]	3778.5	24.3	21	50

No.	Pad Name	X-axis	Y-axis	Width	Height
365	S[101]	3767.5	94.3	21	50
366	S[102]	3756.5	167.3	21	50
367	SX[12]	3745.5	234.3	21	50
368	S[103]	3734.5	27.2	21	50
369	S[104]	3723.5	97.2	21	50
370	S[105]	3712.5	170.2	21	50
371	DUMMY	3701.5	237.2	21	50
372	S[106]	3690.5	30.1	21	50
373	S[107]	3679.5	100.1	21	50
374	S[108]	3668.5	173.1	21	50
375	DUMMY	3657.5	240.1	21	50
376	S[109]	3646.5	33	21	50
377	S[110]	3635.5	103	21	50
378	S[111]	3624.5	176	21	50
379	SX[13]	3613.5	243	21	50
380	S[112]	3602.5	35.9	21	50
381	S[113]	3591.5	105.9	21	50
382	S[114]	3580.5	178.9	21	50
383	DUMMY	3569.5	245.9	21	50
384	S[115]	3558.5	38.8	21	50
385	S[116]	3547.5	108.8	21	50
386	S[117]	3536.5	181.8	21	50
387	DUMMY	3525.5	248.8	21	50
388	S[118]	3514.5	41.7	21	50
389	S[119]	3503.5	111.7	21	50
390	S[120]	3492.5	184.7	21	50
391	SX[14]	3481.5	251.7	21	50
392	S[121]	3470.5	44.6	21	50
393	S[122]	3459.5	114.6	21	50
394	S[123]	3448.5	187.6	21	50
395	DUMMY	3437.5	254.6	21	50
396	S[124]	3426.5	47.5	21	50
397	S[125]	3415.5	117.5	21	50
398	S[126]	3404.5	190.5	21	50
399	DUMMY	3393.5	257.5	21	50
400	S[127]	3382.5	50.4	21	50
401	S[128]	3371.5	120.4	21	50
402	S[129]	3360.5	193.4	21	50
403	SX[15]	3349.5	260.4	21	50
404	S[130]	3338.5	53.3	21	50
405	S[131]	3327.5	123.3	21	50
406	S[132]	3316.5	196.3	21	50
407	DUMMY	3305.5	263.3	21	50
408	S[133]	3294.5	56.2	21	50
409	S[134]	3283.5	126.2	21	50
410	S[135]	3272.5	199.2	21	50
411	DUMMY	3261.5	266.2	21	50
412	S[136]	3250.5	59.1	21	50
413	S[137]	3239.5	129.1	21	50
414	S[138]	3228.5	202.1	21	50
415	SX[16]	3217.5	269.1	21	50
416	S[139]	3206.5	62	21	50
417	S[140]	3195.5	132	21	50
418	S[141]	3184.5	205	21	50
419	DUMMY	3173.5	272	21	50
420	S[142]	3162.5	64.9	21	50
421	S[143]	3151.5	134.9	21	50
422	S[144]	3140.5	207.9	21	50
423	DUMMY	3129.5	274.9	21	50
424	S[145]	3118.5	67.8	21	50
425	S[146]	3107.5	137.8	21	50
426	S[147]	3096.5	210.8	21	50
427	SX[17]	3085.5	277.8	21	50
428	S[148]	3074.5	70.7	21	50
429	S[149]	3063.5	140.7	21	50
430	S[150]	3052.5	213.7	21	50
431	DUMMY	3041.5	280.7	21	50
432	S[151]	3030.5	73.6	21	50
433	S[152]	3019.5	143.6	21	50
434	S[153]	3008.5	216.6	21	50
435	DUMMY	2997.5	283.6	21	50
436	S[154]	2986.5	76.5	21	50
437	S[155]	2975.5	146.5	21	50
438	S[156]	2964.5	219.5	21	50
439	SX[18]	2953.5	286.5	21	50
440	S[157]	2942.5	79.4	21	50
441	S[158]	2931.5	149.4	21	50
442	S[159]	2920.5	222.4	21	50
443	DUMMY	2909.5	289.4	21	50
444	S[160]	2898.5	82.3	21	50
445	S[161]	2887.5	152.3	21	50
446	S[162]	2876.5	225.3	21	50
447	DUMMY	2865.5	292.3	21	50
448	S[163]	2854.5	85.2	21	50
449	S[164]	2843.5	155.2	21	50
450	S[165]	2832.5	228.2	21	50
451	SX[19]	2821.5	295.2	21	50
452	S[166]	2810.5	88.1	21	50
453	S[167]	2799.5	158.1	21	50
454	S[168]	2788.5	231.1	21	50
455	DUMMY	2777.5	298.1	21	50
456	S[169]	2766.5	91	21	50

No.	Pad Name	X-axis	Y-axis	Width	Height
457	S[170]	2755.5	161	21	50
458	S[171]	2744.5	234	21	50
459	DUMMY	2733.5	301	21	50
460	S[172]	2722.5	93.9	21	50
461	S[173]	2711.5	163.9	21	50
462	S[174]	2700.5	236.9	21	50
463	SX[20]	2689.5	303.9	21	50
464	S[175]	2678.5	96.8	21	50
465	S[176]	2667.5	166.8	21	50
466	S[177]	2656.5	239.8	21	50
467	DUMMY	2645.5	306.8	21	50
468	S[178]	2634.5	99.7	21	50
469	S[179]	2623.5	169.7	21	50
470	S[180]	2612.5	242.7	21	50
471	DUMMY	2601.5	309.7	21	50
472	S[181]	2590.5	102.6	21	50
473	S[182]	2579.5	172.6	21	50
474	S[183]	2568.5	245.6	21	50
475	SX[21]	2557.5	312.6	21	50
476	S[184]	2546.5	105.5	21	50
477	S[185]	2535.5	175.5	21	50
478	S[186]	2524.5	248.5	21	50
479	DUMMY	2513.5	315.5	21	50
480	S[187]	2502.5	108.4	21	50
481	S[188]	2491.5	178.4	21	50
482	S[189]	2480.5	251.4	21	50
483	DUMMY	2469.5	318.4	21	50
484	S[190]	2458.5	111.3	21	50
485	S[191]	2447.5	181.3	21	50
486	S[192]	2436.5	254.3	21	50
487	SX[22]	2425.5	321.3	21	50
488	S[193]	2414.5	114.2	21	50
489	S[194]	2403.5	184.2	21	50
490	S[195]	2392.5	257.2	21	50
491	DUMMY	2381.5	324.2	21	50
492	S[196]	2370.5	117.1	21	50
493	S[197]	2359.5	187.1	21	50
494	S[198]	2348.5	260.1	21	50
495	DUMMY	2337.5	327.1	21	50
496	S[199]	2326.5	120	21	50
497	S[200]	2315.5	190	21	50
498	S[201]	2304.5	263	21	50
499	SX[23]	2293.5	330	21	50
500	S[202]	2282.5	122.9	21	50
501	S[203]	2271.5	192.9	21	50
502	S[204]	2260.5	265.9	21	50
503	DUMMY	2249.5	332.9	21	50
504	S[205]	2238.5	125.8	21	50
505	S[206]	2227.5	195.8	21	50
506	S[207]	2216.5	268.8	21	50
507	DUMMY	2205.5	335.8	21	50
508	S[208]	2194.5	128.7	21	50
509	S[209]	2183.5	198.7	21	50
510	S[210]	2172.5	271.7	21	50
511	SX[24]	2161.5	338.7	21	50
512	S[211]	2150.5	131.6	21	50
513	S[212]	2139.5	201.6	21	50
514	S[213]	2128.5	274.6	21	50
515	DUMMY	2117.5	341.6	21	50
516	S[214]	2106.5	134.5	21	50
517	S[215]	2095.5	204.5	21	50
518	S[216]	2084.5	277.5	21	50
519	DUMMY	2073.5	344.5	21	50
520	S[217]	2062.5	137.4	21	50
521	S[218]	2051.5	207.4	21	50
522	S[219]	2040.5	280.4	21	50
523	SX[25]	2029.5	347.4	21	50
524	S[220]	2018.5	140.3	21	50
525	S[221]	2007.5	210.3	21	50
526	S[222]	1996.5	283.3	21	50
527	DUMMY	1985.5	350.3	21	50
528	S[223]	1974.5	143.2	21	50
529	S[224]	1963.5	213.2	21	50
530	S[225]	1952.5	286.2	21	50
531	DUMMY	1941.5	353.2	21	50
532	S[226]	1930.5	146.1	21	50
533	S[227]	1919.5	216.1	21	50
534	S[228]	1908.5	289.1	21	50
535	SX[26]	1897.5	356.1	21	50
536	S[229]	1886.5	149	21	50
537	S[230]	1875.5	219	21	50
538	S[231]	1864.5	292	21	50
539	DUMMY	1853.5	359	21	50
540	S[232]	1842.5	151.9	21	50
541	S[233]	1831.5	221.9	21	50
542	S[234]	1820.5	294.9	21	50
543	DUMMY	1809.5	361.9	21	50
544	S[235]	1798.5	154.8	21	50
545	S[236]	1787.5	224.8	21	50
546	S[237]	1776.5	297.8	21	50
547	SX[27]	1765.5	364.8	21	50
548	S[238]	1754.5	157.7	21	50

No.	Pad Name	X-axis	Y-axis	Width	Height
549	S[239]	1743.5	227.7	21	50
550	S[240]	1732.5	300.7	21	50
551	DUMMY	1721.5	367.7	21	50
552	S[241]	1710.5	160.6	21	50
553	S[242]	1699.5	230.6	21	50
554	S[243]	1688.5	303.6	21	50
555	DUMMY	1677.5	370.6	21	50
556	S[244]	1666.5	163.5	21	50
557	S[245]	1655.5	233.5	21	50
558	S[246]	1644.5	306.5	21	50
559	SX[28]	1633.5	373.5	21	50
560	S[247]	1622.5	166.4	21	50
561	S[248]	1611.5	236.4	21	50
562	S[249]	1600.5	309.4	21	50
563	DUMMY	1589.5	376.4	21	50
564	S[250]	1578.5	169.3	21	50
565	S[251]	1567.5	239.3	21	50
566	S[252]	1556.5	312.3	21	50
567	DUMMY	1545.5	379.3	21	50
568	S[253]	1534.5	172.2	21	50
569	S[254]	1523.5	242.2	21	50
570	S[255]	1512.5	315.2	21	50
571	SX[29]	1501.5	382.2	21	50
572	S[256]	1490.5	175.1	21	50
573	S[257]	1479.5	245.1	21	50
574	S[258]	1468.5	318.1	21	50
575	DUMMY	1457.5	385.1	21	50
576	S[259]	1446.5	178	21	50
577	S[260]	1435.5	248	21	50
578	S[261]	1424.5	321	21	50
579	DUMMY	1413.5	388	21	50
580	S[262]	1402.5	180.9	21	50
581	S[263]	1391.5	250.9	21	50
582	S[264]	1380.5	323.9	21	50
583	SX[30]	1369.5	390.9	21	50
584	S[265]	1358.5	183.8	21	50
585	S[266]	1347.5	253.8	21	50
586	S[267]	1336.5	326.8	21	50
587	DUMMY	1325.5	393.8	21	50
588	S[268]	1314.5	186.7	21	50
589	S[269]	1303.5	256.7	21	50
590	S[270]	1292.5	329.7	21	50
591	DUMMY	1281.5	396.7	21	50
592	S[271]	1270.5	189.6	21	50
593	S[272]	1259.5	259.6	21	50
594	S[273]	1248.5	332.6	21	50
595	SX[31]	1237.5	399.6	21	50
596	S[274]	1226.5	192.5	21	50
597	S[275]	1215.5	262.5	21	50
598	S[276]	1204.5	335.5	21	50
599	DUMMY	1193.5	402.5	21	50
600	S[277]	1182.5	195.4	21	50
601	S[278]	1171.5	265.4	21	50
602	S[279]	1160.5	338.4	21	50
603	DUMMY	1149.5	405.4	21	50
604	S[280]	1138.5	198.3	21	50
605	S[281]	1127.5	268.3	21	50
606	S[282]	1116.5	341.3	21	50
607	SX[32]	1105.5	408.3	21	50
608	S[283]	1094.5	201.2	21	50
609	S[284]	1083.5	271.2	21	50
610	S[285]	1072.5	344.2	21	50
611	DUMMY	1061.5	411.2	21	50
612	S[286]	1050.5	204.1	21	50
613	S[287]	1039.5	274.1	21	50
614	S[288]	1028.5	347.1	21	50
615	DUMMY	1017.5	414.1	21	50
616	S[289]	1006.5	207	21	50
617	S[290]	995.5	277	21	50
618	S[291]	984.5	350	21	50
619	DUMMY	973.5	417	21	50
620	S[292]	962.5	207	21	50
621	S[293]	951.5	277	21	50
622	S[294]	940.5	350	21	50
623	DUMMY	929.5	417	21	50
624	S[295]	918.5	207	21	50
625	S[296]	907.5	277	21	50
626	S[297]	896.5	350	21	50
627	DUMMY	885.5	417	21	50
628	S[298]	874.5	207	21	50
629	S[299]	863.5	277	21	50
630	S[300]	852.5	350	21	50
631	GRID	841.5	417	21	50
632	DUMMY	830.5	207	21	50
633	DUMMY	819.5	277	21	50
634	DUMMY	808.5	350	21	50
635	DUMMY	797.5	417	21	50
636	DUMMY	786.5	207	21	50
637	DUMMY	775.5	277	21	50
638	DUMMY	764.5	350	21	50
639	DUMMY	753.5	417	21	50
640	DUMMY	742.5	207	21	50

No.	Pad Name	X-axis	Y-axis	Width	Height
641	DUMMY	731.5	277	21	50
642	DUMMY	720.5	350	21	50
643	DUMMY	709.5	417	21	50
644	DUMMY	698.5	207	21	50
645	DUMMY	687.5	277	21	50
646	DUMMY	676.5	350	21	50
647	DUMMY	665.5	417	21	50
648	DUMMY	654.5	207	21	50
649	DUMMY	643.5	277	21	50
650	DUMMY	632.5	350	21	50
651	DUMMY	621.5	417	21	50
652	DUMMY	610.5	207	21	50
653	DUMMY	599.5	277	21	50
654	DUMMY	588.5	350	21	50
655	DUMMY	577.5	417	21	50
656	DUMMY	566.5	207	21	50
657	DUMMY	555.5	277	21	50
658	DUMMY	544.5	350	21	50
659	DUMMY	533.5	417	21	50
660	DUMMY	522.5	207	21	50
661	DUMMY	511.5	277	21	50
662	DUMMY	500.5	350	21	50
663	DUMMY	489.5	417	21	50
664	DUMMY	478.5	207	21	50
665	DUMMY	467.5	277	21	50
666	DUMMY	456.5	350	21	50
667	DUMMY	445.5	417	21	50
668	DUMMY	434.5	207	21	50
669	DUMMY	423.5	277	21	50
670	DUMMY	412.5	350	21	50
671	DUMMY	401.5	417	21	50
672	DUMMY	390.5	207	21	50
673	DUMMY	379.5	277	21	50
674	DUMMY	368.5	350	21	50
675	DUMMY	357.5	417	21	50
676	DUMMY	346.5	207	21	50
677	DUMMY	335.5	277	21	50
678	DUMMY	324.5	350	21	50
679	DUMMY	313.5	417	21	50
680	DUMMY	302.5	207	21	50
681	DUMMY	291.5	277	21	50
682	DUMMY	280.5	350	21	50
683	DUMMY	269.5	417	21	50
684	DUMMY	258.5	207	21	50
685	DUMMY	247.5	277	21	50
686	DUMMY	236.5	350	21	50
687	DUMMY	225.5	417	21	50
688	DUMMY	214.5	207	21	50
689	DUMMY	203.5	277	21	50
690	DUMMY	192.5	350	21	50
691	DUMMY	181.5	417	21	50
692	DUMMY	170.5	207	21	50
693	DUMMY	159.5	277	21	50
694	DUMMY	148.5	350	21	50
695	DUMMY	137.5	417	21	50
696	DUMMY	126.5	207	21	50
697	DUMMY	115.5	277	21	50
698	DUMMY	104.5	350	21	50
699	DUMMY	93.5	417	21	50
700	DUMMY	82.5	207	21	50
701	DUMMY	71.5	277	21	50
702	DUMMY	60.5	350	21	50
703	DUMMY	49.5	417	21	50
704	DUMMY	38.5	207	21	50
705	DUMMY	27.5	277	21	50
706	DUMMY	16.5	350	21	50
707	DUMMY	5.5	417	21	50
708	DUMMY	-5.5	207	21	50
709	DUMMY	-16.5	277	21	50
710	DUMMY	-27.5	350	21	50
711	DUMMY	-38.5	417	21	50
712	DUMMY	-49.5	207	21	50
713	DUMMY	-60.5	277	21	50
714	DUMMY	-71.5	350	21	50
715	DUMMY	-82.5	417	21	50
716	DUMMY	-93.5	207	21	50
717	DUMMY	-104.5	277	21	50
718	DUMMY	-115.5	350	21	50
719	DUMMY	-126.5	417	21	50
720	DUMMY	-137.5	207	21	50
721	DUMMY	-148.5	277	21	50
722	DUMMY	-159.5	350	21	50
723	DUMMY	-170.5	417	21	50
724	DUMMY	-181.5	207	21	50
725	DUMMY	-192.5	277	21	50
726	DUMMY	-203.5	350	21	50
727	DUMMY	-214.5	417	21	50
728	DUMMY	-225.5	207	21	50
729	DUMMY	-236.5	277	21	50
730	DUMMY	-247.5	350	21	50
731	DUMMY	-258.5	417	21	50
732	DUMMY	-269.5	207	21	50

No.	Pad Name	X-axis	Y-axis	Width	Height
733	DUMMY	-280.5	277	21	50
734	DUMMY	-291.5	350	21	50
735	DUMMY	-302.5	417	21	50
736	DUMMY	-313.5	207	21	50
737	DUMMY	-324.5	277	21	50
738	DUMMY	-335.5	350	21	50
739	DUMMY	-346.5	417	21	50
740	DUMMY	-357.5	207	21	50
741	DUMMY	-368.5	277	21	50
742	DUMMY	-379.5	350	21	50
743	DUMMY	-390.5	417	21	50
744	DUMMY	-401.5	207	21	50
745	DUMMY	-412.5	277	21	50
746	DUMMY	-423.5	350	21	50
747	DUMMY	-434.5	417	21	50
748	DUMMY	-445.5	207	21	50
749	DUMMY	-456.5	277	21	50
750	DUMMY	-467.5	350	21	50
751	DUMMY	-478.5	417	21	50
752	DUMMY	-489.5	207	21	50
753	DUMMY	-500.5	277	21	50
754	DUMMY	-511.5	350	21	50
755	DUMMY	-522.5	417	21	50
756	DUMMY	-533.5	207	21	50
757	DUMMY	-544.5	277	21	50
758	DUMMY	-555.5	350	21	50
759	DUMMY	-566.5	417	21	50
760	DUMMY	-577.5	207	21	50
761	DUMMY	-588.5	277	21	50
762	DUMMY	-599.5	350	21	50
763	DUMMY	-610.5	417	21	50
764	DUMMY	-621.5	207	21	50
765	DUMMY	-632.5	277	21	50
766	DUMMY	-643.5	350	21	50
767	DUMMY	-654.5	417	21	50
768	DUMMY	-665.5	207	21	50
769	DUMMY	-676.5	277	21	50
770	DUMMY	-687.5	350	21	50
771	DUMMY	-698.5	417	21	50
772	DUMMY	-709.5	207	21	50
773	DUMMY	-720.5	277	21	50
774	DUMMY	-731.5	350	21	50
775	DUMMY	-742.5	417	21	50
776	DUMMY	-753.5	207	21	50
777	DUMMY	-764.5	277	21	50
778	DUMMY	-775.5	350	21	50
779	DUMMY	-786.5	417	21	50
780	DUMMY	-797.5	207	21	50
781	DUMMY	-808.5	277	21	50
782	DUMMY	-819.5	350	21	50
783	GRID	-830.5	417	21	50
784	S[301]	-841.5	207	21	50
785	S[302]	-852.5	277	21	50
786	S[303]	-863.5	350	21	50
787	DUMMY	-874.5	417	21	50
788	S[304]	-885.5	207	21	50
789	S[305]	-896.5	277	21	50
790	S[306]	-907.5	350	21	50
791	DUMMY	-918.5	417	21	50
792	S[307]	-929.5	207	21	50
793	S[308]	-940.5	277	21	50
794	S[309]	-951.5	350	21	50
795	DUMMY	-962.5	417	21	50
796	S[310]	-973.5	207	21	50
797	S[311]	-984.5	277	21	50
798	S[312]	-995.5	350	21	50
799	DUMMY	-1006.5	417	21	50
800	S[313]	-1017.5	204.1	21	50
801	S[314]	-1028.5	274.1	21	50
802	S[315]	-1039.5	347.1	21	50
803	DUMMY	-1050.5	414.1	21	50
804	S[316]	-1061.5	201.2	21	50
805	S[317]	-1072.5	271.2	21	50
806	S[318]	-1083.5	344.2	21	50
807	DUMMY	-1094.5	411.2	21	50
808	S[319]	-1105.5	198.3	21	50
809	S[320]	-1116.5	268.3	21	50
810	S[321]	-1127.5	341.3	21	50
811	SX[33]	-1138.5	408.3	21	50
812	S[322]	-1149.5	195.4	21	50
813	S[323]	-1160.5	265.4	21	50
814	S[324]	-1171.5	338.4	21	50
815	DUMMY	-1182.5	405.4	21	50
816	S[325]	-1193.5	192.5	21	50
817	S[326]	-1204.5	262.5	21	50
818	S[327]	-1215.5	335.5	21	50
819	DUMMY	-1226.5	402.5	21	50
820	S[328]	-1237.5	189.6	21	50
821	S[329]	-1248.5	259.6	21	50
822	S[330]	-1259.5	332.6	21	50
823	SX[34]	-1270.5	399.6	21	50
824	S[331]	-1281.5	186.7	21	50

No.	Pad Name	X-axis	Y-axis	Width	Height
825	S[332]	-1292.5	256.7	21	50
826	S[333]	-1303.5	329.7	21	50
827	DUMMY	-1314.5	396.7	21	50
828	S[334]	-1325.5	183.8	21	50
829	S[335]	-1336.5	253.8	21	50
830	S[336]	-1347.5	326.8	21	50
831	DUMMY	-1358.5	393.8	21	50
832	S[337]	-1369.5	180.9	21	50
833	S[338]	-1380.5	250.9	21	50
834	S[339]	-1391.5	323.9	21	50
835	SX[35]	-1402.5	390.9	21	50
836	S[340]	-1413.5	178	21	50
837	S[341]	-1424.5	248	21	50
838	S[342]	-1435.5	321	21	50
839	DUMMY	-1446.5	388	21	50
840	S[343]	-1457.5	175.1	21	50
841	S[344]	-1468.5	245.1	21	50
842	S[345]	-1479.5	318.1	21	50
843	DUMMY	-1490.5	385.1	21	50
844	S[346]	-1501.5	172.2	21	50
845	S[347]	-1512.5	242.2	21	50
846	S[348]	-1523.5	315.2	21	50
847	SX[36]	-1534.5	382.2	21	50
848	S[349]	-1545.5	169.3	21	50
849	S[350]	-1556.5	239.3	21	50
850	S[351]	-1567.5	312.3	21	50
851	DUMMY	-1578.5	379.3	21	50
852	S[352]	-1589.5	166.4	21	50
853	S[353]	-1600.5	236.4	21	50
854	S[354]	-1611.5	309.4	21	50
855	DUMMY	-1622.5	376.4	21	50
856	S[355]	-1633.5	163.5	21	50
857	S[356]	-1644.5	233.5	21	50
858	S[357]	-1655.5	306.5	21	50
859	SX[37]	-1666.5	373.5	21	50
860	S[358]	-1677.5	160.6	21	50
861	S[359]	-1688.5	230.6	21	50
862	S[360]	-1699.5	303.6	21	50
863	DUMMY	-1710.5	370.6	21	50
864	S[361]	-1721.5	157.7	21	50
865	S[362]	-1732.5	227.7	21	50
866	S[363]	-1743.5	300.7	21	50
867	DUMMY	-1754.5	367.7	21	50
868	S[364]	-1765.5	154.8	21	50
869	S[365]	-1776.5	224.8	21	50
870	S[366]	-1787.5	297.8	21	50
871	SX[38]	-1798.5	364.8	21	50
872	S[367]	-1809.5	151.9	21	50
873	S[368]	-1820.5	221.9	21	50
874	S[369]	-1831.5	294.9	21	50
875	DUMMY	-1842.5	361.9	21	50
876	S[370]	-1853.5	149	21	50
877	S[371]	-1864.5	219	21	50
878	S[372]	-1875.5	292	21	50
879	DUMMY	-1886.5	359	21	50
880	S[373]	-1897.5	146.1	21	50
881	S[374]	-1908.5	216.1	21	50
882	S[375]	-1919.5	289.1	21	50
883	SX[39]	-1930.5	356.1	21	50
884	S[376]	-1941.5	143.2	21	50
885	S[377]	-1952.5	213.2	21	50
886	S[378]	-1963.5	286.2	21	50
887	DUMMY	-1974.5	353.2	21	50
888	S[379]	-1985.5	140.3	21	50
889	S[380]	-1996.5	210.3	21	50
890	S[381]	-2007.5	283.3	21	50
891	DUMMY	-2018.5	350.3	21	50
892	S[382]	-2029.5	137.4	21	50
893	S[383]	-2040.5	207.4	21	50
894	S[384]	-2051.5	280.4	21	50
895	SX[40]	-2062.5	347.4	21	50
896	S[385]	-2073.5	134.5	21	50
897	S[386]	-2084.5	204.5	21	50
898	S[387]	-2095.5	277.5	21	50
899	DUMMY	-2106.5	344.5	21	50
900	S[388]	-2117.5	131.6	21	50
901	S[389]	-2128.5	201.6	21	50
902	S[390]	-2139.5	274.6	21	50
903	DUMMY	-2150.5	341.6	21	50
904	S[391]	-2161.5	128.7	21	50
905	S[392]	-2172.5	198.7	21	50
906	S[393]	-2183.5	271.7	21	50
907	SX[41]	-2194.5	338.7	21	50
908	S[394]	-2205.5	125.8	21	50
909	S[395]	-2216.5	195.8	21	50
910	S[396]	-2227.5	268.8	21	50
911	DUMMY	-2238.5	335.8	21	50
912	S[397]	-2249.5	122.9	21	50
913	S[398]	-2260.5	192.9	21	50
914	S[399]	-2271.5	265.9	21	50
915	DUMMY	-2282.5	332.9	21	50
916	S[400]	-2293.5	120	21	50

No.	Pad Name	X-axis	Y-axis	Width	Height
917	S[401]	-2304.5	190	21	50
918	S[402]	-2315.5	263	21	50
919	SX[42]	-2326.5	330	21	50
920	S[403]	-2337.5	117.1	21	50
921	S[404]	-2348.5	187.1	21	50
922	S[405]	-2359.5	260.1	21	50
923	DUMMY	-2370.5	327.1	21	50
924	S[406]	-2381.5	114.2	21	50
925	S[407]	-2392.5	184.2	21	50
926	S[408]	-2403.5	257.2	21	50
927	DUMMY	-2414.5	324.2	21	50
928	S[409]	-2425.5	111.3	21	50
929	S[410]	-2436.5	181.3	21	50
930	S[411]	-2447.5	254.3	21	50
931	SX[43]	-2458.5	321.3	21	50
932	S[412]	-2469.5	108.4	21	50
933	S[413]	-2480.5	178.4	21	50
934	S[414]	-2491.5	251.4	21	50
935	DUMMY	-2502.5	318.4	21	50
936	S[415]	-2513.5	105.5	21	50
937	S[416]	-2524.5	175.5	21	50
938	S[417]	-2535.5	248.5	21	50
939	DUMMY	-2546.5	315.5	21	50
940	S[418]	-2557.5	102.6	21	50
941	S[419]	-2568.5	172.6	21	50
942	S[420]	-2579.5	245.6	21	50
943	SX[44]	-2590.5	312.6	21	50
944	S[421]	-2601.5	99.7	21	50
945	S[422]	-2612.5	169.7	21	50
946	S[423]	-2623.5	242.7	21	50
947	DUMMY	-2634.5	309.7	21	50
948	S[424]	-2645.5	96.8	21	50
949	S[425]	-2656.5	166.8	21	50
950	S[426]	-2667.5	239.8	21	50
951	DUMMY	-2678.5	306.8	21	50
952	S[427]	-2689.5	93.9	21	50
953	S[428]	-2700.5	163.9	21	50
954	S[429]	-2711.5	236.9	21	50
955	SX[45]	-2722.5	303.9	21	50
956	S[430]	-2733.5	91	21	50
957	S[431]	-2744.5	161	21	50
958	S[432]	-2755.5	234	21	50
959	DUMMY	-2766.5	301	21	50
960	S[433]	-2777.5	88.1	21	50
961	S[434]	-2788.5	158.1	21	50
962	S[435]	-2799.5	231.1	21	50
963	DUMMY	-2810.5	298.1	21	50
964	S[436]	-2821.5	85.2	21	50
965	S[437]	-2832.5	155.2	21	50
966	S[438]	-2843.5	228.2	21	50
967	SX[46]	-2854.5	295.2	21	50
968	S[439]	-2865.5	82.3	21	50
969	S[440]	-2876.5	152.3	21	50
970	S[441]	-2887.5	225.3	21	50
971	DUMMY	-2898.5	292.3	21	50
972	S[442]	-2909.5	79.4	21	50
973	S[443]	-2920.5	149.4	21	50
974	S[444]	-2931.5	222.4	21	50
975	DUMMY	-2942.5	289.4	21	50
976	S[445]	-2953.5	76.5	21	50
977	S[446]	-2964.5	146.5	21	50
978	S[447]	-2975.5	219.5	21	50
979	SX[47]	-2986.5	286.5	21	50
980	S[448]	-2997.5	73.6	21	50
981	S[449]	-3008.5	143.6	21	50
982	S[450]	-3019.5	216.6	21	50
983	DUMMY	-3030.5	283.6	21	50
984	S[451]	-3041.5	70.7	21	50
985	S[452]	-3052.5	140.7	21	50
986	S[453]	-3063.5	213.7	21	50
987	DUMMY	-3074.5	280.7	21	50
988	S[454]	-3085.5	67.8	21	50
989	S[455]	-3096.5	137.8	21	50
990	S[456]	-3107.5	210.8	21	50
991	SX[48]	-3118.5	277.8	21	50
992	S[457]	-3129.5	64.9	21	50
993	S[458]	-3140.5	134.9	21	50
994	S[459]	-3151.5	207.9	21	50
995	DUMMY	-3162.5	274.9	21	50
996	S[460]	-3173.5	62	21	50
997	S[461]	-3184.5	132	21	50
998	S[462]	-3195.5	205	21	50
999	DUMMY	-3206.5	272	21	50
1000	S[463]	-3217.5	59.1	21	50
1001	S[464]	-3228.5	129.1	21	50
1002	S[465]	-3239.5	202.1	21	50
1003	SX[49]	-3250.5	269.1	21	50
1004	S[466]	-3261.5	56.2	21	50
1005	S[467]	-3272.5	126.2	21	50
1006	S[468]	-3283.5	199.2	21	50
1007	DUMMY	-3294.5	266.2	21	50
1008	S[469]	-3305.5	53.3	21	50

No.	Pad Name	X-axis	Y-axis	Width	Height
1009	S[470]	-3316.5	123.3	21	50
1010	S[471]	-3327.5	196.3	21	50
1011	DUMMY	-3338.5	263.3	21	50
1012	S[472]	-3349.5	50.4	21	50
1013	S[473]	-3360.5	120.4	21	50
1014	S[474]	-3371.5	193.4	21	50
1015	SX[50]	-3382.5	260.4	21	50
1016	S[475]	-3393.5	47.5	21	50
1017	S[476]	-3404.5	117.5	21	50
1018	S[477]	-3415.5	190.5	21	50
1019	DUMMY	-3426.5	257.5	21	50
1020	S[478]	-3437.5	44.6	21	50
1021	S[479]	-3448.5	114.6	21	50
1022	S[480]	-3459.5	187.6	21	50
1023	DUMMY	-3470.5	254.6	21	50
1024	S[481]	-3481.5	41.7	21	50
1025	S[482]	-3492.5	111.7	21	50
1026	S[483]	-3503.5	184.7	21	50
1027	SX[51]	-3514.5	251.7	21	50
1028	S[484]	-3525.5	38.8	21	50
1029	S[485]	-3536.5	108.8	21	50
1030	S[486]	-3547.5	181.8	21	50
1031	DUMMY	-3558.5	248.8	21	50
1032	S[487]	-3569.5	35.9	21	50
1033	S[488]	-3580.5	105.9	21	50
1034	S[489]	-3591.5	178.9	21	50
1035	DUMMY	-3602.5	245.9	21	50
1036	S[490]	-3613.5	33	21	50
1037	S[491]	-3624.5	103	21	50
1038	S[492]	-3635.5	176	21	50
1039	SX[52]	-3646.5	243	21	50
1040	S[493]	-3657.5	30.1	21	50
1041	S[494]	-3668.5	100.1	21	50
1042	S[495]	-3679.5	173.1	21	50
1043	DUMMY	-3690.5	240.1	21	50
1044	S[496]	-3701.5	27.2	21	50
1045	S[497]	-3712.5	97.2	21	50
1046	S[498]	-3723.5	170.2	21	50
1047	DUMMY	-3734.5	237.2	21	50
1048	S[499]	-3745.5	24.3	21	50
1049	S[500]	-3756.5	94.3	21	50
1050	S[501]	-3767.5	167.3	21	50
1051	SX[53]	-3778.5	234.3	21	50
1052	S[502]	-3789.5	21.4	21	50
1053	S[503]	-3800.5	91.4	21	50
1054	S[504]	-3811.5	164.4	21	50
1055	DUMMY	-3822.5	231.4	21	50
1056	S[505]	-3833.5	18.5	21	50
1057	S[506]	-3844.5	88.5	21	50
1058	S[507]	-3855.5	161.5	21	50
1059	DUMMY	-3866.5	228.5	21	50
1060	S[508]	-3877.5	15.6	21	50
1061	S[509]	-3888.5	85.6	21	50
1062	S[510]	-3899.5	158.6	21	50
1063	SX[54]	-3910.5	225.6	21	50
1064	S[511]	-3921.5	12.7	21	50
1065	S[512]	-3932.5	82.7	21	50
1066	S[513]	-3943.5	155.7	21	50
1067	DUMMY	-3954.5	222.7	21	50
1068	S[514]	-3965.5	9.8	21	50
1069	S[515]	-3976.5	79.8	21	50
1070	S[516]	-3987.5	152.8	21	50
1071	DUMMY	-3998.5	219.8	21	50
1072	S[517]	-4009.5	6.9	21	50
1073	S[518]	-4020.5	76.9	21	50
1074	S[519]	-4031.5	149.9	21	50
1075	SX[55]	-4042.5	216.9	21	50
1076	S[520]	-4053.5	4	21	50
1077	S[521]	-4064.5	74	21	50
1078	S[522]	-4075.5	147	21	50
1079	DUMMY	-4086.5	214	21	50
1080	S[523]	-4097.5	1.1	21	50
1081	S[524]	-4108.5	71.1	21	50
1082	S[525]	-4119.5	144.1	21	50
1083	DUMMY	-4130.5	211.1	21	50
1084	S[526]	-4141.5	-1.8	21	50
1085	S[527]	-4152.5	68.2	21	50
1086	S[528]	-4163.5	141.2	21	50
1087	SX[56]	-4174.5	208.2	21	50
1088	S[529]	-4185.5	-4.7	21	50
1089	S[530]	-4196.5	65.3	21	50
1090	S[531]	-4207.5	138.3	21	50
1091	DUMMY	-4218.5	205.3	21	50
1092	S[532]	-4229.5	-7.6	21	50
1093	S[533]	-4240.5	62.4	21	50
1094	S[534]	-4251.5	135.4	21	50
1095	DUMMY	-4262.5	202.4	21	50
1096	S[535]	-4273.5	-10.5	21	50
1097	S[536]	-4284.5	59.5	21	50
1098	S[537]	-4295.5	132.5	21	50
1099	SX[57]	-4306.5	199.5	21	50
1100	S[538]	-4317.5	-13.4	21	50

No.	Pad Name	X-axis	Y-axis	Width	Height
1101	S[539]	-4328.5	56.6	21	50
1102	S[540]	-4339.5	129.6	21	50
1103	DUMMY	-4350.5	196.6	21	50
1104	S[541]	-4361.5	-16.3	21	50
1105	S[542]	-4372.5	53.7	21	50
1106	S[543]	-4383.5	126.7	21	50
1107	DUMMY	-4394.5	193.7	21	50
1108	S[544]	-4405.5	-19.2	21	50
1109	S[545]	-4416.5	50.8	21	50
1110	S[546]	-4427.5	123.8	21	50
1111	SX[58]	-4438.5	190.8	21	50
1112	S[547]	-4449.5	-22.1	21	50
1113	S[548]	-4460.5	47.9	21	50
1114	S[549]	-4471.5	120.9	21	50
1115	DUMMY	-4482.5	187.9	21	50
1116	S[550]	-4493.5	-25	21	50
1117	S[551]	-4504.5	45	21	50
1118	S[552]	-4515.5	118	21	50
1119	DUMMY	-4526.5	185	21	50
1120	S[553]	-4537.5	-27.9	21	50
1121	S[554]	-4548.5	42.1	21	50
1122	S[555]	-4559.5	115.1	21	50
1123	SX[59]	-4570.5	182.1	21	50
1124	S[556]	-4581.5	-30.8	21	50
1125	S[557]	-4592.5	39.2	21	50
1126	S[558]	-4603.5	112.2	21	50
1127	DUMMY	-4614.5	179.2	21	50
1128	S[559]	-4625.5	-33.7	21	50
1129	S[560]	-4636.5	36.3	21	50
1130	S[561]	-4647.5	109.3	21	50
1131	DUMMY	-4658.5	176.3	21	50
1132	S[562]	-4669.5	-36.6	21	50
1133	S[563]	-4680.5	33.4	21	50
1134	S[564]	-4691.5	106.4	21	50
1135	SX[60]	-4702.5	173.4	21	50
1136	S[565]	-4713.5	-39.5	21	50
1137	S[566]	-4724.5	30.5	21	50
1138	S[567]	-4735.5	103.5	21	50
1139	DUMMY	-4746.5	170.5	21	50
1140	S[568]	-4757.5	-42.4	21	50
1141	S[569]	-4768.5	27.6	21	50
1142	S[570]	-4779.5	100.6	21	50
1143	DUMMY	-4790.5	167.6	21	50
1144	S[571]	-4801.5	-45.3	21	50
1145	S[572]	-4812.5	24.7	21	50
1146	S[573]	-4823.5	97.7	21	50
1147	SX[61]	-4834.5	164.7	21	50
1148	S[574]	-4845.5	-48.2	21	50
1149	S[575]	-4856.5	21.8	21	50
1150	S[576]	-4867.5	94.8	21	50
1151	DUMMY	-4878.5	161.8	21	50
1152	S[577]	-4889.5	-51.1	21	50
1153	S[578]	-4900.5	18.9	21	50
1154	S[579]	-4911.5	91.9	21	50
1155	DUMMY	-4922.5	158.9	21	50
1156	S[580]	-4933.5	-54	21	50
1157	S[581]	-4944.5	16	21	50
1158	S[582]	-4955.5	89	21	50
1159	SX[62]	-4966.5	156	21	50
1160	S[583]	-4977.5	-56.9	21	50
1161	S[584]	-4988.5	13.1	21	50
1162	S[585]	-4999.5	86.1	21	50
1163	DUMMY	-5010.5	153.1	21	50
1164	S[586]	-5021.5	-59.8	21	50
1165	S[587]	-5032.5	10.2	21	50
1166	S[588]	-5043.5	83.2	21	50
1167	DUMMY	-5054.5	150.2	21	50
1168	S[589]	-5065.5	-62.7	21	50
1169	S[590]	-5076.5	7.3	21	50
1170	S[591]	-5087.5	80.3	21	50
1171	SX[63]	-5098.5	147.3	21	50
1172	S[592]	-5109.5	-65.6	21	50

No.	Pad Name	X-axis	Y-axis	Width	Height
1173	S[593]	-5120.5	4.4	21	50
1174	S[594]	-5131.5	77.4	21	50
1175	DUMMY	-5142.5	144.4	21	50
1176	S[595]	-5153.5	-68.5	21	50
1177	S[596]	-5164.5	1.5	21	50
1178	S[597]	-5175.5	74.5	21	50
1179	DUMMY	-5186.5	141.5	21	50
1180	S[598]	-5197.5	-71.4	21	50
1181	S[599]	-5208.5	-1.4	21	50
1182	S[600]	-5219.5	71.6	21	50
1183	SX[64]	-5230.5	138.6	21	50
1184	S[601]	-5241.5	-74.3	21	50
1185	GRID	-5252.5	-4.3	21	50
1186	DUMMY	-5263.5	68.7	21	50
1187	DUMMY	-5274.5	135.7	21	50
1188	VCOM_PASS	-5285.5	-77.2	21	50
1189	VCOM_PASS	-5296.5	-7.2	21	50
1190	VCOM_PASS	-5307.5	65.8	21	50
1191	VCOM_PASS	-5318.5	132.8	21	50
1192	DUMMY	-5246.5	422	34	40
1193	DUMMY	-5147.5	422	34	40
1194	DUMMY	-5048.5	422	34	40
1195	DUMMY	-4949.5	422	34	40
1196	DUMMY	-4850.5	422	34	40
1197	DUMMY	-4751.5	422	34	40
1198	DUMMY	-4652.5	422	34	40
1199	DUMMY	-4553.5	422	34	40
1200	DUMMY	-4454.5	422	34	40
1201	DUMMY	-4355.5	422	34	40
1202	DUMMY	-4256.5	422	34	40
1203	DUMMY	-4157.5	422	34	40
1204	DUMMY	-4058.5	422	34	40
1205	DUMMY	-3959.5	422	34	40
1206	DUMMY	-3860.5	422	34	40
1207	DUMMY	-3761.5	422	34	40
1208	DUMMY	-3662.5	422	34	40
1209	DUMMY	-3563.5	422	34	40
1210	DUMMY	-3464.5	422	34	40
1211	DUMMY	-3365.5	422	34	40
1212	DUMMY	-3266.5	422	34	40
1213	DUMMY	-3167.5	422	34	40
1214	DUMMY	-3068.5	422	34	40
1215	DUMMY	-2969.5	422	34	40
1216	DUMMY	-2870.5	422	34	40
1217	DUMMY	-2771.5	422	34	40
1218	DUMMY	-2672.5	422	34	40
1219	DUMMY	-2573.5	422	34	40
1220	DUMMY	-2474.5	422	34	40
1221	DUMMY	-2375.5	422	34	40
1222	DUMMY	-2276.5	422	34	40
1223	DUMMY	-2177.5	422	34	40
1224	DUMMY	-2078.5	422	34	40
1225	DUMMY	-1979.5	422	34	40
1226	DUMMY	-1880.5	422	34	40
1227	DUMMY	-1781.5	422	34	40
1228	DUMMY	-1682.5	422	34	40
1229	DUMMY	-1583.5	422	34	40
1230	DUMMY	-1484.5	422	34	40
1231	DUMMY	-1385.5	422	34	40
1232	DUMMY	-1286.5	422	34	40
1233	DUMMY	-1187.5	422	34	40
1234	DUMMY	-1088.5	422	34	40
1235	DUMMY	-989.5	422	34	40

11 Revision History

Table 122. Revision History List

Reversion	Date	Page	Description
V100	2024/3/22	All	First Release
V200	2024/9/19	19 145	Correct Max series resistance table. Update NV Memory Programing Flow chart
V300	2024/11/7	147 11, 151, All 152	Correct I2C Slave Address. Integrating 3 temperature grade in one specification. Update Driver Supply Voltage
V400	2025/7/25	9,10 157	Append 1+2-dot in IC features. Correct POR AC Specification.

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