seL4 IPC Internals (cont)

According to the x86 calling conventions and the seL4 semantics

RDI	stores	**syscall number**
RSI	stores	**message info**
RDX	stores	**capability pointer**
R10	stores	**message reigister 0**
R8	stores	**message reigister 1**
R9	stores	**message reigister 2**
R15	stores	**message reigister 3**
R12	stores	**reply** (only used in MCS configuration)
IPC Buffer	stores	**Other message registers**

According to seL4's design, the only **first four** message registers will be passed using **physical registers** and the rest will be placed in the IPC Buffer. We will strictly follow this semantic so we need to design the IPC emulation protocal. (next slide)