SSD1325

Advance Information

128 x 80, 16 Gray Scale Dot Matrix **OLED/PLED Segment/Common Driver with Controller**

This document contains information on a new product. Specifications and information herein are subject to change without notice.



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1 GENERAL DESCRIPTION

SSD1325 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. It consists of 208 high voltage/current driving output pins for driving 128 segments and 80 commons. This IC is designed for Common Cathode type OLED/PLED panel.

SSD1325 displays data directly from its internal 128x80x4 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from general MCU through the hardware selectable 6800-/8080-series compatible Parallel Interface or Serial Peripheral Interface.

It has a 128-step contrast control and a 16 gray level control. The embedded on-chip oscillator and DC-DC voltage converter reduce the number of external components.

2 FEATURES

- Support max. 128 x 80 matrix panel
- Power supply: $V_{DD} = 2.4V 3.5V$

$$V_{CC} = 8.0V - 16.0V$$

- For matrix display:
 - o OLED driving output voltage, 14V maximum
 - o Can output maximum segment source current: 300uA
 - o Common maximum sink current: 40mA
- Embedded 128 x 80 x 4 bit SRAM display memory
- 128 step contrast current control on monochrome passive OLED panel
- 16 gray scale
- Internal Oscillator
- Programmable Frame Rate
- 8-bit 6800-series Parallel Interface, 8080-series Parallel Interface, Serial Peripheral Interface.
- Row re-mapping and Column re-mapping
- Low power consumption (<5.0uA @sleep mode)
- Wide range of operating temperature: -40 to 85 °C

3 ORDERING INFORMATION

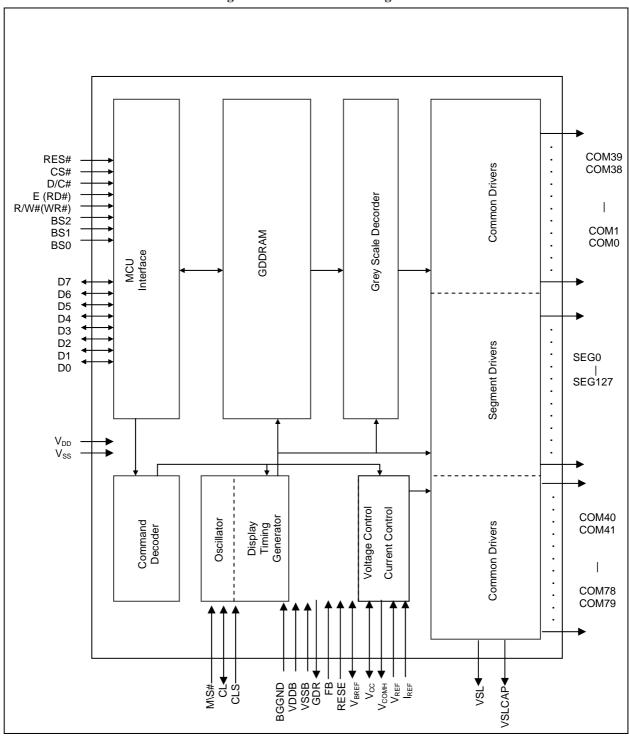
Table 1: Ordering Information

Ordering Part Number	SEG	СОМ	Package Form	Reference	Remarks
SSD1325Z	128	80	COG	Page 8, 57	Min SEG pad pitch: 52.2umMin COM pad pitch: 51.8um
SSD1325T6R1	128	80	TAB	Page 58	 8-bit 80 / 68 / SPI interface Output lead pitch: 0.12mm x 0.998 = 0.11976mm 4 SPH, 35m film Full resolution 128 x 80

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4 BLOCK DIAGRAM

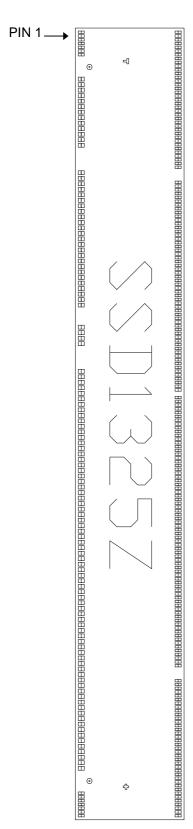
Figure 1: SSD1325 Block Diagram



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5 DIE PAD FLOOR PLAN

Figure 2: SSD1325Z Die Drawing





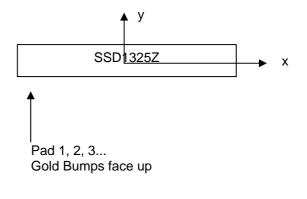
Note

¹+ represents the centre of the alignment mark

Alignment Mark	X-pos (μm)	Y-pos (μm)
G1	4934.100	-557.675
o Shape	-4934.100	-557.675
+ shape	5014.100	-52.200
T shape	-5014.100	-52.200

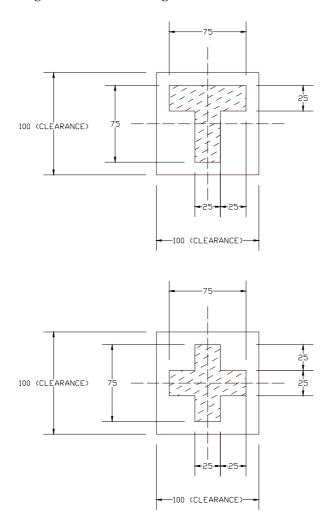
Die Size	10942um x 1508um
Die Thickness	457 +/- 25um
I/O pad pitch	76.2um
SEG pad pitch	52.2um
COM pad pitch	51.8um
Bump Height	Nominal 18um

Bump size	X (um)	Y (um)
Pad 1-7,123-331	34	84
Pad 8-122	54	84



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Figure 3: SSD1325Z Alignment Mark Dimensions



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Table 2 : SSD1325Z Bump Die Pad Coordinates

Pad#	Signal	X-pos	Y-nos
1	DUMMY	-5414.000	Y-pos -672.075
2	DUMMY	-5361.800	-672.075
3	COM75	-5309.600	-672.075
5	COM76 COM77	-5257.800 -5206.000	-672.075 -672.075
6	COM78	-5154.200	-672.075
7	COM79	-5102.400	-672.075
8	DUMMY	-4767.075	-672.075
9	DUMMY	-4690.875	-672.075
10	DUMMY	-4614.675	-672.075
11	DUMMY	-4538.475	-672.075
12	DUMMY	-4462.275	-672.075
13 14	DUMMY	-4386.075 -4309.875	-672.075
15	DUMMY	-4309.675	-672.075 -672.075
16	DUMMY	-4157.475	-672.075
17	DUMMY	-4081.275	-672.075
18	DUMMY	-4005.075	-672.075
19	DUMMY	-3928.875	-672.075
20	DUMMY	-3852.675	-672.075
21	VCL	-3471.675	-672.075
22	VCL	-3395.475	-672.075
23	VCL	-3319.275	-672.075
24 25	VSS VSSB	-3243.075 -3166.875	-672.075 -672.075
25 26	VSSB	-3166.875	-672.075
27	VSL	-3090.675	-672.075
28	VSLCAP	-2938.275	-672.075
29	VSLCAP	-2862.075	-672.075
30	VDD	-2785.875	-672.075
31	VCC	-2709.675	-672.075
32	VCC	-2633.475	-672.075
33	VCOMH	-2557.275	-672.075
34	VCOMH	-2481.075	-672.075
35 36	TR8 TR7	-2404.875 -2328.675	-672.075 -672.075
37	TR6	-2326.675	-672.075
38	TR5	-2176.275	-672.075
39	TR4	-2100.075	-672.075
40	TR3	-2023.875	-672.075
41	TR2	-1947.675	-672.075
42	TR1	-1871.475	-672.075
43	TR0	-1795.275	-672.075
44	VSS	-1719.075	-672.075
45	VSSB	-1642.875	-672.075
46 47	GDR GDR	-1338.075 -1261.875	-672.075 -672.075
48	GDR	-1185.675	-672.075
49	GDR	-1109.475	-672.075
50	VDDB	-728.475	-672.075
51	V DDB	-652.275	-672.075
52	VDD	-576.075	-672.075
53	VDD	-499.875	-672.075
54	FB	-423.675	-672.075
55 56	RESE VBREF	-347.475 -271.275	-672.075 -672.075
57	BGGND	-195.075	-672.075
58	VSS	-118.875	-672.075
59	VCC	-42.675	-672.075
60	GPIO0	33.525	-672.075
61	GPIO1	109.725	070 075
62			-672.075
	VDD	185.925	-672.075
63	VDD BS0	185.925 262.125	-672.075 -672.075
64	VDD BS0 VSS	185.925 262.125 338.325	-672.075 -672.075 -672.075
64 65	VDD BS0 VSS BS1	185.925 262.125 338.325 414.525	-672.075 -672.075 -672.075 -672.075
64 65 66	VDD BS0 VSS BS1 VDD	185.925 262.125 338.325 414.525 490.725	-672.075 -672.075 -672.075 -672.075 -672.075
64 65	VDD BS0 VSS BS1	185.925 262.125 338.325 414.525	-672.075 -672.075 -672.075 -672.075
64 65 66 67 68 69	VDD BS0 VSS BS1 VDD	185.925 262.125 338.325 414.525 490.725	-672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075
64 65 66 67 68 69 70	VDD BS0 VSS BS1 VDD BS2 VSS FR CL	185.925 262.125 338.325 414.525 490.725 566.925 643.125 719.325 795.525	-672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075
64 65 66 67 68 69 70 71	VDD BS0 VSS BS1 VDD BS2 VSS FR CL DOF#	185.925 262.125 338.325 414.525 490.725 566.925 643.125 719.325 795.525 871.725	-672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075
64 65 66 67 68 69 70 71 72	VDD BS0 VSS BS1 VDD BS2 VSS FR CL DOF# VSS	185.925 262.125 338.325 414.525 490.725 566.925 643.125 719.325 795.525 871.725 947.925	-672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075
64 65 66 67 68 69 70 71 72 73	VDD BS0 VSS BS1 VDD BS2 VSS FR CL DOF# VSS CS#	185.925 262.125 338.325 414.525 490.725 566.925 643.125 719.325 795.525 871.725 947.925 1024.125	-672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075
64 65 66 67 68 69 70 71 72 73 74	VDD BS0 VSS BS1 VDD BS2 VSS FR CL DOF# VSS CS# RES#	185.925 262.125 338.325 414.525 490.725 566.925 643.125 719.325 795.525 871.725 947.925 1024.125	-672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075
64 65 66 67 68 69 70 71 72 73 74 75	VDD BS0 VSS BS1 VDD BS2 VSS FR CL DOF# VSS CS# RES# D/C#	185.925 262.125 338.325 490.725 566.925 643.125 719.325 795.525 871.725 947.925 1024.125 1100.325 1176.525	-672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075
64 65 66 67 68 69 70 71 72 73 74 75 76	VDD BS0 VSS BS1 VDD BS2 VSS FR CL DOF# VSS CS# RES# D/C# VSS	185.925 262.125 338.325 414.525 490.725 566.925 643.125 719.325 795.525 871.725 947.925 1024.125 1100.325 1176.525 1176.525	-672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075
64 65 66 67 68 69 70 71 72 73 74 75	VDD BS0 VSS BS1 VDD BS2 VSS FR CL DOF# VSS CS# RES# D/C#	185.925 262.125 338.325 490.725 566.925 643.125 719.325 795.525 871.725 947.925 1024.125 1100.325 1176.525	-672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075
64 65 66 67 68 69 70 71 72 73 74 75 76 77 78	VDD BS0 VSS BS1 VDD BS2 VSS FR CL DOF# VSS CS# RES# D/C# VSS RVW#(WR#/ E(RD#) VDD	185,925 262,125 338,325 414,525 490,725 566,925 643,125 719,325 795,525 871,725 947,925 1024,125 1100,325 1176,525 1176,525 1328,925 1405,125 1481,325	-672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075
64 65 66 67 68 69 70 71 72 73 74 75 76 77 77 78 79	VDD BS0 VSS BS1 VDD BS2 VSS FR CL DOF# VSS FR VSS SS# PC# VSS RES# DC# VSS RES# DC# VSD DO DD	185.925 262.125 338.325 414.525 566.925 643.125 719.325 795.525 871.725 1024.125 1100.325 1176.525 1252.725 1481.325 1481.325	-672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075 -672.075
64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81	VDD BS0 VSS BS1 VDD BS2 VSS FR CL DOF# VSS CS# RES# DC# VSS RW#(WR#) E(RD#) VDD D0	185.925 262.125 338.325 414.525 490.725 566.925 643.125 719.325 795.525 871.725 1024.125 1100.325 1176.525 1252.725 1328.925 1405.125 1481.325 1557.525	672.075 672.075
64 65 66 67 70 71 72 73 74 75 76 77 80 81 82	VDD BS0 VSS BS1 VDD BS2 VSS FR CL DOF# VSS FR ES# DVC# VSS RES# DVC# VSS ROW#(WN#) E(RD#) VDD D0 D1 D2	185,925 262,125 338,325 414,525 490,725 566,925 643,125 795,525 871,725 947,925 1024,125 1100,325 1176,525 1328,925 1405,125 1405,125 1481,325 1457,525 1633,725	-672.075 -672.075
64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83	VDD BS0 VSS BS1 VDD BS2 VSS FR CL DOFF FR CL DOFF VSS CS# RES# RES# FR E(RD#) VDD D1 D2 D3	185,925 262,125 338,325 414,525 566,925 643,125 719,325 795,525 871,725 1024,125 1100,325 1176,525 1252,725 1481,325 1481,325 1481,325 1633,725 1799,925	672.075 672.075
64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84	VDD BS0 VSS BS1 VDD BS2 VSS FR CL DOF# VSS CS# RES# DC# VSS CS# RESE# DC# VDD D0 D1 D1 D2 D3 D4	185,925 262,125 338,325 414,525 490,725 566,925 643,125 795,525 871,725 1024,125 1100,325 1176,525 1252,725 1328,925 1405,125 1481,325 1557,525 1633,725 1709,925 1709,925 1786,125	672.075 672.075
64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 80 81 82 83 84 85	VDD BS0 VSS BS1 VDD BS2 VSS FR CL DOF# VSS CS# D/C# VSS RES# E(RD#) VDD D1 D2 D3 D3 D4	185.925 262.125 338.325 414.525 566.925 643.125 795.525 871.725 1024.125 1100.325 1176.525 1252.725 1328.925 1405.125 1481.325 1481.325 1481.325 1481.325 1481.325 1799.925 1786.125 1862.325	672.075 672.075
64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86	VDD BS0 VSS BS1 VDD BS2 VSS FR CL DOF# VSS CS# RES# DC# VSS CS# RESE# DC# VDD D0 D1 D1 D2 D3 D4	185,925 262,125 338,325 414,525 490,725 566,925 643,125 795,525 871,725 1024,125 1100,325 1176,525 1252,725 1328,925 1405,125 1481,325 1557,525 1633,725 1709,925 1709,925 1786,125	672.075 672.075
64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 80 81 82 83 84 85	VDD BS0 VSS BS1 VDD BS2 VSS FR CL DOF# VSS CS# RES# RES# E(RD#) VDD D1 D2 D3 D4 D5	185,925 262,125 338,325 414,525 490,725 566,925 643,125 795,525 871,725 1024,125 1100,325 1176,525 1252,725 1328,925 1405,125 140	672.075 672.075
64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 80 81 82 83 84 85 86 87	VDD BS0 VSS BS1 VDD BS2 VSS FR CL DOF# VSS CS# RES# DC# VSS RKW(WR# E(RD#) DD	185,925 262,125 338,325 414,525 490,725 566,925 643,125 795,525 871,725 1024,125 1100,325 1176,525 1252,725 1328,925 1405,125 140	672.075 672.075
64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88	VDD BS0 VSS BS1 VDD BS2 VSS FR CL DOF# VSS CS# RES# RES# RES# VSS VSS VSS DOF# VDD D1 D2 D3 D4 D5 D6 D7 VSS	185,925 262,125 338,325 414,525 566,925 643,125 719,325 795,525 871,725 1024,125 1100,325 1176,525 1252,725 1328,925 1405,125 1481,325 1633,725 1799,925 1786,125 1862,325 1938,525	672.075 672.075

99									
99	Pad#	Signal	X-pos	Y-pos	1 1	Pad#	Signal	X-pos	Y-pos
92			2395.725	-672.075	1			2610.000	672.075
98					1				672.075
95 VCOMH 2263-325 672-075 95 VCOMH 2760-525 672-075 96 VREF 2765-225 672-075 97 VCC 2852-325 672-075 98 VCD 3005-325 672-075 98 VCD 3005-325 672-075 99 VCD 3005-325 672-075 100 VSL 3015-225 672-075 101 VSL 3015-225 672-075 102 VCL 3330-225 672-075 103 VCL 3330-225 672-075 104 VSL 3310-225 672-075 105 VCL 3330-225 672-075 106 DUMWY 3348-325 672-075 107 DUMWY 3348-325 672-075 108 DUMWY 3348-325 672-075 109 DUMWY 3349-325 672-075 109 DUMWY 3349-325 672-075 110 DUMWY 3349-325 672-075 111 DUMWY 3349-325 672-075 112 DUMWY 3478-325 672-075 113 DUMWY 4722-325 672-075 114 DUMWY 4722-325 672-075 115 DUMWY 4722-325 672-075 116 DUMWY 4722-325 672-075 117 DUMWY 4722-325 672-075 118 DUMWY 4722-325 672-075 119 DUMWY 4722-325 672-075 110 DUMWY 4722-325 672-075 111 DUMWY 4722-325 672-075 112 DUMWY 4722-325 672-075 113 DUMWY 4722-325 672-075 114 DUMWY 4723-325 672-075 115 DUMWY 4723-325 672-075 116 DUMWY 4723-325 672-075 117 DUMWY 4723-325 672-075 118 DUMWY 4723-325 672-075 129 DUMWY 4723-325 672-075 121 DUMWY 4723-325 672-075 122 DUMWY 4723-325 672-075 123 DUMWY 4723-325 672-075 124 DUMWY 4723-325 672-075 125 DUMWY 4723-325 672-075 126 DUMWY 4723-325 672-075 127 DUMWY 4723-325 672-075 128 DUMWY 4723-325 672-075 129 DUMWY 4723-325 672-075 121 DUMWY 4723-325 672-075 122 DUMWY 4723-325 672-075 123 DUMWY 4723-325 672-075 124 DUMWY 4723-325 672-075 125 DUMWY 4723-325 672-075 126 DUMWY 4723-325 672-075 127 DUMWY 4723-325 672-075 128 DUMWY 4723-325 672-075 129 DUMWY 4723-325 672-075 121 DUMWY 4723-325 672-075 122 DUMWY 4723-325 672-075 123 DUMWY 4723-325 672-075 124 DUM					1 1				
96 VRIE 2776.725 672.075 97 VCC 2892.925 672.075 98 VCC 2993.925 672.075 198 VCC 2993.925 672.075 199 VCC 2893.925 672.075 199 VCC 2893.925 672.075 190 VSL 3081.525 672.075 101 VSS 3157.725 672.075 101 VSS 3157.725 672.075 101 VSS 3157.725 672.075 102 VCL 3238.925 672.075 103 VCL 3336.325 672.075 104 VCL 3336.325 672.075 105 DUMMY 362.525 672.075 106 DUMMY 362.525 672.075 107 DUMMY 362.525 672.075 108 DUMMY 3691.525 672.075 109 DUMMY 3691.525 672.075 101 DUMMY 3691.525 672.075 111 DUMMY 3691.525 672.075 111 DUMMY 3691.525 672.075 111 DUMMY 376.9325 672.075 112 DUMMY 376.9325 672.075 113 DUMMY 376.9325 672.075 114 DUMMY 376.9325 672.075 115 DUMMY 4831.725 672.075 116 DUMMY 4831.725 672.075 117 DUMMY 4831.725 672.075 118 DUMMY 4831.725 672.075 119 DUMMY 4831.725 672.075 111 DUMMY 4831.725 672.075 111 DUMMY 4831.725 672.075 112 DUMMY 4831.725 672.075 113 DUMMY 4831.725 672.075 114 DUMMY 4831.725 672.075 115 DUMMY 4831.725 672.075 116 DUMMY 4831.725 672.075 117 DUMMY 4831.725 672.075 118 DUMMY 4831.725 672.075 119 DUMMY 4831.725 672.075 111 DUMMY 4831.725 672.075 111 DUMMY 4831.725 672.075 113 DUMMY 4831.725 672.075 114 DUMMY 4831.725 672.075 115 DUMMY 4831.725 672.075 116 DUMMY 4831.725 672.075 117 DUMMY 4831.725 672.075 118 DUMMY 4831.725 672.075 119 DUMMY 4831.725 672.075 111 DUMMY 4831.725 672.075 111 DUMMY 4831.725 672.075 113 DUMMY 4831.725 672.075 114 DUMMY 4830.080 672.075 115 COM39 5102.400 672.075 121 DUMMY 4830.080 672.075 122 DUMMY 4830.080 672.075 123 DUMMY 4830.080 672.075 124 COM39 5102.400 672.075 125 COM39 5102.400 672.075 136 COM30 5388.800 672.075 137 COM39 5102.000 672.075 138 COM39 5102.000 672.075 139 COM39 5102.000 672.075 131 COM39 5102.000 672.075 131 COM39 5102.000 672.075 131 COM39 5102.000 672.07									
96									672.075
98	95	VCOMH	2700.525	-672.075		185	SEG18	2401.200	672.075
99	96	VREF	2776.725	-672.075	1 1	186	SEG19	2349.000	672.075
99	97	VCC	2852.925	-672.075	1	187	SEG20	2296.800	672.075
99					1				672.075
100					-				
Top									
103									672.075
100	101	VSS	3157.725	-672.075	1	191	SEG24	2088.000	672.075
100	102	VCL	3233.925	-672.075	1	192	SEG25	2035.800	672.075
105 DUMNY 3482,525 672,075 195 SEG28 1872,000 672, 195 195 SEG28 1872,000 672, 195 195 SEG28 1872,000 672,075 197 SEG39 1773,800 672,075 197 SEG39 1787,800 672,075 178 SEG39					1				672.075
106 DUMMY 3462.525 672.075 196 SEG28 1879.200 672. 197 DUMMY 3814.925 672.075 198 SEG29 1872.000 672. 198 DUMMY 3919.1725 672.075 198 SEG39 1772.800 672. 197 SEG30 1774.800 672. 197 SEG30 1774.800 672. 197 SEG30 1774.800 672. 197 SEG30 1774.800 672. 197 SEG31 1772.800 672. 197 SEG33 1678.000 672. 197 SEG33 1678.000 672. 197 SEG34 1686.000 672. 197 SEG34 1686									
100									672.075
108 DUMMY 3614 325 672 075 199 SEG33 1772 600 672 672 673 674		20111111			1 1				672.075
109 DUMMY 3691-125 672-075 198 SEG32 1670-400 672-175 199 SEG32 1670-600 672-175 199 SEG33	106	DUMMY	3538.725	-672.075		196	SEG29	1827.000	672.075
109 DUMMY 3691-125 672-075 198 SEG31 1722-600 672-175 197 198	107	DUMMY	3614.925	-672.075	1	197	SEG30	1774.800	672.075
100 DUMMY 3767.325 672.075 198 SEG32 1670.400 672. 111 DUMMY 3919.725 672.075 201 SEG33 1518.200 672. 111 DUMMY 3919.725 672.075 203 SEG33 1513.000 672. 111 DUMMY 4072.125 672.075 203 SEG33 1513.000 672. 111 DUMMY 4072.125 672.075 203 SEG33 1513.000 672. 111 DUMMY 4300.725 672.075 205 SEG33 1357.200 672. 111 DUMMY 4300.725 672.075 205 SEG33 1357.200 672. 111 DUMMY 4357.225 672.075 205 SEG33 1357.200 672. 111 DUMMY 4357.225 672.075 207 SEG33 1357.200 672. 111 DUMMY 4357.225 672.075 208 SEG34 1305.000 672. 112 DUMMY 4453.125 672.075 208 SEG34 1368.00 672. 121 DUMMY 4457.325 672.075 208 SEG42 1148.400 672. 121 DUMMY 4457.325 672.075 210 SEG33 1305.000 672. 121 DUMMY 4457.325 672.075 212 SEG35 3096.00 672.075 213 SEG36 398.00 672.075 214 SEG34 398.700 672. 215 SEG34 398.700 672. 216 SEG33 1306.200 672.075 217 SEG30 730.800 672.075 218 SEG34 786.800 672.075 218 SEG34 376.800 672.075 219 SEG35 376.400 672.075 229 SEG35 376.400 672.075 229 SEG35 376.400 672.075 229 SEG35 376.400 672.075 229 SEG35 376.400	108	DUMMY	3691 125		1	198	SEG31	1722 600	672.075
111					- 1				
1112 DUMMY 3919.725 672.075 113 DUMMY 4072.125 672.075 113 DUMMY 4124.325 672.075 114 DUMMY 4124.325 672.075 203 SEG38 1347.200 672.115 114 DUMMY 424.525 672.075 205 SEG38 1397.200 672.115 115 DUMMY 424.525 672.075 205 SEG38 1397.200 672.115 117 DUMMY 4390.725 672.075 205 SEG38 1397.200 672.116 DUMMY 4453.125 672.075 205 SEG38 1397.200 672.117 DUMMY 4453.125 672.075 205 SEG38 1397.200 672.118 DUMMY 4453.125 672.075 205 SEG38 1397.200 672.118 DUMMY 4453.125 672.075 205 SEG38 1397.200 672.118 DUMMY 4453.125 672.075 205 SEG38 1395.200 672.118 DUMMY 4453.125 672.075 210 SEG31 1252.800 672.118 DUMMY 4453.125 672.075 210 SEG31 1348.400 672.118 DUMMY 4605.525 672.075 211 SEG34 1044.000 672.118 DUMMY 4757.925 672.075 212 SEG35 991.800 672.118 DUMMY 5309.600 672.075 214 SEG37 897.800 672.118 DUMMY 5414.000 672.075 215 SEG38 835.200 672.118 DUMMY 5414.000 672.075 216 SEG39 391.800 672.075 217 SEG50 790.800 672.075 218 SEG51 678.600 672.075 219 SEG55 678.600 672.075 229 SEG55 319.800 672.075 229 SEG55 319.800 672.075 229 SEG55 319.800 672.075 229 SEG55					1 1				
1113 DUMMY 4721-215 672-075 113 DUMMY 4748-325 672-075 114 DUMMY 4748-325 672-075 115 DUMMY 4305-725 672-075 116 DUMMY 4305-725 672-075 117 DUMMY 4305-725 672-075 118 DUMMY 4305-725 672-075 119 DUMMY 4509-325 672-075 120 DUMMY 4509-325 672-075 121 DUMMY 4509-325 672-075 121 DUMMY 4509-325 672-075 122 DUMMY 4509-325 672-075 122 DUMMY 4509-325 672-075 122 DUMMY 4509-326 672-075 123 CUM39 5154-200 672-075 125 CUM39 5154-200 672-075 126 CUM36 5257-800 672-075 127 CUM35 5309-800 672-075 128 DUMMY 5318-800 672-075 129 DUMMY 5414-000 672-075 130 DUMMY 5414-000 672-075 131 DUMMY									672.075
1113 DUMMY 4072.125 -672.075 203 SEG36 1481.600 672.	111	DUMMY	3919.725	-672.075		201	SEG34	1566.000	672.075
1113 DUMMY 4072.125 -672.075 203 SEG36 1481.600 672.	112	DUMMY	3995.925	-672.075	1	202	SEG35	1513.800	672.075
1115					1 1				672.075
1116 DUMMY 3224.525 672.075 205 SEG38 1357.200 672. 1117 DUMMY 4376.925 672.075 207 SEG40 1252.800 672. 1118 DUMMY 44376.925 672.075 208 SEG38 1357.200 672. 1118 DUMMY 44376.925 672.075 208 SEG38 1357.000 672. 1118 DUMMY 4453.125 672.075 208 SEG41 1200.600 672. 120 DUMMY 4605.525 672.075 210 SEG43 1096.200 672. 121 DUMMY 4605.525 672.075 210 SEG43 1096.200 672. 122 DUMMY 4757.925 672.075 210 SEG43 1096.200 672. 122 DUMMY 4757.925 672.075 211 SEG44 1044.000 672. 122 DUMMY 4757.925 672.075 212 SEG48 939.800 672. 123 COM38 5154.200 672.075 213 SEG48 939.800 672. 126 COM38 5257.800 672.075 215 SEG48 339.800 672. 126 COM38 5257.800 672.075 216 SEG49 783.000 672. 127 COM35 5309.600 672.075 217 SEG50 730.800 672. 128 DUMMY 5414.000 672.075 218 SEG51 678.600 672.075 131 DUMMY 5414.000 672.075 219 SEG52 628.400 672. 131 DUMMY 5414.000 672.075 220 SEG53 674.200 672. 131 DUMMY 5414.000 672.075 221 SEG56 417.600 672. 131 DUMMY 5414.000 672.075 222 SEG55 648.000 672.075 133 COM33 5102.400 672.075 222 SEG55 648.000 672.075 134 COM25 4843.400 672.075 224 SEG57 368.400 672.075 138 COM38 5102.400 672.075 224 SEG57 368.400 672.075 138 COM38 548.200 672.075 224 SEG57 368.400 672.075 138 COM26 4843.400 672.075 224 SEG57 368.400 672.075 138 COM27 4947.000 672.075 224 SEG56 417.600 672.075 138 COM26 4843.400 672.075 223 SEG66 104.400 672.075 144 COM26 4843.400 672.075 233 SEG66 104.400 672.075 144 COM26 4843.400 672.075 233 SEG66 522.000 672.075 145 COM14 4459.800 672.075 234 SEG67 -768.800 672.075 145 COM14 4479.800 672.075 235 SEG68 522.000 672.075 146 COM					1 1				672.075
1116 DUMMY 3900.725 672.075 206 SEG39 1305.000 672. 1117 DUMMY 4359.925 672.075 207 SEG40 1252.800 672. 1118 DUMMY 4453.125 672.075 208 SEG42 1148.400 672. 120 DUMMY 4529.325 672.075 209 SEG42 1148.400 672. 121 DUMMY 4681.725 672.075 210 SEG43 196.200 672. 121 DUMMY 4681.725 672.075 211 SEG44 1044.000 672. 122 DUMMY 4681.725 672.075 211 SEG44 1044.000 672. 122 DUMMY 4681.725 672.075 212 SEG45 991.800 672. 123 COM39 5102.400 672.075 213 SEG46 393.600 672. 124 COM38 5154.200 672.075 213 SEG46 393.600 672. 125 COM36 S267.800 672.075 215 SEG47 887.400 672. 127 COM35 S309.600 672.075 216 SEG49 783.000 672. 127 SEG50 730.800 672. 128 DUMMY S361.800 672.075 218 SEG51 678.600 672. 130 DUMMY S361.800 672.075 229 SEG55 SEG40 672. 131 DUMMY S361.800 672.075 220 SEG53 S74.200 672. 131 DUMMY S361.800 672.075 221 SEG56 417.600 672. 131 DUMMY S361.800 672.075 222 SEG55 469.800 672. 133 COM33 S5267.800 672.075 222 SEG55 469.800 672. 133 COM32 S206.000 672.075 222 SEG56 417.600 672. 135 COM36 S102.400 672.075 222 SEG56 417.600 672. 135 COM36 S102.400 672.075 223 SEG56 417.600 672. 135 COM36 S102.400 672.075 224 SEG57 368.400 672. 136 COM36 S102.400 672.075 225 SEG56 S16359 S16300 672. 136 COM36 S102.400 672.075 225 SEG56 S16359 S16300 672. 136 COM36 S102.400 672.075 225 SEG56 S16359 S16300 672. 136 COM36 S102.400 672.075 224 SEG67 S66.400 672. 136 COM36 S102.400 672.075 225 SEG56 S16359 S16300 672. 137 COM26 4895.200 672.075 231 SEG66 S200.000 672.075 232 SEG66 S16300 672.075 333 COM62 3493.800 672.075 348 COM36 S102.400 672.075 348 COM36 S102									
111									672.075
118	116	DUMMY	4300.725	-672.075		206	SEG39	1305.000	672.075
118	117	DUMMY	4376.925	-672.075	1	207	SEG40	1252.800	672.075
119					1				672.075
1220 DUMMY 4605,525 -672,075 210 SEG43 1096,200 672,075 122 DUMMY 4757,925 -672,075 211 SEG44 1044,000 672,075 123 COM39 5102,400 -672,075 213 SEG46 939,600 672,075 125 COM37 5206,000 -672,075 213 SEG46 939,600 672,075 125 COM37 5206,000 -672,075 213 SEG46 939,600 672,075 125 COM37 5206,000 -672,075 215 SEG48 835,200 672,075 126 COM36 5257,800 -672,075 215 SEG48 835,200 672,075 127 COM35 5309,600 -672,075 218 SEG51 730,800 672,075 128 DUMMY 5361,800 -672,075 219 SEG52 626,400 672,075 130 DUMMY 5414,000 -672,075 220 SEG53 574,200 672,075 131 DUMMY 5414,000 672,075 220 SEG53 574,200 672,075 133 COM34 5309,600 672,075 221 SEG54 522,000 672,075 133 COM34 5309,600 672,075 222 SEG55 489,800 672,075 133 COM33 5257,800 672,075 223 SEG56 417,600 672,075 133 COM31 5154,200 672,075 224 SEG57 365,400 672,075 136 COM30 5102,400 672,075 225 SEG58 3313,200 672,075 137 COM29 5050,600 672,075 225 SEG58 3313,200 672,075 138 COM24 4491,600 672,075 226 SEG59 261,000 672,075 139 COM24 4491,600 672,075 227 SEG60 208,800 672,075 144 COM25 4883,400 672,075 231 SEG66 103,400 672,075 144 COM25 4884,400 672,075 231 SEG66 104,400 672,075 144 COM25 4884,400 672,075 231 SEG66 104,400 672,075 148 COM18 4480,800 672,075 231 SEG66 104,400 672,075 148 COM18 4480,800 672,075 231 SEG68 -704,400 672,075 148 COM18 4480,800 672,075 231 SEG68 -704,400 672,075 148 COM18 4427,800 672,075 231 SEG68 -704,400 672,075 148 COM18 4325,400 672,075 234 SEG67 -756,600 672,075 155 COM14 4427,800 672,075 234 SEG67 -756,600 672,075 155 COM14 4428,600 672,075 244 SEG77 -730,800 672,075 155 COM14 427,800					1				
121 DUMMY 4881.725 -672.075 221 SEG44 1044.000 672.075 123 COM39 5102.400 -672.075 213 SEG46 939.600 672.075 124 COM38 5154.200 -672.075 214 SEG47 887.400 672.075 125 COM37 5260.000 -672.075 214 SEG47 887.400 672.075 126 COM36 5257.800 -672.075 215 SEG48 835.200 672.075 126 COM36 5259.600 -672.075 216 SEG49 783.000 672.075 129 DUMMY 5361.800 -672.075 218 SEG51 678.600 672.075 129 DUMMY 5414.000 672.075 229 SEG52 626.400 672.075 131 DUMMY 5361.800 672.075 221 SEG45 522.000 672.075 133 DUMMY 5361.800 672.075 221 SEG55 5742.000 672.075 133 COM33 5257.800 672.075 222 SEG53 5742.000 672.075 133 COM33 5257.800 672.075 222 SEG55 469.800 672.075 133 COM33 5250.600 672.075 222 SEG58 313.200 672.075 133 COM33 5250.600 672.075 224 SEG57 365.400 672.075 133 COM29 5056.600 672.075 225 SEG58 313.200 672.075 133 COM29 5056.600 672.075 226 SEG59 281.000 672.075 133 COM29 5056.600 672.075 227 SEG60 208.800 672.075 134 COM25 4843.400 672.075 228 SEG65 104.400 672.075 144 COM25 4843.400 672.075 230 SEG63 52.200 672.075 144 COM25 4843.400 672.075 231 SEG66 104.400 672.075 144 COM25 4848.400 672.075 231 SEG68 502.000 672.075 145 COM24 4791.600 672.075 231 SEG68 502.000 672.075 145 COM17 4429.000 672.075 231 SEG68 502.000 672.075 145 COM18 4436.200 672.075 231 SEG68 502.000 672.075 145 COM19 4536.200 672.075 231 SEG68 502.000 672.075 146 COM20 4884.400 672.075 235 SEG68 502.000 672.075 146 COM19 4536.200 672.075 236 SEG69 261.000 672.075 155 COM14 4773.600 672.075 236 SEG68 503.000 672.075 500.000 500.000 500.000 500.000 500.000 500.000 500.000 500.000 500.0000 500.000 50					. 1				672.075
122		_			j l				672.075
122	121	DUMMY	4681.725	-672.075	1	211	SEG44	1044.000	672.075
123	122	DUMMY	4757.925	-672.075	1	212	SEG45	991.800	672.075
124					1				672.075
125					4				672.075
126									
127									672.075
128	126	COM36	5257.800	-672.075		216	SEG49	783.000	672.075
128	127	COM35	5309.600	-672.075	1	217	SEG50	730.800	672.075
129 DUMMY 5414.000 672.075 219 SEG52 626.400 672.175 130 DUMMY 5414.000 672.075 220 SEG53 574.200 672.175 132 COMM3 5309.600 672.075 221 SEG54 522.000 672.175 132 COMM3 5309.600 672.075 222 SEG55 469.800 672.175 133 COMM3 5257.800 672.075 222 SEG55 469.800 672.175 134 COMM2 5206.000 672.075 222 SEG56 417.600 672.135 COMM3 5154.200 672.075 225 SEG58 313.200 672.135 COMM3 5154.200 672.075 225 SEG58 313.200 672.137 COMM9 5102.400 672.075 225 SEG58 313.200 672.137 COMM9 5102.400 672.075 227 SEG60 208.800 672.137 COMM9 5102.400 672.075 227 SEG60 208.800 672.138 COMM2 4947.000 672.075 228 SEG59 261.000 672.138 COMM2 4947.000 672.075 228 SEG62 104.400 672.138 COMM2 4843.400 672.075 230 SEG62 104.400 672.141 COMM2 4843.400 672.075 233 SEG68 52.200 672.142 COMM2 4791.600 672.075 233 SEG68 52.200 672.143 COMM2 4791.600 672.075 233 SEG66 104.400 672.144 COMM2 4868.000 672.075 233 SEG66 104.400 672.145 COMM2 4868.000 672.075 233 SEG66 104.400 672.145 COMM2 4868.000 672.075 233 SEG68 -208.800 672.075 234 SEG67 1365.600 672.075 235 SEG68 -208.800 672.075 236 SEG69 -261.000 672.075 237 SEG70 -313.200 672.075 237 SEG70 -313.200 672.075 238 SEG71 -335.400 672.075 239 SEG72 -469.800 672.075 240 SEG37 -335.000 672.075 240 SEG37 -335.000 672.075 241 SEG74 -573.000 672.075 242 SEG58 -391.800 672.075 243 SEG68 -208.800 672.075 244 SEG37 -730.800 672.075 245 SEG98 -313.200 672.075 245 SEG98 -313.200 672.075 246 SEG39 -335.000 672.075 247 SEG88 -335.000 672.075 248 SEG98	128			-672 075	1 1				672.075
130 DUMMY 5414.000 672.075 220 SEG53 574.200 672.075 132 COM34 5309.600 672.075 221 SEG54 522.000 672.075 133 COM33 5257.800 672.075 222 SEG55 469.800 672.075 133 COM33 5257.800 672.075 223 SEG56 417.600 672.075 135 COM31 5154.200 672.075 225 SEG58 313.200 672.075 136 COM30 5102.400 672.075 225 SEG58 313.200 672.075 236 SEG59 261.000 672.075 226 SEG59 261.000 672.075 227 SEG60 208.800 672.075 228 SEG60 208.800 672.075 228 SEG60 208.800 672.075 229 SEG62 104.400 672.075 230 SEG63 52.200 672.075 231 SEG64 208.800 672.075 231 SEG64 208.800 672.075 233 SEG63 52.200 672.075 234 SEG64 208.800 672.075 234 SEG64 208.800 672.075 234 SEG64 208.800 672.075 235 SEG66 528.800 672.075 236 SEG65 522.000 672.075 236 SEG66 208.800 672.075 237 SEG66 208.800 672.075 238 SEG66 -104.400 672.075 238 SEG66 -104.400 672.075 239 SEG66 -108.800 672.075 230 SEG68 208.800 672.075 236 SEG69 208.800 672.075 236 SEG69 208.800 672.075 237 SEG66 208.800 672.075 238 SEG69 208.800 672.075 238 SEG69 208.800 672.075 238 SEG69 208.800 672.075 239 SEG72 -469.800 672.075 239 SEG72 -469.800 672.075 239 SEG72 -469.800 672.075 239 SEG72 -469.800 672.075 239 SEG67 -368.800 672.075 239 SEG67 -368.800 672.075 239 SEG67 -368.800 672.075 239 SEG77 -378.800 672.075 239 SEG77 -378.800 672.075 239 SEG77 -378.800 672.075 239 SEG87 -388.200 672.075 239 SEG88 -388.200 672.075 239 SEG88 -398.200 672.075 239 SEG88 -398.200 672.075 239 SEG89 -388.200 672.075 239 SEG89 -388.200 672.075 239 SEG89 -	_								672.075
131 DUMMY 5361,800 672,075 221 SEG55 4522,000 672,075 133 COM33 5257,800 672,075 222 SEG55 489,800 672,075 134 COM32 5206,000 672,075 224 SEG57 365,400 672,075 136 COM30 5102,400 672,075 226 SEG58 313,200 672,075 136 COM20 598,800 672,075 226 SEG58 313,200 672,075 137 COM29 5050,600 672,075 226 SEG59 261,000 672,075 138 COM28 498,800 672,075 228 SEG61 156,600 672,075 139 COM28 498,800 672,075 229 SEG61 156,600 672,075 139 COM26 4895,200 672,075 229 SEG61 156,600 672,075 140 COM26 4895,200 672,075 230 SEG63 52,200 672,075 141 COM25 4843,400 672,075 231 SEG66 52,200 672,143 COM24 4791,600 672,075 232 SEG65 52,200 672,144 COM22 4688,000 672,075 233 SEG66 104,400 672,144 COM22 4688,000 672,075 233 SEG66 104,400 672,144 COM20 48434,400 672,075 233 SEG66 52,200 672,144 COM20 4843,400 672,075 235 SEG68 208,800 672,144 COM20 4843,400 672,075 235 SEG68 208,800 672,144 COM20 4843,400 672,075 235 SEG69 281,000 672,144 COM20 484,400 672,075 236 SEG69 281,000 672,144 COM18 4480,800 672,075 236 SEG69 281,000 672,144 COM18 4480,800 672,075 237 SEG70 313,200 672,144 COM18 4480,800 672,075 238 SEG69 2469,800 672,145 155 COM16 4377,200 672,075 240 SEG37 525,600 672,075 155 COM16 4375,600 672,075 241 SEG74 574,200 672,075 155 COM11 4118,200 672,075 243 SEG67 678,600 672,075 155 COM11 4118,200 672,075 245 SEG89 381,000 672,075 166 COM0 3548,400 672,075 245 SEG89 3157,200 672,075 166 COM0 3548,400 672,075 258 SEG89 3157,200 672,075 166 COM0 3548,400 672,075 258 SEG89 3157,200 672,075 166 COM0 3548,400 672,075 258 SEG89 3157,200 672,075 166 COM0 3548,400 672,075 259 SEG89									
132									672.075
133	131	DUMMY	5361.800	672.075		221	SEG54	522.000	672.075
133	132	COM34	5309.600	672.075	1	222	SEG55	469.800	672.075
134					1 1				672.075
135					4	-			672.075
136					4				
137 COM/28 S950.600 672.075 227 SEG60 208.800 672.075 138 COM/28 4998.800 672.075 228 SEG61 156.600 672.075 140 COM/26 4895.200 672.075 230 SEG63 52.200 672.075 141 COM/25 4843.400 672.075 230 SEG63 52.200 672.075 142 COM/24 4791.600 672.075 231 SEG64 0.000 672.075 143 COM/23 4739.800 672.075 233 SEG65 -52.200 672.075 143 COM/23 4739.800 672.075 233 SEG66 -104.400 672.075 144 COM/24 4688.000 672.075 233 SEG66 -104.400 672.075 145 COM/24 4688.000 672.075 233 SEG66 -104.400 672.075 145 COM/24 4688.000 672.075 235 SEG68 208.800 672.075 146 COM/20 4584.400 672.075 236 SEG69 -281.000 672.075 148 COM/19 4532.600 672.075 237 SEG70 -313.200 672.075 148 COM/19 4432.000 672.075 238 SEG97 -353.200 672.075 149 COM/16 4377.200 672.075 239 SEG72 4688.000 672.075 150 COM/16 4377.200 672.075 240 SEG73 -522.000 672.075 151 COM/15 4325.400 672.075 241 SEG74 -574.200 672.075 153 COM/13 4221.800 672.075 243 SEG76 -578.600 672.075 154 COM/12 4170.000 672.075 243 SEG76 -578.600 672.075 155 COM/11 4118.200 672.075 243 SEG76 -678.600 672.075 156 COM/10 4066.400 672.075 244 SEG77 -730.800 672.075 156 COM/10 4066.400 672.075 245 SEG98 -835.000 672.075 156 COM/10 3600.200 672.075 247 SEG80 887.400 672.075 166 COM/03 3703.800 672.075 251 SEG88 -391.800 672.075 166 COM/03 3703.800 672.075 252 SEG88 -1300.000 672.075 167 SEG0 3340.800 672.075 252 SEG89 -1409.400 672.075 167 SEG3 3340.800 672.075 258 SEG99 -1409.400 672.075 167 SEG3 3340.800 672.075 252 SEG89 -1357.200 672.075 167 SEG3 SEG90 3340.800 672.075 258 SEG99 -1409.400 672.075 170 SEG3 SEG90 372.000 672.075 258 SEG99 -1409.40									672.075
138		COM30	5102.400	672.075		226	SEG59	261.000	672.075
139	137	COM29	5050.600	672.075	1	227	SEG60	208.800	672.075
139	138	COM28	4998.800	672.075		228	SEG61	156,600	672.075
140					1 1				672.075
141									672.075
142									
143									672.075
144	142	COM24	4791.600	672.075		232	SEG65	-52.200	672.075
144	143	COM23	4739.800	672.075	1	233	SEG66	-104.400	672.075
145	144	COM22	4688.000		1			-156,600	672.075
146					1 1				672.075
147									
148									672.075
149	147	COM19	4532.600	672.075		237	SEG70	-313.200	672.075
150	148	COM18	4480.800	672.075	1	238	SEG71	-365.400	672.075
150	149	COM17	4429.000	672.075		239	SEG72	-469.800	672.075
Tell	150				1 1				672.075
152					- 1				672.075
153									
154		COM14							672.075
154			4221.800		j l				672.075
155	154	COM12	4170.000		1	244	SEG77	-730.800	672.075
156	155	COM11	4118.200	672.075	1	245	SEG78	-783.000	672.075
157					1				672.075
158					1				672.075
159 COMP 3911.000 672.075 249 3EG82 3918.00 672.075 160 COMP 3859.200 672.075 250 SEG83 -1044.000 672.075 161 COMP 3859.200 672.075 251 SEG84 -1096.200 672.075 162 COMP 3857.400 672.075 251 SEG84 -1096.200 672.075 163 COMP 3652.000 672.075 253 SEG86 -1200.600 672.075 253 SEG86 -1200.600 672.075 254 SEG87 -1252.800 672.075 255 SEG88 -1305.000 672.075 255 SEG88 -1305.000 672.075 255 SEG88 -1305.000 672.075 256 SEG99 -1357.200 672.075 257 SEG90 -1409.400 672.075 258 SEG90 -1409.400 672.075 259 SEG92 -1513.800 672.075 259 SEG92 -1513.800 672.075 259 SEG92 -1513.800 672.075 250 SEG93 -1566.000 672.075 250 SEG93 -1567.000 672.075 250 SEG93 -1570.400 672.075 250 SEG93 -1570.400 672.075 250 SEG94 -1774.800 672.075 250 SEG99 -1879.200 672.075 250	157	CONTR		672.075	1		OEG00	-007.400	670.075
160	158	COIVIS	0002.000	0/2.0/5	. 1	0	SEG81	-939.600	0/2.0/5
161					j l				672.075
161	160	COM6	3859.200	672.075	1	250	SEG83	-1044.000	672.075
162	161				1				672.075
163					1				672.075
164 COM/2 3652.000 672.075 254 SEG87 1252.800 672.075 165 COM/1 3600.200 672.075 255 SEG88 -1305.000 672.075 167 SEG0 3340.800 672.075 256 SEG99 -1357.200 672.075 168 SEG1 3288.600 672.075 257 SEG90 -1409.400 672.075 169 SEG2 3236.400 672.075 259 SEG91 -1461.600 672.075 170 SEG3 3184.200 672.075 260 SEG93 -1513.800 672.075 171 SEG4 3132.000 672.075 261 SEG94 -1618.200 672.075 172 SEG5 3079.800 672.075 261 SEG94 -1618.200 672.075 173 SEG6 3027.600 672.075 263 SEG96 -1722.600 672.075 175 SEG8 2923.200 672.075 264 SEG99 -17					1				672.075
165					4 I				
166 COMO 3548.400 672.075 255 SEG89 -1357.200 672. 167 SEG0 3340.800 672.075 257 SEG90 -1409.400 672. 168 SEG1 3288.600 672.075 258 SEG91 -1461.600 672. 169 SEG2 3236.400 672.075 259 SEG92 -1513.800 672. 170 SEG3 3182.200 672.075 260 SEG93 -1566.000 672. 171 SEG4 3132.000 672.075 261 SEG93 -1666.000 672. 172 SEG5 3079.800 672.075 262 SEG93 -1670.400 672. 173 SEG6 3027.600 672.075 263 SEG96 -172.600 672. 174 SEG8 2923.200 672.075 264 SEG99 -1872.000 672. 175 SEG9 2817.000 672.075 266 SEG99 -1879.200 672.<					, 1				672.075
166 COMO 3548.400 672.075 255 SEG89 -1357.200 672. 167 SEG0 3340.800 672.075 257 SEG90 -1409.400 672. 168 SEG1 3288.600 672.075 258 SEG91 -1461.600 672. 169 SEG2 3236.400 672.075 259 SEG92 -1513.800 672. 170 SEG3 3182.200 672.075 260 SEG93 -1566.000 672. 171 SEG4 3132.000 672.075 261 SEG93 -1666.000 672. 172 SEG5 3079.800 672.075 262 SEG93 -1670.400 672. 173 SEG6 3027.600 672.075 263 SEG96 -172.600 672. 174 SEG8 2923.200 672.075 264 SEG99 -1872.000 672. 175 SEG9 2817.000 672.075 266 SEG99 -1879.200 672.<	165	COM1		672.075			SEG88		672.075
167 SEG0 3340.800 672.075 257 SEG90 1409.400 672. 168 SEG1 3286.600 672.075 258 SEG91 -1461.600 672. 170 SEG2 3236.400 672.075 259 SEG92 -1513.800 672. 171 SEG3 3184.200 672.075 260 SEG93 -1566.000 672. 171 SEG5 3079.800 672.075 261 SEG94 -1618.200 672. 173 SEG6 3027.600 672.075 263 SEG95 -170.400 672. 174 SEG7 2975.400 672.075 263 SEG96 -1722.600 672. 175 SEG8 2923.200 672.075 265 SEG98 -1879.200 672. 176 SEG9 2871.000 672.075 266 SEG99 -1879.200 672. 177 SEG10 2818.800 672.075 266 SEG99 -1879.200 672.<	166	COM0	3548.400		1	256	SEG89	-1357.200	672.075
168 SEG1 3288.600 672.075 258 SEG91 -1461.600 672. 169 SEG2 3236.400 672.075 259 SEG92 -1513.800 672. 170 SEG3 3184.200 672.075 260 SEG93 -1566.000 672. 171 SEG4 3132.000 672.075 261 SEG94 -1618.200 672. 173 SEG6 3027.600 672.075 262 SEG95 -1670.400 672. 174 SEG7 2975.400 672.075 263 SEG96 -1722.600 672. 175 SEG8 2923.200 672.075 265 SEG99 -1774.800 672. 176 SEG9 2871.000 672.075 265 SEG99 -1879.200 672. 177 SEG10 2818.800 672.075 267 SEG100 -1931.400 672. 177 SEG11 2766.600 672.075 267 SEG100 -1931.400			3340.800		1	257			672.075
169 SEG2 3236 400 672.075 259 SEG92 -1513.800 672.175 170 SEG3 3184.200 672.075 260 SEG93 -1566.000 672. 171 SEG4 3132.000 672.075 261 SEG93 -1568.000 672. 172 SEG5 3079.800 672.075 262 SEG95 -1670.400 672. 173 SEG6 3027.600 672.075 263 SEG96 -172.260 672. 174 SEG7 2975.400 672.075 264 SEG96 -172.260 672. 175 SEG8 2923.200 672.075 265 SEG99 -1872.000 672. 176 SEG9 2817.000 672.075 266 SEG99 -1879.200 672. 177 SEG10 2818.800 672.075 267 SEG100 -1931.400 672. 178 SEG112 2714.400 672.075 268 SEG101 -1933.600 <t< td=""><td></td><td></td><td></td><td></td><td>1 </td><td></td><td></td><td></td><td>672.075</td></t<>					1				672.075
170 SEG3 3184.200 672.075 260 SEG93 -1566.000 672. 171 SEG4 3132.000 672.075 261 SEG94 -1618.200 672. 172 SEG5 3079.800 672.075 262 SEG95 -1670.400 672. 173 SEG6 3027.600 672.075 263 SEG96 -1722.600 672. 175 SEG8 2923.200 672.075 264 SEG97 -1774.800 672. 176 SEG9 2871.000 672.075 265 SEG98 -1827.000 672. 177 SEG10 2818.800 672.075 266 SEG99 -1879.200 672. 177 SEG10 2818.800 672.075 267 SEG100 -1931.400 672. 178 SEG11 2766.600 672.075 268 SEG101 -1933.600 672. 178 SEG12 2714.400 672.075 269 SEG102 -2035.800 <					4 I				
171 SEG4 3132.000 672.075 261 SEG94 -1618.200 672.175 172 SEG5 3079.800 672.075 262 SEG95 -1670.400 672.175 173 SEG6 3027.600 672.075 263 SEG96 -1722.600 672.175 174 SEG7 2975.400 672.075 263 SEG99 -1774.800 672.175 175 SEG8 2923.200 672.075 265 SEG98 -1827.000 672.175 176 SEG9 2871.000 672.075 265 SEG99 -1879.200 672.175 177 SEG10 2818.800 672.075 267 SEG100 -1931.400 672.075 178 SEG11 2766.600 672.075 268 SEG101 -1933.600 672.175 179 SEG12 2714.400 672.075 269 SEG102 -2035.800 672.205					. I				672.075
172 SEG5 3079.800 672.075 262 SEG95 1670.400 672. 173 SEG6 3027.600 672.075 263 SEG96 1722.600 672. 174 SEG7 2975.400 672.075 264 SEG99 1774.800 672. 175 SEG8 2923.200 672.075 265 SEG98 1827.000 672. 176 SEG9 2817.000 672.075 266 SEG99 1879.200 672. 177 SEG10 2818.800 672.075 267 SEG100 1931.400 672. 178 SEG311 2766.600 672.075 268 SEG101 1-933.600 672. 179 SEG12 2714.400 672.075 269 SEG102 2035.800 672.					j l				672.075
172 SEG5 3079.800 672.075 262 SEG95 1670.400 672. 173 SEG6 3027.600 672.075 263 SEG96 1722.600 672. 174 SEG7 2975.400 672.075 264 SEG99 1774.800 672. 175 SEG8 2923.200 672.075 265 SEG98 1827.000 672. 176 SEG9 2817.000 672.075 266 SEG99 1879.200 672. 177 SEG10 2818.800 672.075 267 SEG100 1931.400 672. 178 SEG311 2766.600 672.075 268 SEG101 1-933.600 672. 179 SEG12 2714.400 672.075 269 SEG102 2035.800 672.	171	SEG4	3132.000	672.075	1 I	261	SEG94	-1618.200	672.075
173 SEG6 3027.600 672.075 263 SEG96 -1722.600 672. 174 SEG7 2975.400 672.075 264 SEG97 -1774.800 672. 175 SEG8 2932.200 672.075 265 SEG98 -1879.200 672. 176 SEG9 2871.000 672.075 266 SEG99 -1879.200 672. 177 SEG10 2818.800 672.075 267 SEG100 -1931.400 672. 178 SEG11 2766.600 672.075 268 SEG101 -1983.600 672. 179 SEG12 2714.400 672.075 269 SEG102 2035.800 672.					1				672.075
174 SEG7 2975.400 672.075 264 SEG97 -1774.800 672. 175 SEG8 2923.200 672.075 265 SEG98 -1827.000 672. 176 SEG9 2871.000 672.075 266 SEG99 -1879.200 672. 177 SEG10 2818.800 672.075 267 SEG100 -1931.400 672. 178 SEG11 2766.600 672.075 268 SEG101 -1933.600 672. 179 SEG12 2714.400 672.075 269 SEG102 -2035.800 672.					1				672.075
175 SEG8 2923.200 672.075 265 SEG98 -1827.000 672. 176 SEG9 2871.000 672.075 266 SEG99 -1879.200 672. 177 SEG10 2818.800 672.075 267 SEG100 -1931.400 672. 178 SEG11 2766.600 672.075 268 SEG101 -1983.600 672. 179 SEG12 2714.400 672.075 269 SEG102 -2035.800 672.					4 I				
176 SEG9 2871.000 672.075 266 SEG99 1879.200 672. 177 SEG10 2818.800 672.075 267 SEG100 -1931.400 672. 178 SEG11 2766.600 672.075 268 SEG101 -1983.600 672. 179 SEG12 2714.400 672.075 269 SEG102 -2035.800 672.					ı l				672.075
177 SEG10 2818.800 672.075 267 SEG100 1-933.400 672. 178 SEG11 2766.600 672.075 268 SEG101 -1933.600 672. 179 SEG32 2714.400 672.075 269 SEG102 2035.800 672.									672.075
177 SEG10 2818.800 672.075 267 SEG100 1-931.400 672. 178 SEG11 2766.600 672.075 268 SEG101 -1983.600 672. 179 SEG32 2714.400 672.075 269 SEG102 2035.800 672.	176	SEG9	2871.000	672.075	1	266	SEG99	-1879.200	672.075
178 SEG11 2766.600 672.075 268 SEG101 -1983.600 672. 179 SEG12 2714.400 672.075 269 SEG102 -2035.800 672.					1	267		-1931.400	672.075
179 SEG12 2714.400 672.075 269 SEG102 -2035.800 672.					1				672.075
					4 I				
180 SEG13 2662.200 672.075 270 SEG103 -2088.000 672.					, 1				672.075
	180	SEG13	2662.200	6/2.075	j l	270	SEG103	-2088.000	672.075

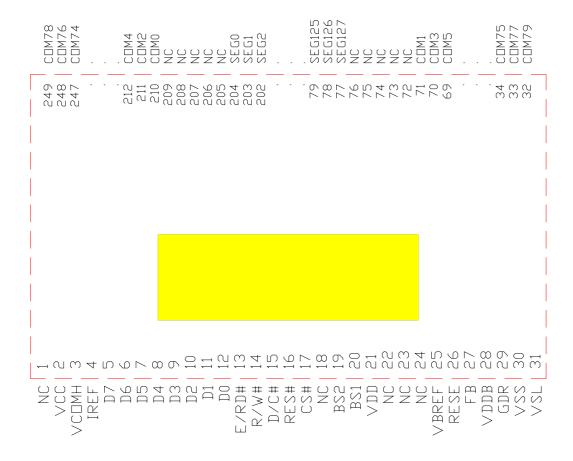
Pad#	Signal	X-pos	Y-pos
271	SEG104	-2140.200	672.075
272	SEG105	-2192.400	672.075
273	SEG106	-2244.600	672.075
274	SEG107	-2296.800	672.075
275	SEG108	-2349.000	672.075
276	SEG109	-2401.200	672.075
277	SEG110	-2453.400	672.075
278	SEG111	-2505.600	672.075
279	SEG112	-2557.800	672.075
280	SEG113	-2610.000	672.075
281	SEG114	-2662.200	672.075
282	SEG115	-2714.400	672.075
283	SEG116	-2766.600	672.075
284	SEG117	-2818.800	672.075
285	SEG118	-2871.000	672.075
286	SEG119	-2923.200	672.075
287	SEG120	-2975.400	672.075
288	SEG121	-3027.600	672.075
289	SEG122	-3079.800	672.075
290	SEG123	-3132.000	672.075
291	SEG124	-3184.200	672.075
292	SEG125	-3236.400	672.075
293	SEG126	-3288.600	672.075
294	SEG127	-3340.800	672.075
295	COM40	-3548.400	672.075
296	COM41	-3600.200	672.075
297	COM42	-3652.000	672.075
298	COM43	-3703.800	672.075
299	COM44	-3755.600	672.075
300	COM45	-3807.400	672.075
301	COM46	-3859.200	672.075
302	COM47	-3911.000	672.075
303	COM48	-3962.800	672.075
304	COM49	-4014.600	672.075
305	COM50	-4066,400	672.075
306	COM51	-4118.200	672.075
307	COM52	-4170.000	672.075
308	COM53	-4221.800	672.075
309	COM54	-4273.600	672.075
310	COM55	-4325,400	672.075
311	COM56	-4377.200	672.075
312	COM57	-4429.000	672.075
313	COM58	-4480.800	672.075
314	COM59	-4532.600	672.075
315	COM60	-4584.400	672.075
316	COM61	-4636,200	672.075
317	COM62	-4688.000	672.075
318	COM63	-4739.800	672.075
319	COM64	-4791.600	672.075
320	COM65	-4843.400	672.075
321	COM66	-4895.200	672.075
322	COM67	-4947.000	672.075
323	COM68	-4998.800	672.075
324	COM69	-5050.600	672.075
325	COM70	-5102.400	672.075
326	COM71	-5154.200	672.075
327	COM72	-5206.000	672.075
	COM73	-5257.800	672.075
			312.013
328 329	COMZ	-5309 600	672 075
328 329 330	COM74 DUMMY	-5309.600 -5361.800	672.075 672.075

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6 PIN ARRANGEMENT

6.1 SSD1325T6R1 pin assignment

Figure 4: SSD1325T6R1 Pin Assignment



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Table 3: SSD1325T6R1 TAB Pin assignment Table

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN N
1	NC VCC	81	SEG123 SEG122	161	SEG43	241	CO.
2	VCC	82	SEG122 SEG121	162	SEG42 SEG41	242	CO
3	IREF	83 84	SEG121	163 164	SEG41	243 244	CO
5	D7	85	SEG119	165	SEG39	245	CO
6	D6	86	SEG118	166	SEG38	246	CO
7	D5	87	SEG117	167	SEG37	247	CO
8	D4 D3	88	SEG116 SEG115	168	SEG36 SEG35	248	CO
10	D2	89 90	SEG113	169 170	SEG33	249	CO
11	D1	90	SEG113	170	SEG33	ł	
12	D0	92	SEG112	172	SEG32	1	
13	E/RD#	93	SEGIII	173	SEG31	1	
14	R/W#	94	SEG110	174	SEG30		
15	D/C# RES#	95	SEG109 SEG108	175	SEG29 SEG28	Į.	
16 17	CS#	96 97	SEG108	176 177	SEG28	ł	
18	NC NC	98	SEG106	178	SEG26	ł	
19	BS2	99	SEG105	179	SEG25	1	
20	BS1	100	SEG104	180	SEG24]	
21	VDD	101	SEG103	181	SEG23		
22	NC NC	102	SEG102 SEG101	182	SEG22 SEG21	ł	
23 24	NC NC	103 104	SEG101	183 184	SEG21	ł	
25	VBREF	105	SEG99	185	SEG19	1	
26	RESE	106	SEG98	186	SEG18	1	
27	FR	107	SEG97	187	SEG17	I	
28	VDDB GDR	108	SEG96	188	SEG16	I	
29 30	VSS	109 110	SEG95 SEG94	189 190	SEG15 SEG14	ł	
31	VSL	111	SEG93	190	SEG14 SEG13	ł	
32	COM79	112	SEG92	192	SEG12	1	
33	COM77	113	SEG91	193	SEG11	1	
34	COM75	114	SEG90	194	SEG10]	
35	COM73	115	SEG89 SEG88	195	SEG9 SEG8		
36 37	COM/1 COM/69	116 117	SEG88	196 197	SEG7	ł	
38	COV67	118	SEG86	198	SEG6	ł	
39	COM65	119	SEG85	199	SEG5	1	
40	COM63	120	SEG84	200	SEG4	1	
41	COM61	121	SEG83	201	SEG3	ļ	
42 43	COM59 COM57	122 123	SEG82 SEG81	202 203	SEG2 SEG1	Į.	
43	COM55	123	SEG80	203	SEG0	ł	
45	COM53	125	SEG79	205	NC	1	
46	COM51	126	SEG78	206	NC]	
47	COM49	127	SEG77	207	NC		
48	COM7	128	SEG76 SEG75	208	NC NC		
49 50	COM45 COM43	129 130	SEG73	209 210	COM0	ł	
51	COV#3	131	SEG73	211	COM2	1	
52	COMB9	132	SEG72	212	COM4	1	
53	COMB7	133	SEG71	213	COM6]	
54	COMB5	134	SEG70	214	COM8 COM10	ļ	
55 56	COMB3 COMB1	135	SEG69 SEG68	215 216	COM10 COM12	ł	
57	COM29	136 137	SEG67	217	COM12	l	
58	COM27	138	SEG66	218	COM16	1	
59	COM25	139	SEG65	219	COM18]	
60	COM23	140	SEG64	220	COM20	I	
61	COM21	141	SEG63 SEG62	221	COM22 COM24	ł	
62 63	COM19 COM17	142 143	SEG62 SEG61	222 223	COM24	ł	
64	COM15	144	SEG60	224	COM28	1	
65	COM13	145	SEG59	225	COM30	1	
66	COM11	146	SEG58	226	COM32	I	
67	COM9	147	SEG57	227	COM34	I	
68 69	COM5	148 149	SEG56 SEG55	228 229	COM36 COM38	ł	
70	COMB	150	SEG55	230	COM40	ł	
70	COMI	151	SEG53	231	COM42	1	
72	NC NC	152	SEG52	232	COM44	1	
73	NC	153	SEG51	233	COM46	I	
74	NC NC	154	SEG50	234	COM48	I	
75 76	NC NC	155 156	SEG49 SEG48	235 236	COM50 COM52	ł	
76	SEG127	156 157	SEG48 SEG47	236	COM54	ł	
78	SEG126	158	SEG46	238	COM56	i	
79	SEG125	159	SEG45	239	COM58]	
80	SEG124	160	SEG44	240	COM60	J	

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7 PIN DESCRIPTION

Key:

I = Input	NC = Not Connected
O = Output	Pull LOW = Connect to Ground
IO = Bi-directional (input/output)	Pull HIGH = Connect to V_{DD}
P = Power pin	

Table 4: Pin Descriptions

Pin Name	Pin Type	Description								
RES#	I	This pin is reset signal input. When the pin is LOW, initialization of the chip is executed. Keep this pin HIGH during normal operation.								
CS#	I	This pin is the CCS# is pulled L		lect input. The chip	is enabled for MC	CU communication	only when			
D/C#	I	This pin is Data/Command control pin. When the pin is pulled HIGH, the data at D[7:0] is treated as data. When the pin is pulled LOW, the data at D[7:0] will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams in Figure 34 to Figure 37.								
E (RD#)	I	pin will be used pulled HIGH ar When connecting	This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled LOW and the chip is selected.							
R/W# (WR#)	I	This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode will be carried out when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected.								
D[7:0]	IO	These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK.								
BS[2:0]	Ι	These pins are l	MCU I	ous interface select	ion.					
		Table 5 : Bus I	Interfa	ce selection						
				6800-parallel interface (8 bit)	8080-parallel interface (8 bit)	Serial interface				
			3S0	0	0	0				
			3S1	0	1	0				
		B	3S2	1	1	0				
		Note $^{(1)}$ 0 is connected to V_{SS} $^{(2)}$ 1 is connected to V_{DD}								
V _{DD}	P	This is a power supply pin. It must be connected to external source.								
V _{SS}	P	This is a ground pin. It also acts as ground reference for the logic pins. It must be connected to external ground.								
CL	Ю			clock input. When						

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Pin Name	Pin Type	Description
		clock is enabled (i.e. CLS is pulled HIGH), this pin should be kept NC and left open.
CLS	I	This is the internal clock enable pin. When this pin is pulled HIGH, internal oscillator is selected. The internal clock will be disabled when it is pulled LOW, an external clock source must be connected to CL pin for normal operation.
V _{CC}	P	This pin is the most positive voltage supply of the chip. It is supplied by external high voltage source.
V _{COMH}	P	A capacitor should be connected between this pin and $V_{\rm SS}$. No external power supply is allowed to connect to this pin.
I_{REF}	I	This pin is the segment output current reference pin. I_{SEG} is derived from I_{REF} . A resistor should be connected between this pin and V_{SS} to maintain the current around 10uA.
COM0 ~ COM79	О	These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is OFF.
SEG0 ~ SEG127	О	These pins provide the OLED segment driving signals. These pins are in high impedance state when display is OFF.
V_{REF}	P	This pin is the voltage reference for the pre-charge voltage in driving OLED device. Voltage should be set matching with the OLED driving voltage in the current drive phase. It can be either supplied externally or connected to V_{CC} .
VCL	О	This is the output pin for the voltage output low level for COM signals. This pin should be connected to $V_{\text{SS.}}$
VSL	О	This is the output pin for the voltage output low level for SEG signals. This pin can be kept NC or connected with a capacitor to V_{SS} for stability. Refer to command BFh for VSL pin connection details.
VSLCAP	0	This is a reserved pin. It has to be kept NC and left open.
M/S#	I	This pin is an input pin and must be pulled HIGH to enable the chip function.
VDDB	P	This is a reserved pin. It should be connected to V_{DD} .
VSSB	P	This is a reserved pin. It should be connected to V_{SS} .
GDR	0	This is a reserved pin. It should be kept NC.
RESE	I	This is a reserved pin. It should be kept NC.
FB	I	This is a reserved pin. It should be kept NC.
VBREF	I	This is an internal voltage reference pin. It should be kept NC and left open.
FR	-	It is No Connection pin. It should be kept NC and left open.
DOF#	-	It is No Connection pin. It should be kept NC and left open.
GPIO0	IO	This is a reserved pin. It should be kept NC and left open.
GPIO1	IO	This is a reserved pin. It should be kept NC and left open.
<u> </u>		1

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Pin Name	Pin Type	Description
TR[8:0]	-	This is a reserved pin. It should be kept NC and left open.
ICAS	-	This is a reserved pin. It should be kept NC and left open.

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8 FUNCTIONAL BLOCK DESCRIPTIONS

8.1 MPU Interface selection

SSD1325 MCU interface consist of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 6. Different MCU mode can be set by hardware selection on BS[2:0] pins (please refer to Table 5 for BS[2:0] setting).

Table 6: MCU interface assignment under different bus interface mode

	Data/	ata/Command Interface							Control Signal				
Bus Interface	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W#	CS#	D/C#	RES#
8-bit 8080		D[7:0]						RD#	WR#	CS#	D/C#	RES#	
8-bit 6800		D[7:0]							Е	R/W#	CS#	D/C#	RES#
SPI	Tie LO	OW				NC	SDIN	SCLK	Tie LC	W	CS#	D/C#	RES#

8.1.1 MPU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation. A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write. The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

Table 7: Control pins of 6800 interface

Function	\mathbf{E}	R/W#	CS#	D/C#
Write command	\downarrow	L	L	L
Read status	\downarrow	Н	L	L
Write data	\downarrow	L	L	Н
Read data	\downarrow	Н	L	Н

Note

L stands for LOW in signal

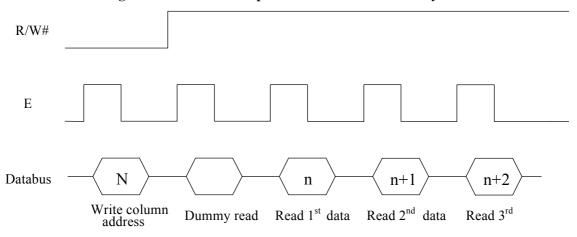
In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 5.

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<sup>(1)

↓</sup> stands for falling edge of signal H stands for HIGH in signal

Figure 5: Data read back procedure - insertion of dummy read



8.1.2 MPU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write. A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW. A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 6: Example of Write procedure in 8080 parallel interface mode

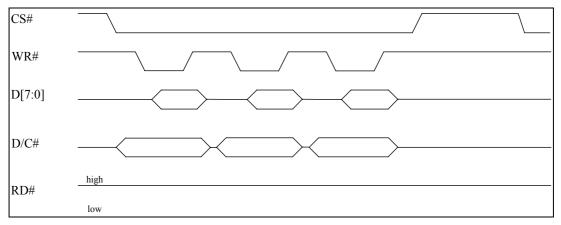
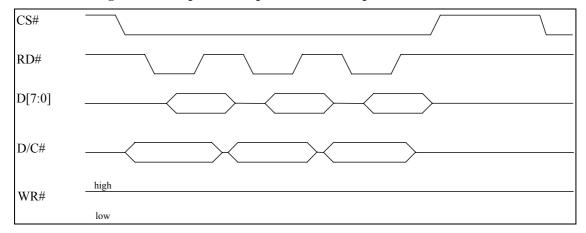


Figure 7: Example of Read procedure in 8080 parallel interface mode



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Table 8: Control pins of 8080 interface (Form 1)

Function	RD#	WR#	CS#	D/C#
Write command	Н	↑	L	L
Read status	↑	Н	L	L
Write data	Н	↑	L	Н
Read data	↑	Н	L	Н

Note

Alternatively, RD# and WR# can be keep stable while CS# serves as the data/command latch signal.

Table 9: Control pins of 8080 interface (Form 2)

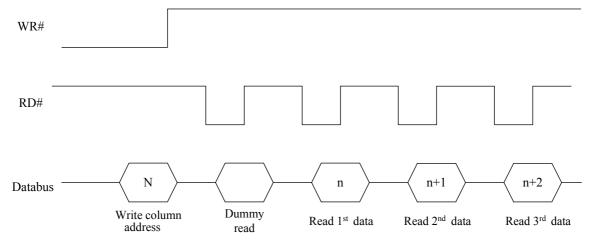
Function	RD#	WR#	CS#	D/C#
Write command	Н	L	1	L
Read status	L	Н	1	L
Write data	Н	L	↑	Н
Read data	L	Н	↑	Н

Note

- (1) ↑ stands for rising edge of signal
- (2) H stands for HIGH in signal
- (3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8.

Figure 8: Display data read back procedure - insertion of dummy read



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^{(1) ↑} stands for rising edge of signal

⁽²⁾ H stands for HIGH in signal

⁽³⁾ L stands for LOW in signal

⁽⁴⁾ Refer to Figure 35 for Form 1 8080-Series MPU Parallel Interface Timing Characteristics

⁽⁴⁾ Refer to Figure 36 for Form 2 8080-Series MPU Parallel Interface Timing Characteristics

8.1.3 MPU Serial Interface

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, E and R/W# can be connected to an external ground.

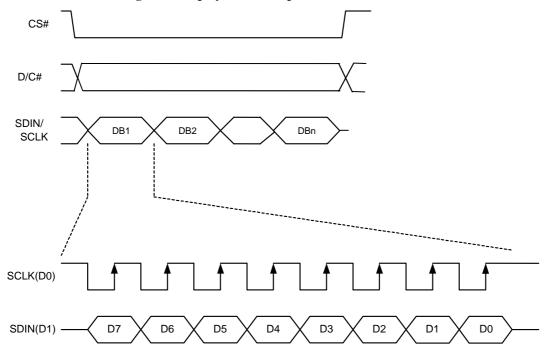
Table 10: Control pins of Serial interface

Function	E	R/W#	CS#	D/C#
Write command	Tie LOW	Tie LOW	L	L
Write data	Tie LOW	Tie LOW	L	Н

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

Figure 9: Display data write procedure in SPI mode



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8.2 Segment Drivers/Common Drivers

Segment drivers have 128 current sources to drive OLED panel. The driving current can be adjusted from 0 to 300uA with 7 bits, 128 steps. Common drivers generate voltage scanning pulses. The block diagrams and waveforms of the segment and common driver are shown as follow.

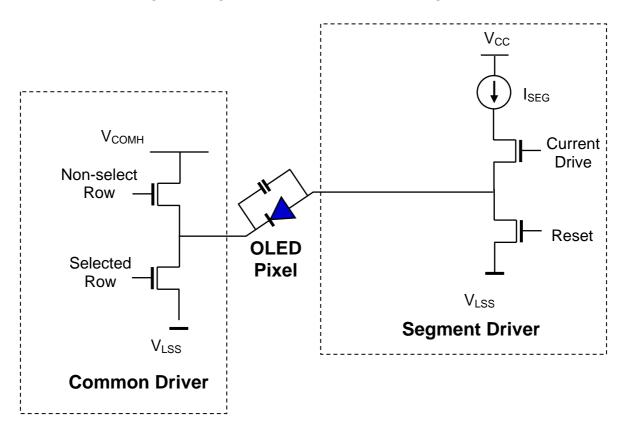


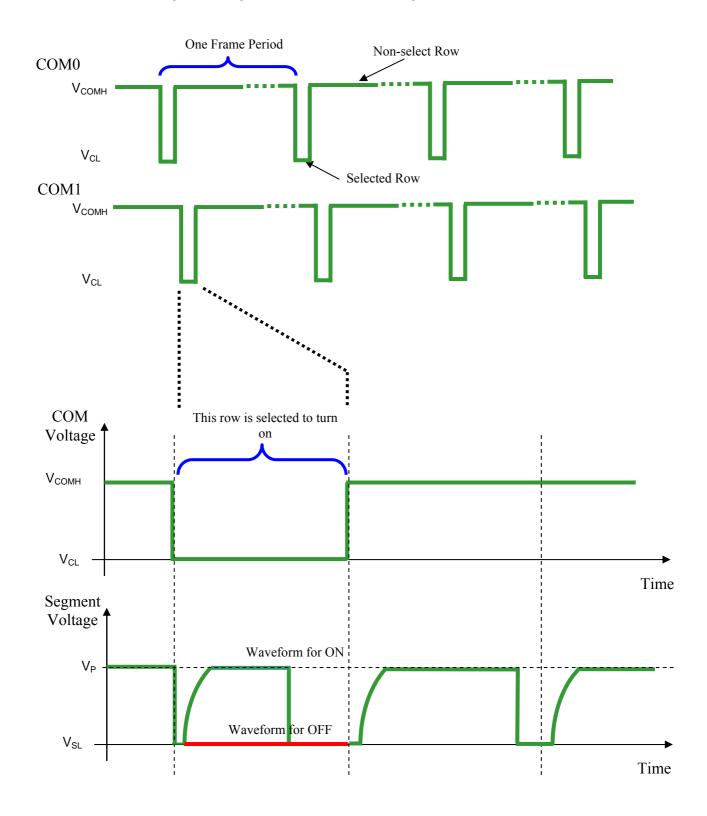
Figure 10 : Segment and Common Driver Block Diagram

The commons are scanned sequentially, row by row. If a row is not selected, all the pixels on the row are in reverse bias by driving those commons to voltage V_{COMH} as shown in Figure 11.

In the scanned row, the pixels on the row will be turned ON or OFF by sending the corresponding data signal to the segment pins. If the pixel is turned OFF, the segment current is kept at 0. On the other hand, the segment drives to I_{SEG} when the pixel is turned ON.

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Figure 11: Segment and Common Driver Signal Waveform



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There are three phases to driving an OLED a pixel. In phase 1, the pixel is reset by the segment driver to V_{SS} in order to discharge the previous data charge stored in the parasitic capacitance along the segment electrode. The period of phase 1 can be programmed by command B1h A[3:0] from 1 to 15 DCLK. An OLED panel with larger capacitance requires a longer period for discharging.

In phase 2, pre-charge is performed. The pixel is driven to attain the corresponding voltage level V_P from V_{SS} . The amplitude of V_P can be programmed by the command BCh. The period of phase 2 can be programmed in length from 1 to 15 DCLK by command B1h A[7:4]. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.

Last phase (phase 3 is current drive stage. The current source in the segment driver delivers constant current to the pixel. The driver IC employs PWM (Pulse Width Modulation) method to control the gray scale of each pixel individually. The wider pulse widths in the current drive stage results in brighter pixels and vice versa. This is shown in the following figure.

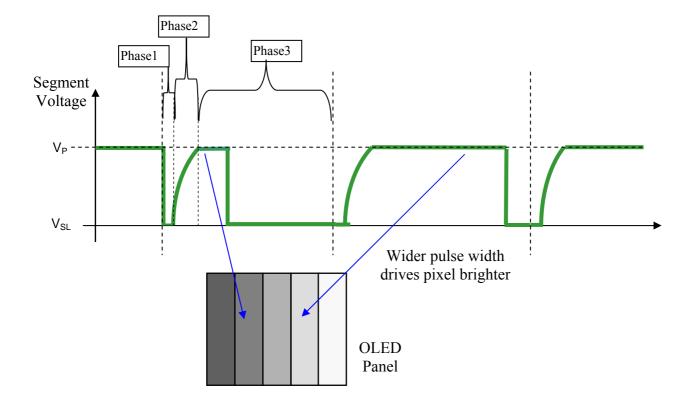


Figure 12: Gray Scale Control by PWM in Segment

After finishing phase 3, the driver IC will go back to phase 1 to display the next row image data. This three-step cycle is run continuously to refresh image display on OLED panel.

The pulse width, which is counted from Phase 2 to Phase 3, is defined by command B8h "Set Gray Scale Table". In the table, the gray scale is defined in incremental way, with reference to the length of previous table entry.

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8.3 Oscillator Circuit and Display Time Generator

This module is an On-Chip low power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled HIGH, internal oscillator is chosen and CL should be left open. Pulling CLS pin LOW disables internal oscillator and external clock must be connected to CL pins for proper operation. When the internal oscillator is selected, its output frequency F_{OSC} can be changed by command B3h, please refer to Table 18.

Internal
Oscillator
Fosc

M
U
X

Divider

Display
Clock

Figure 13: Oscillator Circuit

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor "D" can be programmed from 1 to 16 by command B3h

CLS

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula.

$$F_{FRM} = \frac{F_{osc}}{D \times K \times No. \text{ of } Mux}$$

where

- D stands for clock divide ratio. It is set by command B3h A[3:0]. The divide ratio has the range from 1 to 16
- K is row period. It is configured by command B2h. This value should comply with following condition.

$$K \ge Phase 1 + Phase 2 + Phase 3 + GS15$$

- Number of multiplex ratio is set by command A8h. The power ON reset value is 4Fh.
- F_{OSC} is the oscillator frequency. It can be changed by command B3h A[7:4]. The higher the register setting results in faster frequency.

If the frame frequency is set too low, flickering may occur. On the other hand, higher frame frequency leads to higher power consumption on the whole system.

8.4 Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is HIGH, the input at D_7 - D_0 is written to Graphic Display Data RAM (GDDRAM). If it is LOW, the input at D_7 - D_0 is interpreted as a Command which will be decoded and be written to the corresponding command register.

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8.5 Reset Circuit

When RES# input is LOW, the chip is initialized with the following status:

- 1. Display is OFF
- 2. 128 x 80 Display Mode
- 3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
- 4. Shift register data clear in serial interface
- 5. Display start line is set at display RAM address 0
- 6. Column address counter is set at 0
- 7. Normal scan direction of the COM outputs
- 8. Contrast control register is set at 40h

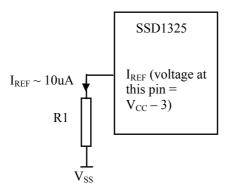
8.6 Current Control and Voltage Control

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

- V_{DD} is an external voltage supply.
- V_{CC} is the most positive external voltage supply.
- V_{COMH} is the Common deselected level. It is internally regulated.
- V_{SS} is the ground path of the analog and panel current.
- I_{REF} is a reference current source for segment current drivers I_{SEG}.

Note that V_{REF} is reference voltage, which is used to derive driving voltage for segments and commons. The magnitude of I_{REF} is controlled by the value of resistor, which is connected between I_{REF} pin and Vss as shown in Figure 14. It is recommended to set I_{REF} to 10uA+/-2uA so as to achieve $I_{SEG} = 300uA$ at maximum contrast 127.

Figure 14: I_{REF} Current Setting by Resistor Value



Since the voltage at I_{REF} pin is $V_{CC} - 3V$, the value of resistor R1 can be found as below. R1 = (Voltage at $I_{REF} - V_{SS}$) / $I_{REF} = (V_{CC} - 3)$ / $10uA \approx 910k\Omega$ for $V_{CC} = 12V$.

8.7 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x80x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. The GDDRAM address maps in

Table 11 to Table 15 show some examples on using the command "Set Re-map" A0h to re-map the GDDRAM. In the following tables, the lower nibble and higher nibble of D0, D1, D2 ... D5117, D5118, D5119 represent the 128x80 data bytes in the GDDRAM.

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Table 11 shows the GDDRAM map under the following condition:

- Command "Set Re-map" A0h is set to:
 - Disable Column Address Re-map
 Disable Nibble Re-map
 Enable Horizontal Address Increment
 Disable COM Re-map
 (A[0]=0)
 (A[1]=0)
 (A[2]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 ... D5119

Table 11: GDDRAM address map 1

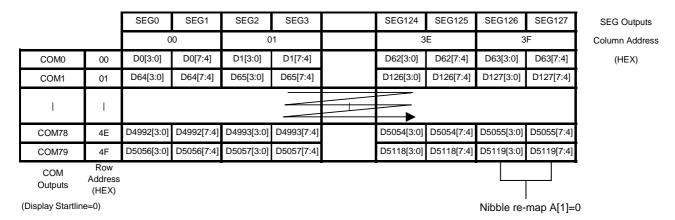


Table 12 shows the GDDRAM map under the following condition:

- Command "Set Re-map" A0h is set to:
 - Disable Column Address Re-map (A[0]=0)
 Disable Nibble Re-map (A[1]=0)
 Enable Vertical Address Increment (A[2]=1)
 Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 ... D5119

Table 12: GDDRAM address map 2

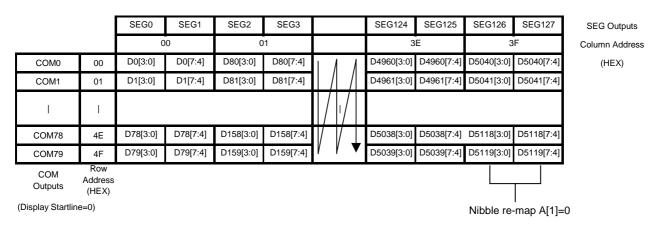


Table 13 shows the GDDRAM map under the following condition:

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- Command "Set Re-map" A0h is set to:
 - Enable Column Address Re-map (A[0]=1)
 Enable Nibble Re-map (A[1]=1)
 Enable Horizontal Address Increment (A[2]=0)
 Disable COM Re-map (A[4]=0)
- Display Start Line=00h

(Display Startline=0)

Data byte sequence: D0, D1, D2 ... D5119

SEG1 SEG124 SEG125 SEG0 SEG2 SEG3 SEG126 SEG127 SEG Outputs 3F ററ Column Address D63[7:4] D63[3:0] D62[7:4] D62[3:0] D1[7:4] D1[3:0] D0[7:4] D0[3:0] COM0 00 (HEX) D127[3:0] D65[3:0] D64[3:0] D127[7:4] D126[7:4] D126[3:0] D65[7:4] D64[7:4] COM1 01 D5055[7:4] D5055[3:0] D5054[7:4] D5054[3:0] D4993[7:4] D4993[3:0] D4992[7:4] D4992[3:0 COM78 4E COM79 4F D5119[7:4] D5119[3:0] D5118[7:4] D5118[3:0] D5057[7:4] D5057[3:0] D5056[7:4] D5056[3:0 Row COM Address Outputs (HEX)

Table 13: GDDRAM address map 3

For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

Nibble re-map A[1]=1

Table 14 shows the example in which the display start line register is set to 10h with the following condition:

- Command "Set Re-map" A0h is set to:
 - Disable Column Address Re-map (A[0]=0)
 Disable Nibble Re-map (A[1]=0)
 Enable Horizontal Address Increment (A[2]=0)
 Enable COM Re-map (A[4]=1)
- Display Start Line=10h (corresponds to COM15)
- Data byte sequence: D0, D1, D2 ... D5119

Table 14: GDDRAM address map 4

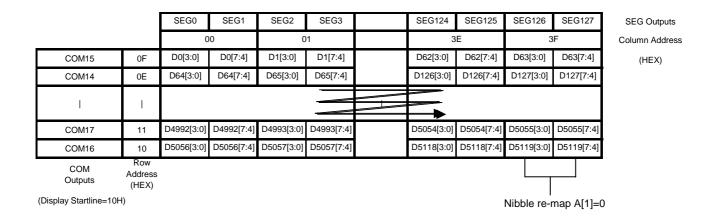


Table 15 shows the GDDRAM map under the following condition:

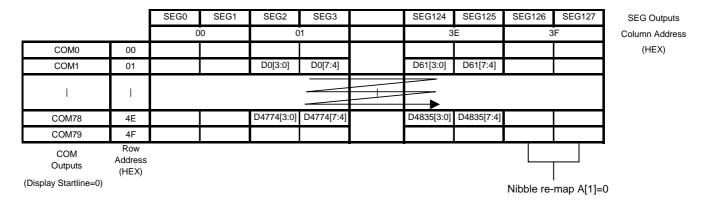
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• Command "Set Re-map" A0h is set to:

Disable Column Address Re-map
(A[0]=0)
Disable Nibble Re-map
(A[1]=0)
Enable Horizontal Address Increment
(A[2]=0)
Disable COM Re-map
(A[4]=0)

- Display Start Line=00h
- Column Start Address=01h
- Column End Address=3Eh
- Row Start Address=01h
- Row End Address=4Eh
- Data byte sequence: D0, D1, D2 ... D4835

Table 15: GDDRAM address map 5



Note

8.8 Gray Scale Decoder

There are 16 gray levels from GS0 to GS15. The gray scale of the display is defined by the pulse width (PW) of current drive phase, GS0 has no pre-charge (phase 2) and no current drive (phase 3). Each L value represents an offset to the corresponding gray scale level. See below table and graphical representation:

Table16: Gray scale pulse width set table

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^{(1]} Please refer to Table 18 for the details of setting command "Set Re-map" A0h.

⁽²⁾ The "Display Start Line" is set by the command "Set Display Start Line" A1h and please refer to Table 18 for the setting details

⁽³⁾ The "Column Start/End Address" is set by the command "Set Column Address" 15h and please refer to Table 18 for the setting details

⁽⁴⁾ The "Row Start/End Address" is set by the command "Set Row Address" 75h and please refer to Table 18 for the setting detail

	Description	Number of DCLKs
L1	Set GS1 level Pulse Width	0-7
L2	Set GS2 level Pulse Width Offset	1-8
L3	Set GS3 level Pulse Width Offset	1-8
•	•	•
•	•	•
•	•	•
L13	Set GS13 level Pulse Width Offset	1-8
L14	Set GS14 level Pulse Width Offset	1-8
L15	Set GS15 level Pulse Width Offset	1-8

DCLK: Internal Display Clock. It is used for defining phase clock period.

Figure 15: Gray scale pulse width set diagram

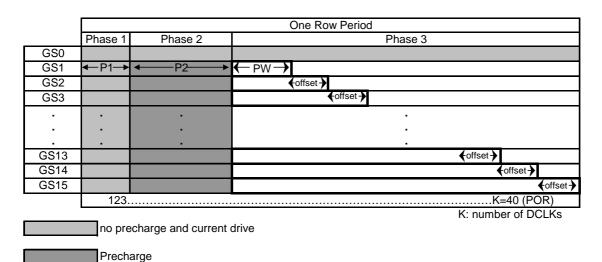


Table 17: Gray scale pulse width default values

Current Drive

RESET	Result
L1=1	GS1 level Pulse width=1
L2=1	GS2 level Pulse width=3
L3=1	GS3 level Pulse width=5
L4=1	GS4 level Pulse width=7
L5=1	GS5 level Pulse width=9
L6=1	GS6 level Pulse width=11
L7=1	GS7 level Pulse width=13
L8=1	GS8 level Pulse width=15
L9=1	GS9 level Pulse width=17
L10=1	GS10 level Pulse width=19
L11=1	GS11 level Pulse width=21
L12=1	GS12 level Pulse width=23
L13=1	GS13 level Pulse width=25
L14=1	GS14 level Pulse width=27
L15=1	GS15 level Pulse width=29

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8.9 Power ON and OFF sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1325. Power ON sequence:

- 1. Power ON V_{DD}.
- 2. After V_{DD} become stable, set RES# pin LOW (logic LOW) for at least 3us $(t_1)^{(4)}$ and then HIGH (logic HIGH).
- 3. After set RES# pin LOW (logic LOW), wait for at least 3us (t₂). Then Power ON V_{CC.}⁽¹⁾
- 4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}) .

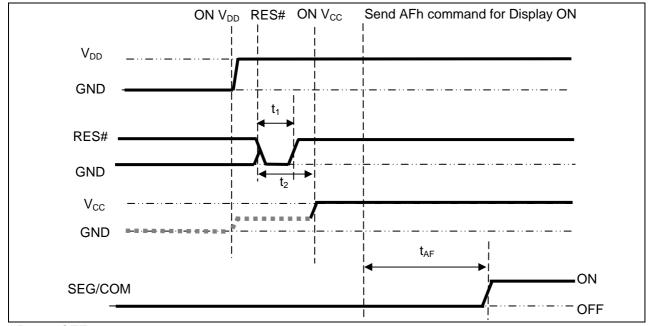


Figure 16: The Power ON sequence

Power OFF sequence:

- 1. Send command AEh for display OFF.
- 2. Wait until panel discharges completely. 3. Power OFF $V_{CC.}^{(1),(2),(3)}$
- 4. Wait for t_{OFF}. Power OFF V_{DD}. (where Minimum t_{OFF}=0ms ⁽⁵⁾ Typical t_{OFF}=100ms)

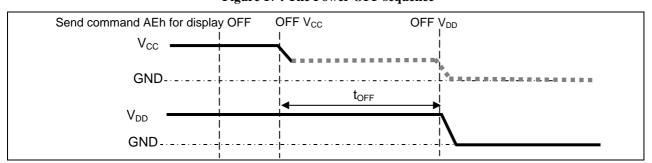


Figure 17: The Power OFF sequence

Note:

- $^{(1)}$ Since an ESD protection circuit is connected between V_{DD} and V_{CC} , V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 16 and Figure 17.
- ⁽²⁾V_{CC} should be kept float (disable) when it is OFF.
- (3) Power Pins (V_{DD} , V_{CC}) can never be pulled to ground under any circumstance.
- (4) The register values are reset after t₁.
- ⁽⁵⁾ V_{DD} should not be Power OFF before V_{CC} Power OFF.

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9 COMMAND TABLE

Table 18: Command Table

(D/C# = 0, R/W# (WR#) = 0, E (RD#) = 1) unless specific setting is stated

Fund	Fundamental Command Table										
D/C						D3	D2	D 1	D 0	Command	Description
0	15	0	0	0	1	0	1	0			Second command A[5:0] sets the column start address
0	A[5:0]	*	*	A_5	_	A_3	A_2	_			from 0-63, POR = 00h
0	B[5:0]	*	*	B ₅	B_4	B ₃	B_2	B_1	B_0		Third command B[5:0] sets the column end address from 0-63, RESET = 3Fh
0	75	0	1	1	1	0	1	0	1	Set Row address	Second command A[6:0]sets the row start address from
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	\mathbf{A}_1			0-79, RESET = 00h
0	B[6:0]	*	B ₆	B ₅	B ₄	B ₃	B_2	B_1	B_0		Third command B[6:0] sets the row end address from 0-79, RESET = 4Fh
0	81	1	0	0	0	0	0	0	1		Double byte command to select 1 out of 128 contrast
0	A[6:0]	*	A_6	A_5	A_4	A_3	\mathbf{A}_{2}	A_1	A_0		steps. Contrast increases as level increase
											The level is set to 40h after RESET
0	84~86	1	0	0	0	0	1	X_1	X_0	Set Current Range	84h = Quarter Current Range (RESET)
											85h = Half Current Range
											86h = Full Current Range
0	A0	1	0	1	0	0	0	0	0	Set Re-map	A[0]=0, Disable Column Address Re-map (RESET)
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	\mathbf{A}_1	A_0		A[0]=1, Enable Column Address Re-map
											A[1]=0, Disable Nibble Re-map (RESET)
											A[1]=1, Enable Nibble Re-map
											A[2]=0, Horizontal Address Increment (RESET)
											A[2]=1, Vertical Address Increment
											A[4]=0, Disable COM Re-map disable (RESET)
											A[4]=1, Enable COM Re-map
											A[5]=0, Reserved (RESET)
											A[5]=1, Reserved
											A[6]=0, Disable COM Split Odd Even (RESET)
											A[6]=1, Enable COM Split Odd Even
0	A1	1	0	1	0	0	0	0	1		Set display RAM display start line register from 0-79
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	\mathbf{A}_1	A_0		Display start line register is reset to 00h after RESET
0	A2	1	0	1	0	0	0	1	0	Set Display Offset	Set vertical scroll by COM from 0-79
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		The value is reset to 00H after RESET

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Fund	ndamental Command Table										
D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	A4~A7	1	0	1	0	0	X_2	X_1	X_0	Set Display Mode	A4h = Normal Display (RESET)
											A5h = Entire Display ON, all pixels turns ON in GS level 15
											A6h = Entire Display OFF, all pixels turns OFF
											A7h = Inverse Display
0	A8 A[6:0]	1	0 A_6	1 A ₅	0 A_4	1 A ₃	0 A_2	0 A_1		Set Multiplex Ratio	The next command determines multiplex ratio N from 16MUX-80MUX,
											A[6:0] = 15 represents 16MUX A[6:0] = 16 represents 17MUX
											A[6:0] = 78 represents 79MUX A[6:0] = 79 represents 80MUX
0 0	AD A[1:0]	1 *	0	1 *	0	1 *	1 *	0		Set Master Configuration	$A[0] = 0$, Select external V_{CC} supply $A[0] = 1$, Reserved (RESET)
											Note (1) Bit A[0] must be set to 0b after RESET. (2) The setting will be activated after issuing Set Display ON command (AFh)
0	AE	1	0	1	0	1	1	1	0	Set Display ON	AEh = Display OFF (Sleep mode) (RESET)
0	AF	1	0	1	0	1	1	1	1	Set Display OFF	AFh = Display ON
0	В0	1	0	1	1	0	0	0		Set Pre-charge Compensation Enable	A[5:0] = 08h (RESET)
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1			A[5:0] = 28h, Enable pre-charge compensation
0	B1 A[3:0]	1 *	0	1 *	1	0 A ₃	0 A ₂	0 A ₁		Set Phase Length	A[3:0] = P1, phase 1 period of 1-15 DCLKs, RESET = 3DCLKS = 3h
0		A_7	A_6	A_5	A_4	*	*	*	*		A[7:4] = P2, phase 2 period of 1-15 DCLKs, RESET = 5DCLKS = 5h
											Note (1) 0 DCLK is invalid in phase 1 & phase 2
0 0	B2 A[7:0]	1 A ₇	0 A ₆	1 A ₅	1 A ₄	0 A ₃	0 A ₂	1 A ₁		(cov mano moquency)	The next command sets the number of DCLKs, K, per row between 2-158 DCLKS RESET = 37DCLKS = 25h The K value should be set as K = P1+P2+GS15 pulse width (RESET: 3+5+29DCLKS)

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Fund	ndamental Command Table										
D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D 0	Command	Description
0	В3	1	0	1	1	0	0	1	1	Set Display Clock	The lower nibble (A[3:0]) of the next command defines
0	A[3:0]	*	*	*	*	A_3	A_2	A_1	A_0	Divide Ratio /	the divide ratio (D) of display clock (DCLK)
0	A[7:4]	A_7	A_6	A_5	A_4	*	*	*	*	Oscillator Frequency	Divide ratio (D)=A[3:0]+1
	[]	,	0		7						(A[3:0]RESET is 0001b, i.e. divide ratio (D) = 2)
											The higher nibble (A[7:4]) of the next command sets the Oscillator Frequency
											Oscillator Frequency increases with the value of A[7:4] and vice versa
											Range: 0000b~1111b
											RESET= 0100b represents 655KHz,
											typical step value: 5% of previous value
	D4	1	0	1	1	0	1	0	0	Cat Dua alamaa	A[2.0] = 0 (DECET)
0	В4	1	U	1	1	0	1	U	U	Set Pre-charge	A[2:0] = 0 (RESET)
0	A[2:0]	*	*	*	*	*	A_2	A_1	A_0	Compensation Level	A[2:0] = 3h, Recommended level
0	В8	1	0	1	1	1	0	0	0	Set Gray Scale Table	The next eight bytes of command set the gray scale level
0	A[2:0]	*	*	*	*	*	A_2	A_1	A_0		of GS1-15 as below:
0	B[2:0]	*	*	*	*	*	B_2	B_1	B_0		A[2:0] = Gray scale level of GS1, RESET=1
0	B[6:4]	*	B_6	B_5	B_4	*	*	*	*		B[2:0] = Gray scale level of GS2, RESET=1
0	C[2:0]	*	*	*	*	*	C_2	C_1	C_0		B[6:4] = Gray scale level of GS3, RESET=1
0	C[6:4]	*	C_6	C_5	C_4	*	*	*	*		C[2:0] = Gray scale level of GS4_RESET=1
0	D[2:0]	*	*	*	*	*	D_2	D_1	D_0		C[6:4] = Gray scale level of GS5, RESET=1 D[2:0] = Gray scale level of GS6, RESET=1
0	D[6:4]	*	D_6	D_5	D_4	*	*	*	*		D[6:4] = Gray scale level of GS7, RESET=1
0	E[2:0]	*	*	*	*	*	E_2	E_1	E ₀		E[2:0] = Gray scale level of GS8, RESET=1
0	E[6:4]	*	E_6	E_5	E_4	*	*	*	*		E[6:4] = Gray scale level of GS9, RESET=1
0	F[2:0]	*	*	*	*	*	F_2	F_1	F_0		F[2:0] = Gray scale level of GS10, RESET=1
0	F[6:4]	*	F_6	F_5	F_4	*	*	*	*		F[6:4] = Gray scale level of GS11, RESET=1 G[2:0] = Gray scale level of GS12, RESET=1
0	G[2:0]	*	*	*	*	*	G_2	G_1	G_0		G[6:4] = Gray scale level of GS12, RESET=1
0	G[6:4]	*	G_6	G_5	G_4	*	*	*	*		H[2:0] = Gray scale level of GS14, RESET=1
0	H[2:0]	*	*	*	*	*	H_2	H_1	H_0		H[6:4] = Gray scale level of GS15, RESET=1
0	H[6:4]	*	H_6	H_5	H_4	*	*	*	*		
0	BC	1	0	1	1	1	1	0	0	Set Precharge Voltage	Second command A[7:0] sets the precharge voltage
0	A[7:0]	A7	A6	A5	A4	A3	A2	A1			level,
											A[7:0] 1xxxxxxx connects to V _{COMH}
											001xxxx 1.0 * V _{REF}
											00000000 0.51* V _{REF} 00000001 0.52* V _{REF}
											 00011000 0.75* V _{REF} (RESET)
											00011111 0.84* V _{REF}
0	BE	1	0	1	1	1	1	1		Set V _{COMH} Voltage	Second command A[4:0] sets the V _{COMH} voltage level,
0	A[4:0]	*	*	0	A4	A3	A2	A1	A0		A[4:0] 00000 0.51*V _{REF}
											00001 0.52* V _{REF}
											10001 0.68* V _{REF} (RESET)
											11101 0.81* V _{REF}
											11110 0.82* V _{REF}
											11111 0.84* V _{REF}

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Fund	Fundamental Command Table											
D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description	
0 0	BF A[3:0]	1 *	0 *	1 *	1 *	1 A ₃	1 A ₂	1 A ₁		Voltage (VSL)	Second command A[3:0] sets the VSL voltage as follow: $A[3:0] = 0010 \text{kept VSL pin NC} \\ A[3:0] = 1110 \text{ (RESET)} \text{connect a capacitor between} \\ VSL \text{ pin and } V_{SS}$	
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No Operation	

Table 19: Graphic acceleration command

Set (GAC) (D/C# = 0, R/W#(WR#)= 0, E(RD#) = 1) unless specific setting is stated

Graph	ic accel	erati	on c	omn	nand					, , ,	<u> </u>
D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D 0	Command	Description
0	23 A[4:0]	0	0	1 *	0 A ₄	0 *	0 *	1 A ₁	1 A ₀		A[0] = 0b: Disable Fill rectangle A[0] = 1b: Enable Fill rectangle (RESET)
										Graphic Acceleration Command Options	A[1] = 0b: Disable x-wrap(RESET) A[1] = 1b: Enable wrap around in x-direction during copying and scrolling A[4] = 0b: Disable reverse copy (RESET) A[4] = 1b: Enable reverse during copying.
0	24	0	0	1	0	0	1	0	0		A[5:0]: Column Address of Start
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		B[6:0]: Row Address of Start
0	B[6:0]	*	B_6	B_5	B_4	B_3	B_2	B_1	B_0		D[0.0]. Now Muliciss of Start
0	C[5:0]	*	*	C_5	C_4	C_3	C_2	C_1	C_0		C[5:0]: Column Address of End
0	D[6:0]	*	D_6	D_5	D_4	D_3	D_2	D_1	D_0		D[6:0]: Row Address of End
0	E[7:0]	E_7	E_6	E_5	E_4	E_3	E_2	E_1	E ₀		D[0.0]. Row Address of End
										Draw Rectangle	E[7:0]: Set Gray scale pattern E[7:0] This byte is divided into two nibbles. The most significant 4 bits represent the gray scale level of the left pixel of each group. The least significant 4 bits represent the gray scale level of the right pixel of each group. Please refer to Figure 31 for the gray scale pattern setting examples.
											Note: $(1) 0 \le A < C \le 63$ $(2) 0 \le B < D \le 79$
0	25	0	0	1	0	0	1	0	1	Copy	A[5:0]: Column Address of Start
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	\mathbf{A}_1	A_0		B[6:0]: Row Address of Start
0	B[6:0]	*	B_6	B_5	B_4	B_3	B_2	\mathbf{B}_1	B_0		D[0.0]. Now Address of Staft
0	C[5:0]	*	*	C_5	C_4	C_3	C_2	C_1	C_0		C[5:0]: Column Address of End
0	D[6:0]	*	D_6	D_5	D_4	D_3	D_2	\mathbf{D}_1	D_0		DICOLD ALL CELL
0	E[5:0]	*	*	E ₅	E ₄	E ₃	E ₂	E ₁	E ₀		D[6:0]: Row Address of End
0	F[6:0]	**	F_6	F_5	F_4	F_3	F_2	F_1	F_0		

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Graph	ic accel	erati	on c	omn	nand						
D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D 0	Command	Description
0 0 0 0	26 A[5:0] B[6:0] C[1:0]	0 * * *	0 * B ₆ *	1 A ₅ B ₅ *	0 A ₄ B ₄ *	0 A ₃ B ₃ *	1 A ₂ B ₂ *	1 A ₁ B ₁ C ₁	$egin{array}{c} 0 \ A_0 \ B_0 \ C_0 \ \end{array}$	Horizontal Scroll	E[5:0]: Column Address of New Start F[6:0]: Row Address of New Start Note: (1) $0 \le A < C \le 63$ (2) $0 \le B < D \le 79$ (3) $0 \le E \le 63$ (4) $0 \le F \le 79$ A[5:0]: 1~63 horizontal offset in number of 2~127 column 0 no horizontal scroll B[6:0]: 2~80 number of rows to be H-scrolled C[1:0]: scrolling time interval 00b 12 frames 01b 64 frames 10b 128 frames 11b 256 frames Note: (1) Scrolling operates during display ON. (2) The parameters should not be changed after scrolling is activated
0	2E	0	0	1	0	1	1	1	0	Stop Moving	Note (1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.
0	2F	0	0	1	0	1	1	1	1	Start Moving	This command activates the scrolling function according to the setting done by Horizontal Scroll command 26h. Note (1) The "wrap around in x-direction" function must be enabled before scrolling start. i.e. Bit A {1} of command 23h must be set to 1b before issuing 2F command.

Table 20: Read Command Table

(D/C#=0 R/W# (WR#)=1 E (RD#)=1 for 6800 or E (RD#)=0 for 8080)

	(D/C#=0, R/W# (WR#)=1, E (RL	$D_{\#}$)=1 for 6800 or E (RD $\#$)=0 for 8080)
		D7 = 0:reserved
		D7 = 1:reserved
		D6 = 0:indicates the display is ON
$D_7D_6D_5D_4D_3D_2D_1$	Status Dogistar Dood	D6 = 1:indicated the display is OFF
D_0	Status Register Read	D5 = 0:reserved
		D5 = 1:reserved
		D4 = 0:reserved
		D4 = 1:reserved

Note
(1) Patterns other than that given in Command Table are prohibited to enter to the chip as a command;
Otherwise, unexpected result will occur

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9.1 Data Read / Write

To read data from the GDDRAM, input HIGH to R/W# (WR#) pin and D/C# pin for 6800-series parallel mode, LOW to E (RD#) pin and HIGH to D/C# pin for 8080-series parallel mode.

In horizontal address increment mode, GDDRAM column address pointer will be increased by one automatically after each data read. In vertical address increment mode, GDDRAM row address pointer will be increased by one automatically after each data read.

Also, a dummy read is required before the first data read. See Figure 5 and Figure 8 in Functional Description.

To write data to the GDDRAM, input LOW to R/W#(WR#) pin and HIGH to D/C# pin for 6800-series parallel mode and 8080-series parallel mode. For serial interface mode, it is always in write mode. In horizontal address increment mode, GDDRAM column address pointer will be increased by one automatically after each data write. In vertical address increment mode, GDDRAM row address pointer will be increased by one automatically after each data write.

It should be noted that, in horizontal address increment mode, the row address pointer would be increased by one automatically if the column address pointer wraps around. In vertical address increment mode, the column address pointer will be increased by one automatically if the row address pointer wraps around.

D/C# **R/W# (WR#) Address Increment Comment** 0 0 Write Command No 0 Read Status 1 No 1 0 Write Data Yes 1 Read Data Yes 1

Table 21: Address Increment Table (Automatic)

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10 COMMAND DESCRIPTIONS

10.1 Fundamental command description

10.1.1 Set Column Address (15h)

This triple byte command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command A0h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

10.1.2 Set Row Address (75h)

This triple byte command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address. This pointer is used to define the current read/write row address in graphic display data RAM. If vertical address increment mode is enabled by command A0h, after finishing read/write one row data, it is incremented automatically to the next row address. Whenever the row address pointer finishes accessing the end row address, it is reset back to start row address.

The diagram below shows the way of column and row address pointer movement through the example: column start address is set to 2 and column end address is set to 61, row start address is set to 1 and row end address is set to 78; horizontal address increment mode is enabled by command A0h. In this case, the graphic display data RAM column accessible range is from column 2 to column 61 and from row 1 to row 78 only. In addition, the column address pointer is set to 2 and row address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation (*solid line in* Figure 18). Whenever the column address pointer finishes accessing the end column 61, it is reset back to column 2 and row address is automatically increased by 1 (*solid line in* Figure 18). While the end row 78 and end column 61 RAM location is accessed, the row address is reset back to 1 and the column address is reset back to 2 (*dotted line in* Figure 18).

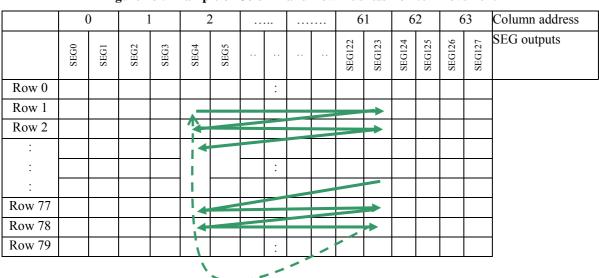


Figure 18: Example of Column and Row Address Pointer Movement

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10.1.3 Set Contrast Current (81h)

This command is to set Contrast Setting of the display. The chip has 128 contrast steps from 00H to 7FH. The segment output current increases with the increase of contrast step. See Figure 19 below.

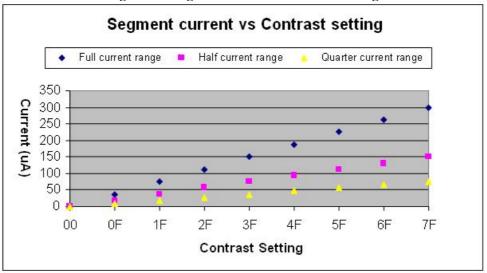


Figure 19: Segment current vs Contrast setting

10.1.4 Set Current Range (84h, 85h, 87h)

This command is used to select quarter range or half range or full range current mode. With the same contrast level, quarter range mode will give a quarter of the current output of the full range mode. Similar to half range current mode, it will give a half of the current output of the full range mode. See Figure 19. In RESET, quarter range current mode is default.

10.1.5 Set Re-map (A0h)

This double command has multiple configurations and each bit setting is described as follows:

- Column Address Remapping (A[0])
 - This bit is made for increase the flexibility layout of segment signals in OLED module with segment arranged from left to right (when A[0] is set to 0) or from right to left (when A[0] is set to 1).
- Nibble Remapping (A[1])
 - When A[1] is set to 1, the two nibbles of the data bus for RAM access are re-mapped, such that (D7, D6, D5, D4, D3, D2, D1, D0) acts like (D3, D2, D1, D0, D7, D6, D5, D4). If this feature works together with Column Address Re-map, it would produce an effect of flipping the outputs from SEG0~127 to SEG127~SEG0 as show in Table 13.
- Address increment mode (A[2])
 - When A[2] is set to 0, the driver is set as horizontal address increment mode. After the display RAM is read / written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and row address pointer is increased by 1. The sequence of movement of the row and column address point for horizontal address increment mode is shown in Figure 20

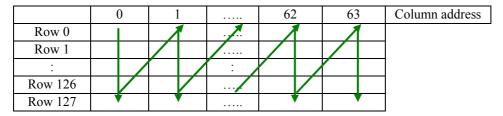
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Figure 20: Address Pointer Movement of Horizontal Address Increment Mode

	0	1		62	63	Column address
Row 0	-				—	
Row 1	-					
:	4.	:	:	٠	:	
Row 78	-					
Row 79	+					

When A[2] is set to 1, the driver is set to vertical address increment mode. After the display RAM is read / written, the row address pointer is increased automatically by 1. If the row address pointer reaches the row end address, the row address pointer is reset to row start address and column address pointer is increased by 1. The sequence of movement of the row and column address point for vertical address increment mode is shown in Figure 21.

Figure 21: Address Pointer Movement of Vertical Address Increment Mode



• COM Remapping (A[4])

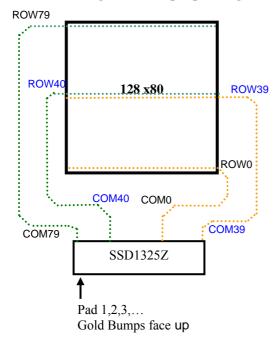
This bit defines the scanning direction of the common for flexible layout of common signals in OLED module either from up to down (when A[4] is set to 0) or from bottom to up (when A[4] is set to 1). Table 14 shows an example of the using the COM Remapping to perform vertical scrolling.

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Splitting of Odd / Even COM Signals (A[6])
 This bit is made to match the COM layout connection on the panel.

When A[6] is set to 0, no splitting odd / even of the COM signal is performed, output pin assignment sequence is shown as below (for 80MUX ratio):

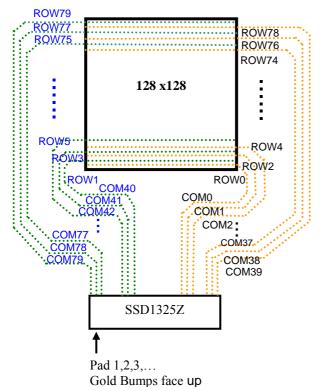
Figure 22: Output pin assignment when command A0h bit A[6]=0.



Output Pin	Connection
SSD1325Z	Panel
COM0	ROW0
COM1	ROW1
COM2	ROW2
COM3	ROW3
• •	• •
COM39	ROW39
COM40	ROW40
:	:
COM77	ROW77
COM78	ROW78
COM79	ROW79

When A[6] is set to 1, splitting odd / even of the COM signal is performed, output pin assignment sequence is shown as below (for 128MUX ratio):

Figure 23: Output pin assignment when command A0h bit A[6]=1.



Output Pin Connection				
SSD1325Z	Panel			
COM0	ROW0 (Even)			
COM1	ROW2			
COM2	ROW4			
:	:			
COM37	ROW74			
COM38	ROW76			
COM39	ROW78			
COM40	ROW1 (Odd)			
COM41	ROW3			
COM42	ROW5			
:	:			
COM77	ROW75			
COM78	ROW77			
COM79	ROW79			

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10.1.6 Set Display Start Line (A1h)

This double byte command is to set Display Start Line register for determining the starting address of display RAM to be displayed by selecting a value from 0 to 79. Figure 24 shows an example using this command of this command when MUX ratio= 80 and MUX ratio= 54 and Display Start Line = 28. In there, "ROW" means the graphic display data RAM row.

Figure 24: Example of Set Display Start Line with no Remapping

	MUX ratio (A8h) = 80			MUX ratio (A8h) = 54
COM Pir	Display Start Line (A1h)			
	= 0	= 28	= 0	= 28
COM0	ROW0	ROW28	ROW0	ROW28
COM1	ROW1	ROW29	ROW1	ROW29
COM2	ROW2	ROW30	ROW2	ROW30
COM3	ROW3	ROW31	ROW3	ROW31
:	:	:	:	•
COM23	ROW23	ROW51	ROW23	ROW51
	ROW24	ROW52	ROW24	ROW52
	ROW25	ROW53	ROW25	ROW53
COM26	ROW26	ROW54	ROW26	ROW54
:	:	:	:	•
•	:	:	:	:
COM49	ROW50	ROW77	ROW50	ROW77
COM51	ROW51	ROW78	ROW51	ROW78
COM52	ROW52	ROW79	ROW52	ROW79
COM53	ROW53	ROW0	ROW53	ROW0
COM54	ROW54	ROW1	-	-
COM55	ROW55	ROW2	_	-
:	:	:	:	•
: COM76	: POW76	ROW24	:	
	ROW77	ROW25		
COM78		ROW26		
	ROW79	ROW27	-	-
Display Example	SOLOMON	SOLOMON		SOLOMON

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10.1.7 Set Display Offset (A2h)

This double byte command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0~COM79. Figure 25 shows an example using this command when MUX ratio= 80 and MUX ratio= 54 and Display Offset = 28. In there, "Row" means the graphic display data RAM row.

Figure 25: Example of Set Display Offset with no Remapping

	MUX ratio (A8h) = 80	MUX ratio (A8h) = 80	MUX ratio (A8h) = 64	MUX ratio (A8h) = 64
COM Pin	Display Offset (A2h)=0	Display Offset (A2h)=18	Display Offset (A2h)=0	Display Offset (A2h)=18
COM0	ROW0	ROW28	ROW0	ROW28
COM1	ROW1	ROW29	ROW1	ROW29
COM2	ROW2	ROW30	ROW2	ROW30
COM3	ROW3	ROW31	ROW3	ROW31
:	•	•		•
:	:	•	:	:
COM23	ROW23	ROW51	ROW23	ROW51
COM24	ROW24	ROW52	ROW24	ROW52
COM25	ROW25	ROW53	ROW25	ROW53
COM26	ROW26	ROW54	ROW26	-
:	•	•		•
:	•	•		•
COM49	ROW50	ROW77	ROW50	-
COM51	ROW51	ROW78	ROW51	-
COM52	ROW52	ROW79	ROW52	-
COM53	ROW53	ROW0	ROW53	ROW0
COM54	ROW54	ROW1	-	ROW1
COM55	ROW55	ROW2	-	ROW2
:	•	:		•
:	•	:		:
COM76	ROW76	ROW24	-	ROW24
COM77	ROW77	ROW25	-	ROW25
COM78	ROW78	ROW26	-	ROW26
COM79	ROW79	ROW27	-	ROW27
Display Example	SOLOMON	SOLOMON		COLOMON

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10.1.8 Set Display Mode (A4h ~ A7h)

These are single byte commands (A4h \sim A7h) and are used to set display status to Normal Display, Entire Display ON, Entire Display OFF or Inverse Display, respectively.

• Normal Display (A4h)
Reset the "Entire Display ON, Entire Display OFF or Inverse Display" effects and turn the data to ON at the corresponding gray level. Figure 26 shows an example of Normal Display.

Figure 26: Example of Normal Display





Set Entire Display ON (A5h)

Force the entire display to be at gray scale level GS15, regardless of the contents of the display data RAM, as shown on Figure 27.

Figure 27: Example of Entire Display ON





Memory

Display

Set Entire Display OFF (A6h)
 Force the entire display to be at gray scale level GS0, regardless of the contents of the display data RAM, as shown on Figure 28.

Figure 28: Example of Entire Display OFF





Display

• Inverse Display (A7h)

The gray scale level of display data are swapped such that "GS0" <-> "GS15", "GS1" <-> "GS14", etc. Figure 29 shows an example of inverse display.

Figure 29: Example of Inverse Display





Display

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10.1.9 Set Multiplex Ratio (A8h)

This double byte command sets multiplex ratio (MUX ratio) from 16MUX to 80MUX. In RESET, multiplex ratio is 80MUX. Please refer to Figure 24 and Figure 25 for the example of setting different MUX ratio.

10.1.10 Set Master Configuration (ADh)

This command selects the external V_{CC} power supply. External V_{CC} power should be connected to the V_{CC} pin. A[0] bit must be set to 0b after RESET.

This command will be activated after issuing Set Display ON command (AFh)

10.1.11 Set Display ON/OFF (AEh / AFh)

These single byte commands are used to turn the matrix display on the OLED panel display either ON or OFF. For AEh, the display is OFF, the segment and common output are in high impedance state and circuits will be turned OFF. When the sleep mode is set to OFF (AFh), the display is ON.

10.1.12 Set V_{COMH} Voltage (BEh)

This double byte command sets the high voltage level of common pins, V_{COMH} . The level of V_{COMH} is programmed with reference to V_{CC} . Please refer to Table 18 for detail information and breakdown levels of each step.

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10.1.13 Set Precharge Voltage (BCh)

This double byte command is used to set the pre-charge voltage (phase 2) level. Please refer to Table 18 for detail information and breakdown levels of each step.

10.1.14 Set Phase Length (B1h)

This is a double byte command. In the second byte of this double command, lower nibble and higher nibble is defined separately. The lower nibble adjusts the phase length of Reset (phase 1). The higher nibble is used to select the phase length of the pre-charge phase (phase 2). The phase length is ranged from 1 to 16 DCLK's. RESET for A[3:0] is set to 3h while reset for A[7:4] is set to 5h. Please refer to Table 18 for detail breakdown levels of each step.

10.1.15 Set Row Period (B2h)

This command is used to set the row period. It is defined by multiplying the internal display clock period by the number of internal display clocks per row (valued from 14h to 7Fh), and RESET is 25h. The larger the value, the more precise of each gray scale level can be tuned. See "Gray Scale Table" command (B8h) for details. Also, it is used to define the frame frequency altogether with the use of "Display Clock Divide Ratio" command (B3h). Row period equals to the sum of phase 1 and phase 2 periods and the pulse width of GS15. See equation in Table 18.

10.1.16 Set Display Clock Divide Ratio (B3h)

This double command is used to set the frequency of the internal display clocks, DCLK's. It is defined by dividing the oscillator frequency by the divide ratio (valued from 1 to 16). Frame frequency is determined by divide ratio, number of display clocks per row, MUX ratio and oscillator frequency. The lower nibble of the second byte is used to select the oscillator frequency. Please refer to Table 18 for detail breakdown levels of each step.

10.1.17 Set Gray Scale Table

This command is used to set each individual gray scale level for the display. Except gray scale level GS0 that has no pre-charge and current drive, the pulse width of each gray scale level is programmed with unit of DCLK. The longer the length of the pulse width, the brighter the OLED pixel when it is turned ON.

The setting of gray scale table entry can perform gamma correction on OLED panel display. Normally, it is desired that the brightness response of the panel is linearly proportional to the image data value in display data RAM. However, the OLED panel is somehow responded in non-linear way. Appropriate gray scale table setting like example below can compensate this effect.

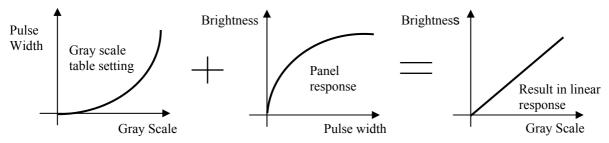


Figure 30: Example of gamma correction by gray scale table setting

As shown in Table16 and

Table 17, GS1 is defined with pulse width equals to the first offset value, L1, select from 0-7 internal display clocks. GS2 is defined with pulse width equals to GS1 plus the next offset value, L2, select from 1-8 internal display clocks. Similarly, the next GS level is defined with pulse width equals to its lower one GS level plus the next offset value, select from 1-8 internal display clocks. In normal operation, GS15 should take the full current drive period as its pulse width. Therefore, the row period should be set as the

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sum of phase 1 period, phase 2 periods, and the pulse width of GS15 with the use of "Row period" command.

10.1.18 NOP (E3h)

This is a no operation command.

10.1.19 Status register Read

This command is issued by setting D/C# LOW during a data read (refer to Figure 34 to Figure 36 parallel interface waveform). It allows the MCU to monitor the internal status of the chip.

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10.2 Graphic Acceleration Command Set Description

10.2.1 Graphic Acceleration Command Options (23h)

This command has two functions.

- Enable / Disable fill (A[0])
 - 0 = Disable filling of rectangle in draw rectangle command.
 - 1 = Enable filling of rectangle in draw rectangle command. (RESET)
- Enable / Disable x-warp (A[1])
 - 0 = Disable wrap around in x-direction during copying and scrolling
 - 1 = Enable wrap around in x-direction during copying and scrolling (RESET)
- Enable / Disable reverse copy (A[4])
 - 0 = Disable reverse copy (RESET)
 - 1 = During copy command, the new image colors are swapped such that "GS0" <-> "GS15", "GS1" <-> "GS14",

10.2.2 Draw Rectangle (24h)

Specify a starting point (Row 1, Column 1) and an ending point (Row 2, Column 2) as well as giving the desire gray scale pattern, a rectangle will then be drawn.

Row 1,
Column 1

Gray scale pattern
=A0h

Gray scale pattern
=A0h

Row 2,
Column 2

Row 2,
Column 2

Figure 31: Example of draw rectangle command

The following example illustrates the rectangle drawing command sequence.

- 1. Enter the "draw rectangle mode" by execute the command 24h
- 2. Set the starting column coordinates, Column 1. e.g., 01h.
- 3. Set the starting row coordinates, Row 1. e.g., 01h.
- 4. Set the finishing column coordinates, Column 9. e.g., 09h
- 5. Set the finishing row coordinates, Row 5. e.g., 05h
- 6. Set the gray scale pattern:

This byte is divided into two nibbles. The most significant 4 bits represent the gray scale level of the left pixel of each group. The least significant 4 bits represent the gray scale level of the right pixel of each group. Please refer to Figure 31 for the gray scale pattern setting examples.

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10.2.3 Copy (25h)

Copy the rectangular region defined by the starting point (Row 1, Column 1) and the ending point (Row 2, Column 2) to location (Row 3, Column 3). If the new coordinates are smaller than the ending points, the new image will overlap the original one.

The following example illustrates the copy procedure.

- 1. Enter the "copy mode" by execute the command 25h
- 2. Set the starting column coordinates, Column 1. E.g., 00h.
- 3. Set the starting row coordinates, Row 1. E.g., 00h.
- 4. Set the finishing column coordinates, Column 2. E.g., 05h
- 5. Set the finishing row coordinates, Row 2. E.g., 05h
- 6. Set the new column coordinates, Column 3. E.g., 03h
- 7. Set the new row coordinates, Row 3. E.g., 03h

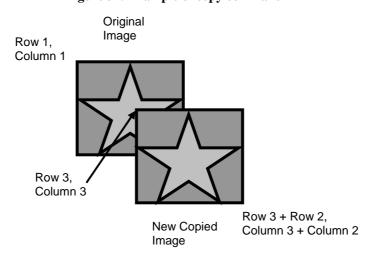


Figure 32: Example of copy command

10.2.4 Horizontal Scroll (26h)

This command consists of 3 consecutive bytes to set up the scrolling parameters. It determined the horizontal scrolling offset, no of scrolling row and scrolling speed. Some scrolling examples are shown in Figure 33.

Before issuing this command, the scrolling must be deactivated (2Eh). Otherwise, RAM content may be corrupted.

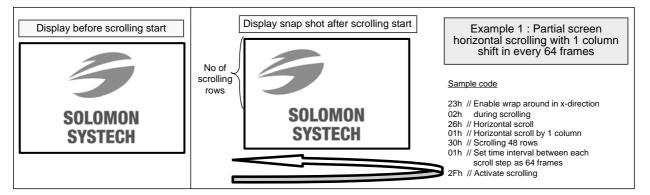


Figure 33: Scrolling examples

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10.2.5 Stop Moving (2Eh)

Stop motion of scrolling. After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.

10.2.6 Start Moving (2Fh)

Start motion of scrolling. This command should only be issued after scrolling setup parameters are defined through command 26h and the function of wrap around in x-direction is enabled through 23h.

The following actions are prohibited after the horizontal scroll is activated

- 1. RAM access (Data write or read)
- 2. Changing scrolling setup parameters

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11 MAXIMUM RATINGS

Table 22 : Maximum Ratings (Voltage Reference to V_{SS})

Symbol	Parameter	Value	Unit
$ m V_{DD}$		-0.3 to +4.0	V
V_{CC}	Supply Voltage	0 to +17.0	V
$ m V_{REF}$		0 to +17.0	V
$ m V_{SEG}$	SEG output voltage	$0 \text{ to } +V_{CC}$	V
V_{COM}	COM output voltage	0 to $+0.9$ x V_{CC}	
$ m V_{in}$	Input voltage	V_{SS} -0.3 to V_{DD} +0.3	V
$T_{\mathbf{A}}$	Operating Temperature	-40 to +85	°C
$\mathrm{T_{stg}}$	Storage Temperature Range	-65 to +150	°C

Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

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12 DC CHARACTERISTICS

Conditions (unless specified):

Voltage referenced to V_{SS};

 V_{DD} = 2.7, V_{CC} = 12.0V, I_{REF} = 10uA, at T_A = 25°C.

Table 23: DC Characteristics

Symbol	Parameter	Test Condition	Min	Тур	Max	Unit
V_{CC}	Operating Voltage	-	8.0	12.0	16.0	V
$V_{ m DD}$	Logic Supply Voltage	-	2.4	2.7	3.5	V
V_{OH}	HIGH Logic Output Level	$I_{OUT} = 100uA, 3.3MHz$	$0.9*V_{DD}$	1	V_{DD}	V
V_{OL}	LOW Logic Output Level	$I_{OUT} = 100uA, 3.3MHz$	0	-	$0.1*V_{DD}$	V
$V_{ m IH}$	HIGH Logic Input Level	-	$0.8*V_{DD}$	•	$V_{ m DD}$	V
$ m V_{IL}$	LOW Logic Input Level	-	0	ı	$0.2*V_{DD}$	V
I_{SLEEP}	Sleep mode Current	No loading	ı	0.2	5	uA
I_{CC}	$V_{CC} \ Supply \ Current$ V_{DD} =2.7V, external V_{CC} =12V, I_{REF} =10uA, Frame rate=110Hz, All one pattern, Display ON, no loading	Contrast = 7F	-	700	-	uA
I_{DD}	$V_{DD} \ Supply \ Current$ $V_{DD} = 2.7V, external \ V_{CC} = 12V, I_{REF} = 10uA, Frame \\ rate = 110Hz, All \ one \ pattern, Display \ ON, \ no \ loading$	Contrast = 7F	-	-	650	uA
	Segment Output Current	Contrast = 7F	270	300	370	
,		Contrast = 5F	-	225	-	
I_{SEG}	V_{DD} =2.7V, V_{CC} =12V, I_{REF} =10uA, Frame rate=110Hz, Display ON, Segment pin under test is	Contrast = 3F	-	150	-	uA
	connected with a 20K resistive load to V_{SS}	Contrast = 1F	-	75	-	
Dev	Segment output current uniformity	Adjacent pin	-1.5		+1.5	%
Bev	V_{DD} =2.7V, V_{CC} =12V, I_{REF} =10uA, Contrast=7F	Overall pin to pin	-3	-	+3	/0

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13 AC CHARACTERISTICS

Conditions (Unless otherwise specified):

Voltage referenced to $V_{\rm SS}$ $V_{DD} = 2.4V \text{ to } 3.5V$ $V_{CC} = 8.0V \text{ to } 16.0V$ $T_A = 25^{\circ}C$

Table 24 : AC Characteristics

Symbol	Parameter	Test Condition	Min	Тур	Max	Unit
F _{OSC}	Oscillation Frequency of Display Timing Generator	$V_{DD} = 2.7V$	535	630	725	kHz
F_{FRM}	Frame Frequency for 128 MUX Mode	128x80 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F _{OSC} * 1/(D*K*80)	-	Hz
	Reset LOW pulse width	-	3	-	-	us
RES#	Reset complete time	-	-	-	2	us

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Note:(1) Fose stands for the frequency value of the internal oscillator and the value is measured when command B3h A[7:4]

⁽²⁾ D stands for divide ratio

 $^{^{(3)}}$ K stands for total number of display clocks per row defined by command B2h $^{(4)}$ N stands for number of MUX selected by command A8h

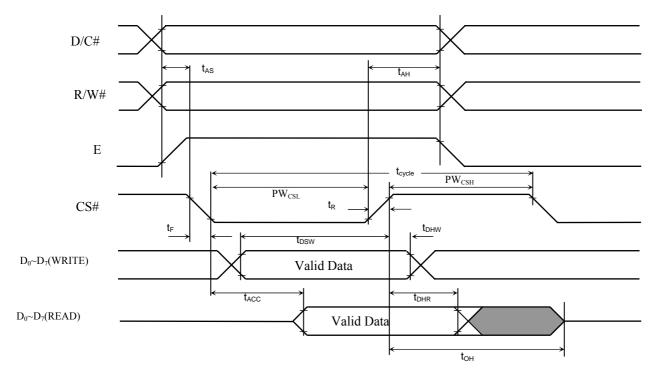
Conditions:

 V_{DD} - V_{SS} = 2.4 to 3.5V T_A = 25°C

Table 25: 6800-Series MPU Parallel Interface Timing Characteristics

Symbol	Parameter	Min	Тур	Max	Unit
t _{cvcle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
$t_{ m DHW}$	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read)	120	-	-	ns
	Chip Select Low Pulse Width (write)	60			
PW_{CSH}	Chip Select High Pulse Width (read)	60	-	-	ns
	Chip Select High Pulse Width (write)	60			
t_R	Rise Time	-	-	15	ns
$t_{\rm F}$	Fall Time	-	-	15	ns

Figure 34: 6800-series MPU Parallel Interface Characteristics



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Conditions:

 V_{DD} - V_{SS} = 2.4 to 3.5V T_A = 25°C

Table 26: 8080-Series MPU Parallel Interface Timing Characteristics

Symbol	Parameter	Min	Тур	Max	Unit
t _{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
$t_{ m DSW}$	Write Data Setup Time	40	-	-	ns
$t_{ m DHW}$	Write Data Hold Time	15	-	-	ns
$t_{ m DHR}$	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_{R}	Rise Time	-	-	15	ns
t_{F}	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure 35: 8080-series parallel interface characteristics (Form 1)

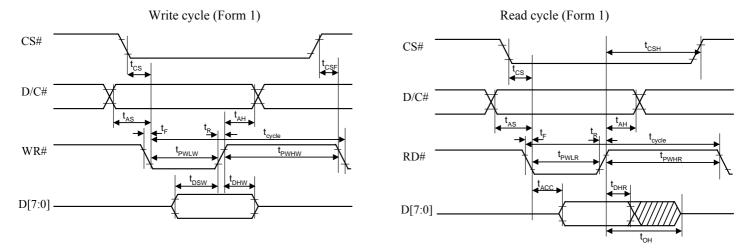
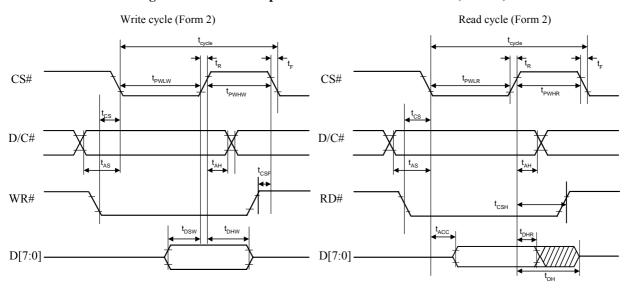


Figure 36: 8080-series parallel interface characteristics (Form 2)



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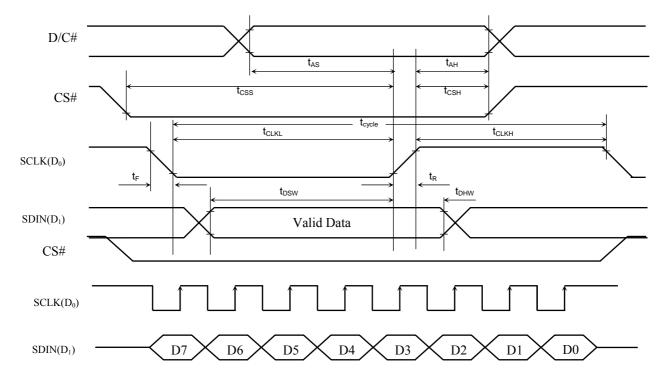
Conditions:

 V_{DD} - V_{SS} = 2.4 to 3.5V T_A = 25°C

Table 27 : Serial Interface Timing Characteristics

Symbol	Parameter	Min	Тур	Max	Unit
t _{cvcle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
$t_{\rm F}$	Fall Time	-	-	15	ns

Figure 37 : Serial Interface Characteristics



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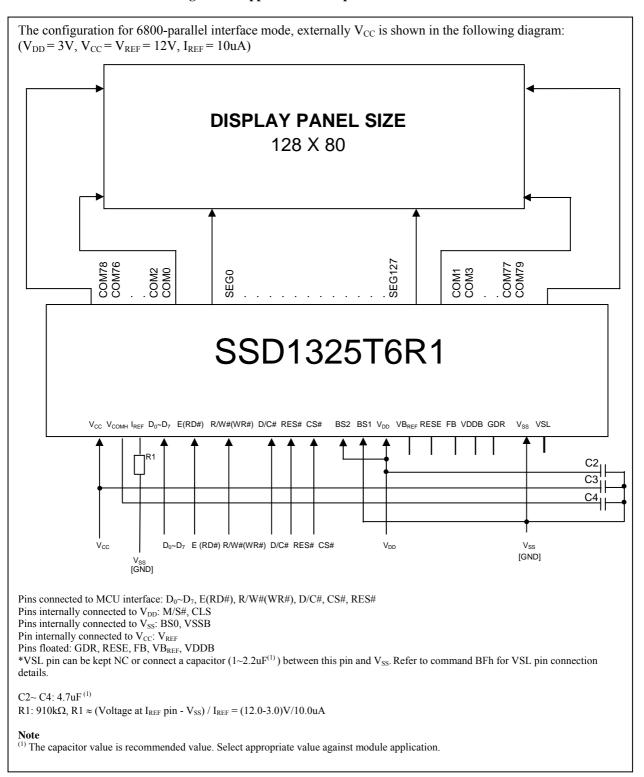
14 APPLICATION EXAMPLES

The configuration for SPI serial interface mode, externally V_{CC} is shown in the following diagram: $(V_{DD} = 3V, V_{CC} = V_{REF} = 12V, I_{REF} = 10uA)$ **DISPLAY PANEL SIZE** 128 X 80 SEG127 SSD1325Z E(RD#) R/W#(WR#) D/C# RES# CS# V_{SS} V_{CC} V_{COMH} V_{DD} C1 C2 С3 V_{CC} D/C# RES# CS# D₀ (SCLK) D₁ (SDIN) V_{SS} (GND) Pins connected to MCU interface: D₀, D₁, D/C#, RES#, CS# Pins internally connected to V_{DD} : M/S#, CLS, VDDB Pins internally connected to V_{SS} : BS0, BS1, BS2, E(RD#), R/W#(WR#), VSSB, VCL Pin internally connected to V_{CC}: V_{REF} Pins floated: CL, GDR, RESE, FB, VB_{REF} *VSL pin can be kept NC or connect a capacitor (1~2.2uF⁽¹⁾) between this pin and V_{SS}. Refer to command BFh for VSL pin connection C1: 1uF, C2~ C3: 4.7uF $^{(1)}$ R1: 910kΩ, R1 ≈ (Voltage at I_{REF} pin - V_{SS}) / I_{REF} = (12.0-3.0)V/10.0uA **NOTE**(1) The capacitor value is recommended value. Select appropriate value against module application.

Figure 38 : Application Example for SSD1325Z SPI serial interface mode

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Figure 39: Application Example for SSD1325T6R1

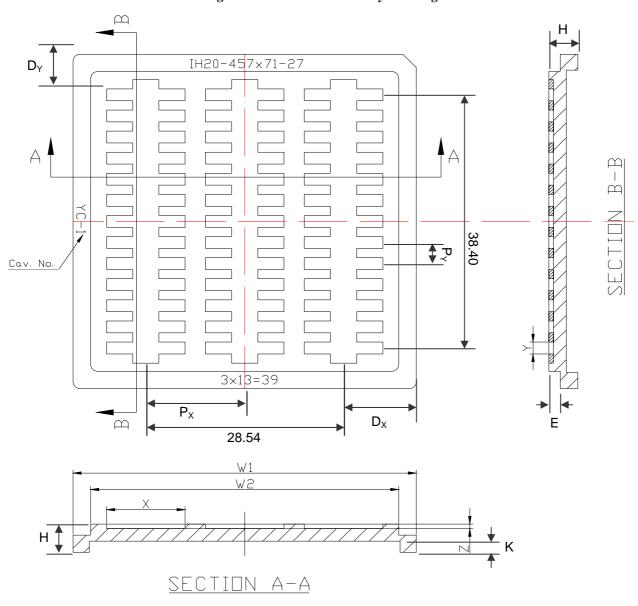


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15 PACKAGE INFORMATION

15.1 SSD1325Z Die Tray Information

Figure 40: SSD1325Z Die Tray Drawing



Remark

1. Depth of text: Max. 0.1mm

2. Tray material: ABS

3. Tray color code: Black

4. Surface resistance $10^9 \sim 10^{11} \Omega$

5. Tray warpage: Max 0.10mm

6. Unspecifier dim's tolerance: ± 0.15mm

7. Pocket size: 13.56 x 1.65 x 0.61mm

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Table 28 : SSD1325Z Die Tray Dimensions

D	Dimensions
Parameter	mm (mil)
W1	50.70±0.2 (1996)
W2	45.50±0.2 (1791)
Н	4.05±0.2 (160)
Е	1.75±0.2 (69)
K	1.45±0.2 (57)
P_{X}	14.27±0.1 (562)
P_{Y}	3.20±0.1 (126)
X	11.60±0.1 (457)
Y	1.80±0.1 (71)
Z	0.68±0.05 (27)
D_X	11.08±0.1 (437)
D_{Y}	6.15±0.1 (242)
N (number of die)	39

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15.2 SSD1325T6R1 Detail Dimension

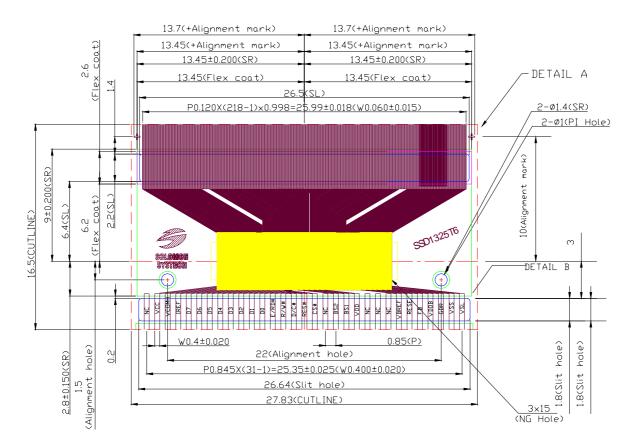
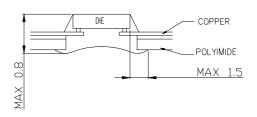


Figure 41: SSD1325T6R1 Detail Dimension

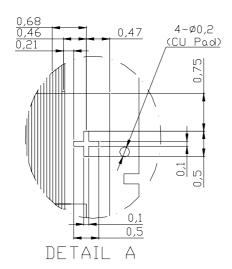
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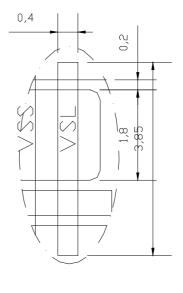
NOTE:

- 1. GENERAL TOLERANCE: ±0.05mm 2. CUTLINE TOLERANCE: ±0.15mm 3. MATERIAL
- - PI: 75±6um CU: 18±5um
 - SR: 26±14um
 - ADHESIVE: 12±2um
- 4. FLEX COATING: Min10um
- 5. SN PLATING: 0.20±0.05um
- 6. TAPSITE: 4 SPH, 19.00mm



MIRROR DESIGN





DETAIL B

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