DSA2000 F-Engine Documentation

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INSTALLATION

The DSA2000 F-engine pipeline firmware and software is available at https://github.com/realtimeradio/dsa2000-fpga. Follow the instructions here to download and install the pipeline.

Specify the build directory by defining the `BUILDDIR` environment variable, eg:

```
export BUILDDIR=~/src/
mkdir -p $BUILDDIR
```

1.1 Get the Source Code

Clone the repository and its dependencies with:

```
# Clone the main repository
cd $BUILDDIR
git clone https://github.com/realtimeradio/dsa2000-fpga
# Clone relevant submodules
cd dsa2000-fpga
git submodule init --recursive
git submodule update
```

1.2 Install Prerequisites

1.2.1 Firmware Requirements

The SOUK MKID Readout firmware can be built with the CASPER toolflow, and was designed using the following software stack:

- Ubuntu 18.04.0 LTS (64-bit)
- MATLAB R2021a
- Simulink R2021a
- MATLAB Fixed-Point Designer Toolbox R2021a
- Xilinx Vivado HLx 2021.2
- Python 3.8

It is *strongly* recommended that the same software versions be used to rebuild the design.

CHAPTER

TWO

F-ENGINE SYSTEM OVERVIEW

2.1 Overview

The DSA2000 F-Engine firmware receives a stream of ADC samples via a JESD204C interface and generates the following channelised data products:

- 9680 channels with ~134 kHz bandwidth, covering the 700-2000MHz band
- 4096 channels with ~8.4 kHz bandwidth, with a tunable center frequency.
- 2048 channels with ~1 kHz bandwidth, with a tunable center frequency.

The firmware also performs beamforming, generating:

- 4 dual-polarization phased-array beams, covering the 700-2000MHz band with 605 ~2.15 MHz channels

A block diagram of the readout system is shown in Fig. 2.1.

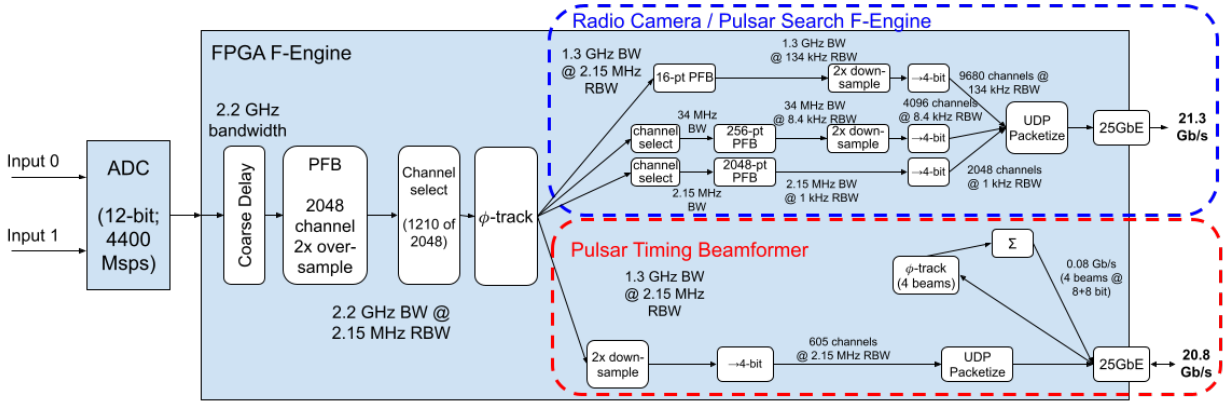

Fig. 2.1: Top-level F-Engine block diagram

2.2 Firmware Source

Currently, a minimal top-level implementation of the DSA2000 F-engine firmware is available as a Simulink model.

The top-level of this Simulink diagram is shown in Fig. 2.2. It includes the main high-bandwidth channelizers, and is currently used for resource and power estimations. This model does not include any of the DSA's high-resolution channelizers, phase-tracking, or beamforming logic.

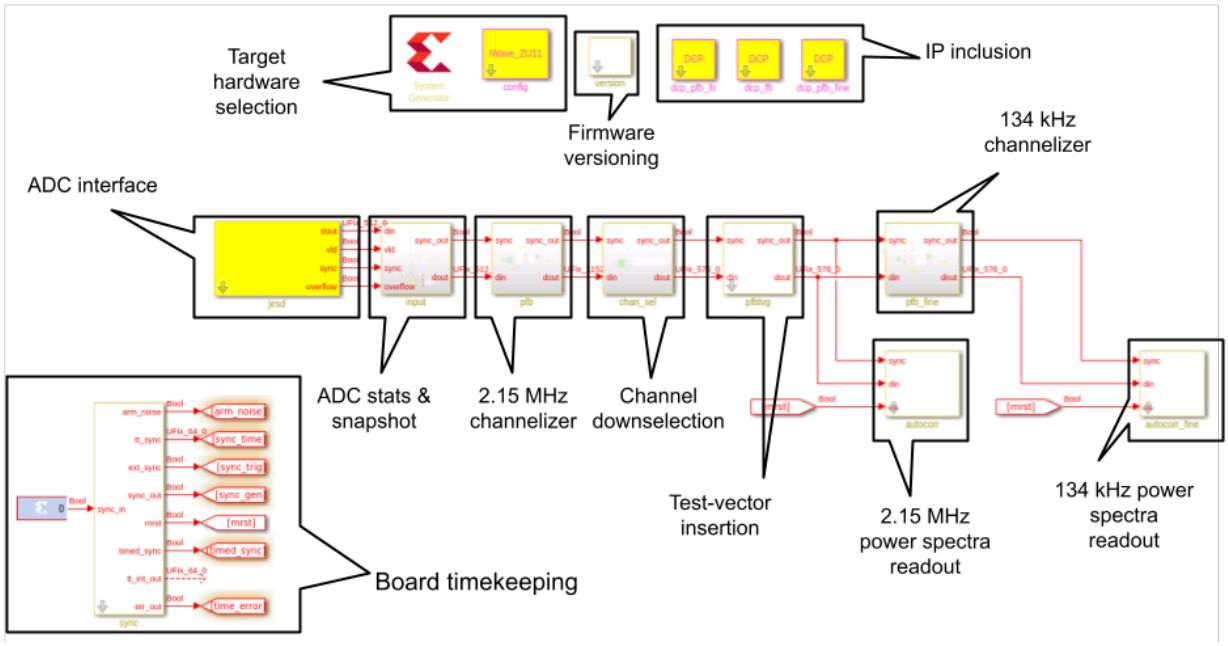

Fig. 2.2: Top-level F-Engine top-level firmware

Relevant firmware files are:

- `firmware/src/models/dsa2k_iwave_v1.slx` - Top-level simulink design
- `firmware/src/models/dsp/pfb_fir_2p_2kpt_12i_18o_os2_core.slx` - 2x oversampling PFB FIR frontend
- `firmware/src/models/dsp/fft_2p_4kc_18i_18o_core.slx` - 2.15 MHz channelizer
- `firmware/src/models/dsp/pfb_fine_core.slx` - second stage 134 kHz channelizer

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