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RCF Preliminary Design

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Revision History

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1	2023-10-02	all	Original	JH
2	2023-10-17	2. Requirements	Re-designate as design document. Minor typo/formatting fixes. Add Beamforming requirement.	JH
2.1	2023-10-17	3. Design	Typo fixes. Cross-ref fixes. Table overflow fixes.	JH
3	2023-10-19	all	Changes after internal review	JH
3.1	2023-10-20	Glossary	Expand gloassary	JH

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1 Glossary

1.1 Abbreviations

AC Zoom band A RCF frequency channels (with resolution ~ 8 kHz)
ADC Analog-to-Digital Converter
ASP Analog Signal Path subsystem
BC Zoom band B RCF frequency channels (with resolution ~ 1 kHz)
CNW Central Control Network subsystem
CPU Central Processing Unit
FAC Facilities subsystem
FPGA Field-Programmable Gate Array
FRX Fiber Receiver board
FSM FPGA Station Module. An FPGA-based processing module responsible for digitizing and channelizing signals from a single antenna.
FWHM Full Width at Half Maximum
GbE Gigabit Ethernet
HI Neutral Hydrogen emission line at 1.42 GHz
HP Horizontal Pitch (unit of length equal to 0.2 inches)
IC Integrated Circuit
LO Local Oscillator
LSR Local Standard of Rest velocity frame
MC Monitor and Control subsystem
NC Narrow-band Continuum RCF frequency channels (with resolution ~ 130 kHz)
NTP Network Time Protocol
PFB Polyphase Filter Bank
PLL Phase-Locked Loop
PT Pulsar Timing subsystem
RCF Radio Camera Frontend subsystem
RcfR-*XXXX* RCF subsystem Requirement *XXXX*
RCP Radio Camera Processor subsystem
RF Radio Frequency
ScR-*XXXX* Science Requirement *XXXX*
SiP System-in-Package
SNW Signal Network subsystem
SoM System-on-Module
SRM Subrack Manager board
TC Pulsar Timing RCF frequency channels (with resolution ~ 2 MHz)
TS Timing and Synchronization subsystem
TT Telescope Time

2 Requirements

A number of science requirements are defined for the DSA2000 system, each designated by a unique identifier of the form "ScR-XXXX".

Here we consider the requirements which are relevant to the design of the RCF, and derive a set of subsystem requirements with designations "RcfR-XXXX".

2.1 Frequency Resolutions and Spans

A number of requirements directly relating to frequency coverage and channel resolutions are present in DSA2000 science requirements.

These are:

1. ScR-0004: Frequency coverage from 0.7 to 2.0 GHz
2. ScR-0026 [High-z continuum]: HI velocity resolution of < 62 km/s for galaxies > -1000 km/s and $z < 1$
3. ScR-0027 [Zoom A]: HI velocity resolution <2 km/s for galaxies >-500 km/s and distance < 100 Mpc.
4. ScR-0028 [Zoom B]: HI velocity resolution <0.3 km/s for galactic HI, covering HI emission between -100 km/s and +100 km/s.
5. ScR-0029 [Tunability]: Zoom bands A and B should be tunable.
6. ScR-0022 [Pulsar Timing]: Pulsar-phase coherent folding with ≥ 2048 phase bins for pulsars with periods > 1 ms.

From these requirements, the following resolutions and bandwidths are inferred:

1. ScR-0004: Total coverage 0.7 to 2.0 GHz
2. ScR-0026 [High-z continuum]: Coverage from 0.71 to 1.425 GHz, at < 146.8 kHz resolution at 0.71 GHz and < 294.5 kHz resolution at 1.425 GHz.
3. ScR-0027 [Zoom A]: Coverage from 1.388 to 1.422 GHz, at < 9.25 kHz (at 1.388 GHz).[1]
4. ScR-0028 [Zoom B]: Coverage of 1419.93 – 1420.88 MHz with a channel width < 1.42 kHz.
5. ScR-0029: Center frequency of Zoom A and Zoom B windows is arbitrarily tunable within the 0.7 – 2.0 GHz band, with resolution and bandwidth set by ScR-0027 and ScR-0028.
6. ScR-0022 [Pulsar Timing]: Coverage from 0.7 to 2.0 GHz at ≥ 2.048 MHz resolution.[2]

There is no science requirement on frequency resolution above 1.425 GHz. Here, the maximum channel bandwidth is likely to be limited by frequency smearing effects. For an array with maximum baseline length of 15 km, and a phase center referenced to the center of the array, a

[1] The minimum frequency is computed by converting 100 Mpc to a redshift, using a Hubble constant of 70 $\frac{\text{km/s}}{\text{Mpc}}$.
[2] This assumes a critically-sampled channelized data stream, with at least 2048 spectra produced every 1 ms.

signal received 1.5 degrees from boresight (the FWHM of the DSA2000 dish is expected to be approximately 3 degrees at 1.35 GHz) has a maximum delay relative to a boresight signal of

$$\sin(1.5^\circ) \times \frac{7.5\text{km}}{c} = 654\text{ns}.$$

This implies that the frequency channel width, Δf at 1.35 GHz should satisfy

$$\Delta f \ll (654\text{ns})^{-1},$$

i.e.,

$$\Delta f \ll 1529\text{kHz}.$$

There is no explicit requirement on how much smearing is tolerable, but, noting that the most stringent ScR-0026 frequency resolution requirement demands a channel width of less than 146.8 kHz at 0.71 GHz, this width is taken as a minimum requirement over the entire band.

> The memory footprint of RCF processing is strongly dependent on the frequency resolution of channels which may be generated – narrow channel bandwidth requires more memory. Downstream RCP processing is also strongly dependent on the number of frequency channels which need to be imaged – more numerous, narrower channels require more processing. These factors both mean that a relaxing of minimum channel bandwidth over some fraction of the 0.7 to 2.0 GHz observing band may potentially make RCF implementation easier, and reduce the size (and cost) of RCP.

The following table summarises *RcfR-0001* through *RcfR-0004*, the bandwidth and resolution requirements which satisfy all science requirements:

Requirement	RCF Product Abbreviation	Frequency Range (MHz)	Bandwidth (MHz)	Δf (kHz)
RcfR-0001	NC	$700 - 2000$	≥ 1300	< 146.8
RcfR-0002	AC	$1388 - 1422$	≥ 34	< 9.25
RcfR-0003	BC	$1419.93 - 1420.88$	≥ 0.95	< 1.42
RcfR-0004	TC	$700 - 2000$	1300	≥ 2048

2.2 Frequency Channel Response

RCF is required to generate multiple narrow-band frequency channels from a single wide-band input signal. It is not possible for each generated channel to have a perfectly flat response nor infinite out-of-band rejection. In general, constructing channels with responses approaching that of an ideal "brick-wall" filter requires increasing computational resources.

There is currently only one science requirement from which a channel response requirement may be derived, and it may be directly mapped into *RcfR-0005*:

1. ScR-0041 / *RcfR-0005*: Attenuation from the center of one channel to an adjacent channel shall be ≥ 60 dB.

   Other requirements may be useful in further specifying channel response, for example:

   - Maximum allowed passband ripple
   - Minimum attenuation at >1 channel offset

2.3 Doppler Tracking

The velocity of the Earth, relative to observed radio sources, changes over the course of time, primarily because of the planet's rotational and orbital motion. Therefore, a time-varying Doppler adjustment is required to convert the observed frequency of a source into a source velocity relative to a Local Standard of Rest (LSR) frame.

Science requirement ScR-0032 states:

- ScR-0032: [The DSA2000 system shall be capable of] correction for all motion relative to LSR with accuracy < 0.01 km/s.

Such adjustment may be carried out after correlation or image-making, by interpolating the frequency channels of a given data set onto a standard velocity frame. Alternatively, the center frequency of each frequency channel may be adjusted in real time to track the Doppler shift of a source. Whatever the mechanism, adjustment must be applied before summing together data from time periods over which the center frequency of a frequency channel moves significantly.

For DSA-2000, it is useful to be able to track the Doppler shift in real time over the coarse of a mosaic observation, which may last for $10 - 100$ hours. This means that the RCP system does not need to add Doppler shift processing to its pipeline prior to writing data to the archiving system.

The following requirement aims to explicitly ensure this is enabled by the RCF design:

- *RcfR-0006*: Over a period of 100 hours, when measured in the solar barycenter rest frame, the center frequency of any RCF frequency channel shall not shift by $> 10\%$ of the channel width.

2.4 Delay & Phase tracking

In order that DSA2000's imaging system is able to correlate and integrate signals from multiple antennas for ~seconds, it is necessary that the signals from each antenna are delayed and phase-aligned to a common reference. The delay and phase which needs to be applied to an antenna signal is a function of the direction of the source being observed, and thus changes over time.

Here the size of the delays which need to be applied to signals from each antenna are considered, as well as the rate at which they are expected to change.

2.4.1 Coarse Delay

The maximum geometric delay between antennas in an array – i.e., the maximum difference in arrival times of a common wavefront at two different antennas – is given by:

$$\tau = \frac{B_{\max}}{c},$$

where c is the speed of light, and $B_{\max}$ is the maximum baseline length. For the DSA, $B_{\max} = 15$ km and **the maximum geometric delay is 50 µs.**

Assuming that digitization of signals from all antennas occurs in a central location, further inter-antenna delays are introduced by analog cabling (and, to a lesser extent, other instrumentation) between the antennas and digitizers. Assuming that cable length differences are of length $\sim \frac{3}{2}B_{\max}$ (the preliminary design expects a maximum cable length of 21 km (Praxis Broadband 2023)), and the speed of light in a cable is $\sim \frac{2}{3}c$, **instrumental inter-antenna delays for the DSA2000 will be approximately 110 µs.**

Compensation of both geometric and instrumental delays is achieved in a radio telescope's digital processing by using memory buffers to delay the earliest arriving data streams such that they may be coherently combined with the latest arriving. The practical implementation of this scheme may utilize buffering in either, or both, of RCF and RCP. For the purposes of producing a viable RCF design, the following requirements are used:

- *RcfR-0007*: RCF shall have sufficient time delay buffers to compensate for DSA2000's maximum geometric delay, 50 µs
- *RcfR-0008*: Where RCF is required to generate beams from multiple antenna elements, it must be capable of compensating for both instrumental and geometric delays, up to 200 µs.

Implicit in the first requirement is a statement that RCF need not use time-delay buffers to compensate for all instrumental delays before emitting data to RCP. This substantially reduces the amount of high-bandwidth memory required by RCF, while still allowing glitch-less tracking

of any source. It is assumed that large - and mostly stable - instrumental delays corresponding to multiples of the channelized sample period may be absorbed into the RCP buffering system.

2.4.2 Fine Delay

For any digital system which implements time-domain delay compensation using a simple sample buffer, the precision of this correction is limited by the system sample rate. Errors of 0.5 samples in the delay applied to a complex data stream equate to residual phase errors over the Nyquist band being processed of up to $\frac{\pi}{2}$ radians (or $\frac{\pi}{4}$ for a real signal). In principle, this residual phase slope across the observing band may corrected in downstream processing outside of RCF. However, this requires that the downstream processor knows the delay applied to the data stream (and its resulting error) at any given time.

Processing is simplified if RCF implements a *fine-delay* - that is, a sub-sample delay which is applied as a phase to each frequency channel - within its processing pipeline.

A requirement is created to ensure that RCF implements a fine delay:

- *RcfR-0009*: RCF shall ensure that, after applying a delay correction to a data stream to phase it to a particular sky position, the residual error across any frequency channel shall be $< 1°$.

2.4.3 Fringe Rate

The delays required to phase-align signals from multiple antennas to a common reference are a function of the direction of the source being observed and thus changes with time.

The maximum rate at which RCF needs to update the delay applied to each antenna signal may be computed by considering the array's maximum *fringe rate*. This is the maximum rate at which the relative phases of signals from two antennas in the array changes through a phase of 2π radians.

Maximum fringe rate $f_{\max}$ is given by:

$$f_{\max} = \Omega_e \frac{B}{\lambda}$$

Where $\Omega_e = 7.27 \times 10^{-5}$ radians/second is the angular speed of the Earth, B is the maximum baseline length, and λ is the minimum observing wavelength.

For DSA2000, $B = 15$ km, $\lambda = 15$ cm, giving a **maximum fringe rate of 7.3 Hz**.

In order that, after correction, the relative phase of two antenna signals not change by more than $1°$ over time, delays must be updated at least 360 times every $\frac{1}{7.3}$ seconds. This yields the further requirement:

- *RcfR-0010*: RCF shall be capable of updating the delay applied to each antenna signal at least 2628 times per second.

2.5 Beamforming

ScR-0025 states that the DSA2000 system shall be capable of simultaneously forming beams with 4 different phase centers within the primary beam, and coherently dedispersing these time-streams. Dedispersion is the purview of the PT subsystem and is outside the scope of RCF. However, with the following requirement the formation of beams is explicitly made part of the RCF system:

- *RcfR-0011*: RCF shall form 4 dual-polarization voltage streams, using the *TC* data products defined by *RcfR-0004*.

2.6 Summary

The following table summarises the derived RCF requirements:

Subsystem Requirement	Description
RcfR-0001	RCF shall generate channels with width < 146.8 kHz over the frequency range 0.7 to 2.0 GHz.
RcfR-0002	RCF shall generate channels with width < 9.25 kHz over a tunable band with bandwidth ≥ 34 MHz between 0.7 and 2.0 GHz
RcfR-0003	RCF shall generate channels with width < 1.42 kHz over a tunable band with bandwidth ≥ 0.95 MHz between 0.7 and 2.0 GHz
RcfR-0004	RCF shall generate channels with width ≥ 2.048 MHz over the frequency range 0.7 to 2.0 GHz.
RcfR-0005	RCF shall generate channels which attenuate a signal at the center of an adjacent channel by ≥ 60 dB.
RcfR-0006	Over a period of 100 hours, the center frequency of any RCF frequency channel shall not shift by $> 10\%$ of the channel width.
RcfR-0007	RCF shall have sufficient time delay buffers to compensate for up to 50 µs delay in the time-domain for all data products.
RcfR-0008	Where RCF is required to generate beams from multiple antenna elements, it must be capable of compensating for delays up to 160 µs.
RcfR-0009	RCF shall ensure that, after applying a delay correction to a data stream to phase it to a particular sky position, the residual error across any frequency channel shall be $< 1°$.

Subsystem Requirement	Description
RcfR-0010	RCF shall be capable of updating the delay applied to each antenna signal at least 2628 times per second.
RcfR-0011	RCF shall form 4 dual-polarization voltage streams, using the *TC* data products defined by *RcfR-0004*.

3 Design

Here, the preliminary design of the Radio Camera Frontend (RCF) is described and justified.

3.1 Interfaces

The top-level RCF interfaces to other DSA2000 subsystems are shown in Figure 1 and are as follows:

1. Analog Signal Path (ASP): 4096 RF signals (two polarizations from each of 2048 dishes) are delivered by ASP, which must be digitized and processed by RCF.
2. Timing and Synchronization (TS): RCF receives timing signals from TS, and uses them to ensure coherent digitization and accurate timestamping of data streams.
3. Central Control Network (CNW): A 1 Gb Ethernet network responsible for delivering control messages to RCF.
4. Monitor and Control (MC): RCF receives and acts on commands from MC, and must be able to report its health status to MC. These commands are delivered via CNW.
5. Facilities (FAC): FAC provide the space, power, and cooling infrastructure to support RCF.
6. Signal Data Network (SNW): SNW is a 25/100/400 Gb/s Ethernet network responsible for transporting high-speed digital data products from RCF to RCP and PT. In addition, SNW provides data transmission paths between different RCF processors.
7. Radio Camera Processor (RCP): RCP receives channelized voltages from RCF, via the SNW network, and uses them to produce images and transient event data products.
8. Pulsar Timing (PT): PT receives channelized beam voltages from RCF, via the SNW network, and uses them to produce pulsar timing data products.

The basic specifications for these interfaces are described in Section 4.

3.2 Processing

The data products which must be produced by RCF are:

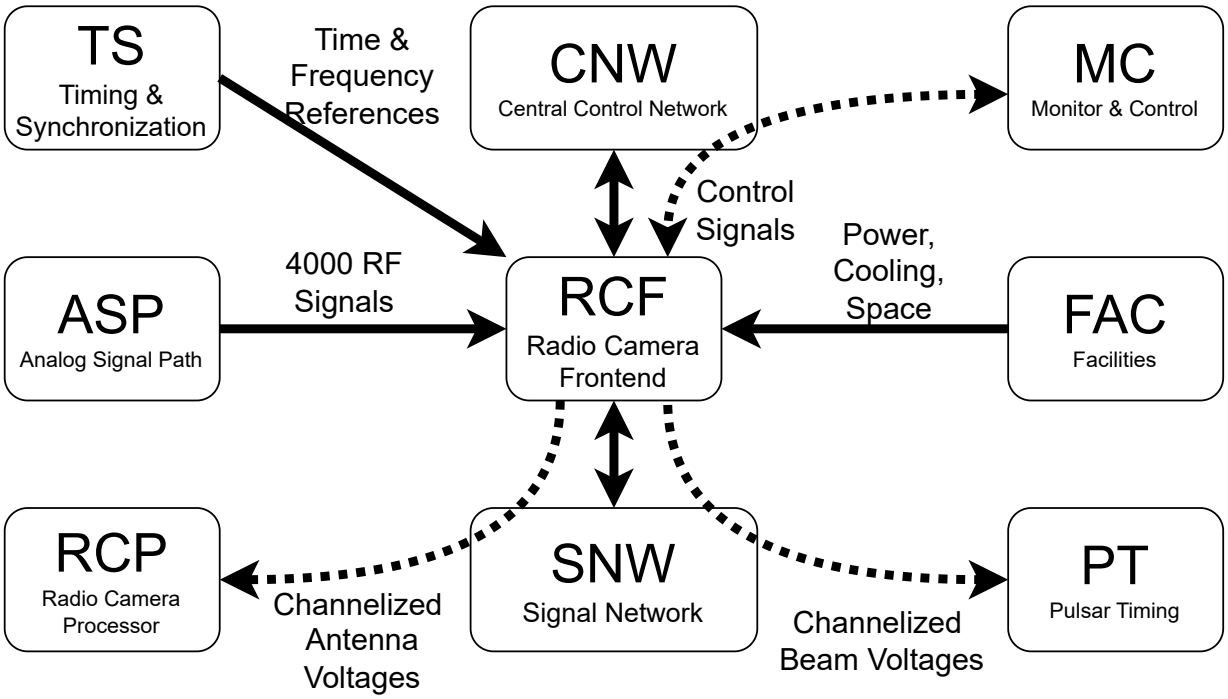

Figure 1: Top-level interfaces to the RCF subsystem. Interfaces which are logical only (MC, whose control messages are delivered via CNW, and RCP, whose data are delivered via SNW) are indicated with dotted arrows.

1. Complex-valued sample streams, representing voltage time series for each polarization, antenna, and frequency channel. These are used by RCP for image processing and transient searching. As discussed in Section 2.1, three different channelization products are required:
    1. Narrowband continuum (NC) channelized voltages, covering 700 - 2000 MHz, with a channel bandwidth of <146.8 kHz.
    2. Zoom band "A" (AC) channelized voltages, covering 1388 - 1422 MHz, with a channel bandwidth of <9.25 kHz.
    3. Zoom band "B" (BC) channelized voltages, covering 1419.93 - 1420.88 MHz, with a channel bandwidth of <1.42 kHz.
2. Complex-valued streams representing voltage time series from channelized, dual-polarization beams formed in 4 different directions. These are used by PT for pulsar timing. Each beam should cover the band 700 - 2000 MHz, with a channel bandwidth of >2048 kHz. It is assumed that the two polarizations of each beam will correspond to the native polarizations of the DSA2000 antennas.

3.3 Hardware

RCF requires hardware to digitize and process the 4096 RF signals provided by ASP. Since ASP is responsible for transporting all analog signals to a central processing facility, RCF is free to use a hardware architecture that requires that any number of signals be processed in each physical hardware module. However, for simplicity and modularity, the chosen RCF architecture is one which uses a separate "FPGA Station Module'' (FSM) to process a dual-polarization pair of signals from a single DSA antenna. This architecture thus requires 2048 FSMs (plus some provision of spares) to process signals from the full DSA telescope. Though this results in a larger number of modules than an equivalent architecture where multiple antennas are processed on common hardware, this design has the following beneficial features:

1. Manufacture of FSMs may make use of economies of scale, and leverage high unit-count component purchases.
2. Dependencies between signal paths from multiple antennas are removed, avoiding system control side effects - for example, the maintenance of one antenna's signal path affecting another.
3. Each FSM has a lower power-dissipation than a module which is tasked with processing signals from multiple antennas, simplifying thermal management.
4. FSMs need not use the most powerful FPGA components available, decreasing prototyping costs, and increasing production cost-efficiency, since more powerful FPGAs often have a higher cost-to-performance ratio than smaller parts.

The main drawbacks of such a system are

1. The increased number of endpoints which the monitor and control system must support.

2. The increased number of endpoints to which the timing distribution system must deliver timing signals.
3. The larger physical footprint of the system.

The first of these drawbacks is mitigated by the choice to use a control and monitoring system designed with scalability in mind. The second is not a significant issue, since the timing distribution system is not a major cost-driver of DSA2000 even in the case of distribution to 2048 endpoints. Finally, as is discussed in Section 3.3.4, the physical size of the RCF system is no a major cost driver for DSA2000. Further, a more compact architecture involving modules processing signals from multiple antennas would likely dissipate enough power per module that any significant compute-density savings could only be realised if significant engineering and infrastructure effort was invested in supporting water-cooling of the RCF system.

3.3.1 FPGA Station Module Design

The primary components of the FSM are an analog-to-digital converter (ADC), and a field-programmable gate array (FPGA) system-on-module (SoM). The former is responsible for digitizing the analog signals, and the latter is responsible for processing the digitized data and packaging them in Ethernet frames for transmission to SNW.

3.3.1.1 Analog-to-Digital Converter The selected digitizer is the ADI AD9207[3], which is a 12-bit ADC capable of sampling a pair of analog signals at up to 6 GS/s.

As well as simple digitization, the AD9207 has a variety of signal processing capabilities, including digital down-conversion and decimation (ADI 2023). These are leveraged by the RCF system in order that downstream DSP may operate on only the frequency range of interest, and at a lower sample rate. This is discussed in more detail in Section 3.4.

The AD9207 outputs digitized data using the industry-standard JESD204C interface, which is a high-speed serial interface capable of transporting data on up to 16 data lanes at up to 32 Gbps per lane. The AD9207 configuration required by RCF utilises a JESD204C interface to an FPGA on the FSM with 8 data lanes, and a lane rate of 13.2 Gb/s per lane.

3.3.1.2 FPGA System-on-Module FPGAs at a vast array of price points and performance levels and may be purchased in a variety of form factors. These include: 1. A packaged chip, for integration onto a custom board assembly 2. A System-on-module (SoM), which is a small board assembly designed to be integrated into a larger system, typically containing an FPGA and critical support infrastructure such as power supply circuitry and memory modules. 3. Complete processing platforms, ready to be deployed in the field.

[3] See https://www.analog.com/en/products/ad9207.html

The DSA2000 project places a high priority on rapid development and deployment, and for this reason the design of a completely custom FPGA board from scratch is not preferable. However, the project also has a very large number of signal paths, and thus needs to leverage custom interfaces (including backplanes and board-to-board connectors) in order to maximise the system density and minimise the number of cables needed to connect different system components. For this reason, the use of an off-the-shelf processing platform is also not preferable.

The compromise chosen is to use an FPGA SoM hosted on a custom carrier board. This provides the customisability of a dedicated board purpose-built for the DSA2000 project, while also leveraging the significant design and testing effort that has gone into the SoM designed commercially.

RCF has chosen the iW-RainboW-G35M SoM from iWave Systems Technologies[4] (Figure 2), populated with a Xilinx/AMD Zynq Ultrascale+ ZU11-EG System-on-Chip, which is, itself, a CPU and FPGA integrated into a single chip package.

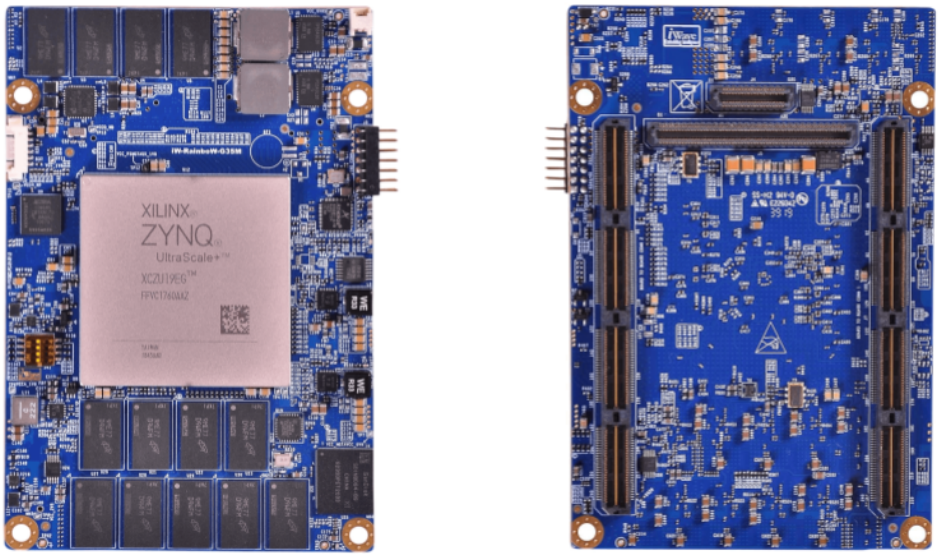

Figure 2: The top (left) and bottom (right) of the iW-RainboW-G35M system on module from iWave Systems Technologies. The module incorporates a Xilinx/AMD Zynq Ultrascale+ System-on-Chip with power and RAM support infrastructure on an assembly designed to be mounted to a larger circuit board. *Image credit: iWave System Technologies*}

The ZU11-EG is a mid-range FPGA, with 0.65 million logic cells, 2928 hardware DSP slices, and 43.6 Mb of dedicated on-chip RAM.

[4]See https://www.iwavesystems.com/product/zu19-zu17-zu11-zynq-ultrascale-mpsocsom/

3.3.1.3 FPGA Station Module Carrier Board With the FPGA SoM and ADC chip selected for RCF, a custom "carrier board" is required to host these components and provide physical interfaces to the other DSA2000 subsystems.

A block diagram of the FSM carrier is shown in Figure 3. The board has the following features:

1. Based around the 100 mm x 220 mm Eurocard form factor, which allows sufficient area for necessary components and can be vertically mounted in a 3U-high subrack of a standard 19" rack.
2. A backplane connector to allow power, timing reference signals (see (D'Addario 2023)), and control and monitoring signals – including a 1 Gb Ethernet connection – to be delivered to the FSM over a backplane with no cables.
3. Blind-mate coaxial connectors to allow RF signals to be delivered from an analog fiber receiver board to the FSM ADC without the need for cables.
4. A blind-mate connector carrying power and low-speed data (eg. I2C) to allow the FSM to supply power and a control and monitoring interface to a connected analog fiber receiver (FRX) board. The FRX is part of the ASP subsystem and is responsible for receiving analog-over-fiber signals from the DSA antennas and converting these to an electrical interface.
5. Basic peripherals for use during development, including an SD card form which the SoM CPU may be booted, and a USB serial interface for debugging.
6. Two QSFP28 connectors, providing up to 200 Gb/s of digital IO to the SNW network. These ports may be configured as either 25 GbE or 100 GbE links.
7. An RJ45 1 Gb Ethernet connector, providing a simple control and monitoring interface to the FSM which does not require the use of the backplane. This is intended to be used during development, with multiple boards sharing a single Ethernet connection via the backplane in production (see Section 3.3.3).

Since the FSM carrier board is relatively simple, it can be designed and tested in a short timeframe at a relatively low cost. Design of the carrier will likely be contracted to the SoM vendor, iWave Systems Technologies, who already have experience in designing carrier boards similar to that which RCF requires.

3.3.2 FSM 19" Subrack

It is desirable for FSMs - of which there are more than 2000 - to be mounted in a standard 19" equipment rack, in a manner that makes it as easy as possible to replace a faulty module.

FSMs are designed to be compatible with 19" subracks supporting the Eurocard standard. Such subracks are readily available from a variety of vendors, and are readily configurable to accommodate cards of different lengths and widths, with backplanes either conforming to an industry standard, or custom-designed to suit the needs of the system. An example of a 3U Eurocard subrack is shown in Figure 4.

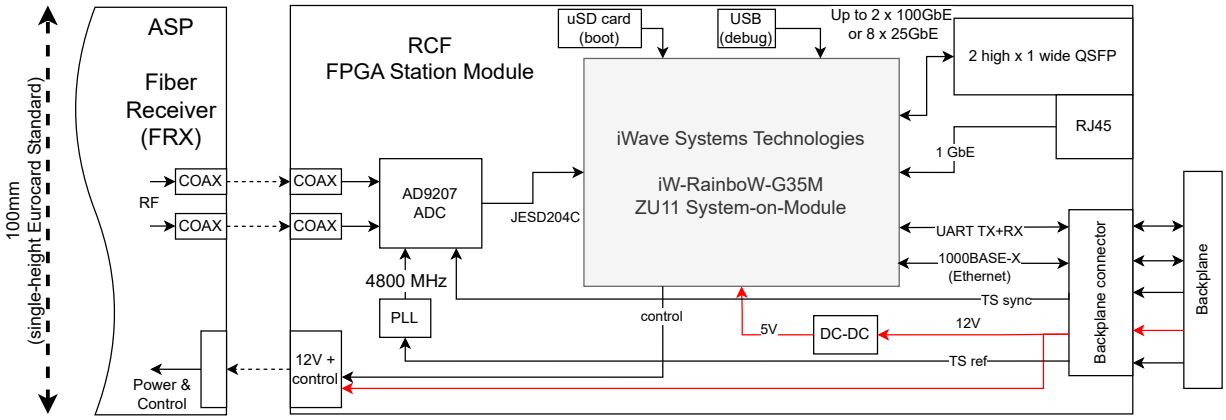

Figure 3: The FSM board, which hosts an AD9207 ADC chip and iWave ZU11-based System-on-Module, connected with an 8-lane JESD204C interface. Power connections are shown in red. The board features a backplane connector, through which power, timing references, and control signals may be delivered. The board interfaces with an analog fiber receiver (FRX, part of the ASP subsystem) via blind-mate connectors, avoiding the use of coaxial cables

Figure 4: A basic 3U eurocard chassis, with card guides installed to accommodate ten 1.6 inch (8HP) cards. *Image Credit: Leeman Geophysical LLC*

Multiple FSMs are slotted vertically into a subrack, whose backplane provides power, timing signals, and control interfaces to the modules. A fiber receiver board can then be slotted in front of the FSM in the same card guide slots passing analog signals to the FSM via blind-mate connectors.

Analog inputs are provided to each board assembly via optical RF connections on the front of the fiber receiver board. Digital data exits the board assembly via QSFP28 connectors on the rear of the FSM. To enable these connectors to be accessible, the rear of the subrack uses a backplane which only occupies the lower half of the subrack height. On the rear of the backplane, a pair of coaxial connectors provide timing signals from the upstream TS system, and high amperage connectors supply 12V power from external power supply units.

Each FSM is fitted with a finned heat-sink, and air is blown through the subrack from bottom to top using external fan trays (See Section 3.3.4). With heat-sinks fitted, the FSMs are 1.6 inches (8HP) wide, and thus 10 FSMs may be mounted in a standard 84 HP subrack.

3.3.3 Subrack Management Card

Since the RCF system contains more than 2000 FSMs, densely packed in a relatively small number of racks, it is desirable to avoid the need for each FSM to have a cabled 1 GbE control and monitoring connection. To this end, a "Subrack Management Card" (SRM, Figure 5) is included in each subrack, which uses a 1 GbE switch chip to allow all FSMs in a subrack to be reached via a single RJ45 Ethernet connection, via the subrack backplane. The SRM is not a critical part of the RCF design - all FSM boards have an RJ45 connector to allow each to be individually connected to the control network - but makes use of the fact that 4HP of spare space is available in each 10-FSM subrack.

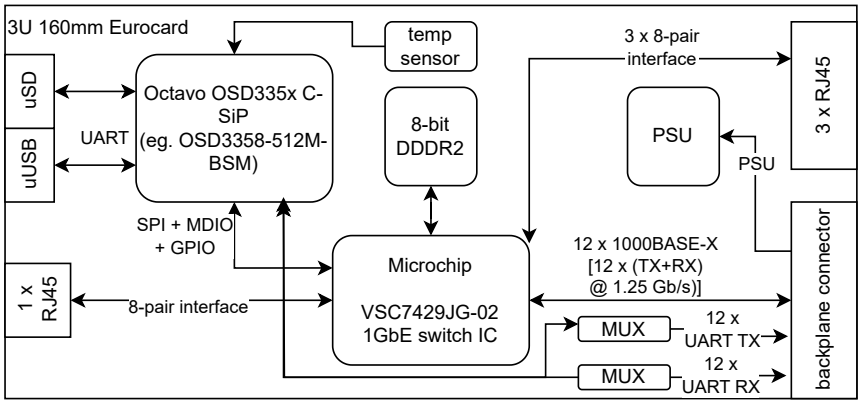

Figure 5: A "Subrack Management Card", which implements 1Gb Ethernet switching functionality to allow all RCF boards in a rack to be reached via a single RJ45 Ethernet connection.

The SRM also features a small CPU subsystem based on a single System-in-Package (SiP) chip, which facilitates connecting to the debug interfaces of the FSMs in the subrack. This feature - somewhat similar to the "out-of-band" management often supported by rack-mounted CPU servers - is designed to allow remote, low-level diagnostics in the event of any software issues which may render the FSMs unresponsive to their usual Ethernet control interface.

3.3.4 Rack Layout

The RCF design is based around an architecture which hosts 80 FSM boards in a standard height (42U) 19" equipment rack. Each rack services 80 dishes in the DSA2000 array, and 26 such racks are required for the full system. Since the number of dishes in the array is not a multiple of 80, one rack in the system will only be partially populated with 48 FSMs, leaving at least 11U of extra empty space in this rack. It is anticipated that this space will be utilized by the TS subsystem (D'Addario 2023). A fully-populated RCF rack servicing 80 dishes is shown in Figure 6.

RCF racks are designed to be used in a data center which provides front-to-back cooling. Since the FSM subracks are cooled bottom-to-top, air deflectors and 1U fan trays are used to channel cold air from the front of the rack and upwards through the subracks, with hot air exhausted from the rear of the rack. These deflectors and fan trays are off-the-shelf components, with the latter providing health monitoring capabilities.

12V DC power is provided to all subracks from a pair of 1U power supply units, which themselves contain multiple hot-swappable power supply modules configured to provide N+1 redundancy. It is estimated that each FSM will dissipate approximately 75W of power (with a further 7.5W dissipated by the 12V power supplies owing to conversion inefficiencies). This estimate is based on hardware tests of an iWave SoM and AD9081 ADC board[5], which yield a total power consumption of 50W in applications with similar requirements to RCF. A 50% margin is added to this figure to account for functionality not yet included in these tests, including the use of off-chip RAM and high-speed Ethernet interfaces.

The breakdown of power consumption in a fully-populated RCF rack is:

Component	Quantity	Unit Power (W)	Total Power (W)	Notes
FSM	80	75	6000	Estimated from development hardware tests using representative firmware
FSM	80	75	6000	Estimated from hardware tests
SRM	8	10	80	Estimate

[5]The AD9082 part is similar to the AD9207, but also includes digital-to-analog conversion capabilities, which RCF does not require. However, unlike the AD9207, the AD9082 is provided as a development board (AD9082-FMCA-EBZ, https://www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boards-kits/eval-ad9082.html) that can be used with iWave's off-the-shelf SoM evaluation kit.

Component	Quantity	Unit Power (W)	Total Power (W)	Notes
Fan Tray	4	97	388	Model Schroff 10713-554
Power Supply	2	304	608	10% inefficiency when supplying FSMs and SRMs
1 GbE switch	1	24	24	Model FS S3910-24TF
100 GbE switch	1	600	600	Model FS N8560-64C
RACK TOTAL			**7700**	

3.3.4.1 Beamformer Rack There is one further rack in the RCF system, which is configured differently to the others.

As discussed further in Section 3.4, RCF performs beamforming in two stages. The first stage beamforms signals from all dishes connected to a single rack. This substantially reduces the amount of data which needs to transported outside the rack. A second stage of beamforming is required to combine sub-array beams from each of the racks into full-array beams. This architecture is shown in Figure 7, and requires a rack configured as shown in Figure 8.

The architecture includes the provision of a small number of "hot" spares in each rack, so that beamforming performance degradation is limited to the loss of a single dish's input signals in the event that an FSM fails.

The signal processing required in the final beamforming stage is very simple, and involves simply summing the data received from each of the other racks. This processing could be performed on any of several off-the-shelf hardware platforms, but using the same FSM hardware as is present in the rest of the system (without fiber receiver cards) reduces the complexity of firmware development and operations.

In the final beamforming stage the quantity of hardware must be sufficient to sink 4.3 Tb/s of data. Since each RCF has two 100 GbE interfaces, at least 22 boards are required for this task. Since FSMs are hosted in subracks holding 10 boards, the beamforming rack holds 30 modules, providing several hot spares.

It is anticipated that each FSM in the beamforming rack will consume much less power than those in the other racks, since they have a much lower compute load. For this reason, only a single fan tray is used to cool three subrack enclosures.

Assuming a power budget of 40W per FSM, and 1500W for each PT server, the breakdown of power consumption in the beamforming rack is:

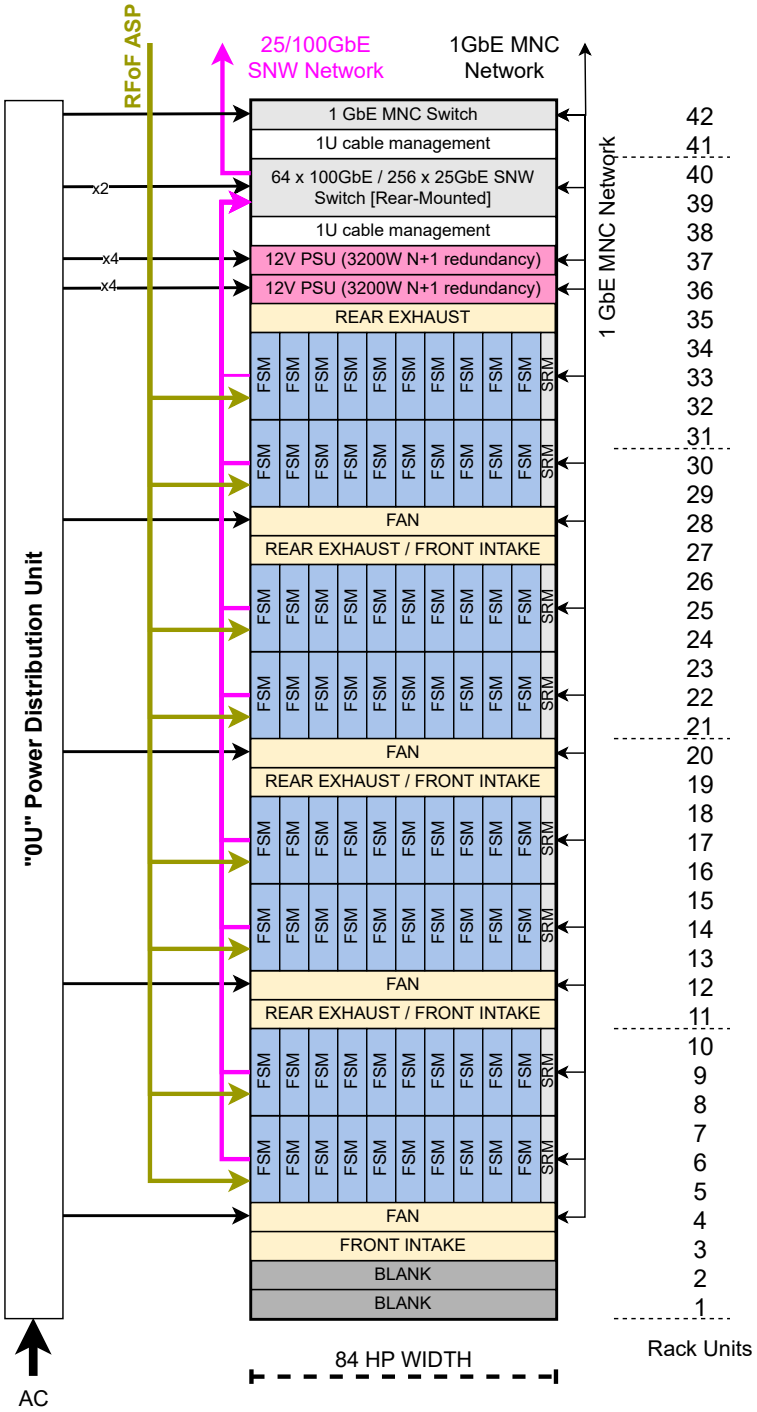

Figure 6: One of 26 racks in the RCF system servicing 80 DSA antennas. The rack comprises 8 3U subracks, each holding 10 FSM assemblies and an SRM board. Pairs of subracks are cooled bottom-to-top using 1U fan trays, with off-the-shelf air deflector trays redirecting airflow so that the rack-level cooling is from front to back. Discrete 1U multi-module power supplies are used to obtain N+1 redundancy and hot-swapability of power supply modules.

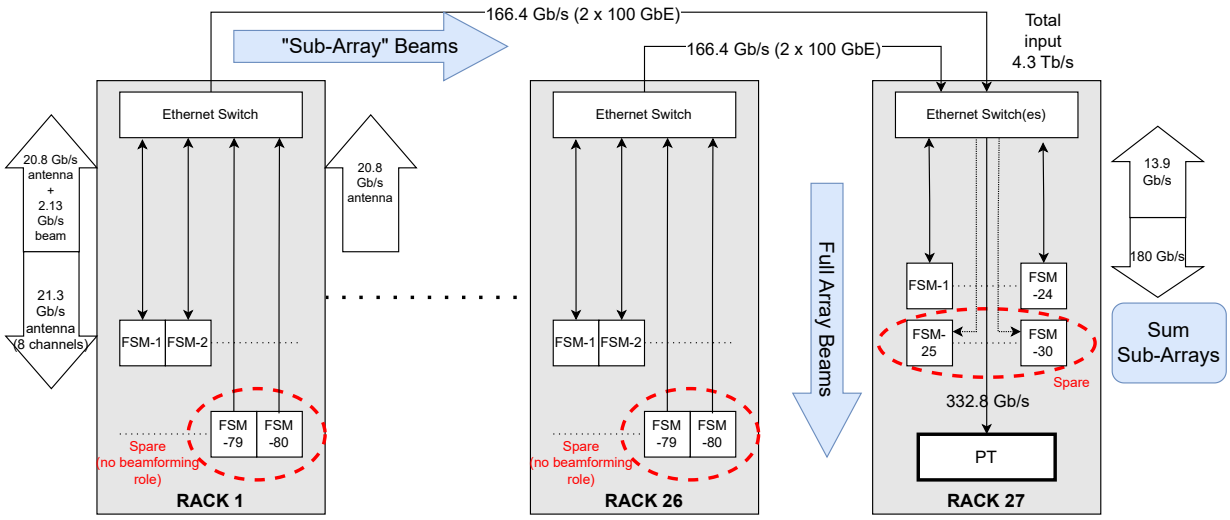

Figure 7: The RCF beamforming hardware architecture forms "sub-array" beams in each of 26 racks, and transmits these to a final rack to be summed into a full array beam and delivered to the PT subsystem. Since there are 2048 DSA antennas, one rack of the 26 is only partially filled, leaving space for TS hardware (D'Addario 2023)

Component	Quantity	Unit Power (W)	Total Power (W)	Notes
FSM	30	40	1200	Estimated from development hardware tests using representative firmware
SRM	3	10	30	Estimate
Fan Tray	1	97	97	Model Schroff 10713-554
Power Supply	1	123	123	10% inefficiency when supplying FSMs and SRMs
1 GbE switch	1	24	24	Model FS S3910-24TF
100 GbE switch	2	600	1200	Model FS N8560-64C
PT CPU/GPU Servers	4	1500	6000	Estimate
RACK TOTAL			**8644**	

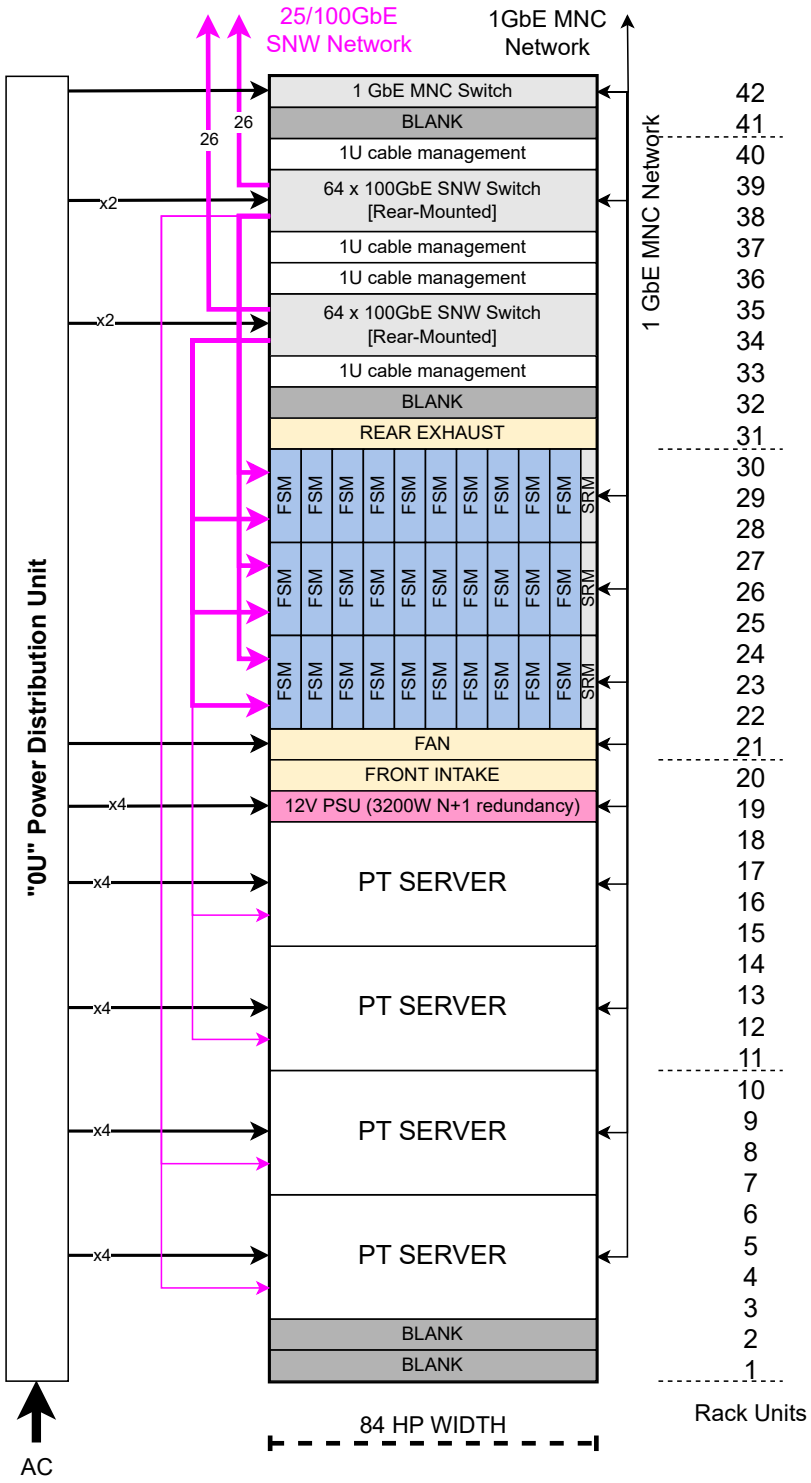

Figure 8: A dedicated beamformer rack holds networking hardware to receive beams formed in all the other racks in the RCF system, and further FSMs which act to sum these beams together. Final beam products are then output to servers which are part of the PT subsystem.

3.4 Firmware

In this section the digitization and processing methods used by the RCF firmware are described.

3.4.1 Digitization

Since the DSA's science band of interest is 700 - 2000 MHz, the simplest digitization configuration is to direct-sample these signals at at least twice the highest RF frequency - i.e., sample at at least 4000 Msps. The RCF design assumes that the sampling rate will be 4800 Msps, which results in analog anti-aliasing filter requirements which should be easy to meet.

Rather than pass the entire digitized band from the ADC chip to FPGA, the RCF leverages the mixing, filtering, and decimation capabilities of the ADC to reduce the bandwidth of the digitized data as early as possible in the processing pipeline. ADC signal processing configuration is shown in Figure 9.

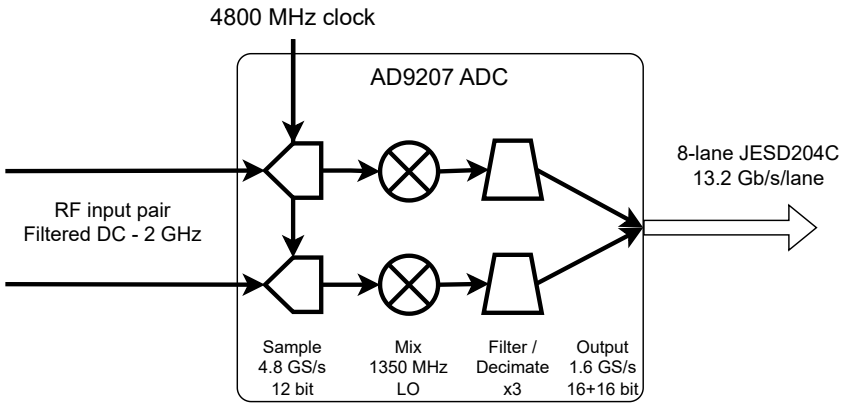

Figure 9: The configuration of RCF's AD9207 data path. RF signals are sampled at 4800 Msps, before being mixed, filtered, and decimated to deliver a 1600 MHz Nyquist band centred at 1350 MHz.

Analog samples are initially digitized at 4800 Msps with 12 bits of resolution, and then quadrature downconverted with a 1350 MHz digitally-generated LO, filtered, and decimated by a factor of 3 to produce a 1600 MHz Nyquist baseband centered at 0 Hz. The AD9207's decimation filters have a usable passband – defined as the region with better than 100 dB image rejection and less than ± 0.001 dB of passband ripple – of 81.4% (ADI 2023). For a sampling rate of 1600 Msps, this corresponds to a passband of 1302.1 MHz, which is sufficient to cover the 700 - 2000 MHz band of interest. This data is passed from ADC to FPGA as an 8-lane JESD204C interface running at 13.2 Gbps per lane.

3.4.2 Signal Processing

Once ADC sample streams for a polarization pair are received by a JESD204C receiver in the FPGA, they enter a signal processing pipeline which implements the following functions:

1. Time stamping, where a counter which represents the telescope's time is used to associate a precise timestamp with each ADC sample. A telescope time (TT) counter is maintained on each FPGA and all are synchronized by the TS system (D'Addario 2023). Timestamps is used to label data which are transmitted to downstream processors, and is also used internally to ensure proper timekeeping in the delay and phase tracking system.
2. Coarse delay correction up to 81920 ADC sampled (up to 51.2 µs at a sample rate of 1600 Msps).
3. First-stage Polyphase Filter Bank (PFB) generating 256 channels, each 8.33 MHz wide and overlapping by a factor of $\frac{4}{3}$.
4. Fine-Delay correction and phase-rotation, to allow the phase and delay of each signal path to be tracked as the sky rotates, and to allow small frequency shifts to be applied to each 8.33 MHz channel to allow potential compensation for any source Doppler shift.
5. Four parallel second-stage filterbank pathways, generating channels at NC, AC, BC, and TC resolutions, and removing the $\frac{4}{3}$ overlap between channels.
6. Requantization of output data to 4+4 bit complex resolution, after multiplication by a frequency-dependent gain factor that can be used to compensate for analog gain slope.
7. Packetization of data into a stream of UDP packets output to the SNW system over a pair of 25 GbE connections.
8. Beamforming of a frequency-subset of TC data from the 80 antennas which are serviced in the same equipment rack. These data are received via a 25GbE connection, and used to form 4 beams at 8+8 bit complex resolution. These data are transmitted back over 25 GbE to be summed by separate FPGAs in the beamformer rack (see Section 3.3.4.1)[6].

This signal processing pipeline is shown in block diagram form in Figure 10. Each processing block is described in more detail below.

3.4.2.1 Time Stamping Network Time Protocol ensures that the CPU subsystem on each FPGA board agrees the time to a precision better than 1 ms. However, this is not sufficient for precisely assigning a time to each ADC sample such that data processed by multiple FPGAs can be coherently combined. To enable timekeeping with the necessary accuracy, each FPGA maintains, in it's programmable fabric, a telescope time (TT) counter, which increments synchronously with ADC sampling. TT counters between multiple FPGAs are synchronized using a reference signal – planned to be a fast-rise 375 Hz clock – provided by the TS system. This system is described in

[6]The firmware running on the FPGAs in the beamformer rack simply receives data from multiple FPGAs, sums it without any further processing, and transmits (via SNW) to the PT system. The firmware running on these FPGAs is not discussed further here.

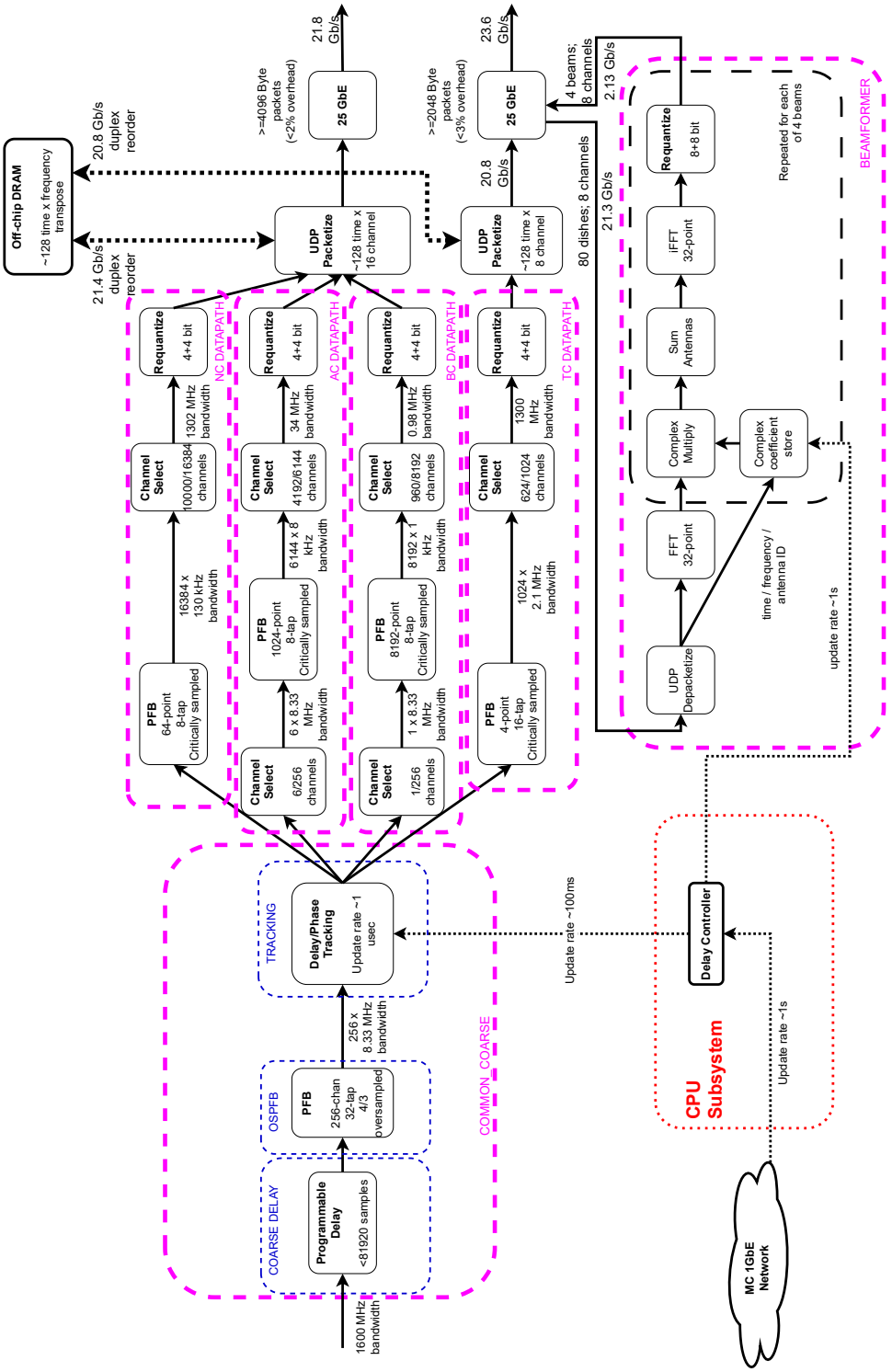

Figure 10: The FPGA signal processing pipeline, for each dual-polarization pair of dish signals.

detail in (D'Addario 2023). The TS sync reference is used to set each FPGA's TT counter with a particular ADC sample. Since edges of the 375 Hz reference occur at a larger separation than NTP precision, successive edges can be disambiguated using the local CPU's system time, and all FPGAs can agree to associate a common time to the ADC sample associated with any given edge. Future samples may be associated with TT by interrogating the value of an FPGA's TT counter.

Timestamps are carried with ADC samples through the processing pipeline, so that processing blocks which need to know the time associated with a sample (eg., the fine delay correction and phase rotation block) can do so.

3.4.2.2 Coarse Delay Correction

On-chip *UltraRAM* blocks are used to implement a coarse delay buffer for each of the two signal paths. These buffers are 640 kiB deep, and allow compensation for delays of up to 81920 samples (51.2 µs at a sample rate of 1600 Msps), satisfying requirement RcfR-0007.

3.4.2.3 First-Stage PFB

The first stage filterbank generates 256 channels, each 8.33 MHz wide and overlapping by a factor of $\frac{4}{3}$. The filterbank is 32-taps long, and uses a Hann window to generate channels with the response shown in Figure 11.

3.4.2.4 Fine Delay Correction and Phase Rotation

Fine delay correction and phase rotation are implemented as a multiplication of each 8.33 MHz channel with a unit-magnitude complex exponential.

The phase of this exponential varies over time, and compensates for the changing path lengths from source to antenna, as well as the related effects of the upstream digital LO.

A tiered approach to time-keeping is used to ensure that phasor values may be updated sufficiently quickly without the need for high data-rate communication between the RCF and MC subsystems.

1. Messages from MC to RCF are sent at a rate of ~1 Hz, and contain a delay polynomial which specifies the delay to be applied to a given antenna at a given time.
2. Every ~100ms, a CPU-based delay control module calculates the delay, phase, and per-spectrum delay-increment and phase-increment which should be applied to a pipeline's signals. This delay, phase, delay-rate, and phase-rate are written to FPGA registers, and a new coarse delay is set. A timed trigger is used so that all new parameters are applied to data simultaneously.
3. Every ~1 µs, the phasors to be applied to each 8.33 MHz channel are updated by the FPGA.

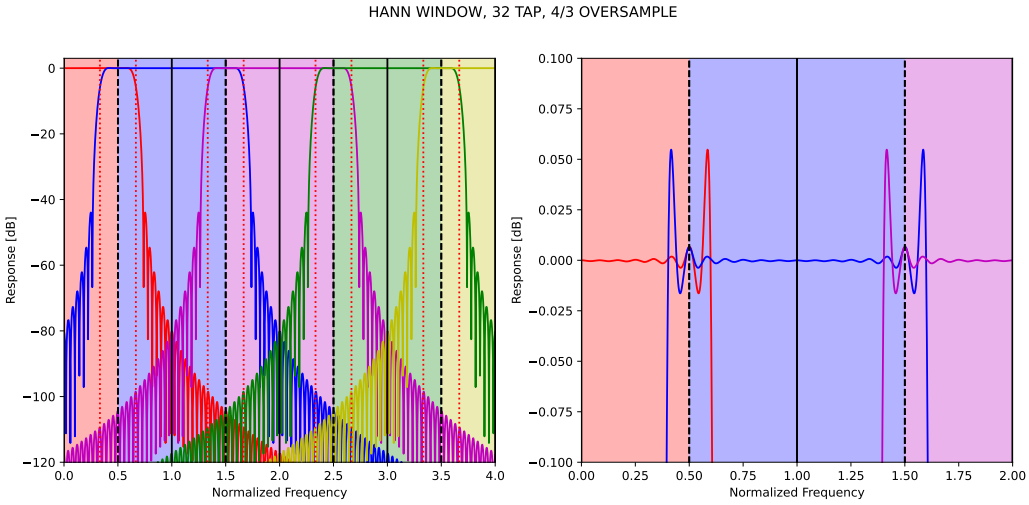

Figure 11: The PFB response of the 32-tap, Hann-windowed first stage filter, which is oversampled by a factor of 4/3. The frequency axis is normalized such that bins centers are separated by 1. Solid black vertical lines indicate location of bin enters. Shaded regions, bounded by dashed black vertical lines indicate the non-overlapping bin widths, which are 6.25 MHz wide. Dotted red vertical lines indicate the Nyquist boundaries of the overlapping bins, each of which is 8.33 MHz wide.

With this architecture, delays are updated at ~MHz rate, comfortably satisfying RcfR-0010. Delay-correcting 8.33 MHz channels also satisfies RcfR-0009 – that the phase error after delay application across a channel be $< 1\circ$ – since, at 1600 Msps – the sub-sample component of delay is 0.625 ns, which represents a maximum phase deviation from the center of an 8.33 MHz channel of $\pm 0.9°$.

3.4.2.5 Second-Stage PFB Second stage filters are constructed to generate the appropriate NC, AC, BC, and TC channelization products. The resolutions are shown below, and satisfy, respectively, RcfR-0001, RcfR-0002, RcfR-0003, and RcfR-0004.

Data Product	Required bandwidth (MHz)	Channel Bandwidth (kHz)	Number of channels	Total bandwidth (MHz)
NC	1300	130.2	10000	1302.1
AC	34	8.138	4192	34.1
BC	0.95	1.017	960	0.977
TC	1300	2083	624	1300
TOTAL (excluding TC)	1334.95	-	15152	1337.2
TOTAL	2634.95	-	15776	2637.2

Second-stage PFBs for the NC, AC, and BC channels are all 8-tap, Hann-filtered, and have a response shown in Figure 12.

The length of these filters is limited to 8-taps in order to fit in available FPGA RAM resources. The second stage TC filter is upchannelizes by only a factor of 4, and thus can be made longer while still fitting in a reasonable RAM footprint. The TC filter has 24 taps, and a response shown in Figure 13.

Other pulsar timing experiments have found it beneficial to tune passband shape to give better isolation at the expense of passband width (Bailes et al. 2020). If necessary, it is easy to modify the shape of the TC filters in a similar fashion, as shown in Figure 14, without impacting other data products.

3.4.2.6 Requantization Requantization of complex samples to 4 bits of precision per real and imaginary component is used to reduce the data output rate of each FPGA. Values are scaled using a frequency-dependent, runtime-programmable scaling factor, and then rounded, with saturation to value in the interval $[-7, 7]$. Though a 4-bit two's complement representation is able to use the value -8, this value is prohibited in order to maintain a symmetric quantization scheme. Instead, the 4 bit code "0b1000" is used to indicate that a value is not valid. This functionality, which is still in development, is intended to be used to support blanking data which are contaminated with interference.

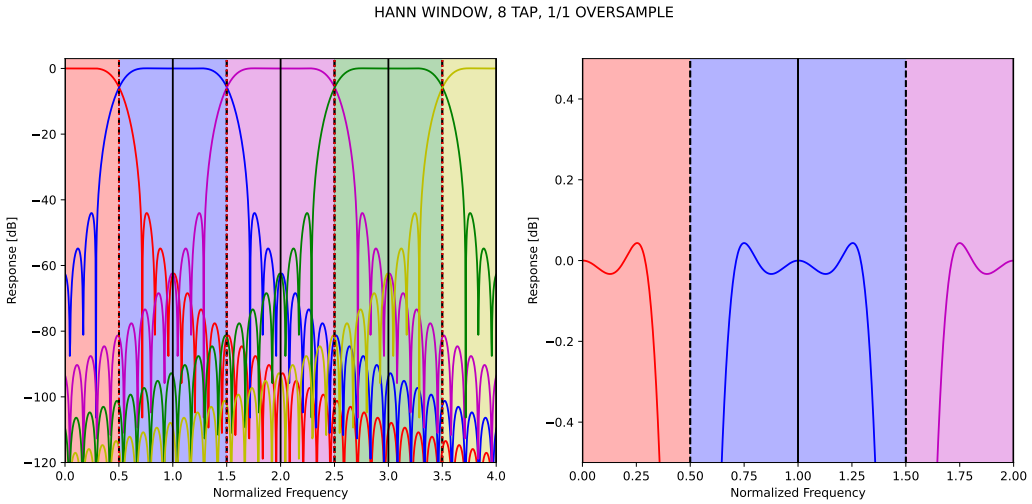

Figure 12: The PFB response of the second stage filters for NC, AC, and BC channelization products.

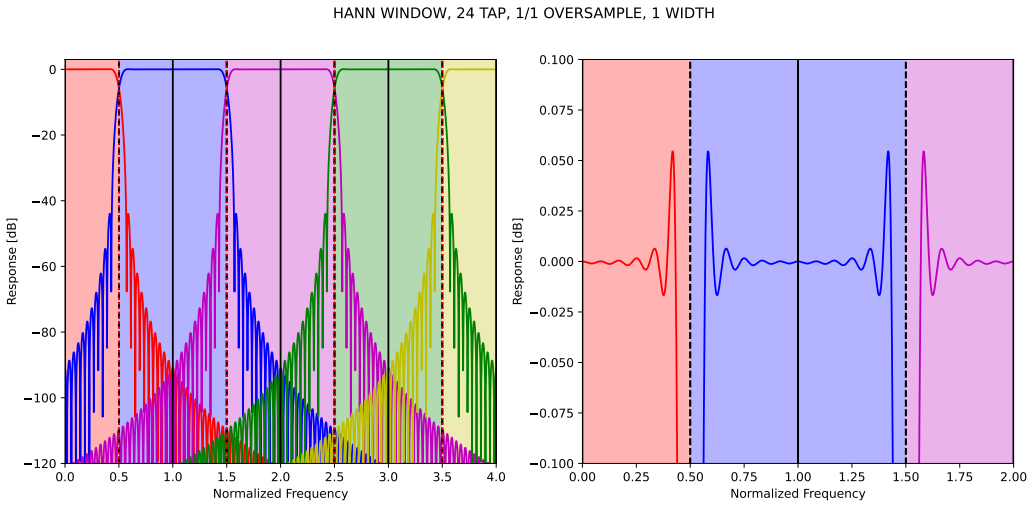

Figure 13: The PFB response of the second stage filters for TC channelization products.

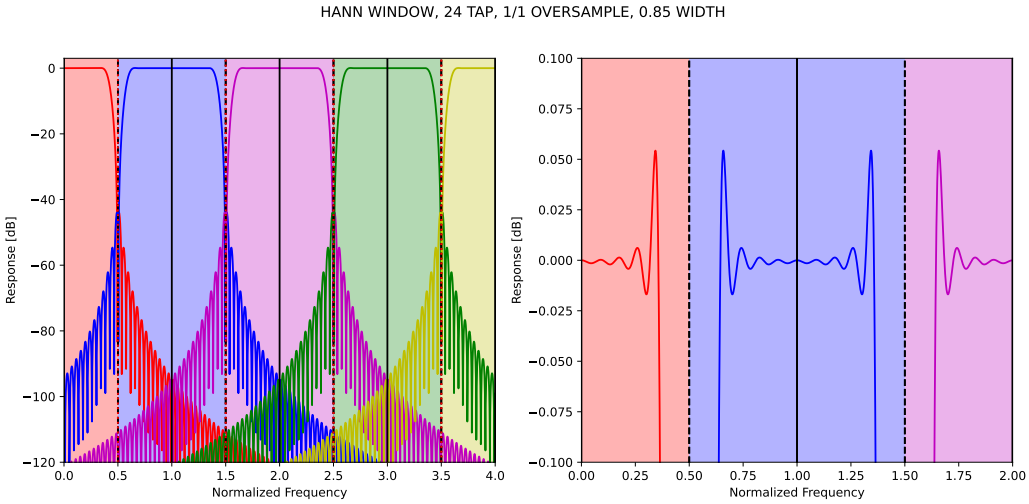

Figure 14: A possible PFB response of the second stage filters for TC channelization products with the filter passbands set to 85% of their usual width.

3.4.2.7 Packetization Data are reordered and packetized into a stream of UDP packets. Each packet contains a header which indicates the timestamp, source antenna and frequency channels present in the packet's payload. NC, AC, or BC data are transmitted over 25 GbE to destinations in the RCP system using the format described in (Hickish 2023). TC data are transmitted over 25 GbE to FPGAs within the same rack, such that each of 78 FPGAs in a rack receive 8 frequency channels of TC data from all dishes serviced by the rack.

Since data entering the packetization system has been quantized to 4+4-bit, it has substantially lower data rate than earlier in the system. This allows reordering to be carried out in high-capacity off-chip DDR4 memory, meaning that large data transpose operations are possible. This allows large packets (e.g. of 256 time samples and 16 frequency channels) to be generated and transmitted to RCP, reducing transmission and processing overheads.

In the case of TC packets, reordering in DDR4 memory means that there is a large amount of buffer space available to compensate for instrumental delays present in the analog system (RcfR-0008).

3.4.2.8 Beamforming The beamformer subsystem receives 8 TC channels of data from the 80 dual-polarization signals being processed in the local equipment rack, and uses these to form 4 sub-array beams.

It would be easiest to simply multiply TC channels by an appropriate complex-valued weight and sum them to form each beam. Unfortunately, this results in an unacceptable level of frequency smearing, given the broad bandwidth of the TC channels and wide field of view of the DSA dishes

(see Section 2.1). Instead, the beamformer implements a 32-point fast-convolution filter on each TC channel, effectively upchannelizing to 65 kHz, phase rotating, and then re-synthesizing 2.1 MHz channels.

Beam pointing delays are received from the TS subsystem and applied to data in a similar fashion to the fine delay correction and phase rotation module. However, since the data input to the beamformer have already been phased to the direction the array is pointing, required delay and phase update rates are relatively low.

Since the beamforming processing combines signals from 80 dishes, output data precision of 8+8 bit is maintained, to allow for an increase in signal-to-noise.

This 8+8 bit data, which totals 2.13 Gb/s from each FPGA in a rack and represents 4 dual-polarization beams, is transmitted over 25 GbE to the beamformer rack, where it is summed with data from other racks to form a full array beam at 16+16-bit precision (see Figure 7).

4 Dependencies and Assumptions

Dependencies of RCF on other DSA2000 subsystems are as follows:

4.1 Analog Signal Path (ASP)

1. ASP must deliver 4096 RF signals to RCF, with a bandwidth of 700 - 2000 MHz, compatible with a Nyquist bandwidth of 2400 MHz.
2. It is assumed that ASP will package fiber receiver boards so that they are compatible with blind-mate connection to the FSM single-height Eurocard boards.

4.2 Timing and Synchronization (TS)

1. TS should deliver a time reference “sync” signal which is resolvable at the precision of NTP.
2. The last stage of TS distribution hardware is integrated into the FSM subrack backplane, and TS hardware includes PLLs on the FSM carrier board. These need to be designed in collaboration with the RCF FSM system, which assumes that this backplane also delivers power and control signals. The full TS design is described in D’Addario (2023).

4.3 Central Control Network (CNW)

1. CNW is assumed to provide a 1 GbE network switch for each RCF rack with sufficient ports to connect all equipment in this rack. The preliminary design requires at least 16 RJ45 ports in each of the 27 RCF 19" equipment racks.

4.4 Monitor and Control (MC)

1. It is assumed that MC will deliver delay polynomials to RCF at a period of ~1 Hz.
2. It is assumed that MC protocols will be carried over the 1 GbE network provided by CNW.

4.5 Facilities (FAC)

1. 27 standard height (42U) 19" equipment racks are required by RCF.
2. Cooling is required for 26 these racks dissipating 7.7 kW each, and 1 rack estimated to dissipate 8.6 kW (including 6kW of PT equipment).
3. Cooling is assumed to be front to back, with “cold aisles” at the front of the racks and “hot aisles” at the back.

4.6 Signal Data Network (SNW)

1. SNW must provide a network switch in each of 26 racks capable of linking:
    1. 160 25 GbE links (to FSM boards)
    2. 2 100 GbE links (to RCF beamforming rack)
    3. at least 20 100 GbE links (or similar bandwidth; to RCP)
2. SNW must provide one rack – the “beamforming rack” – with two switches, each having at least 58 100 GbE ports.

4.7 Radio Camera Processor (RCP)

1. RCP is expected to receive UDP packets from RCF over an Ethernet network.
2. These packets hold 4+4-bit complex-valued samples in a format described in Hickish (2023).

4.8 Pulsar Timing (PT)

1. PT is expected to receive UDP packets from RCF over an Ethernet network.
2. These packets contain 16+16-bit complex-valued beam voltages, in a format yet to be defined.

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