Design of a boost converter fed by a single-phase diode rectifier

Group 9

Arthur Myhra
Elin Aune Forbord
Rebekka Færøyvik Olsen
Sander Olai Antun

April 9, 2022

TET4190
Norwegian University of Science and Technology

1. Abstract

In this project, the design process and simulations of a step-up boost converter fed by a full bridge rectifier is presented. To achieve a maximum of 5% output voltage ripple and $1A_{\text{peak-peak}}$ inductor current ripple, a 6μF output capacitor and 1.43mH inductor were chosen. Additionally, to keep the input voltage at a maximum of 3% ripple, the input capacitor was calculated to 30mF. The boost converter in this project has a maximum load current of 24A, and is operating in continuous conduction mode when supplying between 20-100% of this maximum load current. The switching energy losses were found through simulations in LTspice, and the conduction losses were calculated from the components respective data sheets. To minimize losses, a combination of SiC MOSFET and Si diode were chosen. To keep losses at a minimum, the switching frequency was calculated to 37.88 kHz. A heat sink with a thermal resistance of $0.72\frac{^\circ C}{W}$ was needed to keep the junction temperature of the converter at $150^\circ C$ at maximum load. When simulating, the efficiency of the converter was found to be 97.46% at maximum load, and inversely proportional with the load current.

Contents

2. Introduction

The goal of this project is to design a step-up boost converter to meet a set of criterias. The converter is to be supplied by a voltage of $230V_{RMS}$ at a frequency of 50Hz, with a ripple if no more than 3%. It should boost this voltage up to $V_o = 385V_{dc}$ with an output voltage ripple of no more than 5%. It should have a max inductor current ripple of $\Delta I_L = 1A_{peak-peak}$. The converter is supposed to be in continuous conduction mode (from now on shortened to CCM) when operating between 20-100% of its peak output current of $I_{o,max} = 24A$.

3. Size of load

The size of the load at $I_{o,max}$ for the converter can easily be found using ohm's law. Both the voltage over the load, and the maximum current delivered from the converter is given.

$$R_{load} = \frac{V_o}{I_{o,max}} = \frac{385V}{24A} = 16.04\Omega \tag{1}$$

4. Duty cycle

The duty cycle is found using equation 2 for step-up boost converters.[1, p. 173] The duty cycle only depend on the voltages the converter is intended to operate on.

$$\frac{1}{1-D} = \frac{V_o}{V_d} \tag{2}$$

The output voltage, V_o is given in the task description, but the average value of the input voltage, V_d, needs to be calculated. The peak value of V_d will be $\sqrt{2}$ times the RMS input voltage. With a maximum ripple of 3%, the lowest possible value of V_d will be $\sqrt{2} \cdot (1 - 0.03)$ times this peak value. Then the average value is approximated to the mean between these two values. See equation 3.

$$V_d = \frac{230 \cdot \sqrt{2} + 230 \cdot \sqrt{2} \cdot (1 - 0.03)}{2} = 320V \tag{3}$$

The duty cycle can then be calculated by rearranging and inserting values into equation 2. This gives the result shown in equation 4.

$$D = 1 - \frac{V_d}{V_o} = 1 - \frac{320V}{385V} = 0.169 \approx 0.17 \tag{4}$$

For this converter, a duty cycle of about 0.17 is needed to boost the voltage up to sufficient levels.

5. Losses of diodes and MOSFETs

Now that the duty cycle is found, the next step in the converter design process is to determine the losses of the different diodes and MOSFETs that are available for the project. The goal is to make the converter as efficient as possible, and hence the losses must be kept to a minimum.

To make for a easier reading, the product names of the different diodes and MOSFETs will not be used, but rather if they are of a silicon design (Si), or silicon carbide design (SiC).

Therefore the RFV15TG6S diode and IPP60R099C7 MOSFET will be referred to as Si, and the CVFD20065A diode and C3M0065090D MOSFET will be referred to as SiC.

5.1. Switiching losses - LTspice simulation

Simulations in LTspice were used to find the switching losses of the two diodes and the two MOSFETs when turning the semiconductor ON and OFF. A double pulse test was used to find both the on-losses and the off-losses.

The losses from one of the simulations done in LTspice is shown in figure 1. The switching energy losses was found by integrating the peaks of the power that flows in the MOSFET and the diode when the semiconductor is turned ON and OFF.

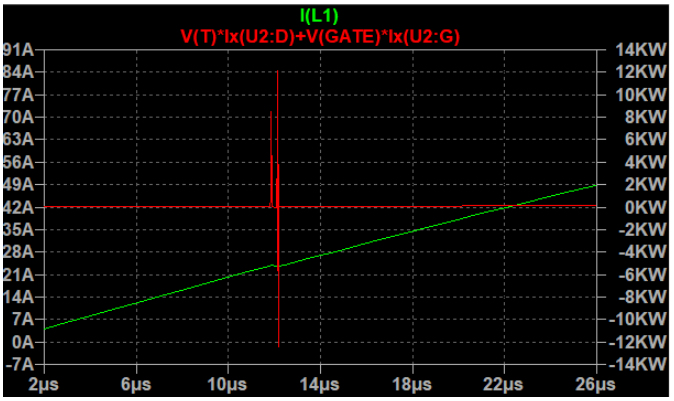

Figure 1: Simulation of the power to the SiC MOSFET in LTspice.

To better understand how the losses of the components behave, simulations with different load current magnitudes (I_o) were done. I_o = 20, 22, 24 and 26A where chosen for the simulation.

When a load current I_o flows at the output, a current I_d and I_{DS} will flow through the diode and MOSFET respectively. The current will practically be the same in the diode and the MOSFET, hence $I_d = I_{DS}$, see equation 5. When the MOSFET switches ON/OFF, the

current will just change direction. Therefore, the losses in LTspice was simulated using $I_d = I_{DS}$, not I_o.

$$I_d = I_{DS} = I_o \cdot \frac{V_o}{V_d} \tag{5}$$

The switching losses from the simulations are given in the tables below (see table 1 and 2).

Table 1: Switching energy losses ($E_{sw,M}$) for the MOSFETs from LTspice simulation.

MOSFET energy switching losses					
		$I_o = 20A$	$I_o = 22A$	$I_o = 24A$	$I_o = 26A$
Si	Off	191.4 μJ	193.6 μJ	234.6 μJ	258.1 μJ
	On	305.4 μJ	331.2 μJ	385.7 μJ	413.4 μJ
	Total	496.8 μJ	524.8 μJ	620.3 μJ	671.5 μJ
SiC	Off	317.9 μJ	377.7 μJ	458.9 μJ	518.1 μJ
	On	198.6 μJ	228.8 μJ	271.5 μJ	301.2 μJ
	Total	516.5 μJ	606.5 μJ	730.4 μJ	819.3 μJ

Table 2: Switching energy losses ($E_{sw,D}$) for the diodes from LTspice simulation.

Diode energy switching losses					
		$I_o = 20A$	$I_o = 22A$	$I_o = 24A$	$I_o = 26A$
Si	Off	1.1 μJ	1.2 μJ	1.3 μJ	1.7 μJ
	On	0.1 μJ	0.3 μJ	0.5 μJ	0.8 μJ
	Total	1.2 μJ	1.5 μJ	1.8 μJ	2.6 μJ
SiC	Off	8.3 μJ	8.0 μJ	7.8 μJ	7.7 μJ
	On	7.5 μJ	7.5 μJ	7.6 μJ	7.5 μJ
	Total	15.8 μJ	15.5 μJ	15.4 μJ	15.2 μJ

By observing the tables, it can be observed that the MOSFETs have a lot more switching losses than the diodes. This is expected since MOSFETs are an active component while diodes are passive. Active components contribute to more switching losses.

5.2. Conduction losses - data sheets

From the given data sheets the conduction losses (P_{cond}) for the MOSFETs and the diodes can be calculated. Since the components are from different manufacturers, there are different methods for obtaining these losses.

Using equation 5, 6 and 7 the RMS current through the MOSFETs ($I_{DS,RMS}$) can be found. The ON-resistance (R_{DS}) can be found using diagram 7 in the Si MOSFET data sheet,[2] and figure 5 in the data sheet for the SiC MOSFET.[3]

$$I_{DS,RMS} = \sqrt{\frac{1}{T_s} \cdot \int_0^{T_s} i_{DS}^2 dt} = I_{DS} \cdot \sqrt{\frac{1}{T_s} \cdot \int_0^{T_s \cdot D} 1 dt} \tag{6}$$

$$I_{DS,RMS} = \frac{V_o}{V_d} \cdot I_o \cdot \sqrt{\frac{1}{T_s} \cdot (T_s \cdot D - 0)} = \frac{V_o}{V_d} \cdot I_o \cdot \sqrt{D} \tag{7}$$

When R_{DS} and $I_{DS,RMS}$ is known, $P_{cond.M}$ for the MOSFETs can be found using equation 8.[1, p. 588]

$$P_{cond,M} = R_{DS} \cdot {I_{DS}}^2 \tag{8}$$

It is worth noting that the data sheets are using different testing conditions. The ON-resistance of the Si MOSFET is given for $T_j = 125°C$. Therefore it can be expected that R_{DS}, and consequently $P_{cond,M}$, can be slightly higher then calculated when operating at $T_j = 150°C$.

Table 3 shows the calculated conduction losses for both the MOSFETs for all of the four current magnitudes used in LTspice.

Table 3: $P_{cond,M}$ of the two MOSFETs calculated from the data sheets. NOTE: The test conditions for the Si MOSFET are $T_j = 125°C$ and $V_{GS} = 20V$, while the SiC MOSFET is tested at $T_j = 150°C$ and $V_{GS} = 15V$.

MOSFET conduction losses				
	$I_o = 20A$	$I_o = 22A$	$I_o = 24A$	$I_o = 26A$
Si	18.50 W	22.81 W	27.33 W	32.45 W
SiC	8.99 W	10.98 W	13.18 W	15.61 W

The losses in the diode can be found using equation 9. [4, p. 6] Here V_f is the voltage drop over the diode, and R_f is the resistance. Both for when the diode is conducting from cathode to anode.

$$P_{cond,D} = V_f \cdot I_{D,avg} + R_f \cdot I_{D,rms}^2 \tag{9}$$

For the SiC diode, R_f and V_f was found using the given equations on page 6 in its data sheet, with a junction temperature of $T_j = 150°C$.[5] See equation 10 and 11.

$$V_f = 1.0081 + (T_j \cdot -1.6 \cdot 10^{-3}) \tag{10}$$

$$R_f = 0.0146 + (T_j \cdot 1.7 \cdot 10^{-4}) \tag{11}$$

However for the Si diode, interpolating the forward current to forward voltage graph is needed to obtain R_f and V_f.[6] Equation 9 was used for both the SiC and Si diode after R_f and V_f was known.

Table 4 shows the calculated conduction losses for both diodes for all of the four current magnitudes used in LTspice.

Table 4: $P_{cond,D}$ for the two diodes calculated from the data sheets.

Diode conduction losses				
	$I_o = 20A$	$I_o = 22A$	$I_o = 24A$	$I_o = 26A$
Si	19.87 W	23.61 W	27.67 W	32.03 W
SiC	34.65 W	40.24 W	46.23 W	52.57 W

5.3. Total losses - choosing MOSFET and diode

Now that the losses of the MOSFETs and diodes are known, the total loss in watts can be found. The relation between the switching frequency, switching losses, and conduction losses is used to obtain an equation for the total losses, see equation 12 and 13.

$$P_{cond} = E_{sw} \cdot f_{sw} \tag{12}$$

$$\Rightarrow P_{tot} = P_{cond} + E_{sw} \cdot f_{sw} = 2 \cdot P_{cond} \tag{13}$$

Using these equations, a graphical representation of how the different combinations of components would behave is shown in figure 2.

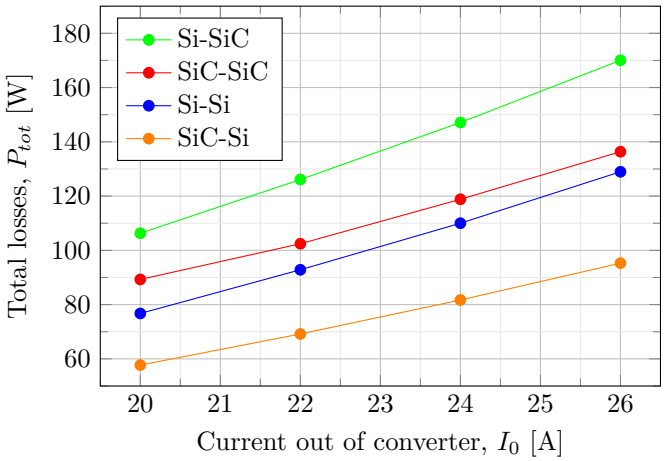

Figure 2: Total losses for the four different combinations of components.

It is quite clear from the figure that using a SiC MOSFET and Si diode is the best combination of components to minimize the losses for the converter. The SiC-Si combinations is both the one with the lowest total losses, as well as showing a lower growth rate than the ones with a Si MOSFET.

6. Frequency

Now that the MOSFET and diode is chosen, the frequencies of the converter can be found.

6.1. Frequency after rectifier

The converter will be connected to an input voltage operating at 50Hz. We know that for a full bridge rectifier, the frequency gets doubled [7], therefore the input frequency after the rectifier (f_{d2}) is:

$$f_{d2} = f_d \cdot 2 = 100Hz \tag{14}$$

6.2. Switching frequency of MOSFET

The switching frequency is determined by setting the total conduction losses at maximum load current ($I_o = 24A$) equal to the total switching losses. The switching losses for the MOSFET and diode accordingly, can be found in table 1 and table 2, with I_o equal to 24A. Putting these values into equation 12, the switching frequency at which the conduction losses are equal to the switching losses can be calculated to 37.88kHz, see equation 15.

$$f_{sw} = \frac{P_{cond}}{E_{sw}} = \frac{27.67W}{730.4\mu J} = 37.88kHz \tag{15}$$

7. Inductor and capacitor

7.1. Calculating inductance and capacitance

Since both of the frequencies now are determined, the size of the conductor and both capacitors can be calculated. By rearranging the inductor equation, an equation for the inductor can be found. See equation 16, 17 and 18. All values needed have been found and presented earlier in the project report.

$$v_L = L \cdot \frac{di_L}{dt} \Rightarrow V_d = L \cdot \frac{\Delta I_l}{\Delta t_s} \tag{16}$$

$$L = V_d \cdot \frac{\Delta t_s}{\Delta I_L} = V_d \cdot \frac{D \cdot \frac{1}{f_{sw}}}{\Delta I_L} \tag{17}$$

$$L = 320V \cdot \frac{0.17 \cdot \frac{1}{37.88 \cdot 10^3 Hz}}{1A} = 1.43mH \tag{18}$$

By rearranging the capacitor equation, an equation for the input capacitor (C_{in}) can be found using known values. See equation 19, 20 and 21.

$$i_c = C \cdot \frac{dv_c}{dt} \Rightarrow I_d = C_{in} \cdot \frac{\Delta V}{\Delta t} \tag{19}$$

$$C_{in} = I_d \cdot \frac{\Delta t}{\Delta V} = I_d \cdot \frac{\frac{1}{f_{d2}}}{3\% \text{ of } V_d} \tag{20}$$

$$C_{in} = \frac{28.875A \cdot \frac{1}{100Hz}}{3\% \cdot 320V} = 30mF \tag{21}$$

Finally for the output capacitor (C_{out}), the same analogy can be used. Rearranging the capacitor equation, and using the calculated duty cycle and switching frequency, the needed size of C_{out} can be found. See equation 22, 23 and 24.

$$i_c = C \cdot \frac{dv_c}{dt} \Rightarrow I_o = C_{out} \cdot \frac{\Delta V}{\Delta t} \tag{22}$$

$$C_{out} = I_o \cdot \frac{\Delta t}{\Delta V} = I_d \cdot \frac{D \cdot \frac{1}{f_{sw}}}{5\% \text{ of } V_o} \tag{23}$$

$$C_{out} = \frac{24A \cdot 0.17 \cdot \frac{1}{37.88 \cdot 10^3 Hz}}{0.05 \cdot 385V} = 5.60\mu F \tag{24}$$

7.2. Capacitor configuration

For the input capacitor, a capacitance of 30mF is needed. This can be achieved by using three capacitors of the type EPCOS B43484 with a capacitance of 10000µF = 10mF in parallel. This capacitors are chosen due to their large capacitance and ease of use when mounting.[8]

For the output capacitor, a capacitance of 5.60µF is needed. But to lower the cost of the converter, and to make for a simpler design, two capacitors of the type TDK B58035U*FA3 with a capacitance of 3µF each is used in parallel, for a total of 6µF. The margin of error is under 10% of the calculated capacitance, and reduces the number of needed capacitors.[9]

8. Heat sink

To keep the junction temperatures of the diode and MOSFET below $150°C$ a heat sink is added. The resulting thermal circuit of this is shown in figure 3.

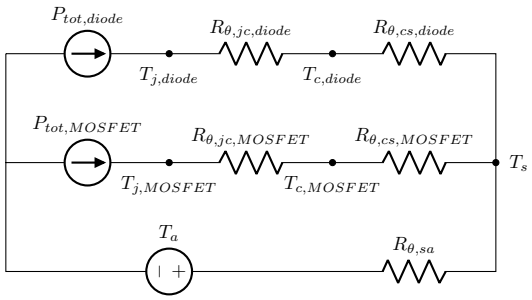

Figure 3: The thermal circuit when a heat sink is added.

To calculate the dimension of the heat sink, the thermal resistances from junction to case of the MOSFET and diode are needed, which can be found in the data sheets.[3][6] They are given as $R_{\theta,jc,MOSFET} = 1\frac{°C}{W}$ and $R_{\theta,jc,diode} = 1.2\frac{°C}{W}$

The thermal circuit can be solved equivalently to an electric circuit, meaning the formula needed to find the thermal resistance of the heat sink is the following equation 25.

$$R_{\theta,ca} = \frac{T_c - T_a}{P_{tot}} \tag{25}$$

Where T_c is different for the two components and can be found using equation 26.

$$T_{c,x} = T_{j,max} - P_{tot,x} \cdot R_{jc,x} \tag{26}$$

This will give one solution for each of the components. To dimension the heat sink correctly, the thermal resistance needs to be the lower of the two to solutions, so the heat sink is able to keep both junctions below $150°C$. In this circuit the diode is the limiting factor. Resulting in this thermal resistance.

$$R_{\theta,ca} = \frac{150°C - 55.34W \cdot 1.2\frac{°C}{W} - 25°C}{81.7} = 0.72\frac{°C}{W} \tag{27}$$

The connection between junction temperature and load current can be visualized by plotting them against each other using equation 28.

$$T_{j,x} = P_{tot,x} \cdot R_{\theta,jc,x} + P_{tot} \cdot R_{\theta,ca} + T_a \tag{28}$$

Using this formula for the load currents from 20 to 100% of maximum load current and plotting the results for each of the components, gives the graph in figure 4.[1, p. 734]

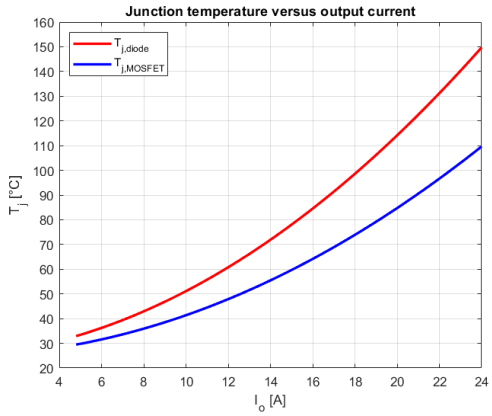

Figure 4: Plot of junction temperature for load current in range of 20 to 100% of maximum load.

9. Simulations

The SiC/SiC model was used instead of SiC/Si for the simulations due to recurring error in LTspice with the SiC/Si model. This means that the calculated switching frequency, and size of the inductor and output capacitor will not be a perfect match for the model used in the simulations. This means that some results may be slightly wrong.

9.1. Boundary Between Continuous and Discontinuous Conduction Mode

At the edge of continuous conduction, the current through the inductor i_l goes to zero after each time period. Since i_l reaches zero at the end of the interval, the average current I_{oB} is half of the peak value. The peak current can be found by using the inductor equation $v_l = L \cdot \frac{di_l}{dt}$, where the change in current will be the peak value, and the change in time will be t_{on}. Turn-on time is found by multiplying one full period with the duty cycle. Finally I_{oB} is this current times $(1-D)^2$, since $V_d = (1-D) \cdot V_o$ and $I_o = (1-D) \cdot I_d$ when assuming $P_{in} = P_{out}$. I_{oB} can therefore be calculated as shown in equation 29 and 30.

$$I_{oB} = \frac{T_s \cdot V_o}{2 \cdot L} \cdot D \cdot (1-D)^2 \tag{29}$$

$$I_{oB} = \frac{\frac{1}{37.88kHz} \cdot 385V}{2 \cdot 1.43mH} \cdot 0.17 \cdot (1-0.17)^2 = 0.416A \tag{30}$$

When simulated in LTspice, R_{load} is set to $\frac{385V}{0.416A} = 925.48\Omega$ to observe the waveforms of the inductor current during boundary conditions.

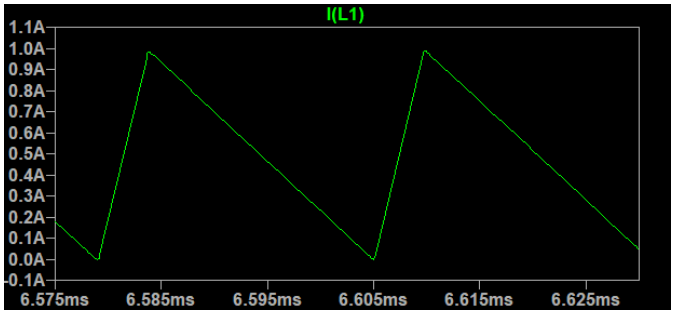

Figure 5: Inductor current at boundary conditions for SiC/SiC model.

The simulated waveforms behaves as expected, they reach zero at the end of each period, but are not zero over a longer period of time.

9.2. Steady-state results

9.2.1. Inductor and capacitor ripple as function of increasing load current

When the ripple of the output capacitor and inductor as a function of load current was to be obtained, a variable load resistance was used in LTspice. Adjusting it from to 16.04 to 80.20Ω, led to a load current varying from 4.8 to 24A, or 20-100% of max output current.

For the inductor current, it can be seen in figure 6 that the ripple is stable around 1A, just as the project description asked for.

On the other hand, the output voltage ripple varies linearly with input current. When increasing I_o it is expected that the ripple will increase, but not to more than 5%. This can be seen in Figure 6, the ripple does increase quite linearly with the load current, and is approximately within 5% of V_o as I_o increases. It should be mentioned that all components are designed for a different model than the one used for the simulations. This could be a reason for why the ripple slightly exceeds the limit of 5%.

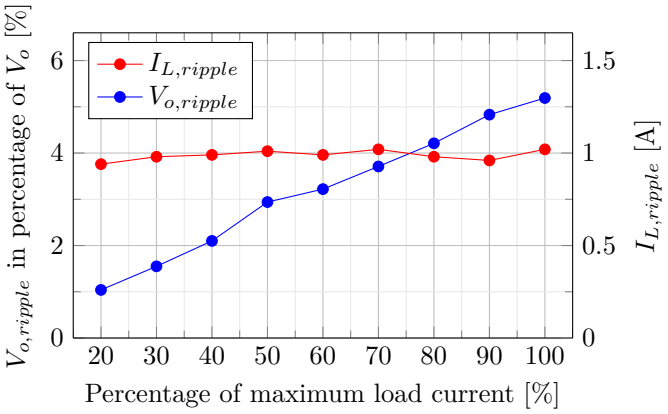

Figure 6: Ripple in output voltage and inductor current for an load between 20-100% of maximum output for the converter.

From equation 31, it can be observed that the inductor ripple varies with the input voltage, duty cycle, switching frequency and inductor size, which all are constant with increasing current. This just proves that the results from the simulation shown if figure 6 makes sense.

$$\Delta I_L = V_d \cdot \frac{D \cdot \frac{1}{f_{sw}}}{L} \tag{31}$$

The output voltage ripple varies linearly with input current, as shown in equation 32. When increasing I_o it is expected that the ripple will increase, just like it did in the simulations shown in figure 6.

$$\Delta V_c = I_o \cdot \frac{D \cdot \frac{1}{f_{sw}}}{C_{in}} \tag{32}$$

9.2.2. Efficiency and total losses

The total losses consists of the switching and conduction losses in the MOSFET and diode, as well as total simulated losses from the diode rectifier. As explained earlier, and shown in equation 13, the switching and conduction losses are equal. The conduction losses were found for load currents varying from 20-100% of maximum, with 20% intervals. The conduction losses were calculated the same way as shown in section 5.

To find the losses in the diode bridge rectifier, the simulation of the boost converter was run for a few 100Hz periods. This was to achieve steady state operation, and correct average power loss in the rectifier bridge. Table 5 show the losses in different parts of the converter, as well as total losses for different percentages of max load current.

Table 5: Total switching energy losses, conduction losses and rectifier losses for different % of max load current.

% of $I_{o,max}$	P_{sw}	P_{cond}	P_{rect}	$P_{loss,tot}$
100 %	46.21 W	46.21 W	148.49 W	240.91 W
80 %	32.53 W	32.53 W	107.13 W	172.19 W
60 %	21.06 W	21.06 W	71.18 W	113.30 W
40 %	11.81 W	11.81 W	41.41 W	65.05 W
20 %	4.80 W	4.80 W	18.66 W	28.26 W

The efficiency of the step-up boost converter was calculated by dividing P_{out} by P_{in}. P_{out} was obtained by multiplying the square of the load current by the load resistance. Then P_{in} was found by adding the losses from the rectifier, switching losses and conduction losses to the power delivered at the output. The efficiency for different percentages of load current are shown in table 6. A plot of the efficiency and total losses as function of increasing load current is shown in figure 7.

Table 6: The efficiency of the converter for different % of maximum load current.

% of $I_{o,max}$	P_{in}	P_{out}	Efficiency
100 %	9479.95 W	9239.04 W	97.46 %
80 %	7563.42 W	7563.42 W	97.72 %
60 %	5658.11 W	5544.81 W	98.00 %
40 %	3760.67 W	3695.62 W	98.27 %
20 %	1877.30 W	1848.04 W	98.49 %

From the table and figure it can be seen that the converter has an efficiency of 97.46% at maximum load current, and that the efficiency is inversely proportional to the load current.

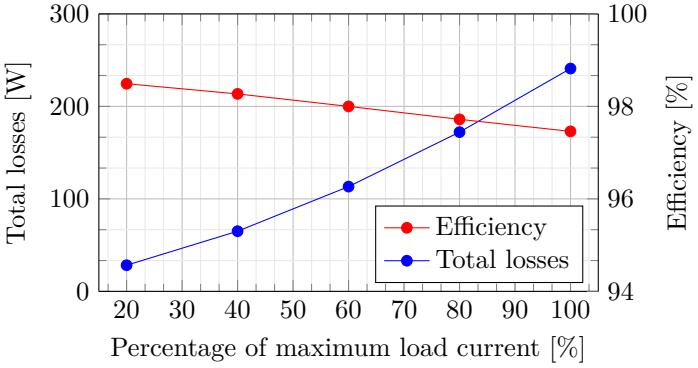

Figure 7: Efficiency and total losses for the step-up boost converter.

10. Conclusion

In this project a step-up boost converter has been designed and simulated. There was a set of given requirements that needed to be taken into account in the design process. The goal was to get a converter that fit the design criterias, and for the converter to be in CCM in 20-100% of the peak output current of $I_{o,max} = 24A$. The combination of SiC MOSFET and a Si diode where chosen due to their lowest overall losses. The efficiency of the converter was 97.47% at maximum load current, and inversely proportional with the load current. To get the output voltage ripple at a maximum of 5% and the inductor current ripple to $1A_{peak-peak}$, a 6μF output capacitor and a 1.43mH inductor was chosen. To keep the junction temperature to a maximum of $150°C$ a heat sink with a thermal resistance $0.72\frac{°C}{W}$ was calculated to be sufficient for the converter design.

References

[1] Ned Mohan, Tore Undeland, and William P. Robbins. *Power Electronics: Converters, Applications, and Design*. John Wiley & Sons, Inc, third edition edition, 2003.

[2] Infineon Technologies. Datasheet for MOSFET CoolMOS^{TM} C7, IPP60R099C7, 05-2015.

[3] CREE. Datasheet for Silicon Carbide Power MOSFET C3M0065090D, 03-2017.

[4] STMicroelectronics group of companies. Calculation of conduction losses in a power rectifier, 2011. URL `https://www.st.com/resource/en/application_note/an604-calculation-of-conduction-losses-in-a-power-rectifier-stmicroelectronics.pdf`.

[5] CREE. Datasheet for Silicon Carbide Schottky Diode, CVFD20065A, 08-2016.

[6] ROHM Semiconductor. Datasheet for Super Fast Recovery Diode RFV15TG6S, 07-2016.

[7] electronics tutorials. Full wave rectifier, 2014. URL `https://www.electronics-tutorials.ws/diode/diode_6.html`.

[8] EPCOS. Datasheet for Aluminum electrolytic capacitors, Capacitors with screw terminals, Series/types: B43464, B43484, 02-2014.

[9] TDK Electronics AG 2019. Datasheet CeraLink, Capacitors for fast-switching semiconductors, Flex Assembly (FA) series, B58035U*, 09-2019.