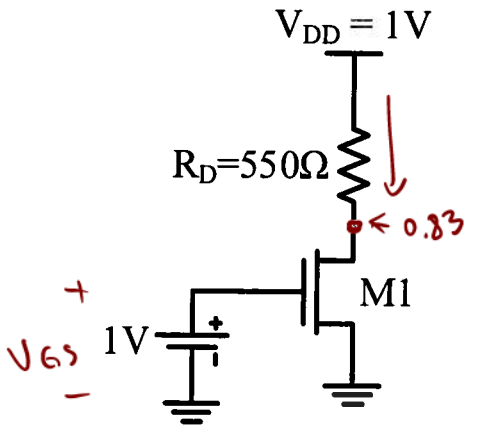
PROBLEM 1: Warm up

a. In the figure below, what is the minimum allowable value of V_{DD} (initially 1V) if M_1 must not enter the triode region? Assume λ=0. **(3 pts)**



$V_{DSAT} = 0.3V, V_{TN} = 0.17V, k_n' = 130\frac{\mu A}{V^2}, \left(\frac{W}{L}\right)_{M1} = \frac{480nm}{100nm}$

$V_{DS} \geq V_{GS} - V_T = 0.83V$ (1V, 0.17) boundary of triode

$V_{GT} > V_{DSAT} \Rightarrow$ device in VSAT ✓

$I_D = k_n' \cdot \frac{W}{L} \cdot \left[(V_{GT}) V_{DSAT} - \frac{V_{DSAT}^2}{2} \right]$

$= 127.3\,\mu A$

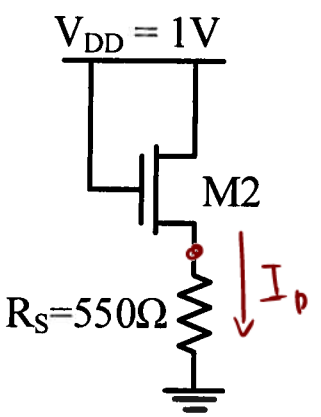
$V_{DD} = V_{DS} + I_D R_D$

$= 0.83 + (127.3\,\mu A) \cdot 550\Omega$

$= 0.9V$

$V_{DD\text{-}min} =$ 0.9V

b. In the figure below, $I_{D_{M2}} = 175\mu A$. What region of operation is M2 in? What is $\left(\frac{W}{L}\right)_{M2}$ ratio? Assume λ=0. **(3 pts)**



$V_{DSAT} = 0.3V, V_{TN} = 0.17V, k_n' = 130\frac{\mu A}{V^2}$

$V_{GS} = V_{DS} = V_{DD} - I_D \cdot R_S = 0.904V$

$= 0.904V$

$\Rightarrow V_{GT} = V_{GS} - V_T$

$\Rightarrow V_{GT} = 0.734V > V_{DSAT} \Rightarrow$ VSAT

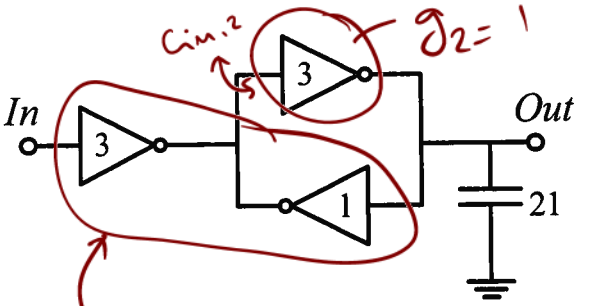
$I_D = k_n' \left(\frac{W}{L}\right) \left[(V_{GT}) V_{DSAT} - \frac{V_{DSAT}^2}{2} \right]$

$\Rightarrow \frac{W}{L} = 7.68$

$(W/L)_{M2} =$ 7.68

Region of Operation = V-sat

c. What is the path effort from *In* to *Out* in the circuit below? **(4 pts)**



$C_{in,2}$ $g_2 = 1$

$g_1 = \frac{3}{2}$

$F = G \cdot B \cdot H$ (G: $3/2$)

$H = \frac{21}{3} = \frac{C_{out}}{C_{in,1}}$

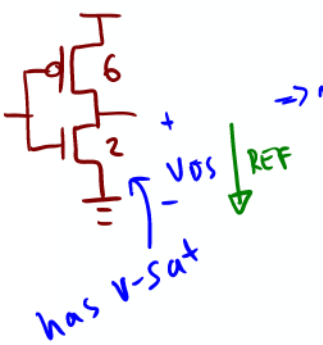
$\frac{21}{3} \times \frac{3}{2} = \frac{21}{2}$

$F = 21/2$

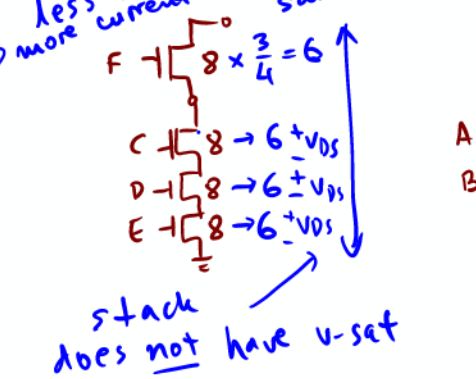
PROBLEM 2: CMOS Logic

Design $\boldsymbol{OUT} = ((\bar{A} + \bar{B})(\bar{C} + \bar{D} + \bar{E}) + \bar{F})\bar{G}$ in static CMOS.
Draw the schematic and size the transistors so that the worst-case equivalent resistances are equal to that of a unit-size 6:2 inverter. For sizing, use velocity saturation scaling factors of $X_n = 4/3$, and $X_p = 6/5$.
Hint: Use De-Morgan's law to convert OUT to $\overline{OUT}$.

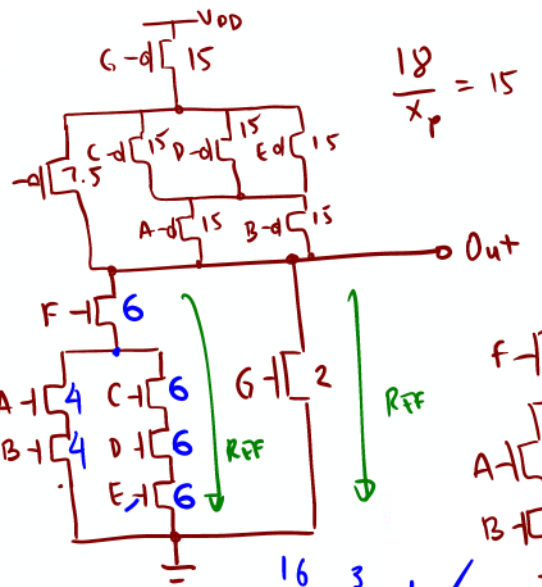
$Out = \overline{(AB + CDE)F + G}$



ignore v-sat
less v-sat impact
=> more current or less W for same current



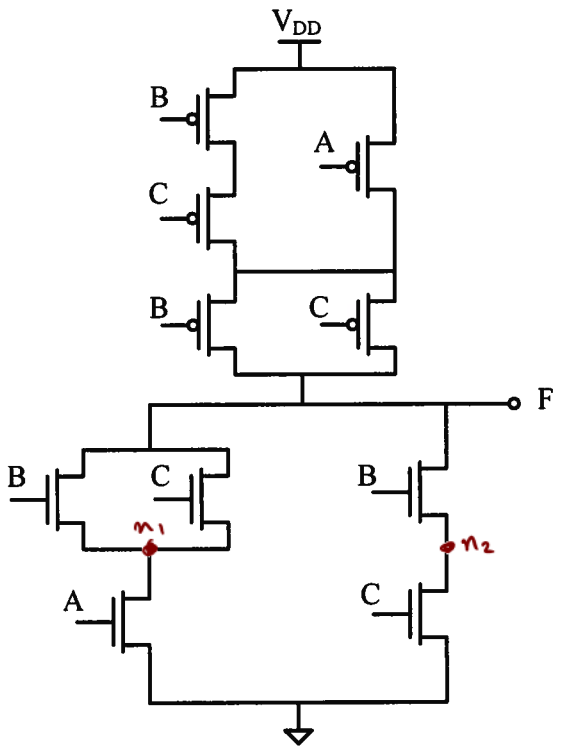
stack does not have v-sat



$\frac{16}{3} \times \frac{3}{4} = 4$ ✓

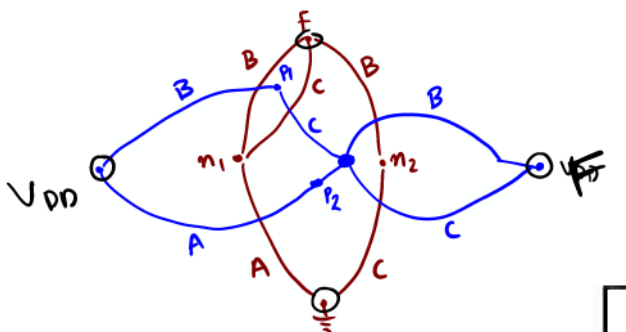
PROBLEM 3: Layout Techniques

a. Consider the logic gate shown below. What is the logic function implemented by the circuit? **(2 pts)**



$F = \overline{A \cdot (B + C) + B \cdot C}$

b. Draw the Euler graph for the circuit. Find a consistent Euler path. **(4 pts)**

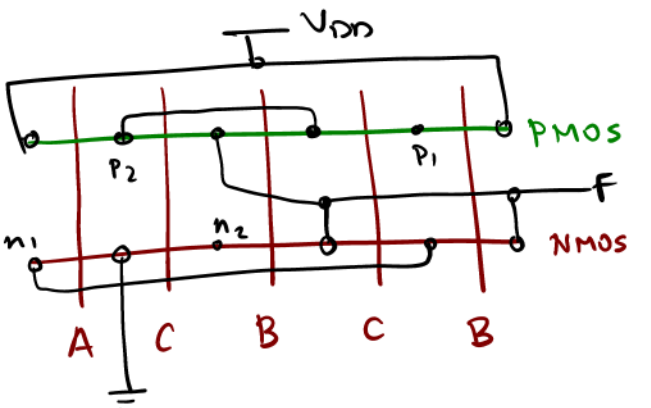


ACBCB ✓

Consistent Euler Path = ACBCB

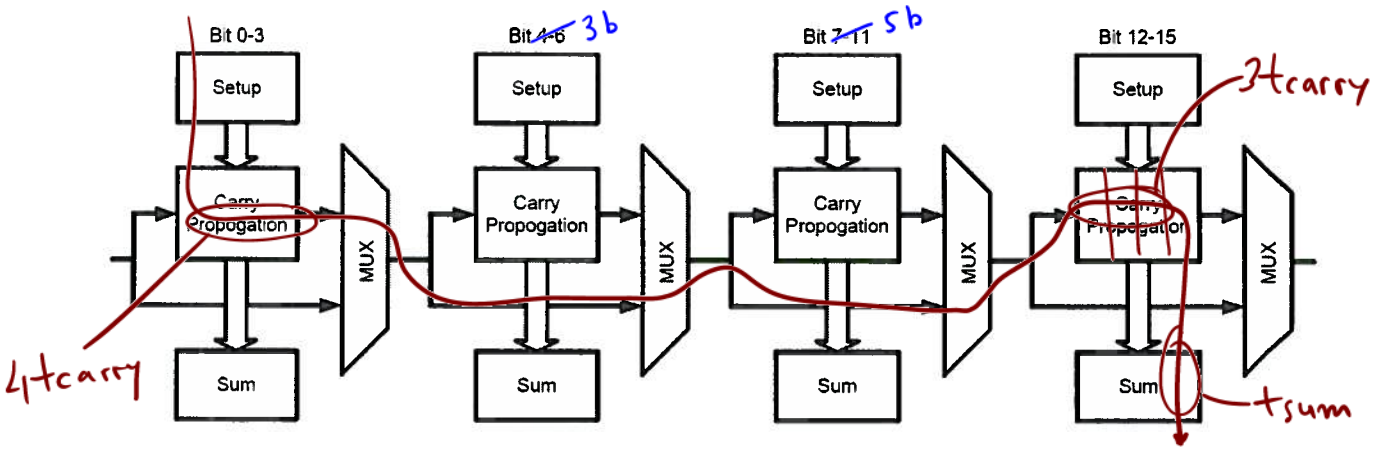
c. Implement the circuit in part (a) in one diffusion region using stick diagram. Each gate must be used for both PMOS and NMOS. Use static CMOS. Clearly denote if crossing wires are connected or not. **(4 pts)**

Hint: Use the Euler path you found in part (b).



PROBLEM 4: Arithmetic Block

A linear 16-bit carry-bypass adder has been shown below.



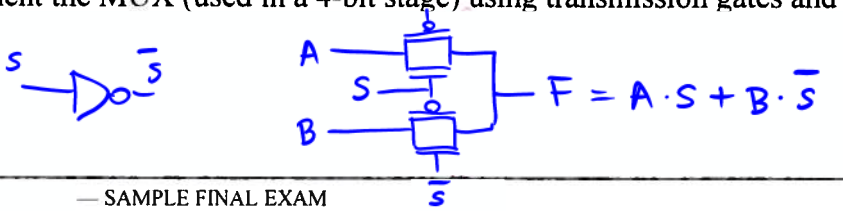
a. Calculate the worst case delay of this adder. (In terms of t_{setup}, t_{carry}, t_{sum}, and t_{mux}). **(3 pts)**

$t_{\text{linear 16-bit carry-bypass}} =$ $t_{setup} + 4t_{carry} + 3t_{MUX} + 3t_{carry} + t_{sum}$

b. A smart engineer from 115cTechnologies designed the same adder for her boss. By mistake she had 3-bits in the second stage and 5-bits in the third stage. Calculate the worst-case delay of this adder and compare it to the linear 16-bit carry-bypass. Argue whether the engineer's boss should give this engineer a raise or fire her. **(4 pts)**

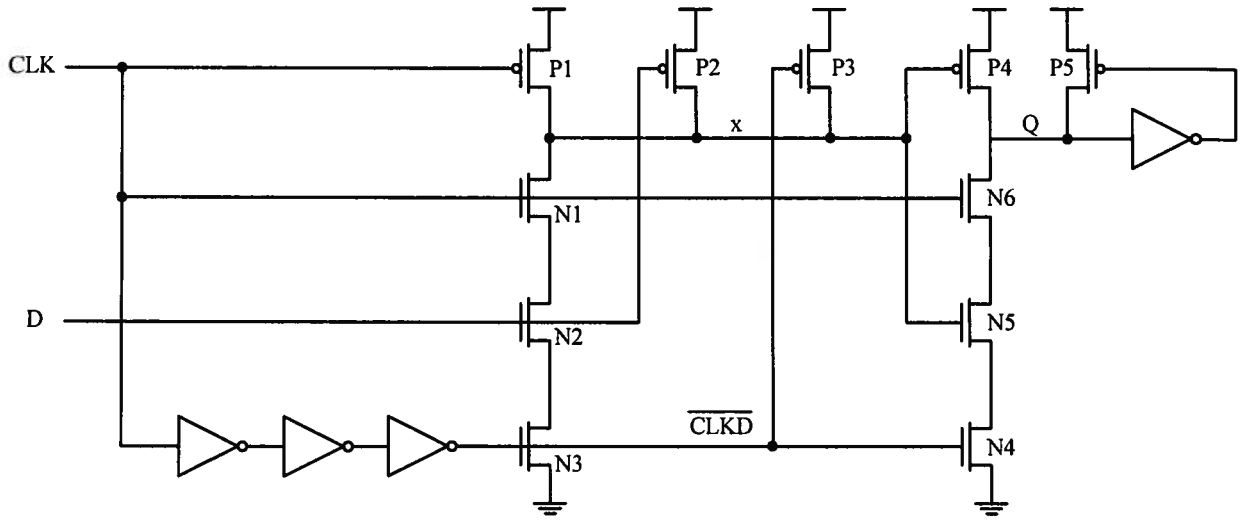
$t_{\text{115cTechnologies Adder}} =$ $t_{setup} + 7t_{carry} + 3t_{mux} + t_{sum}$			
She should:	***Get fired*** ☐	***Get a raise*** ☐	***Neither*** ☒

c. Implement the MUX (used in a 4-bit stage) using transmission gates and inverters. **(3 pts)**

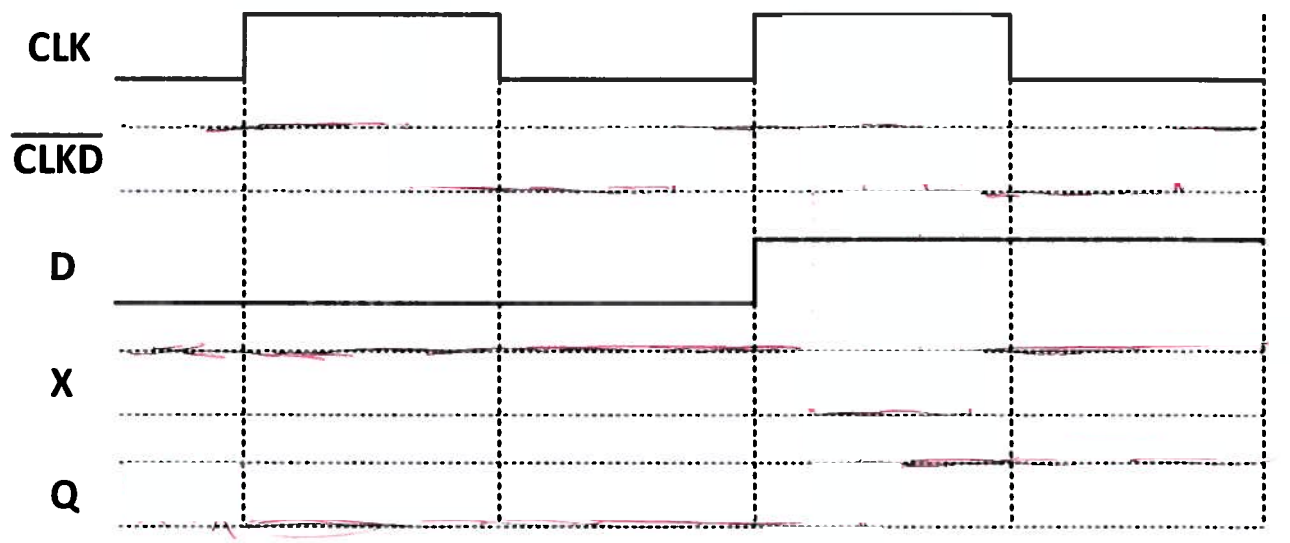


PROBLEM 5: Flip-Flop Timing

Consider the sequential circuit shown below.



a. Assume that all the transistors have been sized such that the delay from any input to the immediate output equals $t_{inv} = 100ps$, and an external clock CLK operates at 1GHz with 50% duty cycle. Draw the waveforms at nodes $CLK, \overline{CLKD}, X$, and Q for two clock cycles, with D equals 0 in first cycle and 1 in the second. **(4 pts)**



b. Would the sequential circuit above be considered a latch, a master-slave pair, or a pulse-triggered latch? **(1 pts)**

c. Are the setup and hold time of this sequential circuit positive, negative, or approximately zero? Why? **(2 pts)**

d. Calculate the propagation delay t_{clk-q} for output (Q) high-to-low and low-to-high transitions. **(4 pts)**

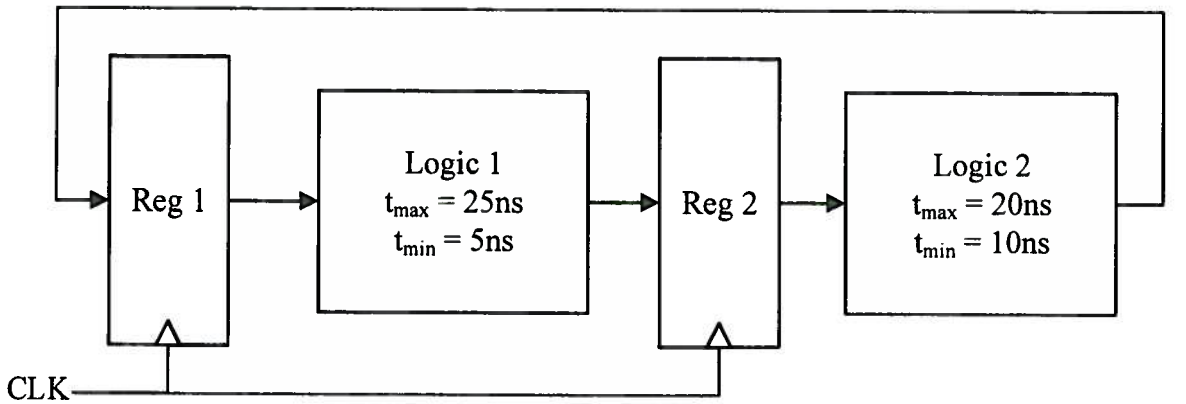
$\mathbf{t_{clk-q,HL}}$ =
$\mathbf{t_{clk-q,LH}}$ =

e. Can we increase the number of inverter stage between CLK and $\overline{CLKD}$ from three to five? Why or Why not? **(2 pts)**

f. Can we reduce the number of inverter stage between CLK and $\overline{CLKD}$ from three to one? Why or Why not? **(2 pts)**

PROBLEM 6: Timing Analysis

Figure below shows a data path structure with feedback. Registers are edge triggered with the following parameters: $t_{c-q,max} = 4ns, t_{c-q,min} = 2ns, t_{setup} = 1ns$, and $t_{hold} = 1ns$.



a. What is the maximum frequency at which this data path can operate properly? Assume zero skew between the clocks and no jitter. **(4 pts)**

f_{max} =

b. What is the maximum random clock skew that this system can tolerate? **(4 pts)**

$t_{skew,max}$ =

c. Assume there is no random skew and you are able to introduce the clock skew into this system. How do you do this to maximize the system performance without sacrificing the functionality? What is the maximum operating frequency we can achieve? When operating at the highest speed, what is the maximum random clock jitter that this system can tolerate? **(7 pts)**

f_{max} =
$t_{jitter,max}$ =

PROBLEM 7: Job Interview Question

a. When using flip-flops, sometimes in addition to CLK, we might want to use an ENABLE signal to store data. Meaning Data is passed to the output at the edge of the clock if ENABLE is high. Figures 8(a) and 8(b) show two different implementations for this.

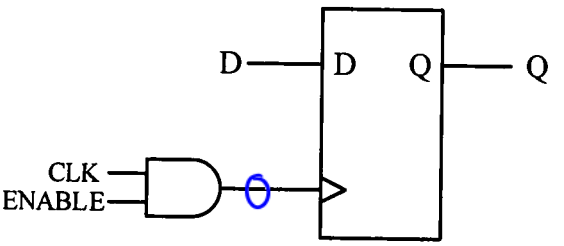


Figure 8(a)

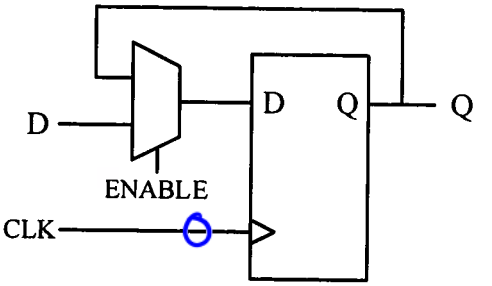
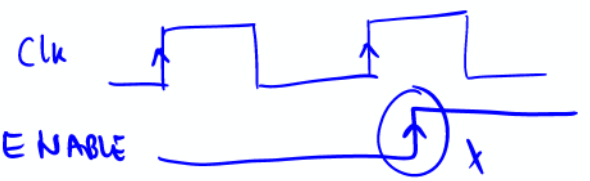


Figure 8(b)

Which implementation is more robust? Why? **(5 pts)**



(b) is more robust b/c you don't want ENABLE to trigger Clk input of FF

b. Built a 4:1 MUX using only 2:1 MUXes. **(5 pts)**