HW6: Chris Baker

Thursday, May 20, 2021 1:09 PM

Problem 1 – Sizing of Adder Cell (Project related)

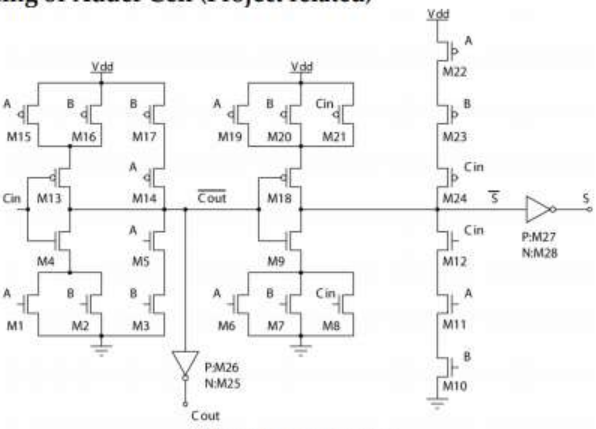


Figure 1: Mirror adder

Study the mirror adder cell. Assume unit sized inverter with the following parameters (W_p = 480nm, W_n = 240nm, L_p = L_n = 100nm). Also assume that each output is driving a load capacitor of 20fF, and C_{in} = $C_{intrinsic}$ =1.5fF.

(a) Size the above adder topology to minimize worst-case t_{p_y}. Provide transistor sizes in absolute units (nm or µm). Assume that y can be either S or C_{out}, and t_{p_y} is the propagation delay of any input node to node y. Please write down the strategies to show your thinking process.

(b) Create schematic of the adder with the sizing from (a) and measure the propagation delay in Spectre.

A)

Strategy:

Let the sizes remain consistent, but adjust the outputs. By modifying the output we can adjust the effort values to around a magnitude of 3. We assume that the pull up and pull down models are symmetrical. Also we note that the NMOS drives approximately twice as much compared to a PMOS. Given our values for capacitance and transistors we can adjust the sizes for the inverters.

Path to Cout:

Logical Effort

1st stage LE = 2

Second Stage LE = 1

Make tpCout/X -> 1 - (20fF/1.5F)/X^2 = 0

X = 3.65

Path to S:

Logical Effort

1st stage LE = 2

Second Stage LE = 1

Make tpS/Y -> 1 - (20fF/1.5F)/Y^2 = 0

Y = 3.65

M	Value	M	Value	M	Value	M	Value
1	2	9	2	17	4	25	2.6
2	2	10	3	18	4	26	5.2
3	2	11	3	19	4	27	2.6
4	2	12	3	20	4	28	5.2
5	2	13	4	21	4		
6	2	14	4	22	6		
7	2	15	4	23	6		
8	2	16	4	24	6		

B)

Worst Case

S = 0	S = 1	tpLH	tpHL	C=0	C=1	tpLH	tpHL

110	010	145	136	100	101	101	99

Figure 2 shows a Full Adder (FA) symbol. Here A, B, and Ci are inputs. S and Co are outputs.

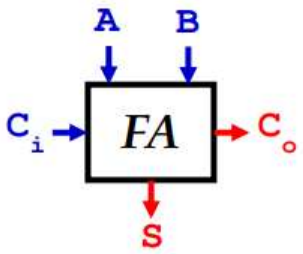


Figure 2: Full Adder

2A Write down the functions for both Sum (S) and Carry-out (Co) as a function of inputs.

S = A ⊕ B ⊕ C
Co = AB + Ci(A+B)

2B To implement the Full-Adder cell, different topologies and circuit styles can be used. The mirror adder in problem 1 is an example of a Full Adder cell design.

As you noticed from problem 1 this design can be involved. However, if some prior knowledge about the inputs is available the logic can be optimized.

For this problem consider the two cases shown in table 1. Optimize and simplify Sum (S) and Carry-out (Co) functions as much as you can.

Table 1: Adder Optimization for Specific Inputs

	A	B	C_i	S	C_o
Case 2B-1	x	1	0		
Case 2B-2	x	0	y		

2b-1:

S2b-1 = x ⊕ 1 ⊕ 0 = x ⊕ 1 = ~x
C2b-1 = AB + Ci(A+B) = x1 + 0(x+1) = x + 0 = x

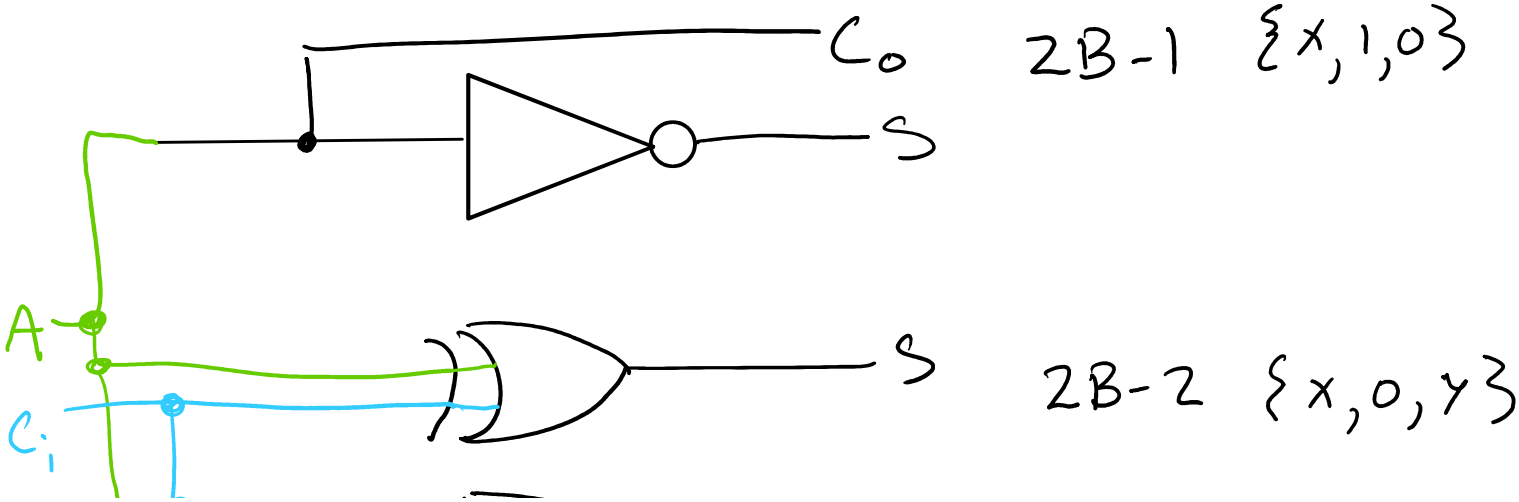
2b-1:

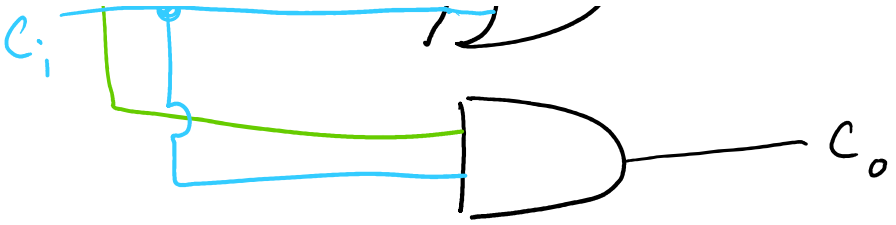
S2b-1 = x ⊕ 0 ⊕ y = x ⊕ y
C2b-1 = AB + Ci(A+B) = x0 + y(x+0) = yx = xy

	A	B	Ci	S	Co
2b-1	x	1	0	~x	x
2b-2	x	0	y	x ⊕ y	xy

2C Draw gate level schematics implementing cases 2B-1 and 2B-2 from 2B.

Note *Think about how this exercise can help you in your project.*





Problem 3 – Elmore Delay

Calculate the Elmore "delay" (time constant) from node A to node B in Figure 3 using the resistor and capacitor values given in Table 3.

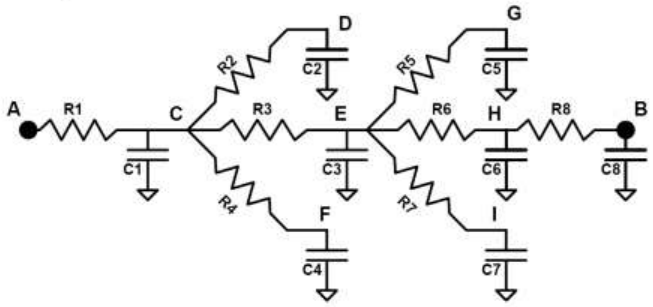


Figure 3

Table 3: Resistor/Capacitor Values

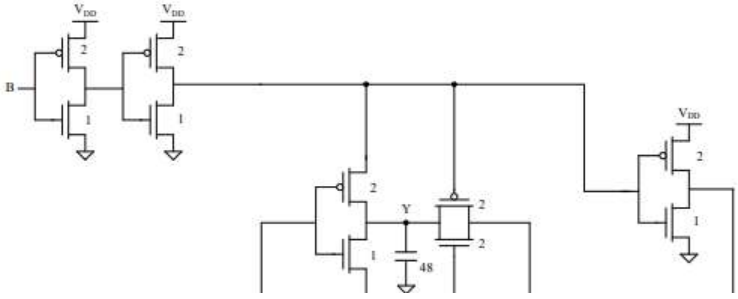
Resistor	Value (Ω)	Capacitor	Value (fF)
R1	0.06	C1	60
R2	0.06	C2	180
R3	0.12	C3	60
R4	25	C4	60
R5	0.06	C5	250
R6	0.25	C6	60
R7	0.18	C7	120
R8	250	C8	60

C	Mutual Resistance
1	R1
2	R1
3	R1+R3
4	R1
5	R1+R3
6	R1+R3+R6
7	R1+R3
8	R1+R3+R6+R8

Tau = R1(C1+C2+C4) + (R1+R3)(C3 + C5 + C7) + (R1+R3+R6)(C6) + (R1+R3+R6+R8)(C8)
Tau = 15.13 pS

Problem 4 – Transmission Gate, Logical Effort Analysis

Consider the following pass transistor based XOR gate. The inputs to the gate are driven by two unit sized inverters as shown in the figure. The gate drives a capacitance equivalent to 48 device widths at the output node Y.



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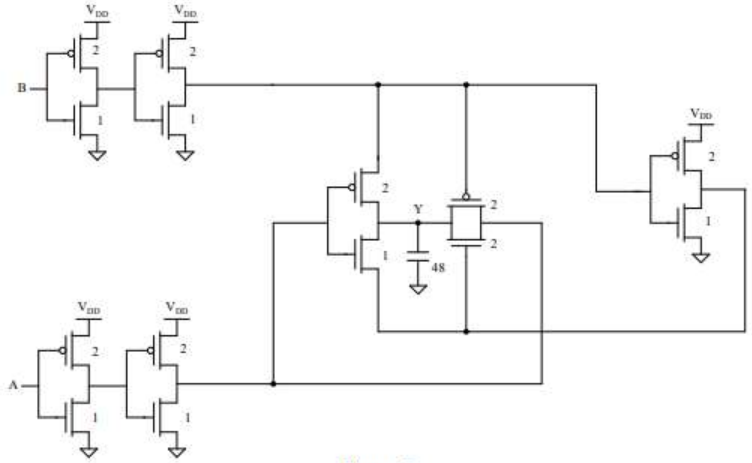

Figure 2

Determine the logical effort delay (d=gh+p) for the circuit for the following conditions:

a) B = 0; A: 0 → 1
b) B = 1; A: 0 → 1
c) A = 0; B: 0 → 1
d) A = 1; B: 0 → 1

You can assume that $R_{pull\text{-}up}$ for NMOS = 2* $R_{pull\text{-}down}$ for NMOS and $R_{pull\text{-}down}$ for PMOS = 2* $R_{pull\text{-}up}$ for PMOS. Assume $\gamma_{INV} = 1$. Clearly state the assumptions that you make. Be sure to include effect of all capacitances.

Based on the above analysis identify the critical path in the above XOR gate.

A)
B is constant so ignore the top path of the circuit.
The second inverter after A drives the transmission and the PMOS Buffer just before the Y node.
The NMOS for this buffer gives a pull up current of about .5 . The PMOS leading to this drives approximately a size of 2/3 for an inverter. Taking both of these into consideration the node should output about 7/6 and the capacitance should be 3.

g = 3/(3.5) = 6/7 = 0.8571

Total Delay = gh1 + p1 + ghc + pc = 1*1 + 1 + (6/7)(48/3) + (10/3)+(7/(21/6)) = 21.05

B)
The diagram reduces to three inverters where the B inverters are remove and the last Vdd inverter is not present either. We turn off the transmission gate.

Total Delay = gh1 + p1 + gh2 + p2 + ghc + pc = 1*1 + 1 + 1*(7/3) + 1 + 1*(52/3) + 1 = 23.6667

C)
We remove the A Inverters in this case and have 4 inverters left over. Because of the quick charging we assume the transmission gate has minimal effect. We also assume that the second inverter from B does not influence delay since the NMOS of the following third inverter (in the middle) is turned off. The last inverter adds to the load of the output of the second Inverter after B.

The results are similar to a pass transistor gate. We can assume a inverter width of .5 and capacitance o 3 for the gate. Thus, logical effort g is 2.

Total Delay = gh1 + p1 + ghc + pc = 1*1 + 1 + 2*(52/3) + (3/(1.5) + (10/3)) = 42

D)
Again we remove the first two inverters from A, but instead of grounding the middle inverter on the input we pass Vdd. As such the output nodes for the middle inverter (3) and last inverter (4) have the Vdd as they discharge. The Transmission gate should be off at a earlier time in this case due to the discharging as well.

Total Delay = gh1 + p1 + gh2 + p2 + ghc + pc = 1*1 + 1*(7/3) + 1 + 2*(52/3)+ (3/(1.5) + (6/3)) = 43

D > C > B > A
Thus, D is the critical delay for the circuit with a value of 43 which occurs when
A = 1; B:0 -> 1