AN3326
Application note

SPC56EL60 hardware design guideline

Introduction

This application note serves as a guideline to hardware designers and provides configuration and layout recommendations for the SPC56EL60 microcontroller unit.

The document covers the following topics:

- Voltage regulator (V_{REG})
- Main oscillator
- Supply pins
- Analog input pins
- Reference reset circuit

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1 Overview

SPC56EL60 devices are members of a new family of microcontrollers designed for Safety Integrity Level 3 (SIL3) and Automotive SIL D (ASILD) compliant chassis and safety applications. These microcontrollers are based on two high-performance e200z4d cores built on Power Architecture® technology.

The device is supplied externally with a single voltage supply, 3.3 V. Internally the chip operates with two supply voltages, namely the main supply (3.3 V) and the core logic supply (1.2 V).

Moreover, the analog reference voltage, which is supplied externally as well, can be either 3.3 V or 5 V depending on the application requirements.

All SPC56EL60 electrical characteristics, including the absolute maximum ratings and recommended operating conditions (for example, threshold voltages, maximum and minimum supply voltages, etc.), as well as the package mechanical drawings, can be found in the device datasheet. Pin assignments can be found in both the device reference manual and datasheet.

2 On-chip voltage regulator

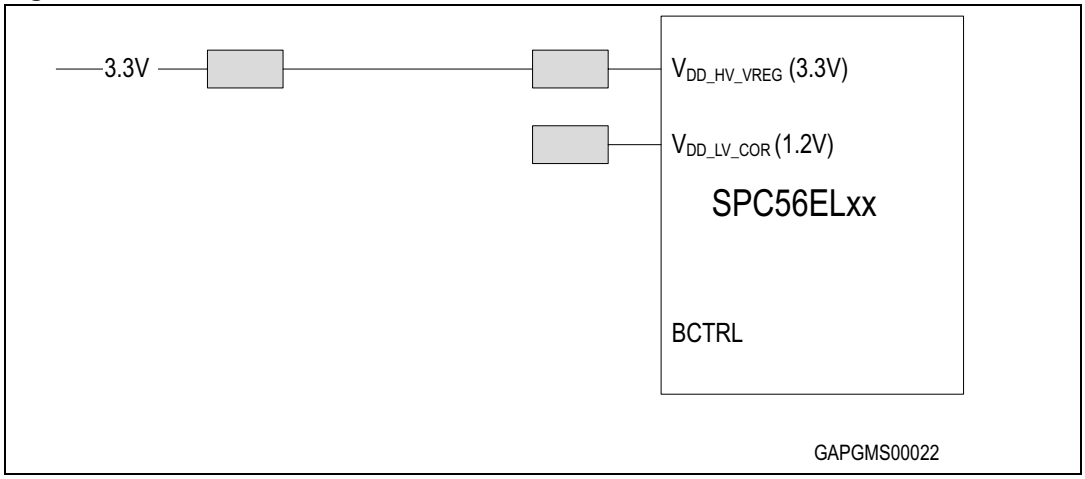
The SPC56EL60 device is supplied with 3.3 V ±10% (3.0–3.6 V). Additionally, the device's on-chip linear voltage regulator (V_{REG}) generates a reference voltage enabling the regulation of the 1.2 V via the internal or external ballast from the external 3.3 V voltage supply.

The on-chip voltage regulator module provides the following main features:

- Works with either an NPN external ballast transistor or the internal one
- Auto-detection of the external ballast (if external ballast is not detected, SPC56EL60 works with the internal one)
- Low- and high-voltage detection on the 1.2 V supply
- Low-voltage detection on the 3.3 V supply voltages

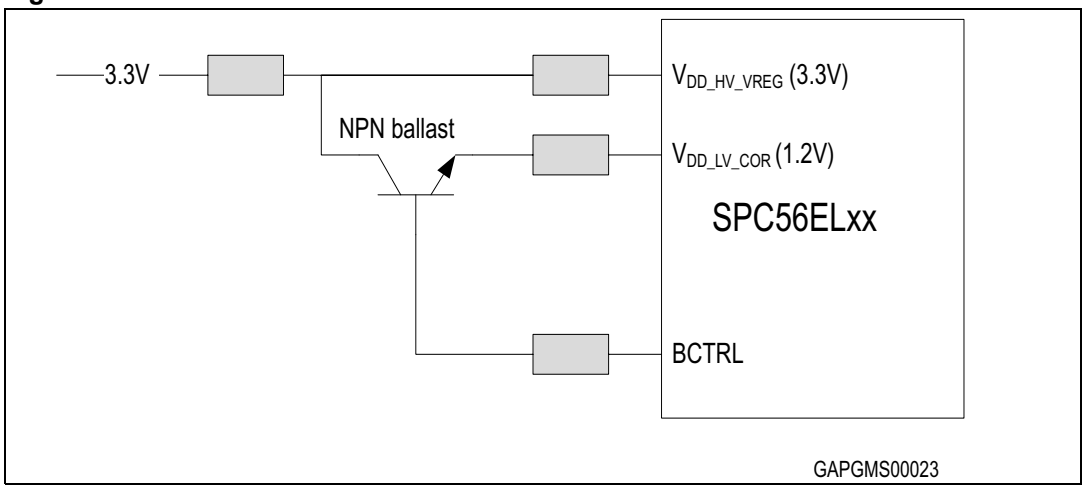
SPC56EL60 can work using either the internal ballast (see *Figure 1*) or an external one (see *Figure 2*).

Figure 1. Block scheme of SPC56EL60 used with the internal ballast



1. Grey blocks represent external passive components.

Figure 2. Block scheme of SPC56EL60 used with an external ballast



1. Grey blocks represent external passive components.

The use of the internal ballast eliminates all external components shown in *Figure 5* (that is, the bipolar transistor used as ballast and two decoupling capacitors). However, in this configuration the consumption caused by the drop in the externally supplied 3.3V, and 1.2V, used by the digital logic, is dissipated by the package of SPC56EL60 itself. This dissipation does not permit a high consumption to be achieved.

If an external ballast is used, the consumption due to this drop is dissipated by the external bipolar regulator. In such a way a higher consumption can be achieved.

The selection between either external or internal ballast is done by the V_{REG} module itself through its auto-detection feature:

1. After a destructive reset (for example, power on), SPC56EL60 always starts using the internal ballast.
2. External ballast detection begins.
3. If external ballast is detected, SPC56EL60 switches to it; if not, SPC56EL60 continues working with the internal one.

The device cannot be used with the 1.2 V supplied directly from the external regulator, but the 1.2 V has to be controlled by the internal regulator.

2.1 Recommended transistor

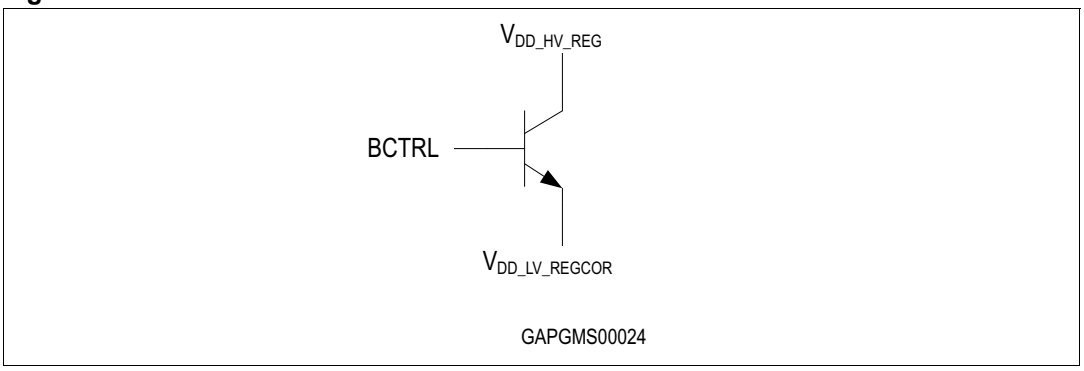
The V_{REG} circuit is a classic emitter-follower configuration. The voltage regulator external NPN ballast base control (BCTRL) pin controls the the voltage on the 1.2 V pin by controlling the current on the base of the transistor.

The nominal target output is 1.2 V. Due to all variations the actual output has an accuracy of ± 10% (that is, 1.08 V to 1.32 V).

The stabilization of the output voltage is achieved using an external capacitance of several µF (see *Section 4*).

Figure 3 shows how the external ballast has to be connected to the related SPC56EL60 pins.

Figure 3. External NPN ballast connection



The gain of the bipolar ballast must be high enough to start up the device and low enough to prevent the V_{REG} becoming instable.

The BCP68 from ON Semiconductor is a recommended bipolar transistor[a] able to provide a stable low voltage digital supply to the device. The list of supported transistors can be found in the SPC56EL60L3, SPC56EL60L5 datasheet (see *Appendix A: Reference document*).

2.1.1 Power dissipation of external transistor

The power dissipation required by the bypass transistor is dependent upon the voltage drop across it, the core current and the selected supply range.

Assuming the CPU draws 250 mA[b] and a 3.3 V supply, the worst case voltage drop with +10% 3.3 V supply is 2.5 V (that is, 3.6 V – 1.08 V = 2.52 V). This leads to about 0.62 watts of power dissipation.

2.1.2 Ballast transistor junction temperature

The ballast transistor maximum junction temperature is typically 150 °C, although in some transistors it may be as high as 165 °C.

Depending on the maximum ambient temperature, the ballast transistor may have a limited allowed temperature rise and thus requires adequate heatsinking. Thermal characteristics of the board and heatsink are required for this calculation.

2.1.3 Ballast transistor $V_{CE(sat)}$ (collection-emitter saturation voltage)

To reduce the power dissipation in the transistor, a series resistor that will drop the collector voltage can be added. If such a resistor is added, the user must ensure that the transistor does not enter saturation phase. The transistor must remain out of saturation with the minimum expected supply and the maximum expected V_{CORE} rail (that is, 1.32 V).

2.1.4 Ballast transistor inductance

SPC56EL60 boards must be designed carefully to decrease the parasitic inductance.

a. For complete details on these bipolar transistors, please refer to the respective transistor datasheet.

b. Please check value for your configuration in the latest SPC56EL60 datasheet.

Two kinds of parasitic inductance are present:

- Inductance due to the distance between the ballast transistor's heatsink rail and the microcontroller
- Inductance due to the lengths of the 1.2 V traces and of the BCTRL signal

Those inductances reduce the phase margin. It is recommended that:

- Inductance on BCTRL is kept below 15 nH
- Inductance on 1.2 V is kept below 15 nH

3 Main oscillator

The SPC56EL60 uses an external crystal as input for both PLLs. The main oscillator provides the following main features:

- Input frequency range: 4–40 MHz
- Crystal input mode
- External reference clock (3.3 V) input mode
- FMPLL reference

For noise immunity reasons, the oscillator uses a dedicated 3.3 V supply. This supply is provided by the pins $V_{DD\_HV\_OSC}$ and $V_{SS\_HV\_OSC}$ (see *Section 4*).

Table 1 shows a list of the recommended crystals and their main parameters.

Note: User shall configure the XOSC_MARGIN bit through the user option bit depending on the chosen crystal.

XOSC_MARGIN must be set to '0' if a 4 MHz crystal is chosen and set to '1' in all other cases.

XOSC_MARGIN does not need to be configured if SPC56EL60 cut 1 is used.

Table 1. Recommended crystals and their main parameters

Nominal frequency [MHz]	Crystal model	Load on EXTAL/XTAL(1) $C_1 = C_2$ [pF]
4.0	NX8045GB	4.7
8.0	NX5032GA	23.0(2)
8.0	NX8045GB	23.0(2)
10.0	NX5032GA	21.0(2)
12.0	NX5032GA	19.0(2)
16.0	NX5032GA	5.6
40.0	NX5032GA	8.0
40.0	NX3225GA	8.0

1. C_1 and C_2 include the parasitic capacitors which must be taken into account to choose the proper external capacitors.
2. Value to be confirmed by characterization

3.1 Reference oscillator circuit

This section describes the key items of the oscillator circuit.

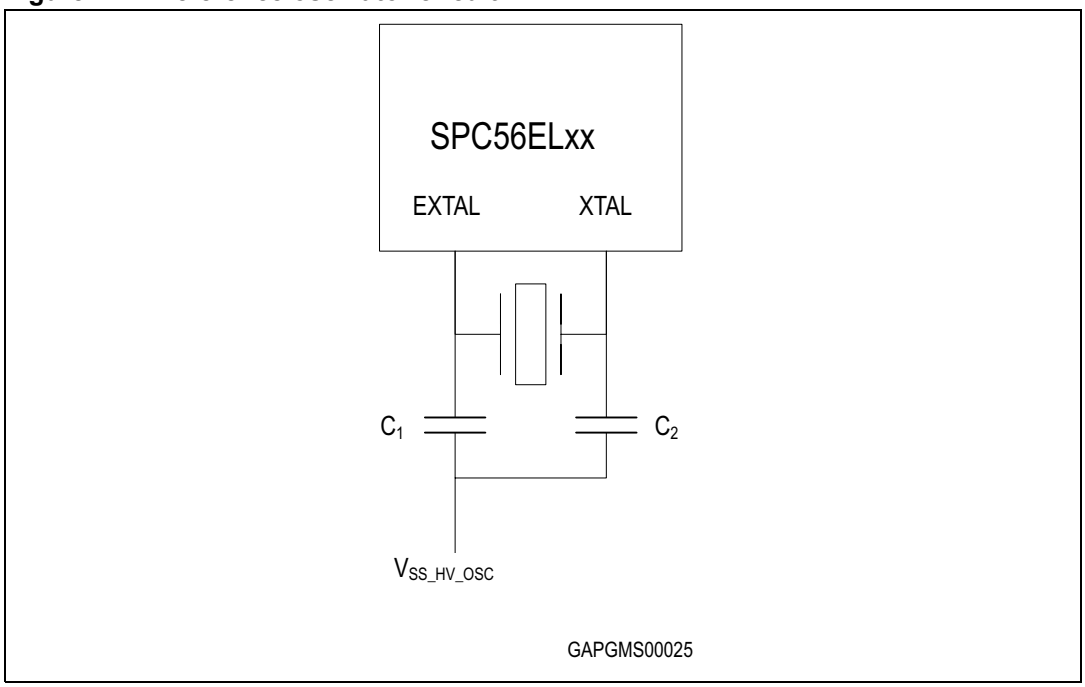
The oscillator circuit consists of the following components:

- Crystal
- Two capacitors

Figure 4 contains a schematic of the on-chip oscillator(c). *Table 1* provides a list of recommended crystals and the suggested value of the two load capacitors C_1 and C_2.

No other external components (for example, a bias resistor) are needed.

Figure 4. Reference oscillator circuit



c. Main oscillator supply pins are not shown; see *Section 4: Supply pins and decoupling* for pin details.

3.1.1 Oscillator hardware recommendations

To optimize performance and minimize EMC (electromagnetic compatibility) susceptibility, the following recommendations are provided:

- Use the crystal with the lowest frequency and set the FMPLL multiplication factor to obtain the chosen system operating frequency.
- Keep the oscillator circuit as compact as possible in order to minimize the amount of emissions generated by currents due to high order harmonics[d].
- For the crystals listed in *Table 1*, the maximum PCB parasitic capacitance between EXTAL and XTAL shall not exceed 1.5 pF.
- Connect $V_{SS\_HV\_OSC}$ directly to the ground plane so that return currents can flow easily between $V_{SS\_HV\_OSC}$ and the two capacitors (C_1 and C_2).
- Avoid other high frequency signals near the oscillator circuitry as they can have an undesirable influence on the oscillator.
- Lay out/configure the ground supply on the basis of low impedance.
- Shield the crystal with an additional ground plane underneath the crystal.
- Do not lay out sensitive signals near the oscillator (analyze cross-talk between different layers).
- Place capacitors at both ends of the crystal, connected directly to the ground plane.
- The crystal package, when metallic, should be connected directly to ground, while keeping the overall loop as small as possible.
- EXTAL
  - Oscillator not in bypass mode: EXTAL is the analog output of the oscillator amplifier circuit.
  - Oscillator in bypass mode: EXTAL is the analog input for the clock generator.
- XTAL is the analog input of the oscillator amplifier circuit. The XTAL pin needs to be grounded (connected to $V_{SS\_HV\_OSC}$) if the oscillator is used in bypass mode.

d. The oscillator circuit has currents flowing at the crystal's fundamental frequency. Even if the oscillator is clipped, higher order harmonics are present as well.

4 Supply pins and decoupling

The SPC56EL60 has different supply/decoupling pins:

- Core logic pins ($V_{DD\_LV\_CORx}$ and $V_{SS\_LV\_CORx}$)
- Voltage regulator pins[e] ($V_{DD\_HV\_PMU}$ and $V_{DD\_HV\_REGx}$)
- ADC_0 and ADC_1 pins ($V_{DD\_HV\_ADV}$ and $V_{SS\_HV\_ADV}$)
- Input/Output pins ($V_{DD\_HV\_IO}$ and $V_{SS\_HV\_IO}$)
- Crystal oscillator amplifier pins ($V_{DD\_HV\_OSC}$ and $V_{SS\_HV\_OSC}$)
- Flash pins ($V_{DD\_HV\_FLA}$ and $V_{SS\_HV\_FLA}$)
- FMPLL pins ($V_{DD\_LV\_PLL0\_PLL1}$ and $V_{SS\_LV\_PLL0\_PLL1}$)

Other pins which must by considered are:

- External NPN ballast base control pin (BCRTL)
- ADC_0 and ADC_1 high voltage reference ($V_{DD\_HV\_ADR0}$ and $V_{DD\_HV\_ADR1}$)
- ADC_0 and ADC_1 low voltage reference ($V_{DD\_LV\_ADR0}$ and $V_{DD\_LV\_ADR1}$)

Please refer to the device reference manual and datasheet for complete details on these pins.

4.1 Decoupling capacitors

This section provides the values of the different recommended capacitors.

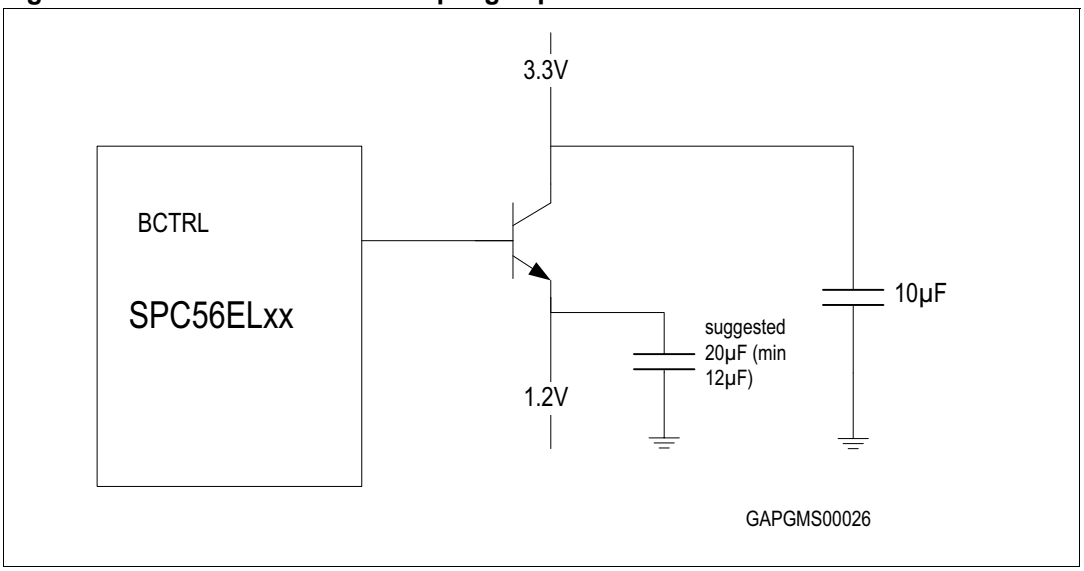
Hardware designers must pay particular attention to place the decoupling capacitors beside the respective pins.

Figure 5 shows the connection between the external ballast and SPC56EL60. The diagram shows the two required capacitors. Designers must place a min capacitor of 12µF beside the transistor emitter close to the microcontroller (max ESR 100 mOhm).

Suggested value for this capacitor is 20µF; this value considers de-rating with regard to the voltage, temperature and aging.

e. $V_{DD\_HV\_PMU}$ pin is the voltage supply of the internal regulator; $V_{DD\_HV\_REGx}$ pins are the collector of the internal ballasts.

Figure 5. External ballast decoupling capacitors



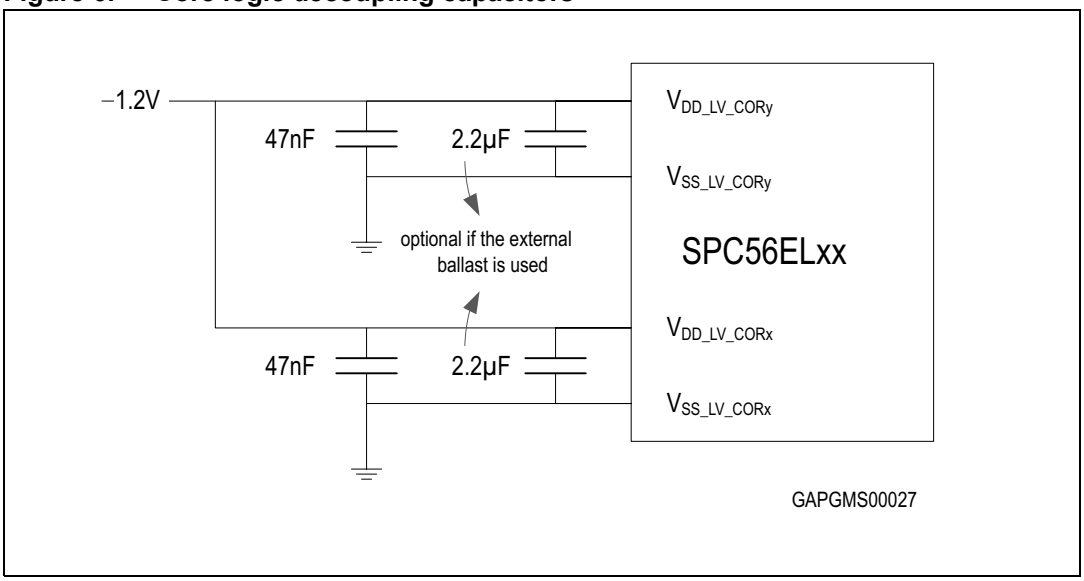
1. The 20 µF capacitor is optional (see *Figure 6* footnote).

In case the user would like to use the SPC56EL60 with the internal ballast, the 12 µF and 10 µF capacitor of *Figure 5* are not needed.

Note: A base capacitor is not needed in external or internal ballast configuration.

Figure 6 shows the decoupling capacitors needed by the logic supply pins (1.2 V). The number of these pins depends on the chosen SPC56EL60 package (for example, the 144-pin package includes six pairs of logic supply pins).

Figure 6. Core logic decoupling capacitors

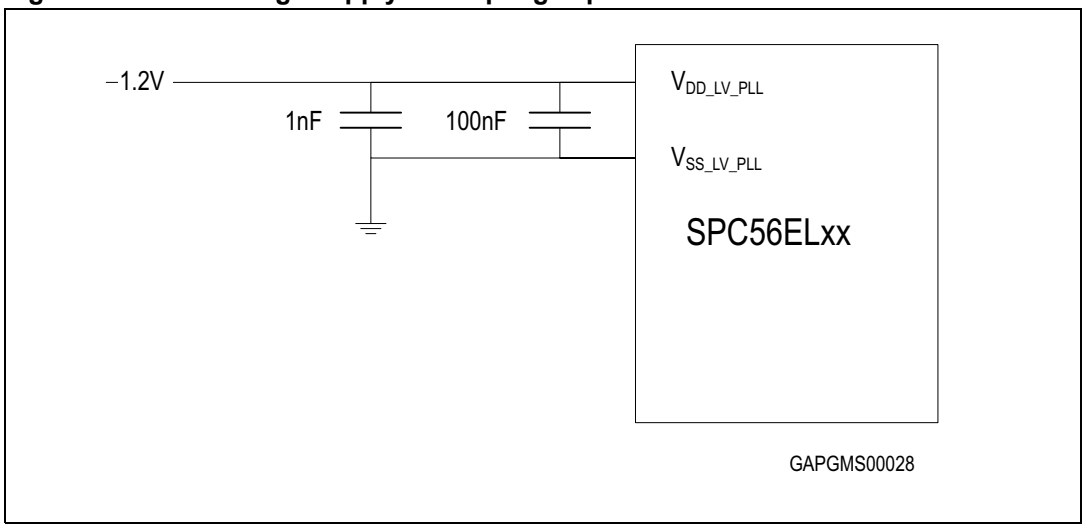


1. In case of external ballast, the 2.2µF capacitor is optional. If a 2.2µF capacitor is placed on every VDD_LV_CORx pins, the 20µF capacitor on the ballast can be removed.

Figure 7, *Figure 8* and *Figure 9* show the recommended decoupling capacitors for the following supply pins:

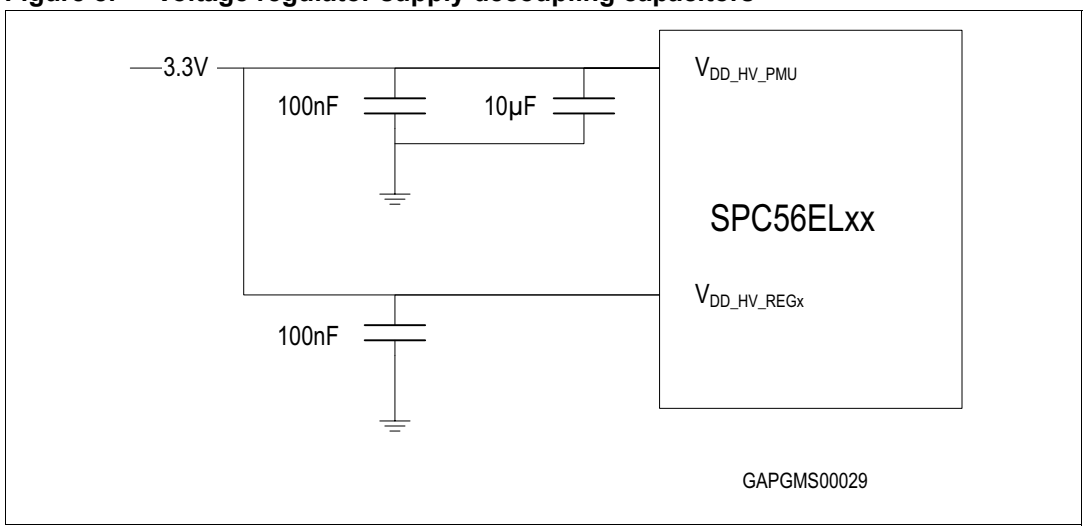
- PLL
- Voltage regulator
- IO
- Flash
- Oscillator

Figure 7. PLL voltage supply decoupling capacitors



1. The VDD_LV_PLL pin must be connected at PCB level to the other 1.2 V pins. This connection is required in both cases, leopard working with the internal or external ballast.

Figure 8. Voltage regulator supply decoupling capacitors



SPC56EL60 devices always start using the internal ballast, which means that the decoupling capacitors connected to $V_{DD\_HV\_REGx}$ are needed even if the external ballast is present on the board.

The number of $V_{DD\_HV\_REGx}$ pins depends on the chosen package (for example, the 144-pin package includes three of these pins).

Figure 9. IO voltage supply decoupling capacitors

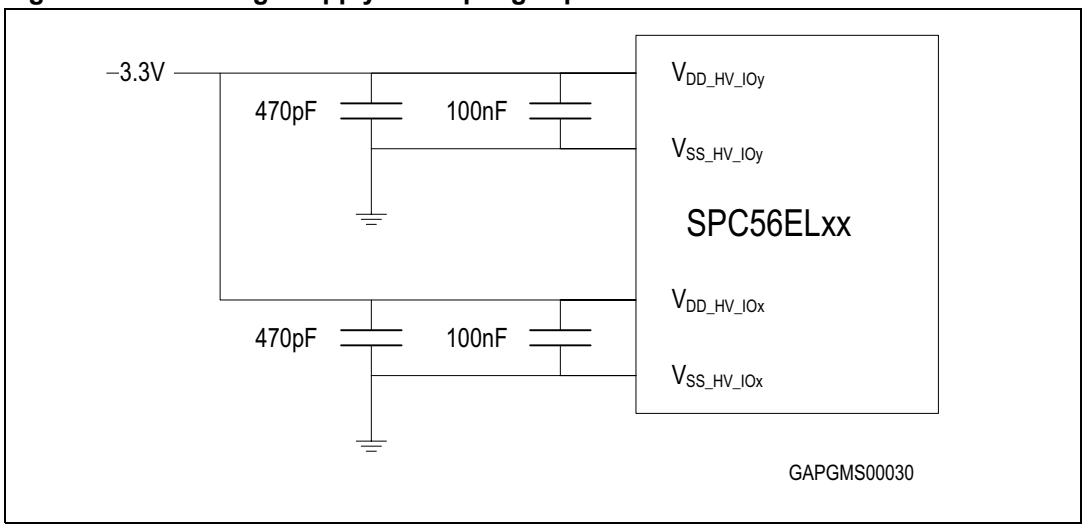
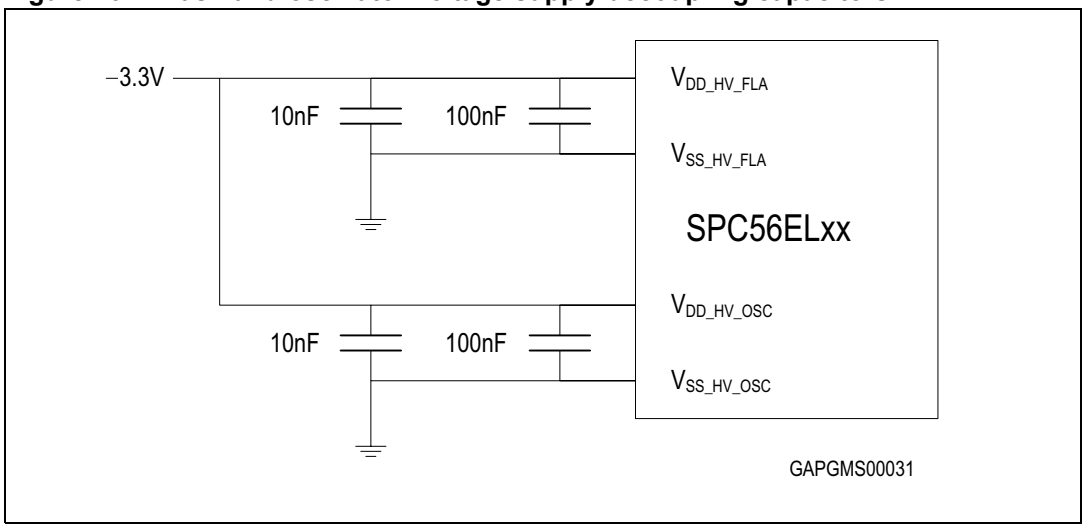
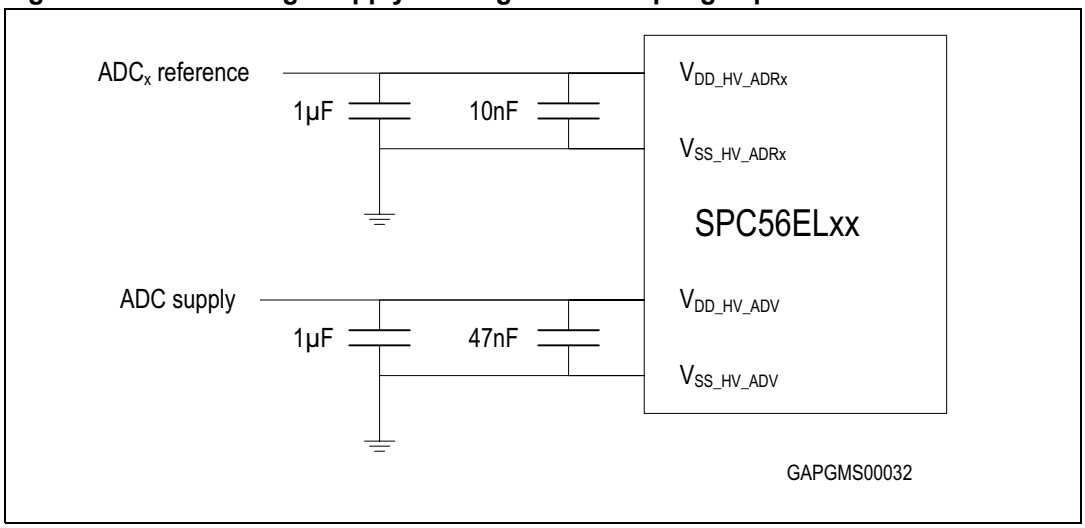


Figure 10. Flash and oscillator voltage supply decoupling capacitors



SPC56EL60 ADCs can be supplied either with 3.3 V or 5 V (both ADCs must use the same voltage supplies). *Figure 11* shows the capacitors needed by the ADC supply and reference.

Figure 11. ADC voltage supply filtering and decoupling capacitors



4.2 Layout recommendations

Some recommendations on the layout and component distribution are listed below:

- Each decoupling capacitor should be placed next to the respective pin.
- If possible use a small plane to distribute V_{CORE} (1.2 V) with a low parasitic inductance to each pin.
- The parasitic inductance on the ballast output (1.2 V) must be kept below 15 nH.
- The parasitic inductance between the BCTRL pin and the ballast input must be kept below 15 nH.
- Low Equivalent Series Resistance (ESR) and low Equivalent Series Inductance (ESL) capacitors should be used for the 1.2 V stability capacitors[f]. Use preferably ceramic capacitors. Do not use electrolytic capacitors as stabilization capacitors.
- Use a multi-layer printed circuit board with a separate layer dedicated to the ground and another one to the voltage supply.

f. Please refer to the device datasheet for the recommended maximum ESR value.

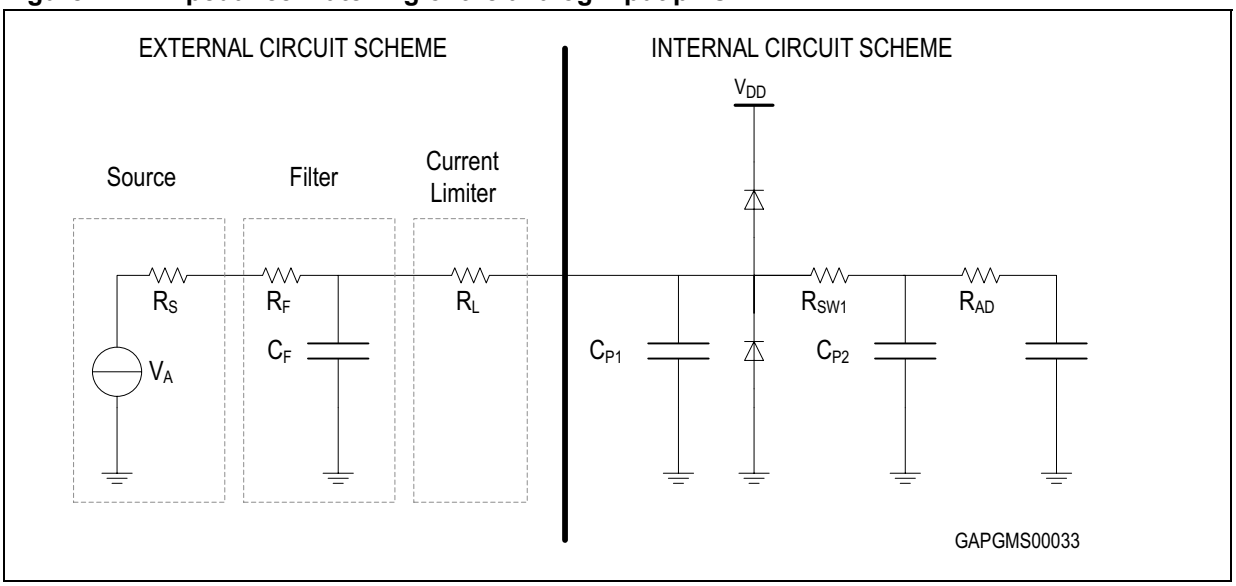
5 Analog input pins

To maximize the performance of the internal ADC without sacrificing conversion accuracy, hardware designers must take into account the impendance matching of the analog input pins.

Figure 12 shows the recommended circuit to match this impedance. The external components (R_F, C_F and R_L) must be chosen accordingly to the application parameters (for example, conversion rate, internal resistance of the input signal (R_S), etc.).

The device datasheet includes all needed steps and equations needed to choose these external components (please refer to the *Input Impedance and ADC Accuracy* section of the device datasheet).

Figure 12. Impedance matching of the analog input pins



6 Reference reset circuit

The SPC56EL60 external reset pin is a bidirectional low active signal.

For safety reasons an internal weak pull down structure is implemented. In such a configuration, if the reset pin is open (for example, due to a faulty condition), the device is remains in reset state.

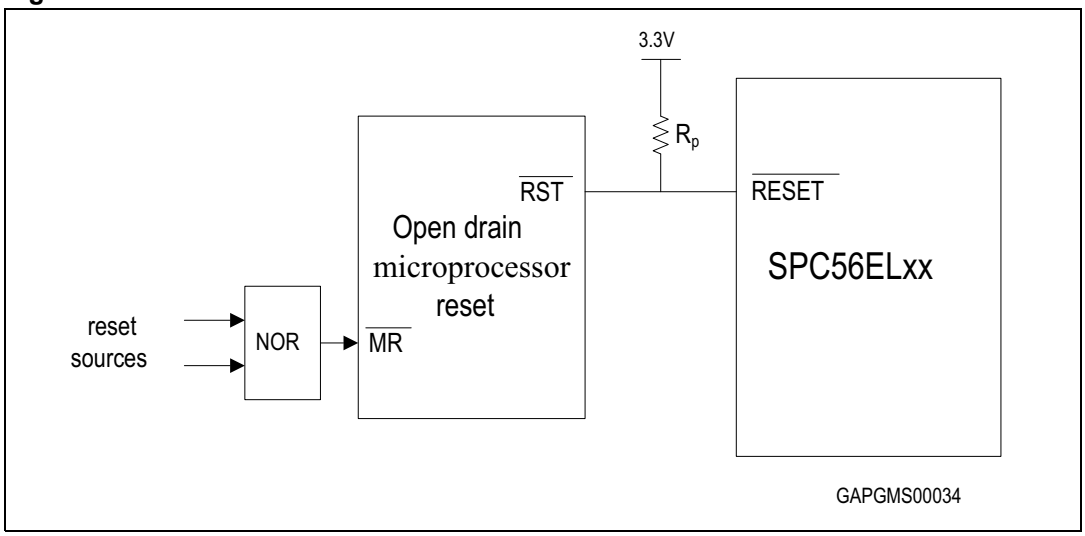
This pin acts as an input to initialize the SPC56EL60 to a known start-up state and acts as an output when an internal device function causes a reset.

The minimum reset pulse duration is 500 ns.

Figure 13 shows the suggested reset circuit. Basic components are:

- External open-drain microprocessor reset device
- External pull-up resistor (R_P)
- NOR gate digital port to manage multiple reset sources

Figure 13. Reference reset circuit



The value of the pull-up resistor must be chosen according to the internal pull-down resistor integrated in SPC56EL60 and the external reset device component. For example, using the STM6315RDW13F as microprocessor reset, a resistor of 2.2KΩ works properly.

Appendix A Reference document

- *SPC56EL60L3, SPC56EL60L5 32-bit Power Architecture® microcontroller for automotive SIL3/ASILD chassis and safety applications* (Doc ID 15457)

Revision history

Table 2. Document revision history

Date	Revision	Changes
17-Dec-2010	1	Initial release.
04-Mar-2011	2	Added the footnote under the figure 7. Updated *Section 4.1: Decoupling capacitors*. Added the footnote under the figure 5. Modified the footnote under the Fig 6. Updates Fig 5 and Fig 6.