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AN-9113

Bootstrap Circuit Design Guide for Motion SPM® Products

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1. Introduction of Bootstrap Circuit

To drive high side power switches in three phase inverters, three additional isolated and floated control supplies are required because floating control supply is necessary to drive each high side. These additional three floating control supplies can be replaced by a bootstrap circuit which is simple and inexpensive. A bootstrap circuit consists of three components; bootstrap diode (D_{boot}), bootstrap capacitor (C_{boot}) and bootstrap resistor (R_{boot}). In bootstrap circuit design, many considerations are required to select proper bootstrap components based on electrical characteristics of the device, including Motion SPM® products and user's operating conditions.

1.1. Bootstrap Circuit Operation

The charged voltage of C_{boot} (V_{BS}) operates as a floating supply to control a high side power switch. It is necessary to charge C_{boot} initially because V_{BS} is 0 V at initial state. V_{BS} should be higher than its under-voltage reset level (generally more than 13 V is recommended) to operate high side power switches according to high side PWM input. C_{boot} is charged from a low side 15 V control supply (V_{DD}) when the low side power switch or diode is turned on. Figure 1 shows C_{boot} charging path when low side IGBT is turned on. In initial charging stage, all three C_{boot} can be charged by one phase IGBT turning on when output is connected to the motor load, but charging time might be longer than all three phase turn on due to series resistance and inductance of load. Recommendations and a guide of initial charging are explained in section 1.2. Figure 2 shows a C_{boot} charging path when a low side diode is turned on during inverter operation.

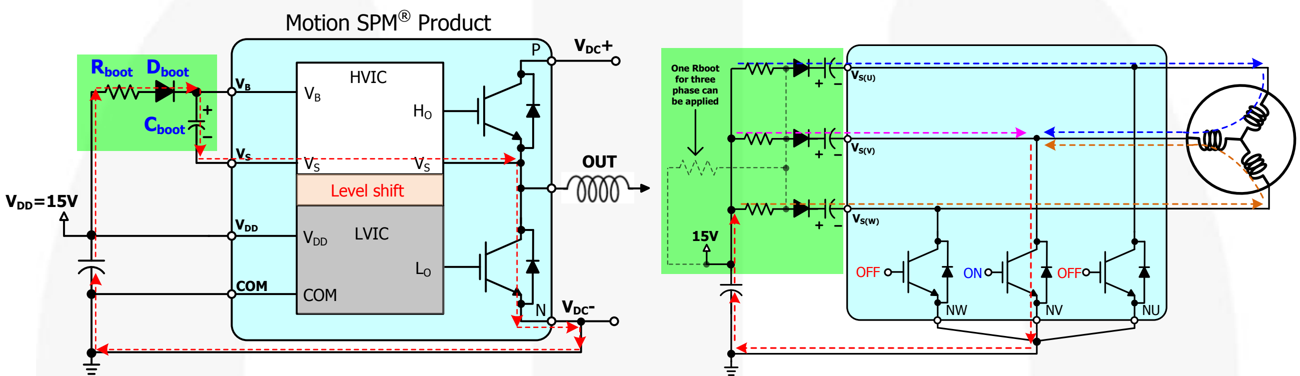

Figure 1. Charging Mechanism of C_{boot} by Low Side Power Switch Turn On

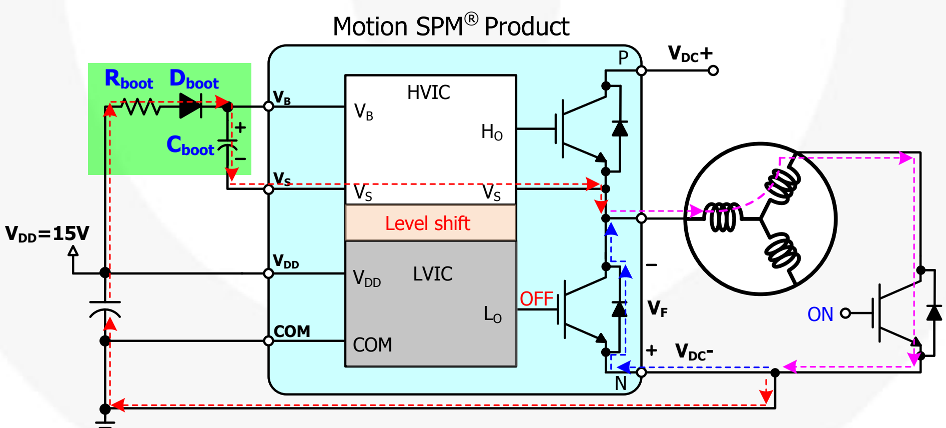

Figure 2. Charging Mechanism of C_{boot} by Low Side Diode Freewheeling

V_{BS} can be charged up to below value according to operation state.

A. *Initial charging and low side power switch turning on. (I_{QBS}: Quiescent current of V_{BS} supply)*

$$\boldsymbol{VBS = VDD - (IQBS \times Rboot) - \ VF\ of\ Dboot\ at\ IQBS - Vcesat\ or\ Vdson\ of\ low\ side\ switch\ at\ IQBS}$$

B. *Low side Diode freewheeling.*

$$\boldsymbol{VBS = VDD - (IQBS \times Rboot) - \ VF\ of\ Dboot\ at\ IQBS + VF\ of\ low\ side\ Diode\ at\ operating\ current}$$

A C_{boot} is discharged by current consumed for high side driving. The current consumed is consistent with quiescent current of high side gate driver (I_{QBS}), level shift driving and gate charge of power switch (Q_g).

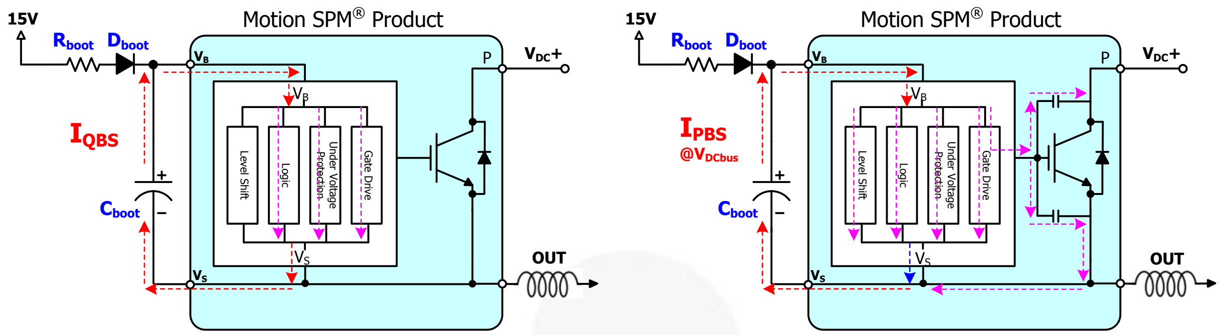

Figure 3. Discharging Mechanism of C_{boot} (Left: Steady State, Right: High Side Power Switch Operate)

1.2. Initial Charging

First, C_{boot} should be charged up to proper V_{BS} for stable operation of high side. There are several methods for initial charging of C_{boot}. A suitable method needs to be applied based on system requirements. Points to be considered as system requirement are below.

A. Capacitance of C_{boot} and resistance of R_{boot}.

B. Over-current protection level from external shunt resistor.

C. Target maximum initial charging time.

C_{boot} is initially charged from 0 V by low side turn on. Required charging time (t_{charge}) depends on duty ratio of the low side PWM input, capacitance of C_{boot} and resistance of R_{boot}. C_{boot} charging with full duty (D=1, Full on) is preferred to reduce initial charging time, however sometimes C_{boot} charging with specific duty is required considering the limitation of R_{boot} pulse power rating or control supply current capability and so on. Examples of a timing chart and required charging time for V_{BS} supply are shown in Figure 4. Initial charging time graph is based on three R_{boot} for three phase condition. If one R_{boot} is used for all three phases, three times longer t_{charge} is required compared with three R_{boot} condition. It is noted that C_{boot} should be charged up to under-voltage V_{BS} reset level (UVBSR) when it is charged initially for high side operation.

Recommended initial charging time is determined by equation (1).

$$\boldsymbol{MOSFET version: Initial\ charging\ time} = -\boldsymbol{Rboot} \times \boldsymbol{Cboot} \times \frac{\boldsymbol{ln}\left(1 - \frac{\boldsymbol{UVBSR\ max.}}{\boldsymbol{VDD - Dboot\ Vth\ @IQBS\ max.}}\right)}{\boldsymbol{low\ side\ on\ duty}}$$

$$\boldsymbol{IGBT\ version: Initial\ charging\ time} = -\boldsymbol{Rboot} \times \boldsymbol{Cboot} \times \frac{\boldsymbol{ln}\left(1 - \frac{\boldsymbol{UVBSR\ max.}}{\boldsymbol{VDD - Dboot\ Vth\ @IQBS\ max. - IGBT\ CE\ Vth\ @IQBS\ max.}}\right)}{\boldsymbol{low\ side\ on\ duty}} \tag{1}$$

Where;

IQBS max. is maximum quiescent current of V_{BS} supply.

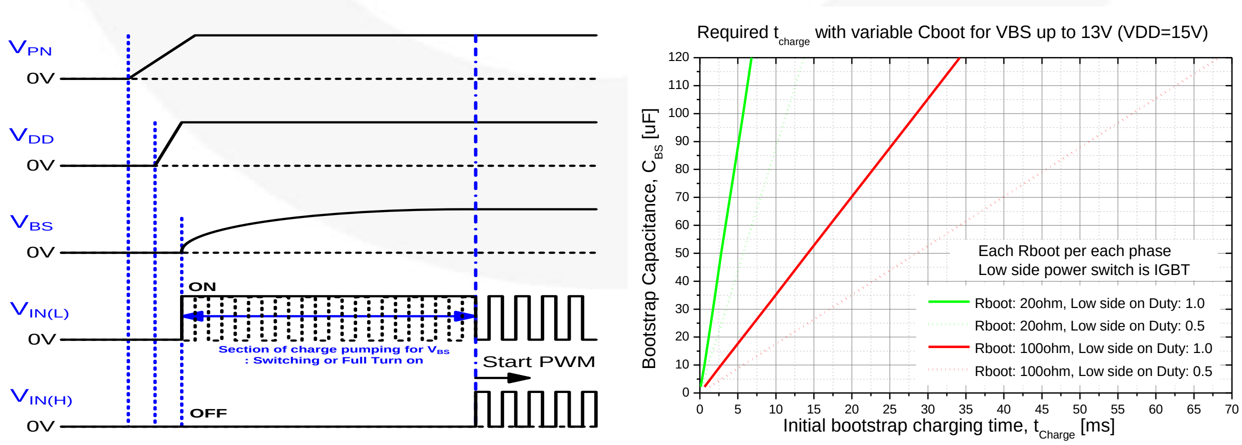

Figure 4. Timing Chart and Required Charging Time for Initial Charging of C_{boot}

Examples of initial C_{boot} charging waveform are shown in Figure 5 under full turn on and switching pulses conditions. Hardware design engineers need to select proper values of R_{boot} and initial charging duty ratio based on target maximum V_{BS} charging time. High side PWM input should be operated after V_{BS} supply is sufficiently charged. For a stable operation, it is recommended to operate high side power switch after V_{BS} supply is charged more than 13 V.

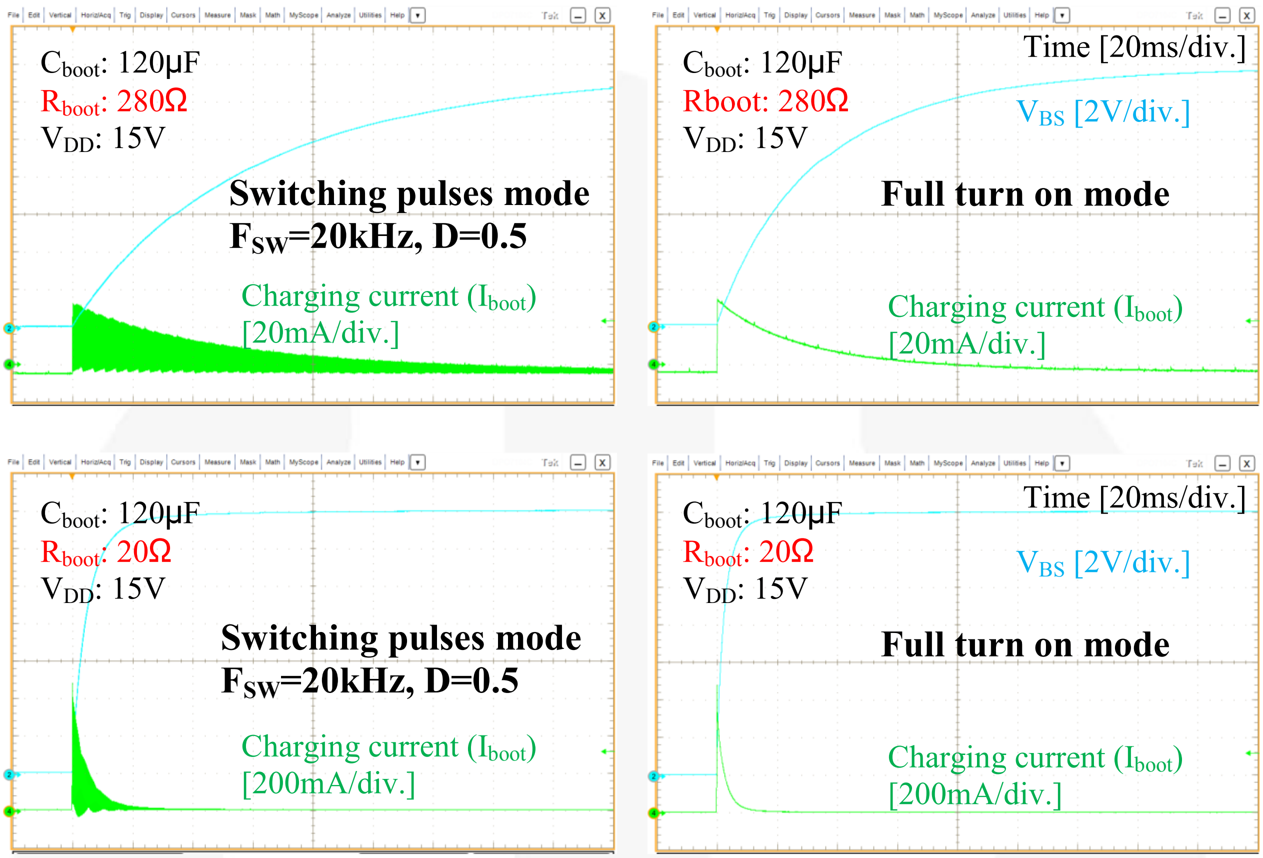

Figure 5. VBS supply initial charging waveforms with variable R_{boot} and Duty ratio

There is an Under-Voltage Lockout function (UVLO) in gate driver to prevent power switches from operating under a low gate voltage condition which may cause large power loss of power switches. This UVLO protection function can be triggered when V_{BS} supply is initially charged with low R_{boot}, large C_{boot} and high duty ratio as shown in Figure 6. To prevent this unexpected fault event, switching pulses with low duty or enough source capacitance for 15 V control supply are recommended.

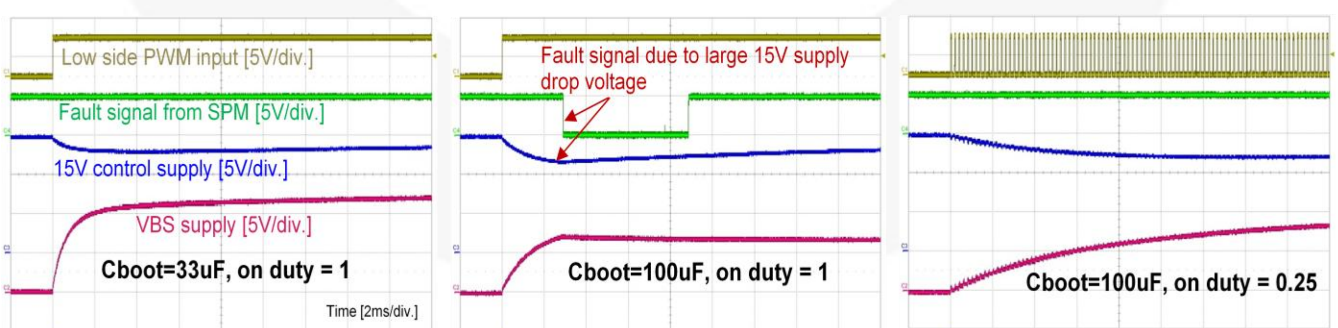

Figure 6. Initial Charging According to Bootstrap Capacitance and Charging Method (Ref. Condition: V_{DD} = 15 V / 300 mA, V_{DD} Capacitor = 220 μF, C_{boot}=100 μF, R_{boot} = 20 Ω)

Generally, a low power inverter uses a MOSFET as a power switch. Thus, Over-Current Protection (OCP) level is low because the applied MOSFET's current rating is low. If three shunt resistors are connected to each low side N terminal, all three low side turn on is recommended for C_{boot} initial charging to prevent potential risk of OCP since one low side turn on causes increase of current at one shunt resistor. Therefore, all three MOSFET turn on is recommended when C_{boot} is charged initially if three shunt is used for current sensing considering OCP level. For 15 V supply point of view, one low side turn on can be recommended because peak bootstrap current (I_{boot_peak}) is lower than that of all three low side turn on due to series resistance and inductance in load. On the contrary to this, voltage drop in shunt R is reduced by one low side turn on in one shunt R system due to a small I_{boot}.

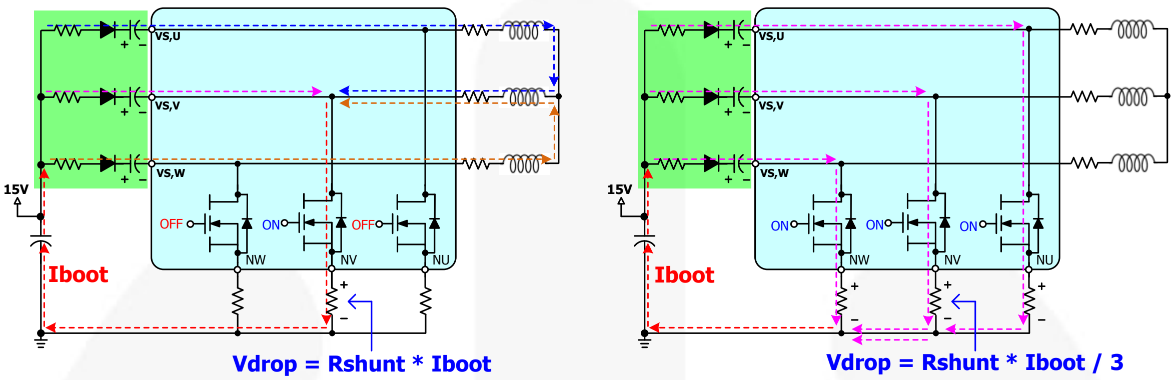

Figure 7. Initial Charging Mechanism according to Low Side Turn On State in Three Shunt R (I_{boot} peak value of left schematic is lower than that of right schematic due to the impedance of load)

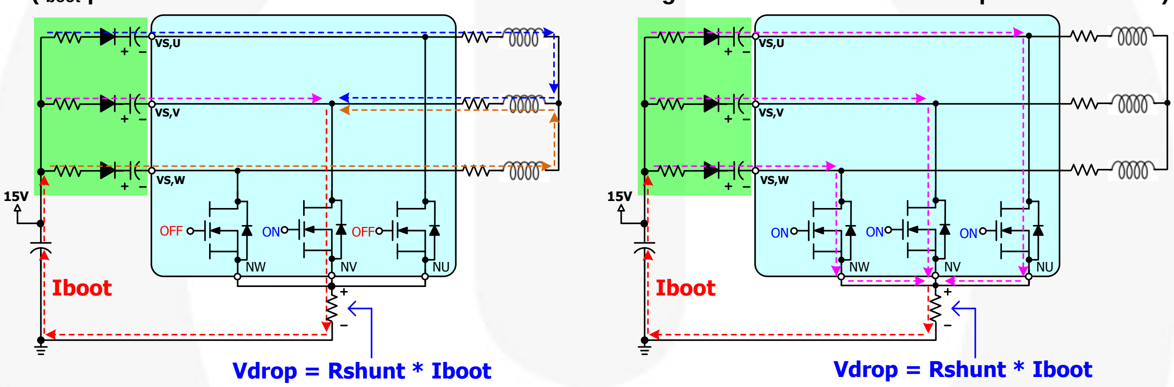

Figure 8. Initial Charging Mechanism according to Low Side Turn On State in One Shunt R

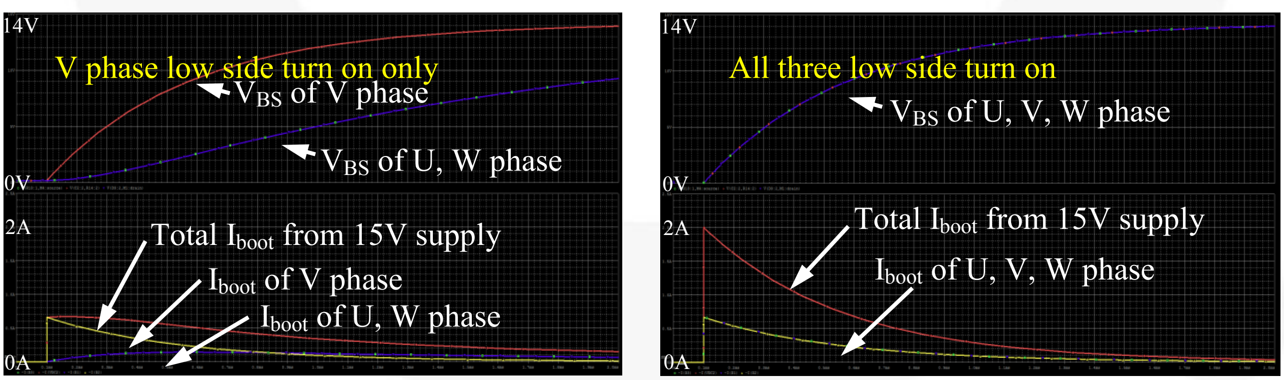

Figure 9. Initial charging of each phase according to low side turn on state (Each R_{boot} = 20 Ω, Each C_{boot} = 22 µF, Load impedance = 20 Ω + 5 mH)

For initial C_{boot} charging by bootstrap circuit, it is recommended to consider:

A. *To reduce risk of UVLO fault: switching with duty ratio and increase of 15 V supply capacitance (or decrease of C_{boot}) needs to be considered.*

B. *To reduce risk of OCP fault: three shunt R condition ➔ three low side turn on, one shunt R condition ➔ one low side turn on.*

C. *To reduce total I_{boot} from 15 V supply due to lack of output current: one low side switching with small duty is recommended.*

1.3. Normal Operation

V_{BS} supply voltage ripple and average values are influenced by R_{boot}, C_{boot} and operating conditions. For stable operation, this ripple voltage should be kept within a recommended V_{BS} supply voltage range. In inverter operation, C_{boot} is charged when low side IGBT (MOSFET) or diode are conducted. When high side power switch operates, low average V_{BS} voltage causes increase of switching loss and conduction loss due to lower gate control voltage. And also high side gate driver's under-voltage lockout for V_{BS} supply should be considered. V_{BS} supply voltage should be higher than UVLO reset level before high side power switches operate if minimum V_{BS} supply voltage is lower than UVLO detection level.

Figure 10 shows explanation and recommendations of $_{VBS}$ supply voltage during inverter operations based on Motion SPM® products with variable R_{boot} and C_{boot} values.

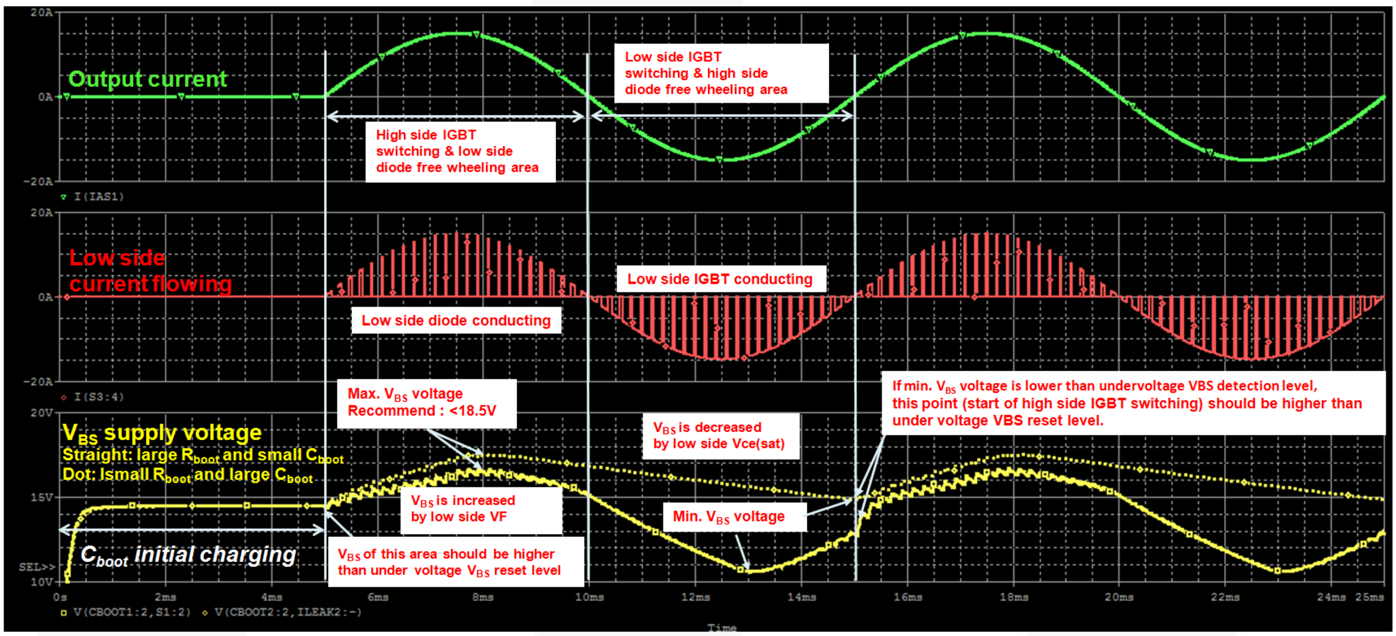

Figure 10. Example Waveform of I_{OUT} vs. V_{BS} supply voltage

V_{BS} supply ripple voltage and average voltage are influenced mainly by factors below. Please note that below results came from a general trend and can be different depending on device characteristics and conditions.

A. Small C_{boot} ➔ Ripple voltage of V_{BS} supply increases.
B. Large R_{boot} during ➔ Average voltage of V_{BS} supply decreases.
C. Large Shunt R (in three shunt resistors for each N terminal) ➔ Average voltage of V_{BS} supply decreases.
D. High V_{BS} supply current consumption ➔ Average voltage of V_{BS} supply decreases.
E. High operating current ➔ Average voltage of V_{BS} supply increases, ripple voltage of V_{BS} supply increases.
F. Low output current frequency ➔ V_{BS} supply ripple increases.
G. High modulation index (M.I) ➔ Average voltage of V_{BS} supply decreases.
H. High switching frequency ➔ Average voltage of V_{BS} supply decreases.

Figure 11 shows comparison results of V_{BS} supply voltage by variable condition.

Below condition is applied as a reference condition for each comparison.

A. Ideal circuit without any stray impedance in the loop.
B. C_{boot} initial charging mode: Low side IGBT full on for 15 ms.
C. 15A rated IGBT//diode Motion SPM® product, three shunt R at each N-terminal, High side IGBT Q_g = 45 nC
D. R_{boot} = 20 Ω, C_{boot} = 22 uF, Shunt R at N-terminal = 25 mΩ, V_{BS} supply current consume = 100 μA
E. V_{DC} = 300 V, V_{DD} = 15 V, f_{SW} = 10 kHz, F_O = 100 Hz, I_{OUT} = 15 A_{pk}, M.I = 0.9, SVPWM

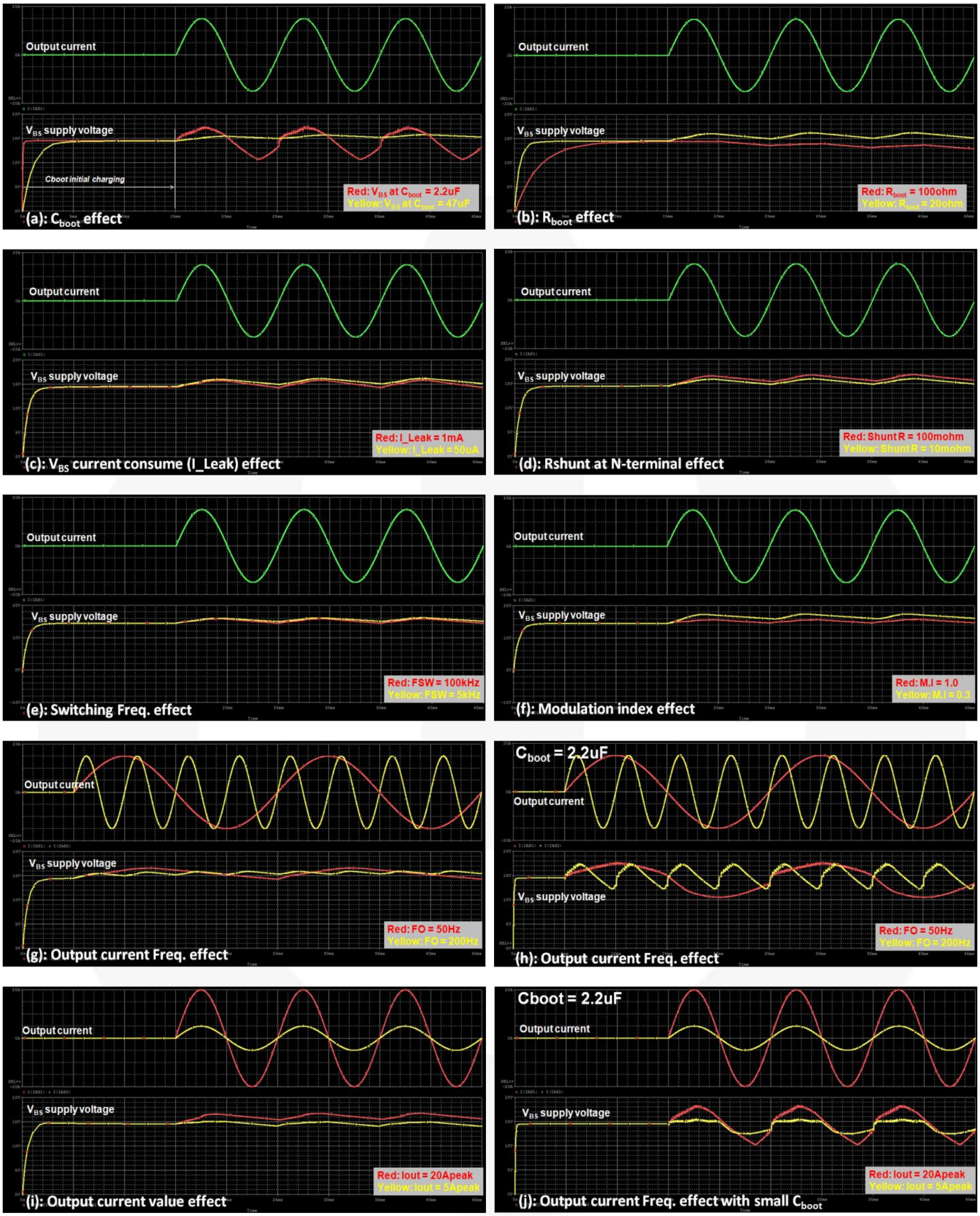

Figure 11. Example waveform of I_{OUT} vs. V_{BS} supply voltage according to parameters of passive components and operating condition

1.4. C_{boot} Selection Guide

The bootstrap capacitance needs to be selected based on V_{BS} supply positive and negative ripple voltage considering PWM methods. In trapezoidal PWM, sufficiently large C_{boot} is recommended because V_{BS} supply can go very low due to long discharge time without charging time. Allowable discharge voltage of C_{boot} (ΔV_{BS}) is determined by Under-voltage V_{BS} Detection (UVBSD) level. Usually, max. UVBSD is around 12.5 V in most of motion SPM® products. Thus, recommended allowable ΔV_{BS} is 2~3 V.

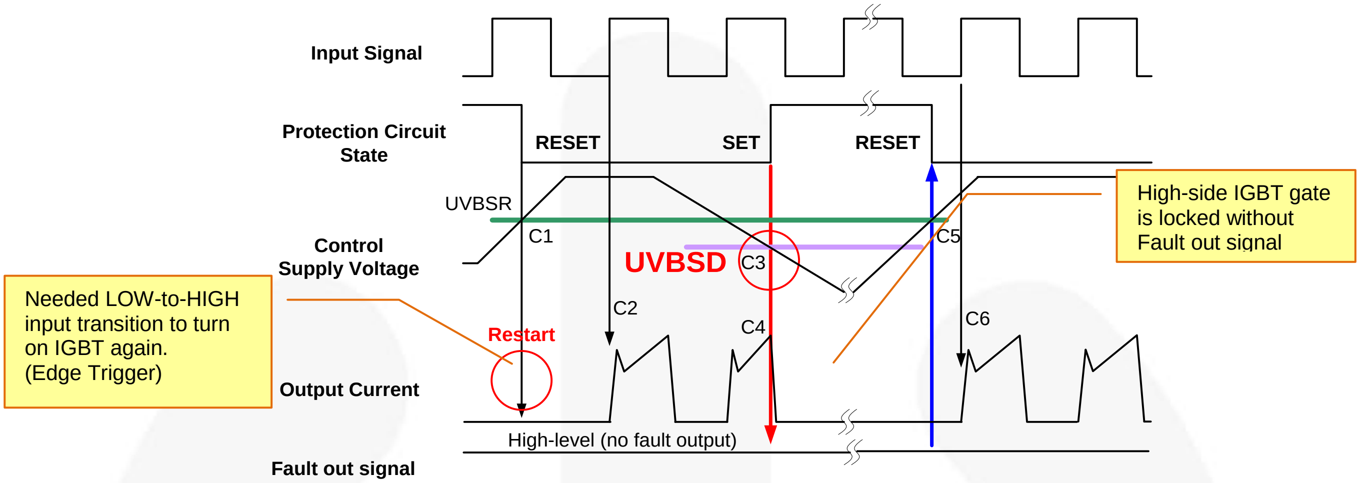

Figure 12. Timing Chart of High-Side Under-Voltage Protection Function

Discharge voltage of C_{boot} (ΔV_{BS}) is calculated by equation (2).

$$\Delta VBS = \frac{\Delta t \times ILeak}{Cboot} \qquad (2)$$

Δt: maximum time of C_{boot} discharging (All PWM 0V or high side turn on period);
ΔV_{BS}: the allowable discharge voltage of the C_{boot} and
I_{Leak}: maximum discharge current of the C_{boot}. Mainly via the following mechanisms:

- Quiescent current to the high-side control circuit in HVIC (IQBS).
- C_{boot} leakage current (ignored for non-electrolytic capacitors).

In sine-wave PWM with dead time, V_{BS} supply ripple voltage is varied by many factors. This ripple voltage is reduced efficiently by increase of C_{boot} capacitance. However, many users want to use small C_{boot} in low power system for cost reduction. It is necessary to measure V_{BS} voltage under the overload condition to check whether V_{BS} is within recommended range. Figure 13 shows a selection guide to determine proper C_{boot} value in the system.

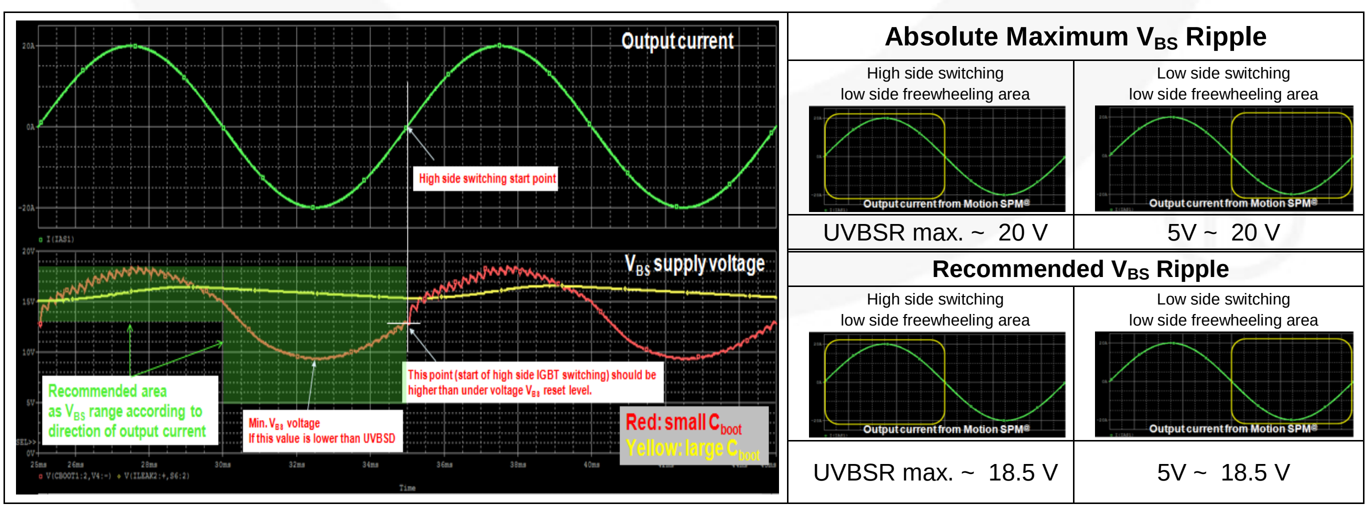

Figure 13. V_{BS} Supply Ripple Voltage Waveform, Maximum and Recommended Values

1.5. R_{boot} Selection Guide

1.5.1.Resistance Value of R_{boot}

Both initial charging time from 0 V to UVBSR as explained in page 3 of section '**Initial Charging**' and allowable peak current should be considered in selecting the resistance value

Required initial charging time defined by equations below:

$$MOSFET version: Initial\ charging\ time = -Rboot \times Cboot \times \frac{ln\left(1 - \frac{UVBSR\ max.}{VDD - Dboot\ Vth\ @IQBS\ max.}\right)}{low\ side\ on\ duty} \quad (3)$$

$$\boldsymbol{IGBT\ ver}sion: Initial\ charging\ time = -Rboot \times Cboot \times \frac{ln\left(1 - \frac{UVBSR\ max.}{VDD - Dboot\ Vth\ @IQBS\ max. - IGBT\ CE\ Vth\ @IQBS\ max.}\right)}{low\ side\ on\ duty} \quad (4)$$

Required min. Rbs considering peak inrush current:

$$\boldsymbol{MOSFET\ version: Peak\ inrushed\ current = \frac{(VDD - Dboot\ Vth - IGBT\ CE\ Vth\ @IQBS\ max.)}{Rboot}} \quad (5)$$

$$\boldsymbol{IGBT\ version: Peak\ inrushed\ current = \frac{(VDD - Dboot\ Vth\ @IQBS\ max. - IGBT\ CE\ Vth\ @IQBS\ max.)}{Rboot}} \quad (6)$$

Generally, each 0.6 V for both D_{boot} V_{th} and IGBT CE V_{th} can be available as its voltage drop.

A resistor R_{boot} must be added in series with the bootstrap diode to slow down the d_{VBS}/d_t. It also determines the time to charge the bootstrap capacitor during system operation after initial charging. The bootstrap capacitor has to be charged by ΔV during the minimum ON pulse width of low-side MOSFET or the minimum OFF pulse width of high-side MOSFET, t_O. Therefore, the value of R_{boot} needs to be determined by equation (7).

$$\boldsymbol{Rboot = \frac{(VDD - VBS) \times to}{Cboot\ \times \Delta VBS}} \quad (7)$$

1.5.2.Power Rating of R_{boot}

In terms of power rating of R_{boot}, pulse power rating should be considered for initial charging of bootstrap capacitor. To use a large bootstrap capacitor, high pulse power rating is required for the bootstrap resistor. An example of resistor pulse power rating is shown in Figure 14.

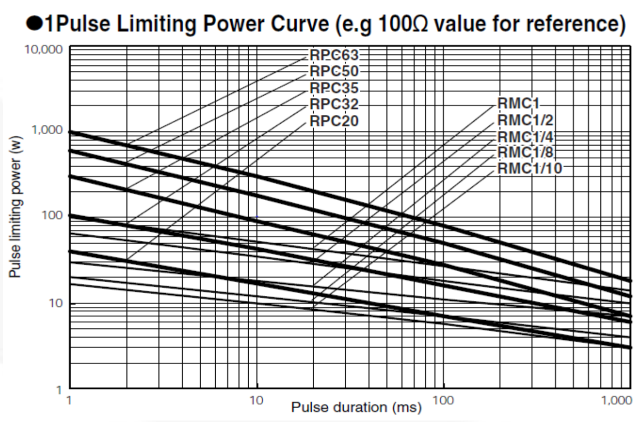

Figure 14. Example of Pulse Power Curve of Resistor (from KAMAYA OHM)

Required power and pulse duration times are calculated by equation (8) when C_{boot} is initially charged.

$$\boldsymbol{MOSFET\ version\ pulse\ power = \frac{(VDD - Dboot\ Vth\ @IQBS\ max.)^2}{Rboot}}$$

$$\boldsymbol{IGBT\ version\ pulse\ power = \frac{(VDD - Dboot\ Vth\ @IQBS\ max. - IGBT\ CE\ Vth\ @IQBS\ max.)^2}{Rboot}} \quad (8)$$

$$\boldsymbol{Pulse\ duration\ time = 0.5 \times Rboot \times Cboot}$$

1.6. Dboot Selection Guide

When high side IGBT (MOSFET) or diode conducts, the bootstrap diode (DBS) supports the entire bus voltage. Hence the withstand voltage higher than rated voltage of Motion SPM® product is recommended. It is important that this diode should be a fast recovery (recovery time < 100 ns) device to minimize the amount of charge that is fed back from the bootstrap capacitor into the V_{DD} supply. Similarly, the high voltage reverse leakage current is important if the capacitor has to store charge for long periods of time.

1.7. Integrated Bootstrap Circuit Information in Motion SPM® Products

Many Motion SPM® product provides integrated bootstrap circuit for user's convenience.

Table 1. Integrated Bootstrap Circuit information and Allowable max. C_{boot} values

Series of Motion SPM® products	Related Part Name	Max. Repetitive Reverse Voltage	Integrated Bootstrap Circuit	Allowable Max. C_{boot}
Motion SPM 5, V2	FSB50xx0Ax FSB50xx0SFx	600 V	Bare bootstrap diode R_{boot} is around 20 Ω	Up to 220 µF
Motion SPM 8	FNB8xx60Tx	600 V	Integrated in driver R_{boot} is around 280 Ω	Up to 220 µF
Motion SPM 55, V2	FNx5xx60TDx	600 V	Integrated in driver R_{boot} is around 280 Ω	Up to 220 µF
Motion SPM 45H	FNx4xx60xx	600 V	Bare bootstrap diode R_{boot} is around 20 Ω	Up to 220 µF
Motion SPM 3, V4~V6	FSBBxxCH60x FNB3xx60T	600 V	Bare bootstrap diode R_{boot} is around 20 Ω	Up to 220 µF
Motion SPM 2	FNx2xx60	600 V	Bare bootstrap diode No R_{boot} (external R_{boot} is required)	Limited by external R_{boot}
	FNx2xx12Ax	1200 V		

1.8. Required Precautions to Prevent Malfunction or Damage

For output current sensing, V_{BS} supply can be used for current sensor circuit. At this condition, V_{BS} supply current consumption is increased by additional current consumption for current sensor circuit. This should be considered for R_{boot} values because avg. V_{BS} voltage drop is large if R_{boot} value is high in this condition. Thus, high side shut down by UVBS or high power loss of high side by low control voltage can occur if large R_{boot} is used when V_{BS} supply current consumption is very high.

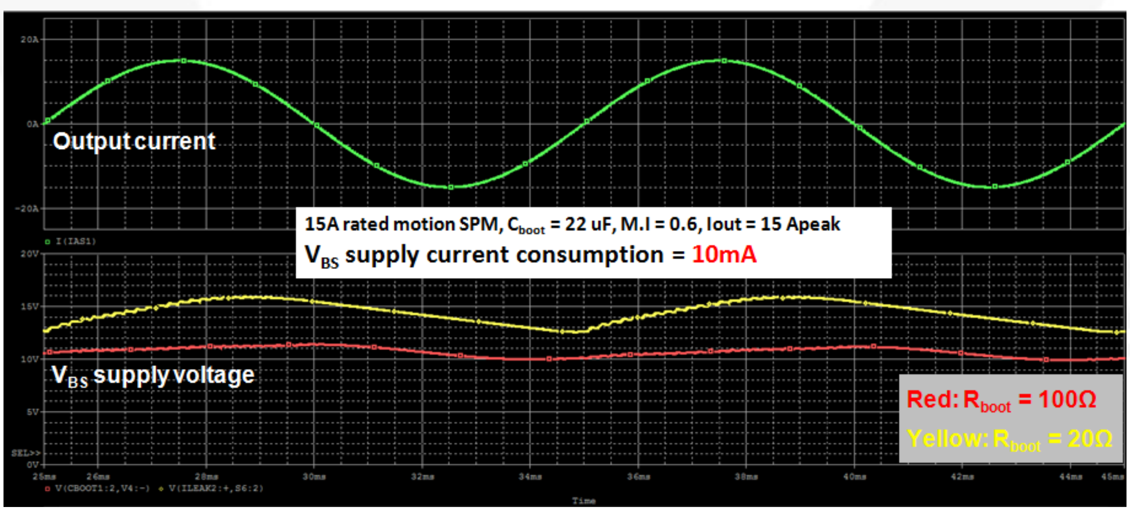

Figure 15. Example waveform of I_{OUT} vs. V_{BS} supply voltage under the variable R_{boot} and high V_{BS} supply current consumption condition

Small R_{boot} and C_{boot} can cause overcharging of C_{boot} when high side is turned by stray inductance and turn off di/dt. The C_{boot} can become overcharged, and the high side gate driver has damage by over-voltage stress if it exceeds the absolute maximum rating of high side gate driver. To prevent this situation proper selections of C_{boot} and R_{boot} are required considering overload condition like high operating current.

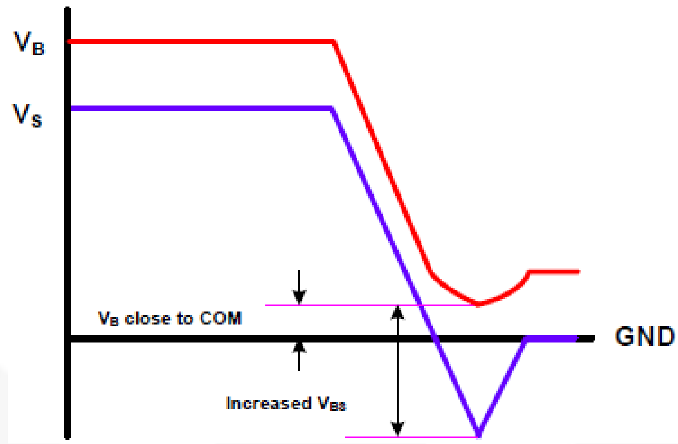

Figure 16. Typical Response of V_B and V_S when High Side Turn Off

1.9. Frequently Asked Questions and Answers

A. *Is it possible to use one R_{boot} for all three phase?*

:Yes, one R_{boot} can be used as a common R_{boot}. Charging time can increase to charge parallel C_{boot}. Please refer to Section 1.1.

B. *There are over-current detection problem when C_{boot} is charged initially. How to prevent this event?*

:Soft ware debugging to ignore OCP at initial charging

:In one shunt R configuration ➔ One low side turn on to reduce total I_{boot} for all three C_{boot} initial charging

:Connect resistor between output (U, V, W) and GND (N-termianls or COM) for C_{boot} charging in advance before initial charging sequence (recommended resistor value is around several hundred of kΩ)

C. *What is allowable maximum C_{boot}?*

:It depends on pulse power rating and resistance of R_{boot}.

:In Motion SPM® products which provides integrated bootstrap circuit, allowable max. C_{boot} is 220 µF.

D. *Ceramic type capacitors can be used as C_{boot}?*

:Yes, ceramic capacitors can be used. Please select proper capacitance

E. *7 times larger 15 V source capacitor is recommended to prevent UVLO fault. We want to apply large capacitance as C_{boot}. How can we reduce 15 V source capacitor without UVLO risk?*

: Please refer to below recommended circuit.

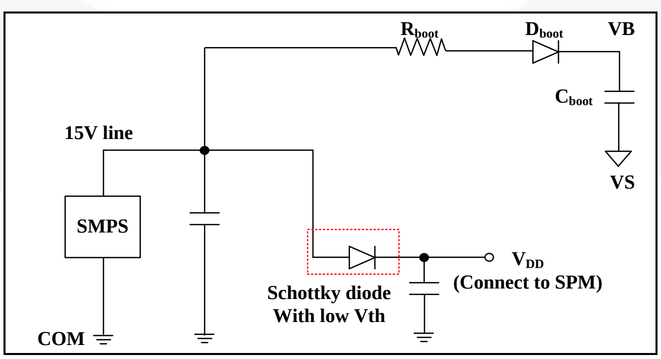

Figure 17. Recommended Circuit to Apply Small Source Capacitor

2. Related Resources

AN-9096, Smart Power Module, Motion SPM® 55 Series User's Guide

AN-6067, Design and Application Guide of Bootstrap Circuit for High-Voltage Gate-Drive IC

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