

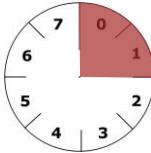

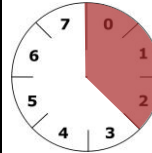
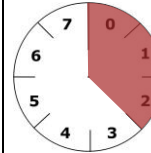
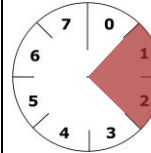
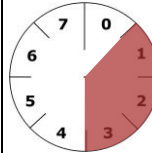


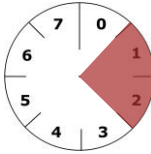
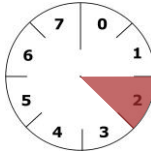

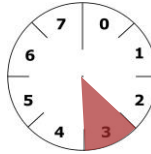
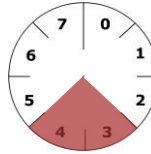
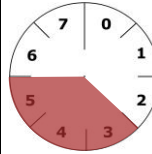


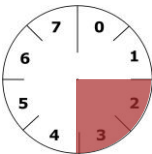
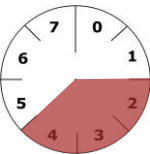
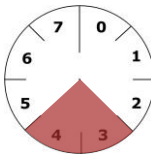
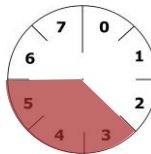
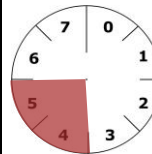
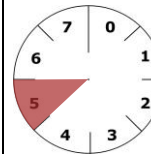
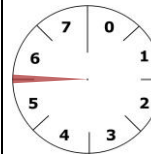
Sender:

8	9	10	11	12	13	14	
							
init	send F0	send F1	send F2	-	-	recv A0	send F3

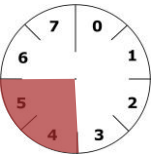

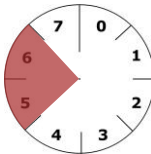

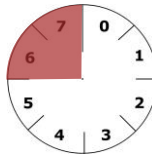


Receiver:

8	9	10	11	12	13	14	
							
init	-	recv F0	recv F1	recv F2	send A0	send A1	send A2

Sender:

8	9	10	11	12	13	14	
							
recv A1	send F4	recv A2	send F5	recv A3	ack F4	recv A5	

Receiver:

8	9	10	11	12	13	14	
							
recv F3	send A3	recv F4	send A4	recv F5	send A5	-	