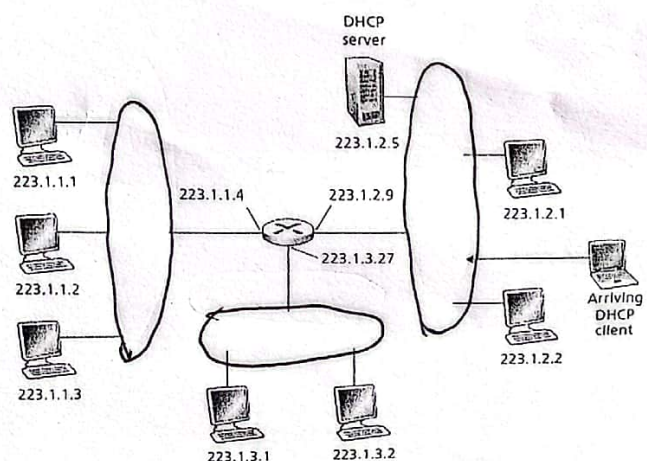


1. (2 marks) Suppose Host A wants to send a large file to Host B. The path from Host A to Host B has three links, connected sequentially, of rates $R_1 = 500$ kbps, $R_2 = 100$ Kbps, and $R_3 = 1$ Mbps.
 - a. Assuming no other traffic in the network, what is the throughput for the file transfer?
 - b. Suppose the file is 4 million bytes. Roughly, how long will it take to transfer the file to Host B?
2. (2 marks) Consider a router buffer preceding an outbound link. In this problem, you will use Little's formula, a famous formula from queuing theory. Let N denote the average number of packets in the buffer plus the packet being transmitted. Let a denote the rate of packets arriving at the link. Let d denote the average total delay (i.e., the queuing delay plus the transmission delay) experienced by a packet. Little's formula is $N = a * d$. Suppose that on average, the buffer contains 100 packets, and the average packet queuing delay is 20 msec. The link's transmission rate is 100 packets/sec. Using Little's formula, what is the average packet arrival rate, assuming there is no packet loss?
3. (3 marks) What is traffic intensity? What causes it to grow at higher values? How can you mitigate the negative effect of higher values of traffic intensity? Explain with the help of a figure.
4. (2+2 marks) Consider a TCP Reno connection between a source and destination, with $CWND = 1024$, experiences a loss of 10 consecutive packets starting from 1 to 10. However, the later packets are received by the destination. Thus, the losses are detected by the reception of duplicate acknowledgment packets.
 - a. What will be the size of $CWND$ before the source handles the first lost packet?
 - b. Suppose an extended version of Reno, namely TCP New Reno, introduces a concept of partial acknowledgment. Unlike decreasing the $CWND$ by 50% on detecting the loss of every packet in Reno, it identifies whether the loss is within the same window of the previous loss; if yes, it doesn't decrease the $CWND$ further; otherwise, it follows the same process as Reno does. Do you think the proposed approach will bring additional benefits for the connection? Justify your answer.

5.

(3 marks) In the figure shown at the right side, a client arriving at subnet 223.1.2/24 will be able to get an IP address from the DHCP server. How can a client arriving at subnet 223.1.3/24 or 223.1.1/24 will get an IP address? Explain the steps with help of a figure.



6. (2 marks) How does DNS help to implement 'load distribution'? Briefly explain.
7. (2 marks) Does server pushing in HTTP/2 enhance data transfer performance? Justify.
8. (2 Marks) Write down the process of calculating timeout period for a TCP sender. Mention appropriate reasons of choices made for different parameters involved in this calculation.

Answer all the questions

1. A use case should cover all likely exceptions. Consider the use case "Data Entry" for an e-commerce system where a customer is asked to complete and send in an electronic form including name, address, goods wanted and payment details. The details sent by the user are validated and saved to the database. 5

List at least 2 exceptions you think can occur for this use case.
2. What is the difference between a scenario and a use case? When do you use each construct? 5
3. A hotel reservation system allows customers to book rooms online. Create a formal use case for the scenario of a customer booking a room for a specific date and duration. The hotel offers rooms of various sizes, with availability based on the dates, which the customer will also need to identify. 5
4. Consider the following description of a system and give a use case diagram to model this system. 5

A user can request a quiz for the system. The system picks a set of question from its database and composes them together to make a quiz. It rates the user's answers, and gives hints if the user requests it. In addition to users, we also have tutors who provide questions and hints. And also examiners who must certify questions to make sure they are not too trivial, and that they are sensible.

5. Consider the following description of a *buy a product* system. 10

Customer browses catalog, selects items to buy and then goes to check out. Customer fills in shipping information (address, receive time). System presents full pricing information and customer fills in credit card information. System authorizes purchase, confirms sale and sends confirming email to customer.

Identify and name all objects (entity, boundary and control). Give statechart for 'customer' object.

University of Dhaka
Department of Computer Science and Engineering
3rd Year 1st Semester Incourse Examination, Session: 2021-2022
CSE – 3104, Database Management System II

Total Marks: 25

Time: 1 Hour 30 Minutes

(Answer All of the following Questions)

1. a) Why leaf nodes of a B⁺ tree are chained together? 1
 b) Mention one advantage and one disadvantage of dynamic hashing. 1
 c) You have 10 million tuples in a relation and you have to create a B⁺ index on it. If no. of pointers $n = 100$, what will be height of the tree? 1
 d) Classify hashing. 1
 e) What is fudge factor? 1
 f) Why closed hashing is preferred for managing database system? 1
 g) Which is better for range query: 'Ordered Indexing' or 'Hashing'? Explain briefly. 1
2. Consider an 'Employee' relation below and its three orientations shown in Fig. 2.1, Fig. 2.2 and Fig. 2.3.

Emp_Id	Age	Designation	Salary
E_001	27	Sr. Executive	50,000
E_002	42	Sr. Manager	100,000
E_003	33	Asst. Manager	70,000
E_004	25	Executive	33,000
E_005	53	GM	150,000
E_006	48	Sr. Manager	90,000
E_007	26	Executive	35,000
E_008	36	Sr. Executive	55,000
E_009	65	MD	200,000
E_010	35	Asst. Manager	67,000
E_011	28	Executive	27,000
E_012	39	Manager	80,000
E_013	50	DGM	130,000
E_014	32	Asst. Manager	70,000
E_015	23	Executive	33,000

Fig. 2.1 Employee (Order by 'Emp_id')

Emp_Id	Age	Designation	Salary
E_003	33	Asst. Manager	70,000
E_010	35	Asst. Manager	67,000
E_014	32	Asst. Manager	70,000
E_013	50	DGM	130,000
E_004	25	Executive	33,000
E_007	26	Executive	35,000
E_011	28	Executive	27,000
E_015	23	Executive	33,000
E_005	53	GM	150,000
E_012	39	Manager	80,000
E_009	65	MD	200,000
E_001	27	Sr. Executive	50,000
E_008	36	Sr. Executive	55,000
E_002	42	Sr. Manager	100,000
E_006	48	Sr. Manager	90,000

Fig. 2.2 Employee (Order by 'Designation')

Emp_Id	Age	Designation	Salary
E_011	28	Executive	27,000
E_004	25	Executive	33,000
E_015	23	Executive	33,000
E_007	26	Executive	35,000
E_001	27	Sr. Executive	50,000
E_008	36	Sr. Executive	55,000
E_010	35	Asst. Manager	67,000
E_003	33	Asst. Manager	70,000
E_014	32	Asst. Manager	70,000
E_012	39	Manager	80,000
E_006	48	Sr. Manager	90,000
E_002	42	Sr. Manager	100,000
E_013	50	DGM	130,000
E_005	53	GM	150,000
E_009	65	MD	200,000

Fig. 2.3 Employee (Order by 'Salary')

- a) Build a dense primary index on 'Designation' and a secondary index on 'Salary' for relation in Fig. 2.2. 5
- b) Build a B⁺ tree index based on the search key 'Age' for relation in Fig. 2.1. Consider the value of $n = 4$. Show the minimum necessary tree structure to reflect changes in the B⁺ tree while adding different 'Age' values as per tuple sequence. 6
- c) After building the tree, delete the values 33 and then 27 from the B⁺ tree mentioned in 2.b) (Show only the area of modified tree structure). 2
- d) Arrange the relation in Fig. 2.1 into a 'Hash' file organization with 5 buckets with a capacity of 4 tuples per bucket and based on the search key value 'Age' and use the hash function $h(\text{Age} \text{ MOD } 5)$. Show overflow chaining if needed. 5

CSE3103: Microprocessor and Microcontroller

Computer Science and Engineering, University of Dhaka,
Mid Term Exam

Marks : 20

Time: 1 hour 15 Minutes

March 07, 2023

[Answer All the Following Questions]

1. Convert the following ARM assembly code into machine language. Write the instructions in hexadecimal.[2]

- ROR R4,R8,#21
- SUBGT R1, R2, R3 LSR #4

2. What are the three registers that are initialized on Reset?

3. Register R1 has the value 0x80008001, what is its value after the following operations are performed independently:

Operation	R1
LSR R1,R1,#3	
LSL R1,R1,#4	
ASR R1,R1,#1	

4. Write the equivalent ARM based assembly code for the following C code:

```
for(i = 0, f = 0; i < N; i++)  
    f = f + c[i] * x[i];
```

5. Consider the following ARM assembly language snippet. The numbers to the left of each instruction indicate the instruction address.[6]

```
0x000A0028 MOV R4, R1  
0x000A0030 SUB R4, R0, R3, ROR R4  
0x000A0034 BL func2
```

- List the addressing mode used at each line of code.
- Calculate the Effective address (EA) for each instruction

6. Consider a four bit ALU which does four bit arithmetic. When the following four bit numbers are added, what is the status of NZCV flags? 1101 + 1011

- (i) NZCV = 0111 (ii) NZCV = 1000 (iii) NZCV = 1001 (iv) NZCV = 1010
7. How many bits are required to specify the Register operands in an ARM7 instruction?
- (i) 32 bits (ii) 4 bits (iii) 2 bits (iv) 16 bits
8. State whether the following statement is either true or false. Reset vector is the location of the first instruction executed by the processor when power is applied. This instruction branches to the initialization code.
- (i) True (ii) False
9. If the initial register contents of $R0$, $R1$ and $R2$ were $R0 = 0x00000000$, $R1 = 0x02040608$, $R2 = 0x10305070$. Assume $R0$ is the result register, after one of the operations below was performed on $R1$ and $R2$, which has been modified to $R0 = 0x12345678$. What was the operation performed on the contents of $R2$ and $R1$?
- (i) AND (ii) ~~BIC~~ (iii) ORR (iv) MUL
10. Which of the following instruction ignores Operand1
- (i) MOV, (ii) MUL, (iii) ADD, (iv) SUB

CSE3102– Microprocessor and Microcontroller
Midterm, 2023 (Microcontroller)
Computer Science and Engineering
University of Dhaka

This exam contains 4 questions. Answer all 4 questions. **Total marks is 20.**

1. (5 points) Let the peripheral RCC (Reset and Clock Control) located at address 0x40023800H and offsets for AHB1ENR, APB1ENR, and APB2ENR are 0x30H, 0x40H, 0x44H. Write 'C' statements to activate peripheral clocks for GPIOB, UART2, and TIM1. Where GPIOB clock enables bit is '1' and connected to AHB1 bus, TIM1 enable bit is '0' and connected to APB2 bus, and USART2 connected to APB1 bus and enable bit is '17'.
2. (5 points) Why is setting or resetting a GPIO pin via the BSRR register recommended rather than using ODR? Let a push switch is connected to pin PA5, and write 'C' statements to verify whether the switch is on or off.
3. (5 points) A timer TIM3 is connected to the APB1 bus at bit '1' (clock enable bit) via a 16-bit pre-scaler register 'PSC,' The bus clock speed is 25 MHz. Moreover, the TIM3 has two well-known registers, TIM2_ARR and TIM2_CNT. Write a piece of code to generate a one-second delay.
4. (5 points) Let the clock speed of the APB1 bus is 45 MHz. Determine the mantissa and fraction to set the USART2 baud rate 115200. Remember that the USART2_BBR register has 12 bits to set mantissa, and the fractional part is coded in 4 bits. The equation for baud rate calculation is:

$$TX/RXbaud_rate = \frac{f_{CK}}{2 \times (8 - OVER8) \times USARTDIV}$$