EEE-1212: Digital Logic Design Lab

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Experiment Number: 06

Name of the Experiment:

a)Verification of IC-7483A
b) Design and construction of 3 Bit Adder/subtractor.

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Experiment name:

6. a)Verification of IC-7483-A
6. b) Design and construction of 3 Bit Adder/subtractor.

Objectives:

1. Testing the IC-7483A and find the summation of two numbers .
2. Setting up the circuit of 3 bit adder/subtractor and find the summation and subtraction of 3 bit numbers.

Theory:

Most modern computers use the 2's-complement system to represent negative numbers and to perform subtraction. The operations of addition and subtraction of signed numbers can be performed using only the addition operation if we use the 2's-complement form to represent negative numbers.

Combined Addition and Subtraction:

It should now be clear that the basic parallel-adder circuit can be used to perform addition or subtraction depending on whether the B number is left unchanged or is converted to its 2's complement. A complete circuit that can perform both addition and subtraction in the 2's-complement system is shown in the following figure:

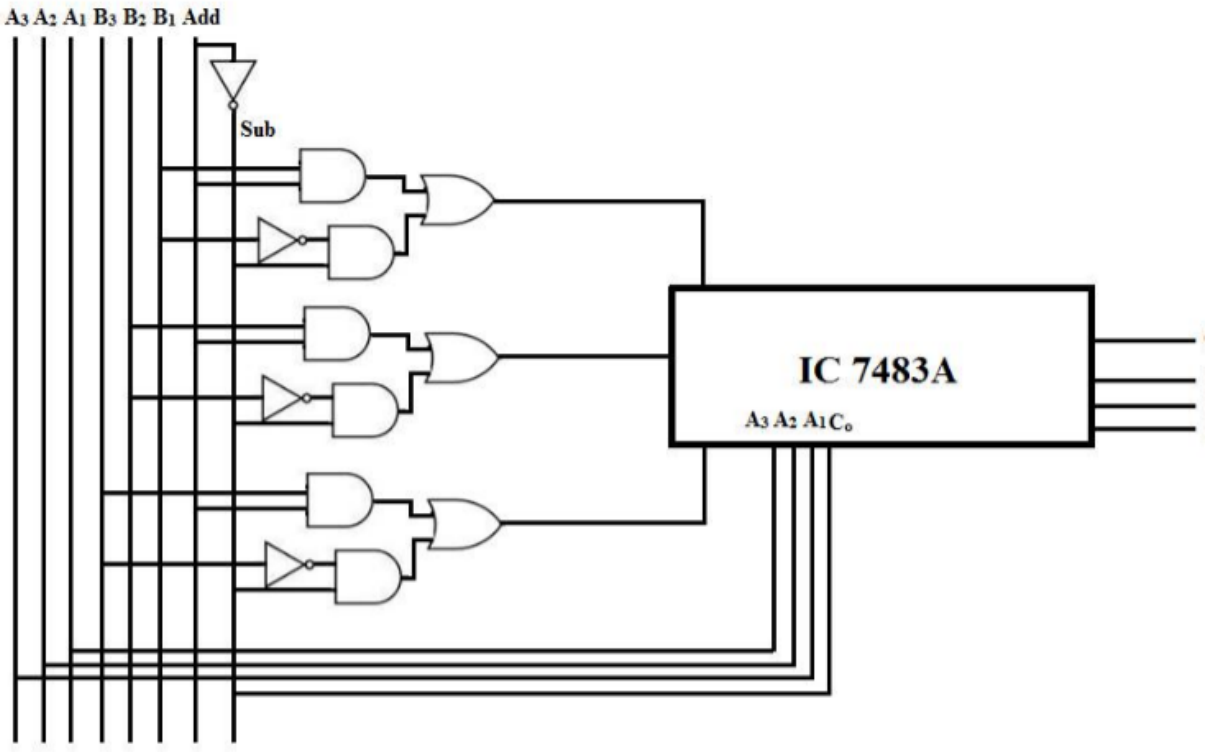

Fig: 3 bit adder / subtractor circuit

This adder/ subtractor circuit is controlled by the two control signals ADD and SUB. When the ADD level is HIGH, the circuit performs addition of the numbers stored in the A and B registers. When the SUB level is HIGH, the circuit subtracts the B-register number from the A-register number. The operation is described as follows:

1. Assume that and The disables (inhibits) AND gates 2, 4, and 6 holding their outputs at 0.The enables AND gates 1, 3 and 5 allowing their outputs to pass the B_1,B_2 and B_3 and levels, respectively.

2. The levels B_1 to B_3 pass through the OR gates into the three-bit parallel adder to be added to the bits A_1 to A_3 .The sum appears at the outputs $\sum_1$ to to $\sum_3$.

3. Note that SUB = 0 causes a carry $C_0 = 0$ into the adder.

4. Now assume that and The inhibits AND gates 1, 3, and 5.The enables AND gates 2, 4, and 6 so that their outputs pass the $\overline{B_1}$, $\overline{B_2}$, and $\overline{B_3}$ levels, respectively.

5. The levels $\overline{B_1}$to $\overline{B_3}$pass through the OR gates into the adder to be added to the bits A_1 to A_3. Note also that is now C_0 =1. Thus, the B-register number has essentially been converted to its 2's complement.

6. The difference appears at the outputs to $\sum_1$ to $\sum_3$.

Circuits like the adder/subtractor of Figure 6-14 are used in computers because they provide a relatively simple means for adding and subtracting signed binary numbers. In most computers, the outputs present at the $\sum$ output lines are usually transferred into the A register (accumulator), so that the results of the addition or subtraction always end up stored in the A register. This is accomplished by applying a TRANSFER pulse to the CLK inputs of register A.

Instruments:

1. A Trainer Board
2. IC(s) IC-7432, 2 IC(s)-7408,IC-7404,IC-7483A
3. Connecting wires.

Procedure (a):

1) At first we placed the integrated circuit with IC-7483A on a breadboard properly. This IC is placed across the gap in the center of the breadboard.

2) Then we connected the inputs of the logic gate to the logic sources and its output to the logic indicator.

3) We gave biasing to the ICs with the VCC (5 volt) and GND (0 volt).

4) Then we implemented the logic circuits using logic gates and obtained equations. We connected the inputs with input switches and the output with output LEDs. The output of the circuit will be shown on the LED. (LED Off = 0, LED On = 1).

5) We observed outputs for various input combination .

Procedure (b):

1) At first we placed the integrated circuit with IC-7404,IC-7432 and 2 IC(s)-7408 on a breadboard properly. This IC(s) are placed across the gap in the center of the breadboard.

2) Then we connected the inputs of the logic gate to the logic sources and its output to the logic indicator.

3) We also connected an input ADD. We also used an input SUB by complementing ADD.

4) Then we connected the three output of the three OR gates to IC-7483A as an input. We gave other three input of IC-7483A from the logic sources.

5) We gave biasing to the ICs with the VCC (5 volt) and GND (0 volt).

6) Then we implemented the logic circuits using logic gates and obtained equations. We connected the inputs with input switches and the output with output LEDs. The output of the circuit will be shown on the LED. (LED Off = 0, LED On = 1).

7) We observed outputs for various input combination .

Result (a):

Ic no : 7483A

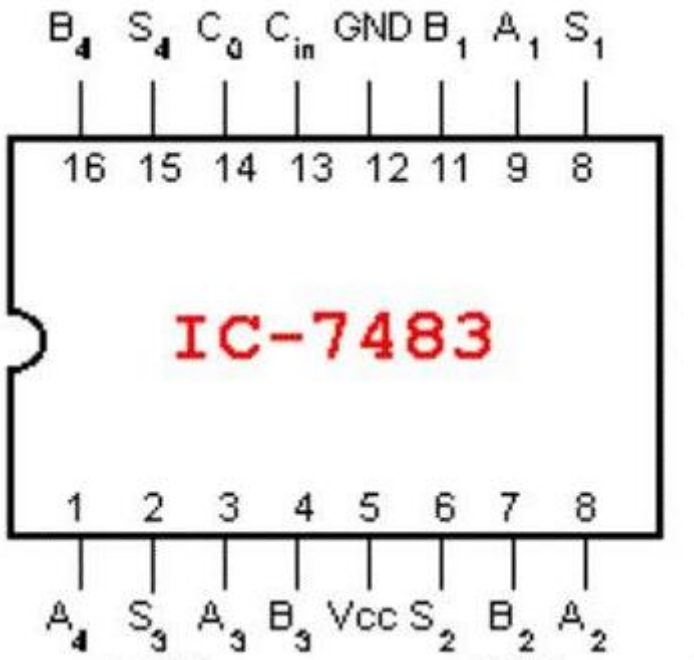

Fig : Pin diagram of IC-7483A

Example: If we add 3 and 8

3 = 0011

8 = 1000

11 = 1011

Here $A_1 = 1$ $A_2 = 1$ $A_3 = 0$ $A_4 = 0$

And here $B_1 = 0$ $B_2 = 0$ $B_3 = 0$ $B_4 = 0$

And here $C_0 = 0$

So we get $\sum 1 = 1$ $\sum 2 = 1$ $\sum 3 = 0$ $\sum 4 = 1$

So we see LED light is on at the logic indicator source at $\sum 1$, $\sum 2$, $\sum 4$ and LED is off at the place $\sum 3$.

So by this IC we can add two numbers by various combination of numbers from 0 to 15.

Result (b):

In this experiment we add two numbers(3 bits) or subtract two numbers(3 bits) from each other and then get the output.

Addition:

If we add 3 and 7

3 = 011

7 = 111

10 = 1010

Here $A_1 = 1$ $A_2 = 1$ $A_3 = 0$

And here $B_1 = 1$ $B_2 = 1$ $B_3 = 1$

And here $C_0 = 0$

So we get $\sum 1 = 0$ $\sum 2 = 1$ $\sum 3 = 0$ $C_4 = 1$

So we see LED light is on at the logic indicator source at $\sum 2$, C4 and LED is off at the place $\sum 3$ and $\sum 1$.

So by this process we can add two numbers and get summation of two numbers.

Subtraction:

If we subtract 7 from 3 so it means

=7-3

=7+ (-3)

So we have to add 7 and -3. We have to find the value of -3. We can find the value of -3 by using 2's complement system.

We know

3 = 011

1's complement form of 011 is 100

If we add 1 then we get 2's complement form.

So 2's complement form is 101.

So -3 = 101

7 = 111

-3 = 101

4 = 100

Here $A_1 = 1$ $A_2 = 1$ $A_3 = 1$

And here $B_1 = 0$ $B_2 = 0$ $B_3 = 1$

And here $C_0 = 1$

So here we get $\sum 1 = 0$ $\sum 2 = 0$ $\sum 3 = 1$ $C_4 = 1$

So we see LED light is on at the logic indicator source at $\sum 3$, C_4 and LED is off at the place $\sum 1$ and $\sum 2$.

So by this process we subtract from one no to another and get the result of the subtraction form of two numbers.

Discussion:

In this experiment we had to design and construct a 3 bit adder/subtractor. We also have to test the IC-7483A and find the summation of the two numbers by this IC. We constructed the circuit in the bread board using the IC's but faced some problem during the experiment.

1. At first we don't understand what we have to find out by using this IC. So we need a little bit more to start our experiment.
2. The logic circuit of 3 bit adder/ subtractor is very complicated and we used 5 IC(s) at the same time. So needed so many wires to construct the circuit. So we also faced some problems to do this work.
3. Besides, we also faced some technical difficulties when using trainer board. All input gates weren't working properly and the output LED was also not functioning properly. So we changed this board and started our work with another trainer board.

But we figured them out and completed the experiment successfully.