University of Dhaka

Department of Computer Science and Engineering 3rd Year 1st Semester Incourse Examination, 2023 CSE-3105: Multivariable Calculus and Geometry

Total Marks: 100 Time: 1.5 Hour

94	Determine whether the points lie on a straight line or not. (i) $< 5, -3, -6 >$ (ii) $< 7, -3, 4 >$ (iii) $< 1, 0, 5 >$	[10]
92	Consider the vectors, (i) < 2, 2, -1 > (ii) < 5, -3 , 2 > Find a unit vector u such that u is perpendicular to both the vectors	[10]
Q 3	Find the scalar projection and vector projection of < 2 , 2 , $1 > $ onto < 1 , 1 , $1 > $	[10]
94	Find $\lim_{t\to 0} r(t)$, where $r(t) = <(1+t^2-3t^3)$, te^{-t} , $\frac{\sin(t)}{t} >$	[10]
Q 5	Two aircrafts travel along the space curves considering the following parametric equations.	
	\square Aircraft 1: $P_1(t) = \langle t, 1 + t^2, t^3 \rangle$	
	\square Aircraft 2: $P_2(t) = \langle 2t - 1, 3t^3, t^2 + 14 \rangle$	
	The aviation company has a computing system to determine whether these two traveling paths are conflicting or not. Now,	
	 Find whether the aircrafts will collide or not. Find the space point where their paths intersect, if exist. 	[10] [10]
Q6/	A wagon is pulled a distance of 100 m along a horizontal path by a constant force of 70 N. As a result, 6000J work is done by the force.	
	 Find the angle between the wagon handle with the horizon. 	[10]
	 Explain how the amount of work done could be increased. 	[10]
97.	Find the length of the arc of the circular helix with vector equation	
V	$\mathbf{r}(t) = \cos(t)\mathbf{i} + \sin(t)\mathbf{j} + t^2\mathbf{k} \text{ from the point } (1,0,0) \text{ to the point } (1,0,2\pi).$	[10]
Q8.	A batter hits a baseball 3m above the ground toward the center field fence, which is 10m high and 400m from home plate. The ball leaves the bat with a speed of 150m/s at an angle of 60° above the horizontal. Is it a home run? [In other words, does the ball clear	
	the fence?] [Consider the gravity value as 10 m/s ²]	[10]



University of Dhaka

Dept. of Computer Science and Engineering 3rd Year 1st Semester Incourse Examination, 2023

Answer all the questions. Marks are indicated at the left side bracket of each question.

Time: 75 Minutes

CSE 3101 - Computer Networking

Total Mark: 20

- 1. (a) (2 points) Define traffic intensity. "Propagation delay and Processing delay depends on the hardware of the router." Do you agree with this statement? Explain your answer.
 - (b) (3 points) Briefly discuss how cookies can solve the lack of HTTP being a stateless protocol. Explain with the help of an interaction diagram between an HTTP client and a server.
- 2. (a) (2 points) Define the HOL blocking issue in HTTP/1.1 with the help of an example. Explain how HTTP/2 attempts to solve it.

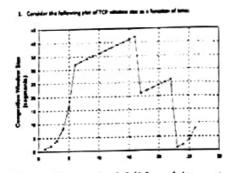
(b) (3 points)

Given a UDP segment (at the right side) to be sent by a sender to a receiver. Investigate the value of the checksum of the payload of the segment. Show all the steps. Finally, calculate the value of the length field in decimal. Show all steps of calculation.

	32 bits —
Source Port#	Destination Port#
Length =?	Checksum=?
01100110011001	10 0000111100001111

UDP Segment

- 3. (a) (2 points) Suppose, Mr. X uses an email client (mail reader) to send an email to Mr. Y who uses a web-based email account (such as Hotmail or Gmail). The IP address of Mr. Y's mail server is initially unknown to Mr. X's mail server. List all the application layer protocols that might be used to transfer the messages when Mr. X sends the email to the time when Mr. Y reads it. Draw a diagram and clearly mention how these application-layer protocols are used when transferring the message.
 - (b) (3 points) Consider a packet of length L that begins at router A and travels over three links to a destination router B. Suppose the packet is 1500 bytes. The propagation speed on all three links is 2.5 x 108 m/s and the transmission rates of all three links are 2.5 Mbps. The packet switch processing delay of all the routers is 3 msec. If the lengths of the first, second, and third links are 5000 km, 4000 km, and 1000 km respectively, analyze the scenario and calculate the end-to-end delay.
 - i) In the right side figure, identify the time intervals when TCP congestion avoidance is operating.
- 4. (a) (3 points)
- ii) What are the values of cwnd and ssthresh at the time slot 24?
- iii) Let x represent the last digit of your class roll number multiplied by 30. During what time slot the xth segment is sent?



(b) (2 points) An ISP wants to generate a block of addresses starting with 171.81.0.0/16 and it wants to distribute these blocks to 1152 business customers as follows. The first group has 128 medium-sized businesses; each needs 128 addresses. The second group has 1024 small businesses; each needs 32 addresses. Design the subblocks by giving the network address and address range using slash notation, i.e., in the form of a.b.c.d/x for each subblock.

University of Dhaka Department of Computer Science and Engineering Incourse Examination 3rd Year 1st Semester, Session: 2022-2023

CSE – 3104, Database Management System II

Total Mark	s: 25 Time: 1 Hour 30 Minutes	
	(Answer All of the following Questions)	
by For	sidering reliability and performance of disks explain why we should use RAID. a DBMS system which RAID level suits better? Explain your answer. w the slotted page structure of variable length records for storing records within a k.	3 2 2
fi) I "B ⁺ sear	the is fat and short but binary tree is thin and tail. For have been given $\frac{1}{1}$ in the hard short but binary tree is thin and tail. For have been given $\frac{1}{1}$ in the hard short but binary tree is thin and tail. For have been given $\frac{1}{1}$ in this is the hard short but binary tree is thin and tail. For have been given $\frac{1}{1}$ in this is the hard short but binary tree is thin and tail. For have been given $\frac{1}{1}$ in this is the hard short but binary tree is thin and tail.	3 2 2
and and Is B	width of the tree. tree better than B ⁺ -tree as an index? Express your opinion.	3
b) Wri	sify index. e down the disadvantages of static hashing and also dynamic (extendable) hashing. sose you are a database designer. What file organization and indexing technique will prefer and why? Explain your answer.	1 3 4

CSE 3102: Software Engineering

Marks: 30

Time: 75 minutes

Answer all the questions

Consider the following description of a system and based on the description answer the following questions

A token-ring based local-area-network (LAN) is a network consisting of nodes, in which network packets are sent around. Every node has a unique name within the network, and refers to its next node. Different kinds of nodes exist: workstations are originators of messages; servers and printers are network nodes that can receive messages. Packets contain an originator, a destination and content, and are sent around on a network. A LAN is a circular configuration of nodes.

Describe any two scenarios formally.	5 5
Give use case diagram and mention to which use case(s) the aforementioned	10
scenarios are related to. Identify and name all objects (entity, boundary and control) and give their	5
aggregation. Give state chart for the 'Packet' object.	5

CSE3103- Microprocessor and Microcontroller Midterm Exam, Jan-June, 2024 Computer Science and Engineering University of Dhaka Exam Duration: 90 Minutes

March 13, 2024

This exam contains 4 questions. Answer any 3 (three) questions. Total marks is 30.

(a) (5 points) Convert the following ARM assembly code into machine language. Write the instructions in hexadecimal.

- i. EORGTS R6, R3, #5
- ii. ADD R1, R2, R3, LSL #9
- (b) (5 points) Translate the following machine language to the ARM assembly code
 - i. 0xE3821F21
 - ii. 0xE1A04638

STR R3, [R5], #4

- 2. (a) (2 points) Assuming that the registers R1, R1, R3, R4 contain the values 0x11aa, 0x22bb, 0x33cc, 0x44dd respectively, and that the register R5 contains the value 0x1000, what is the value in R5 after each of the following ARM instructions in this program fragment and what byte value is stored in each affected memory location? (Assume a little-endian configuration.)

 STR R2, [R5, #4]
 - (1) point) What are the three registers that are initialized on Reset in cortex M4?
 - (c) (4 points) For each ARM instruction below, answer the following questions:
 - i. What is the addressing mode of the instruction?
 - ii. What is the effective address (EA) of the operand?
 - iii. What will be change to the content of memory or registers after the instruction is executed?

Note that, the instructions are executed individually. No dependency preserves among the instructions. You can assume the initial value of the registers

- i. LDR R3, [R4, #-4]!
- ^ii. ADD R5, R6, #13
- (d) (3 points) Write an assembly language to disable all the interrupts with priority 0x30.
- 3. Timer 'TIM6' is a basic timer that keeps counts of the clock plus feeds into it. Timer 'TIM6' is connected to the 'APB1' bus running with a 45MHz clock. 'TIM6_PSC' is a 16-bit prescaler register or divider to feed the desired clock to the timer. 'TIM6_ARR' and 'TIM6_CNT' are 16-bit registers dedicated to auto-reloading the timer's counting range and instantaneous count value. The timer generates an update interrupt for the count configuration whenever the 'TIM6_CNT' register value equals the counting range. (hints: other registers are given)
 - (2 points) Enable and configure the timer for upcounter that generate an update interrupt after every 1 (one) millisecond.

- (b) (3 points) The 'TIM6_SR' (32-bit) shows the status of the timer, including update interrupt at be position '0'. The update interrupts service routing is 'tim6_update_isr()', which updates a global variable (say uint64_t) to keep the millisecond count. Write down the update function.
- (g) (3 points) Next, write down a delay function say 'ms_delay(uint32_t x)' to sleep or wait for 'x' / milliseconds.
- (d) (2 points) Now, write a program/function that can determine the number of millisecond to print hello world 10000 times.
- UART4 connection to APB1 bus running in 22.5MHz using PC10 and PC11 for TX and RX. Configure the UART4 with BAUD rate 115200 with no 8 or 16 sampling. To do so determine the steps and write down the content of the UART4 and coresponding GPIO port. The alternate function for TX/RX GPIO is AF8. (hints: registers are given)

3 3 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 1 1 1 1	9 8 7 6 5 4 3 2 1 0	Instruction Type
Condition 0 0 1 OPCODE S Rn Rs	OPERAND-2	Deta processing
0000 = EQ - Z set (equal) 0001 = NE - Z clear (not equal) 0010 = HS / CS - C set (unsigned higher or same) 0011 = LO / CC - C clear (unsigned lower)	1001 = LS - C clear or 2 or same) 1010 = GE - N set and N clear (>or =) 1011 = LT - N set and N V set (>)	v set, or N clear and V
0100 = MI -N set (negative) 0101 = PL - N clear (positive or zero) 0110 = VS - V set (overflow) 0111 = VC - V clear (no overflow)	1100 = GT - Z clear, and set, or N clear at 1101 = LE - Z set, or N clear and V set (nd V set (>) set and V clear,or N
1000 = HI - C set and Z clear (unsigned higher)	1110 = AL - always 1111 = NV - reserved.	

Opcode	Instruction
0000	AND
0001	EOR
0010	SUB
0100	ADD
0101	ADC
0110	SBC
1010	CMP
1100	ORR
1101	MOV /Shift
1110	BIC

\mathbf{sh}	Instruction
00	LSL
01	LSR
10	ASR
11	ROR

Table 1: Binary of the Opcodes

												/	/		
31	30	- 29	28	27	26	25	24	23	22	21	20	19	18	17	16
		DAC EN	PWR EN	CEC EN	CAN2 EN	CAN1 EN	FMPI2C1 EN	I2C3 EN	I2C2 EN	I2C1 EN	UART5 EN	UART4 EN	USART3 EN	USART2	SPDIFRX EN
		rw	rw	w	w	ſW	ſW	rw	ſW	ſW	ſw	w	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI3 EN	SPI2 EN			WWDG EN			TIM14 EN	TIM13 EN	TIM12 EN	TIM7 EN	TIMS EN	TIM5 EN	TIM4 EN	TIM3 EN	TIM2 EN
rw	rw			8			rw	rw	w	w	~	w	w	w	rw
31	30	29	2	8 2	27 2	6 2	5 24	23	22	21	20	19	18	17	16
-	OTGHS ULPIEN	OTGHS EN	3				1		DMA2 EN	DMA1 EN		Ĕ.	BKP SRAME	in in	t _{es}
	rw	ſW							ſw	rw			ſw		
15	14	13	1	2 1	1 1	0 1	9 8	7	6	5	4	3	2	1	0
13			CF E	RC N	į			GPIOH EN	GPIOG EN	GPIOF EN	GPIOE EN	GPIOD EN	GPIOC EN	GPIOE EN	GPIOA EN
			0	w				rw	rw	w	rw	rw	rw	rw	ſW

Figure 1: RCC_APB1ENR & RCC_AHB1ENR registers

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								ARPE				ОРМ	URS	UDIS	CEN
								rw				ſW	rw	ſW	ſw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			11				UDE				T	\top			UIE
							rw								rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															UIF
									1						rc_w0

Figure 2: Timer registers: CR1, DIER, SR,

	Table 164. USART register map and reset values															_																	
Offset	Register	뜐	30	53	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	9	2	7	3	7	1	0
0x00	USART_SR																							CTS	LBD	TXE	TC	RXNE	IDLE	ORE	NF	FE	Ä
	Reset value	Ħ				П																		0	0	1	1	0	0	0	0	0	0
0x04	USART_DR																											D	R[8:	:0]			
	Reset value	П				\sqcap	\neg																		0	0	0	0	0	0	0	0	0
0x08	USART_BRR	П																			DI	V_M	lant	38 2	(15:	4]			DIV_Fra [3:0]				on
	Reset value	П	\neg	\neg			7	\exists										0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	USART_CR1					1												OVER8		UE	M	WAKE	PCE	PS	PEE	TXEIE	TCIE	RXNEIE	IOLEIE	Œ	RE	RWC	XBS
	Reset value	H	7	7	7	7	7	7	1									0		٥	0	0	0	0	0	0	0	0	0	٥	0	0	0
\longrightarrow			_	_	_	_	_	_	7	_			_	7	7	7	7		•	٧	✓'	•		•			•	•	7	J,	✓		

Table 26. GPIO register map and reset values

		_	_	_	_	_					9:-			<u></u>		_	res				_												
Offset	Register	31	30	53	58	27	5 6	22	77	2	7 2	20	19	18	11	16	15	*	5	Ŧ	9	6	æ	7	9	5	4	•	7	-	•		
0x00	GPIOA_ MODER	MODED1811-01	MODEN 19(1.9)	MODER14[1:0]		MODER13(1:0)	MODER12[1:0]			- MODER11[1:0]		MODER10[1:0]		MODER9[1:0]	MODER8[1:0]		MODER7[1:0]		MODER6[1:0]		MODERS[1:0]		MODERS[1:0]		MODER4[1:0]	0.000 C	MODERS[1:0]	MODED 21-01	modernal reg	MODER 171-01		MODERO(1:0)	
	Reset value	1	0	1	0	1	0	0	0	0 (0	o	0	0	0	0	0 (9	0 0	0	0	0	0	0	0	0	0	0	0	ग	0		
0x00	GPIOB_ MODER	MODER15[1:0]		MODER 14[1:0]		MODER13[1:0]		MODER12[1:0]		MODER 01[1:0]		MODER10[1:0]		MODERS[1:0]	MODERBIT:01	66	MODER7[1:0]		MODER6[1:0]		MODER5[1:0]	2000	MODER4[1:0]	1000	MODERAL: UJ	MODER 21-01	[0::1]	MODER 171:01		MODERO(1:0)	•		
	Reset value	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0	7	0 0	0	0	1	0	1	0	0	0	0	0	٥	0		
0x00	GPIOx_MODER (where x = CH)	10.513407004.01	MODER 19[1:0]	MODER14[1-0]	MODER14[1:0]		MODER IST. 5	MODER12[1:0]		MODER11[1:0]		MODER10[1:0]		MODERS[1:0]	MODER8(1:0)		MODER7[1:0]		MODER6[1:0]		MODER5[1:0]	MODE STATE	MODER4[1:0]	MODED 214-01	MODERAJ I.UJ	MODER 211-01	io: lavaou	MODER 1[1:0]		MODEROI1:01			
	Reset value	0	0	0	0	0	0	0	0	0 (0	0	0	0	0	0	0 0	,	0 0	0	0	0	0	0	0	0	٥	0	0	٥	0		
0x04	GPIOx_ OTYPER (where x = AH)																OT15	5	OT13	1110	OT10	ОТЭ	ОТВ	017	ОТ6	OTS	OT4	OT3	OT2	OT1	οTο		
	Reset value	Γ							7	\top	T						0 0	1	0 0	0	0	0	0	0	0	0	0	0	0	0	0		
0x08	GPIOx_ OSPEEDER (where x = AH except B)	2717	OSPEEDK15[130]	OSPEEDR14H-01	Contraction in	IO: NEFOUSSISSI	in lei necestros	OSPEEDR12(1:0)		OSPEEDR11110	A STATE OF THE PROPERTY OF THE	OSFEEDRIO(1:0)		CSreenwall.ul	OSPEEDR8[1:0]		OSPEEDR7[1:0]		OSPEEDR6[1:0]		OSPEEDR5[1:0]	OSPEEDD411-0	OSF EEDNA [1:4]	OSPEEDB314:01	001 55000	OSPEEDRANGO	In a land	OSPEEDR1[[1:0]		OSPEEDROI1:01			
	Reset value	0	0	0	0	0	0	S	0	6 1	3 0	0	0	0	0	0	0 0	1	0 0	0	0	0	0	0	0	0	0	0	0	0	0		
0x08	GPIOB_ OSPEEDER	2000	USPEEDK15[1:0]	OSPEEDR14I1-01	6	CONTRACTOR	COLECTIVE INC.	OSPEEDRIMIN		OSPEEDRING		OSPEEDR10[1:0]	300000	OSPEEDR9(1:0)	OSPEEDR8(1:0)		OSPEEDR7[1:0]		OSPEEDR6[1:0]		OSPEEDR5(1:0)	OSBEEDBAILO	OSPEEDAN I.O.	OSPEEDB3(1-0)	סט בבסיים יים	OSPEEDR2(1:0)	1	OSPEEDR1[1:0]		OSPEEDR0[1:0]			
	Reset value	0	0	0	0	0	0	0	0	0 (0 0	0	0	0	0	0	0 0	1	0 0	0	0	0	0	1	1	0	0	0	0	0	0		
0x20	GPIOx_AFRL (where x = AH)	AF	RL	7[3:0	ני	j AFRL6				AFF	L5[3	:0]	AI	FRL	4[3:0	oj l	AFR	1.3	[3:0]	Ā	FRL	ب 2[3:	0]	AF	RL	1[3:0	ונ	AF	RL0	(3:0	ı		
	Reset value	0	0	0	0	0	0	0 (0	0 0	0	0	0	0	0	٥	0 0	Ī	0 0	0	0	0	0	0	0	0	٥	0	0	0	0		
0x24	GPIOx_AFRH (where x = AH)	AF			_	H13]	_	0 AFRH1				AFRH		_	╙	FRH]		Ь,	RH	_	4	_	RH8	_	4							
	Reset value	0	0	٥	٥	0	0	0 0	١	0 0	0	0	0	0	٥	٥	0 0	1	9 0	0	0	0	0	0	0	이	의	0	<u>•</u>	0	0		