Cache Simulator

This projects implement a cache simulator that will:

* Allow user configuration of associativity, size and block size.
* Read the user specified trace.
* Classify each memory read/write as a:

– Hit – Compulsory Miss

– Capacity Miss

– Conflict Miss

* Output to stdout the miss rate, number of read and write transactions to memory and emit a file indicating the classification of each memory access

When run, the simulator should output the parameters of the cache (number of ways, number of sets, size of a line), the size of each field in the address (tag, index, offset), the miss rate (as a percentage), and the number of read and write transactions to main memory.

* An example run is included below:
* ./cacheSim -t traces/gcc.trace -s 1 -w 2 -l 256 Ways: 2; Sets: 2; Line Size: 256B Tag: 23 bits; Index: 1 bits; Offset: 8 bits Miss Rate: 21.030943%
* Read Transactions: 108453 Write Transactions: 19014
* Output a file indicating the classification of each access.