COL216 Computer Architecture
Notes on Lab Assignment 4

Here are some clarifications/suggestions regarding this lab assignment.

Which modules are combinational circuits and which ones are sequential circuits?

ALU, Shifter, Multiplier and Processor-Memory path are combinational circuits. Register file has asynchronous read and synchronous write. That means, it acts as a combinational circuit while reading (data is read continuously from the registers selected by the given addresses), and as a sequential circuit while writing (state change of the selected register takes place on a clock edge).

ALU

Design the ALU with just DP instructions in mind. The ability to do address offset addition/subtraction for DT | b | bl instructions and addition required for mla instruction comes for free. We assume that arrangement of feeding the right inputs at right time will be made outside ALU. When ALU is asked to perform addition, it need not be told whether this addition is for add instruction or ldr instruction or bl instruction or mla instruction.

Shifter

ARM assemblers translate LSL # 0 or LSR # 0 or ASR # 0 or ROR # 0, all of these to LSL # 0. On the other hand, at machine code level, LSR # 0, ASR # 0 and ROR # 0 have special meanings (see the instruction set document for details). For the current exercise, we ignore these special meanings and treat at machine level all shifts with shift amount zero as no shift. The carry output in this case is equal to carry input.

When a register specifies the shift amount, what happens in case this register has a value more than 31? Again the instruction set document defines the instruction behavior for these cases. However, we will assume that the value in the register is not more than 31 and look at only least significant 5 bits of that register.

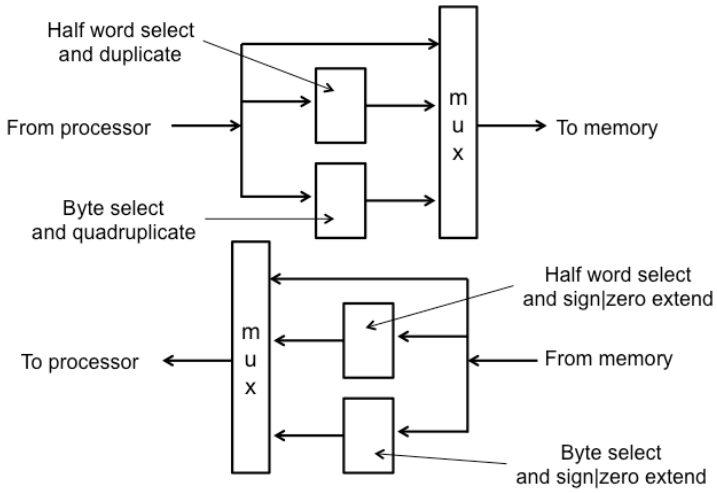
Register File

If you have already designed RF with synchronous read, you will still be able to work with it if the data read from RF is to be operated upon in a subsequent cycle (this would be true in the current exercise). Synchronous read means that you have created registers in the output ports. These registers will replace the registers that are typically required between the RF outputs and modules like ALU when the RF has asynchronous read.

Duplication of register 15 out side the array is not essential. An additional output port driven by register 15 to supply memory address for instruction fetching may be provided.

Processor-Memory path

In the lecture, I had shown only bits and pieces of processor-memory path design. These need to be put together using multiplexers. A conceptual diagram is shown below. Logic to generate memory write enable signals is not shown here.



The boxes shown in the figure need not be created separately and instantiated. The entire module may be described behaviourally. Decoding of instruction may be kept out of this module. The multiplexers only needs to know whether it is word transfer or half word transfer or byte transfer. The sign|zero extension boxes only need to know whether it is sign extension or zero extension.