Figure 1: Functional Performance Across Capacitive Loads (In SS Corner)

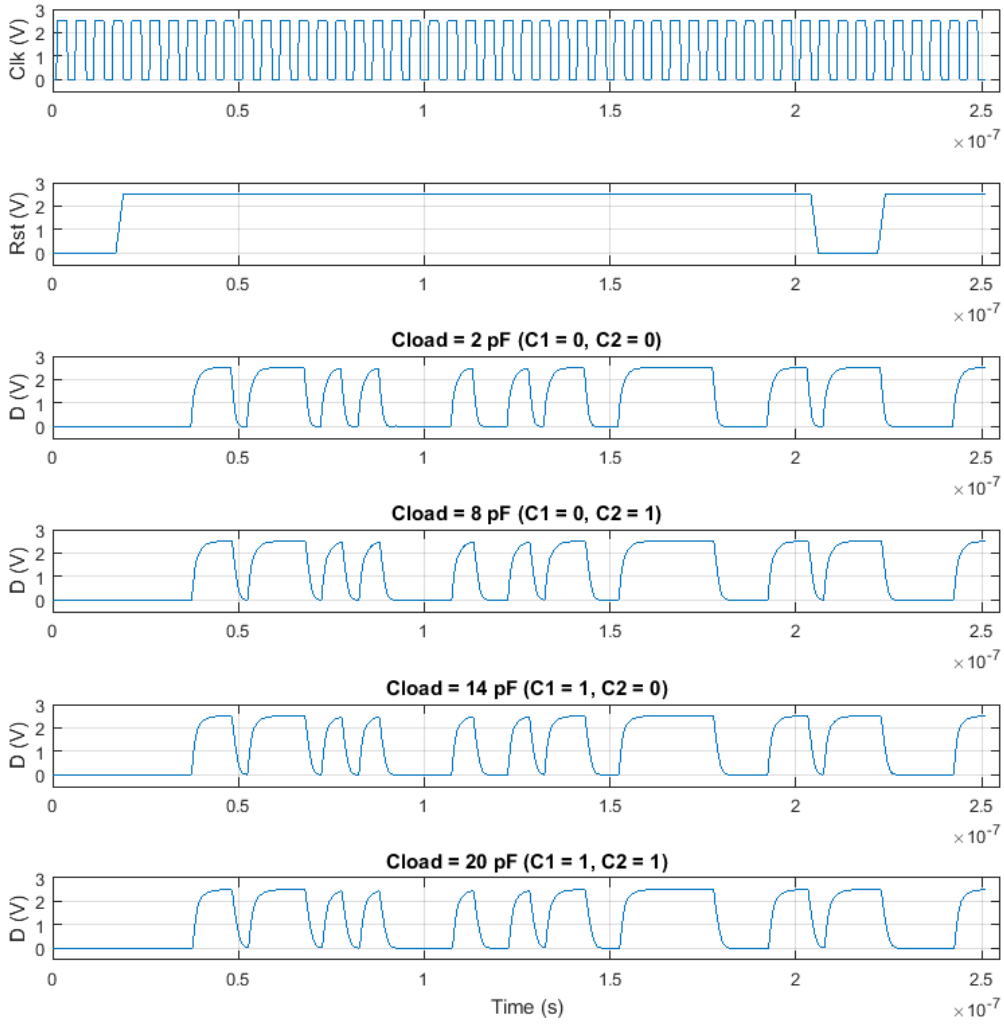

Table 1: Power Dissipation Across Capacitive Loads (In TT Corner)

Capacitive Load	Average Power
2 pF (C1=0, C2=0)	1.042 mW
8 pF (C1=0, C2=1)	2.789 mW
14 pF (C1=1, C2=0)	4.604 mW
20 pF (C1=1, C2=1)	6.340 mW

The power consumption of this system is dominated by the switching power required to drive the parasitic capacitances in the superbuffer connected to the output as well as the capacitive load at the output. The switching power consumed by the clock as well as the static and short-circuit power consumed by the transistors in the system contributed a small but meaningful amount of power, while the power consumed by the reset and select signals was negligible. As expected based on these observations, there is a large change in the power consumed by the circuit as the capacitive load is varied from its largest value (consuming maximum power) to its smallest value (consuming minimal power).