Statements of Contribution

Steven Blair: At a high level, I was primarily responsible for maintaining the library of circuit symbols and schematics that were used in the final design; producing the top level schematic for the final design; running simulations on the final design to verify performance; and teaching and debugging the various tools that our team during the project used that were not used in normal classroom assignments (i.e., Virtuoso Schematic and ADE). At a lower level, I produced schematics for two pulse registers that were considered for selection as our final register, refined the schematic for the TSPC register that was selected as our final register, and produced schematics for the Schmitt trigger and decoder module; additionally, I produced layouts for the Schmitt Trigger and NAND2 gate. Toward the end of the project, I found the final sizes for the superbuffers and multiplexer that achieved the minimum necessary sizing for timing closure, and I contributed to the final report by generating waveforms and diagrams for the report, producing writeups for the report, and putting the report together prior to printing.

Alex Kaputska: When the team examined the various register designs before deciding which one to use for the final design, I created the schematic for a complementary static CMOS design and ran several simple simulations to verify the performance of the design. When we moved on to the other components of the design, I did the calculations and schematics for the four superbuffers used for the four different capacitive load ranges. When it came time to do layouts, I did the initial layouts for the multiplexer and demultiplexer which needed to be tweaked later when the design changed. When we moved onto the simulations, I worked with Jeffrey to simulate our extracted netlist with all four loads over every operating corner, verifying correct operation and exporting the plots needed for the main part of the report. Finally, when we had to draw the schematics for the report in Microsoft Visio, I did the TSPC register and the decoder then gathered all of the transistor-level schematics together so that Steven and Alex could do the final layout for the report.

Jeffrey Lee: During the schematic production part of the project, everyone produced a different register design so that we could compare the designs and select the best design for implementation in the linear feedback shift register. While I worked on a C^2MOS register, we decided that the C^2MOS register consumed too much power and decided on a different register instead. During the layout production part of the project, I produced initial layouts for each of the superbuffers based on designs that my group members gave me. When the report was being put together, I collected the extracted the netlists and ran the simulations needed to acquire plots for the report, and I created transistor-level schematics for the demultiplexer, multiplexer, and XOR modules as well as gate-level schematics for the pulse generator module.

Alexandra Wleklinski: I contributed schematics and layouts for the XOR gate, TSPC register, pulse generator, and linear feedback shift register; produced layouts for many other blocks in the system including the final implementations of the superbuffers, multiplexer, demultiplexer, linear feedback shift register, and decoder; and contributed to the routing of the top-level system. The most challenging task of layout was resizing the superbuffers and incorporating multipliers and fingers in the layout to get a good fit for the top-level system. Additionally, I helped in verifying and debugging correct operation throughout the project and especially during the transition from schematic to layout.