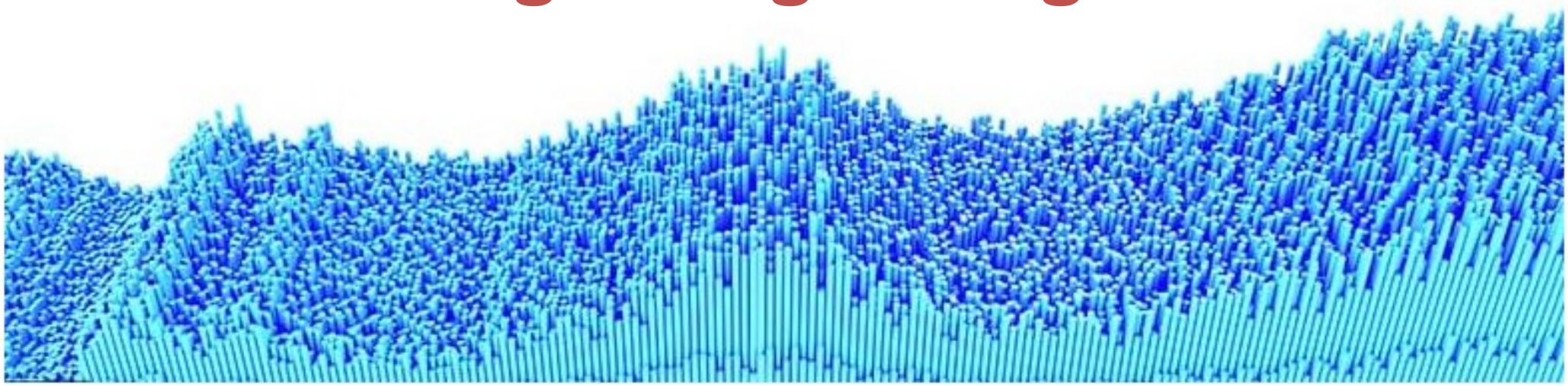
Verilog Description Language Tutorials

Digital Logic Design



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Verilog Description Language Tutorials

Testbench

Test Bench for Combination Logic

Test Bench for 4-to-1 MUX

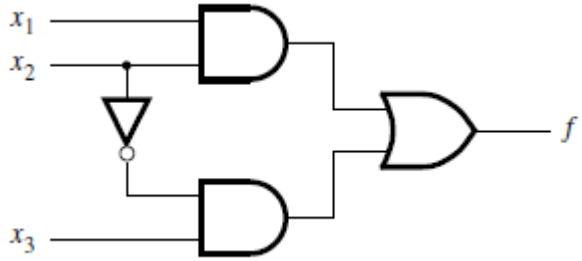
Description Level

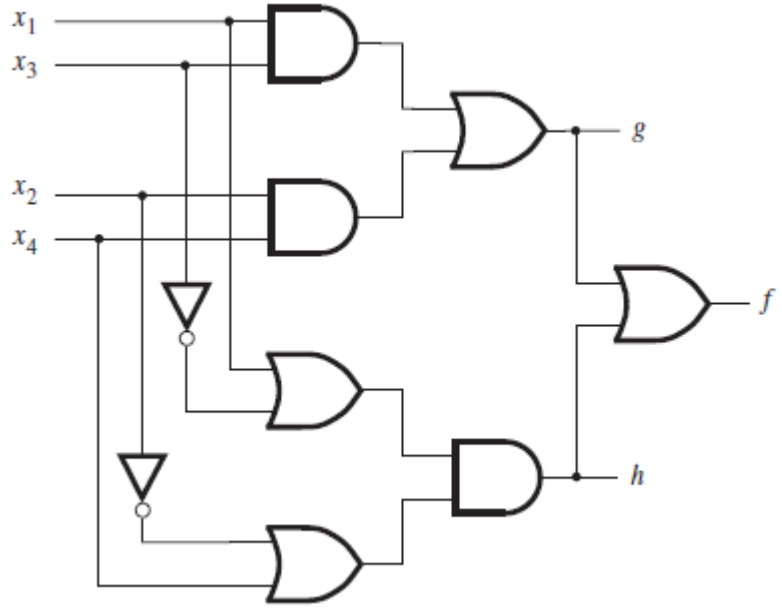
Verilog Success Story

- Verilog had been developed by Gateway Design Automation inc, 1984
- The success of Verilog is because of
  - Support of Programming Language Interface (PLI)
    - So users can expand a Verilog simulator for special objectives
  - Cooperation with major ASIC vendors like Motorola, National, UTMC, etc
    - Hardware Implementation could have been developed by ASIC chip designers
  - Development of logic synthesis tools developed by Synopsis
    - So Verilog have had capabilities of logic simulation as well as logic synthesis to a hardware
- The Verilog book by Samir can provide a easy jump start to Verilog world

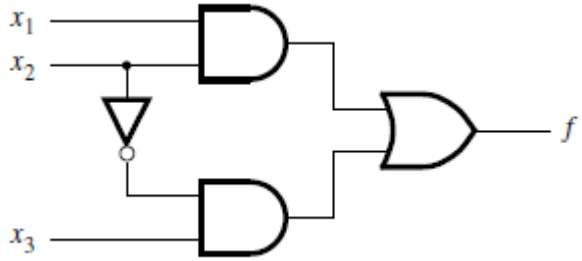
Level of Verilog Description Model

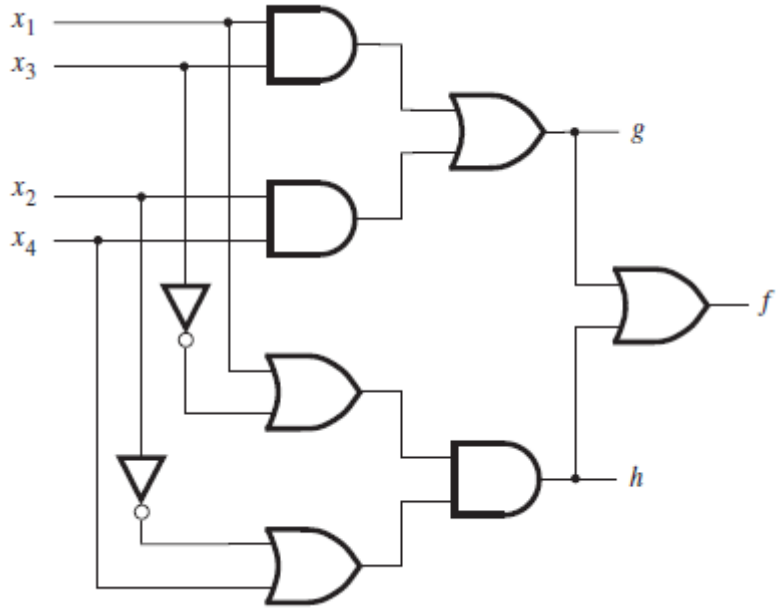
Simple Logic Design using Verilog (Gate-level)





Simple Logic Design using Verilog (RTL-level)





Brief Syntax of Verilog

Token

Data Types

Data Types

Data Types

Data Types

System Tasks

System Tasks

Compiler Directive

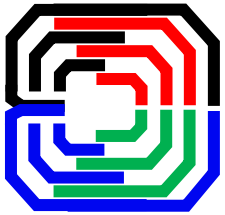
Test bench Concept

System Tasks for Simulation

Generating Stimulus - Clock

Q & A

Thank you for your attention



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