Main board – gyro boar – 4 wires:

|  |  |  |  |
| --- | --- | --- | --- |
| Red | Blue | White | Dark |
| +v | From main to gyro | From gyro to main | Gnd |

UART

Start – 0 stop – 1

mySerial.write9(sp & 0xFF); // 0110 0100\*/

mySerial.write9((sp >> 8) & 0xFF); // 0000 0000

mySerial.write9(sp & 0xFF); // 0110 0100

mySerial.write9((sp >> 8) & 0xFF); // 0000 0000

Segnals:

While(1):

{frondsidedown (255 going to 0);

frondsidedown (255 going to 0);

0000000001;

sp & 0xFF

(sp >> 8) & 0xFF

sp & 0xFF

(sp >> 8) & 0xFF

101010100;

}

Стм :

2 юсарта – по прерываниям, начинаем отправлять уходим из прерывания, заходим в прерывание когда отправилось

2 ацп – по прерываниям, считываем каждые н секунд

**Status register (USART\_SR)**

Bit 7 **TXE**: Transmit data register empty

This bit is set by hardware when the content of the TDR register has been transferred into

the shift register. An interrupt is generated if the TXEIE bit =1 in the USART\_CR1 register. It

is cleared by a write to the USART\_DR register.

0: Data is not transferred to the shift register

1: Data is transferred to the shift register)

*Note: This bit is used during single buffer transmission*

Bit 6 **TC**: Transmission complete

This bit is set by hardware if the transmission of a frame containing data is complete and if

TXE is set. An interrupt is generated if TCIE=1 in the USART\_CR1 register. It is cleared by

a software sequence (a read from the USART\_SR register followed by a write to the

USART\_DR register). The TC bit can also be cleared by writing a '0' to it. This clearing

sequence is recommended only for multibuffer communication.

0: Transmission is not complete

1: Transmission is complete