An Executable Formal Model of the VHDL in Isabelle/HOL

Wilayat Khan
COMSATS University Islamabad-Wah Campus
Pakistan
wilayat@ciitwah.edu.pk

Zhe Hou
Griffith University
Australia
z.hou@griffith.edu.au

David Sanan
Singapore Institute of Technology
Singapore
sanan.baena@gmail.com

Jamel Nebhen
Prince Sattam bin Abdulaziz University
Saudi Arabia
j.nebhen@psau.edu.sa

Yang Liu
Nanyang Technological University
Singapore
yangliu@ntu.edu.sg

Alwen Tiu
Australian National University
Australia
alwen.tiu@anu.edu.au

Abstract—In the hardware design process, hardware components are usually described in a hardware description language. Most of the hardware description languages, such as Verilog and VHDL, do not have mathematical foundation and hence are not fit for formal reasoning about the design. To enable formal reasoning in one of the most commonly used description language VHDL, we define a formal model of the VHDL language in Isabelle/HOL. Our model targets the functional part of VHDL designs used in industry, specifically the design of the LEON3 processor's integer unit. We cover a wide range of features in the VHDL language that are usually not modelled in the literature and define a novel operational semantics for it. Furthermore, our model can be exported to OCaml code for execution, turning the formal model into a VHDL simulator. We have tested our simulator against simple designs used in the literature, as well as the div32 module in the LEON3 design. The Isabelle/HOL code is publicly available: https://zhehou.github.io/apps/VHDLModel.zip

Index Terms—Formal Modelling, Verification, Isabelle/HOL, VHDL, Thoerem Proving, Hardware Description Language

I. INTRODUCTION

VHDL is one of the most widely used hardware description languages in hardware specification, verification and documentation. However, VHDL is known to have a partially blurred semantics which is defined in plain English [1], [2]. Formal verification, on the other hand, is usually performed in logic. To close this gap, a formal model for VHDL is needed to verify properties of interest for hardware designs.

As a concrete motivation, this research work is a step towards building a verified execution stack ranging from CPU, micro-kernel, libraries, to applications. We are interested in verifying correctness and security properties for those components. Since the complexity of our intended goal is high, we use a multi-layer verification approach where we would formalise each layer separately and would use a refinement-based approach to show that important properties proved at the top level (applications) are preserved to the bottom level (CPU). We choose to formalise the XtratuM [3] micro-kernel that runs on top of a multi-core LEON3 processor [4], which

is designed in VHDL. A formal model for VHDL is thus vital for the low-level verification in a verified execution stack.

We build our formal model in theorem prover Isabelle/HOL in three layers. In the bottom layer, the syntax in our model is influenced by the model of Umamageswaran et al. [5], except that 1) we focus on a synthesisable subset of VHDL while they model a timed language for simulation; and that 2) we model sub-program calls, which are not treated by Umamageswaran et al. We identify key concepts in the VHDL design of LEON3 and give a "core syntax" from which more complicated language constructs can be obtained. This is similar to the dynamic model in [5], however, they modeled VHDL in denotational semantics, whereas we give a novel operational semantics for VHDL, called "core semantics", which essentially converts VHDL statements to Isabelle/HOL functions. This idea is similar to the ACL2 model for VHDL [6], but we model many features that are missing in their work, such as sensitivity list for processes, loops, etc. To support hierarchical designs and compositional verification, the next layer extends the core with the syntax and semantics for *components* [7]. The top layer further extends the model with the necessary VHDL features used in the LEON3 design and translates the more complex syntax to the core syntax. As everything is modelled in Isabelle/HOL, we do not rely on external tools to perform heavy translation tasks, only a simple, mostly syntactical conversion from VHDL to Isabelle/HOL is required, which is much easier to handle.

This work is a part of a research project called Securify, which aims to verify an execution stack ranging from CPU, micro-kernel, libraries to applications. The project adopts a multi-layer verification approach where we formalise each layer separately and use a refinement-based approach to show that properties proved at the top level are preserved at the lower levels. This work closely connects with the other components of the project such as the formal modelling and verification of verilog [8] and the SPARCv8 instruction set architecture for the LEON3 processor [9], [10], a verification framework for concurrent C-like programs [11], and automated reasoning

techniques for separation logic [12]–[14]. For easy integration, these related sub-projects partly determine our software choices such as Isabelle/HOL and hardware choices such as LEON3 and VHDL.

The rest of the paper is organized as follows. In the next section, the core syntax of our language is defined. The core semantics of the language is defined in the Section IV. To simulate designs, a formal semantics is defined for it in Section V. Different components of the architecture are formalized in Section VI. The complex syntax of the language is given in the Section VII. A detailed experimental analysis is carried out in Section VIII. A literature survey is included in the related work Section II and the paper is concluded in the Section IX.

II. RELATED WORK

There are a number of papers on formalising hardware description languages in theorem prover. Braibant et al. [15] defined a simplified version of the language Bluespec in theorem prover Coq. Their simplified version of Bluespec, called Fe-Si, is deeply embedded language. In a recent effort, we defined a domain-specific language dubbed as VeriFormal [16]. The language VeriFormal is a formal version of Verilog, which is deeply embedded in Isabelle/HOL. It is available with a translator that translates Verilog designs into the syntax of VeriFormal. As the syntax of this language has been defined in a functional style, an automatically extracted version is executable, hence servers as the simulator with formal foundation.

Similarly, there are formalized versions of the VHDL, however, some are less relevant as they focus on timed VHDL models (e.g., [17]) or they focus on the theory behind formal semantics rather than the mechanisation of it, whereas we are mainly interested in formalising the functional part of the LEON3 design in a theorem prover. We focus on a synthesisable subset of VHDL which does not involve statements such as wait and delayed assignment. Eisenbiegler et al. gave a formal model for a synchronous VHDL subset called $\mathcal{ABC}$-VHDL [18], which divides VHDL statements in three types: $\mathcal{A}$ statements, including null, variable assignment, and signal assignment, never reach a wait statement during execution; $\mathcal{B}$ statements sometimes reach a wait; while $\mathcal{C}$ statements, namely wait statements, always reach a wait. The authors modelled VHDL statements as functions that describe the transition from one clock tick to the next, they also implemented a translation from their model to HOL. Goldschlag surveyed and formalised a few important VHDL concepts, including signal assignments for both timed and untimed models, delta delays, resolution functions, components, and a few extensions [19]. Breuer et al. [20] proposed a refinement calculus for VHDL, effectively reducing the verification of VHDL to a problem in temporal logic. Their model handles signal assignments, wait, null, if, while, and process statements at its core, and they gave a denotational semantics for their language. For some mechanised examples, van Tassel embedded the simulation cycle of a VHDL subset called Femto-VHDL in HOL [21]. The Femto-VHDL subset contains simplified conditional statements and signal assignments (with delay) for the sequential part, and process statements for the concurrent part. Bawa and Encrenaz gave a VHDL translation to Petri nets [22]. Their model, although does not support features such as subprogram calls and components, does include most of features surveyed in related work and has a rather strong tool support. Ralf Reetz's deep embedding of VHDL into HOL [2] covers a significant subset of VHDL and includes the elaboration and execution processes. Kloos and Breuer's book gives an excellent review of related work in that era [23].

Two other VHDL models are worth mentioning: Umamageswaran et al.'s book [5] documented their VHDL model in PVS. Their syntax covers a rich subset of VHDL, for which they gave a denotational semantics, as they mainly concern timed models. Their model is divided in two layers: a static model which covers a complicated syntax; and a dynamic model which is a much simpler subset. They gave a reduction algebra to covert a static model to a dynamic model. Their model is capable of proving some interesting properties, such as the equivalence of two VHDL designs. Another deeply developed work is the ACL2 model for VHDL [6], [7], [24]. The ACL2 model focuses on a synthesisable subset of VHDL, which is very close to our line of work. This model can handle some rather involved examples, such as modules to compute factorial and power. Furthermore, the authors also extended their work to cover components in VHDL. This is an important step, as it enables compositional verification.

The above work laid a solid foundation for the research in this area. However, this cannot be used directly in the projects like verifiable execution stack for two major reasons: First, most of the related papers were published in the 1990s and their detailed reports and source code could not be retrieved. Some authors confirmed with us that their source code was lost. Second, most of the related work uses a rather "abstract" syntax. Moreover, many models assume that the VHDL code is elaborated. This is nice when demonstrating the technique, but real industrial designs often contain many features that are not covered by those models, such as assignments with a range specification (rarely supported, except by [24], [25] etc.) and "others", vector member access, records, types in the std_logic_1164 library, cases, among many others. One can argue that these features can be translated to some of the previous formal models, but it would have required to verify the translation or the elaboration process, which may not be straightforward. Therefore, while the related work focus on simplified models and elegant theories, we go on the opposite direction and model VHDL with complicated features used in industry designs.

III. CORE SYNTAX

In this section, we identify a core subset of VHDL as the base of our model. This subset can be extended with many features that are widely-used in LEON3 designs. For space reasons, the reminder of this paper only introduces our model at a high level and all the definitions are not expanded and explained.

Our core model captures the basic VHDL types (boolean, bit, char, integer, positive, natural, real, time, positive, natural, string, bitstr, boolstr) and operations over these types (logical, relational, shift, and arithmetic operations). Our language also supports other widely-used VHDL types such as `signed`, `unsigned`, `std_logic`, `std_ulogic`, `std_logic_vector` and `std_ulogic_vector`. These types are modelled by built-in Isabelle/HOL types and the operations are modelled as Isabelle/HOL functions. This is similar to the treatment in the ACL2 model [24]. We define `expression` in Figure III, where `e` is a shorthand for `expression`.

```
datatype expression =
  uexp uop e              unary expressions
 |bexpl e lop e           logical expressions
 |bexpr e rop e           relational expressions
 |bexps e sop e           shifting expressions
 |bexpa e aop e           arithmetic expressions
 |exp_sig signal          signals
 |exp_prt port            ports
 |exp_var variable        variables
 |exp_con const           constants
 |exp_nth e e             get the nth member of
                          a vector
 |exp_sl e e e            get a subvector of a vector
 |exp_tl e                convert an expression to
                          a vector
 |exp_trl e               convert an expression to
                          a reversed vector
 |exp_r rhsl              records
```
Fig. 1. Syntax of expression.

In `exp_nth`, the first expression must be of a vector type and the second expression must have the type natural. In `exp_sl`, the first expression must be a vector, the last two must be naturals respectively indicating the index of the first element in the subvector and the length of the subvector. We introduce the last two types of expressions because VHDL overloads the vector concatenation operator and the append operator. In Isabelle/HOL, when appending a list of type `'a list` to an element of type `'a`, we explicitly convert the element to a singleton list, then concatenate it with another list. The two types of vectors are distinguished: a list is used for big endian vectors (corresponds to `to`) ; a reversely stored list is used for little endian vectors (corresponds to `downto`). The last type of expression is for record types of signals, ports and variables. We deal with record types as lists. For example, a signal record instance corresponds to a list of signals or nested signal records as its members. Members of a record can be accessed by checking their `names`, which are string identifiers. A similar treatment is implemented for variable records. Record types of signals and ports are inductively defined as follows:

```
datatype seq_stmt =
  sst_sa name sp_lhs amst_rhs        signal assignment
 |sst_va name v_lhs asmt_rhs         variable assignment
 |sst_if name condition              if statement
 "seq_stmt list" "seq_stmt list"
 |sst_l name condition               while loop
 "seq_stmt list"
 |sst_fn name v_clhs                 function call
  subprogcall
 |sst_rt name asmt_rhs               return statement
 |sst_pc name subprogcall            procedure statement
 |sst_n name name condition          next statement
 |sst_e name name condition          exit statement
 |sst_nl                             null statement
```
Fig. 2. Syntax of sequential statements.

```
datatype spl =
    spl_s signal
  | spl_p port
  | spnl "(name × (spl list))"
```

The above definition of `expression` does not include functions. Our core model treats functions as a type of statements instead and we restrict them to the form of "variable := function call". The core syntax includes the sequential statements in Figure III.

Every statement has a `name`, which is an identifier of type string. The left hand side `sp_lhs` (resp. `v_lhs`) of an assignment may be a signal/port (resp. variable) possibly with a `discrete_range`. The right hand side `asmt_rhs` is either an `expression` or of the form `others => expression`. In the if statement, the `condition` is a boolean expression, the two `seq_stmt list`s are for the "then" part and the "else" part respectively. The `seq_stmt list` in the while loop is the loop part. In function calls and procedure calls, `subprogcall` is defined as `subprogcall = "(name × (v_clhs list) × type)"`, where `name` is the string identifier for the subprogram, `v_clhs list` is the list of arguments, which can only be variables in the core model, and `type` is the return type of function calls (not used in procedure calls). Return statements are only used in functions, they simply return the `asmt_rhs` part, which is later assigned to the `v_clhs` part in the function call. In next and exit statements, the first `name` is the identifier of the statement, and the second `name` is the identifier of the loop statement to be exited.

As in most previous VHDL models, our core model only considers one type of concurrent statements: process statement. Other concurrent statements can be translated to this one, as will be shown in Section VII. Process statements are defined as below.

```
datatype conc_stmt =
  cst_ps name sensitivity_list
  "seq_stmt list"
```

Note that we support a list of signals/ports as the `sensitivity_list` in the process statement. Models without this, e.g., [6], are restricted to activate the process with a single signal/port, which may not be practical.

Finally, a VHDL file corresponds to a model of type `vhdl_desc`, which is a tuple of (`environment × res_fn × conc_stmt_list × subprogram list`), where `environment` is a record containing the list of signals/ports, variables, and types; `res_fn` are the resolution functions; `conc_stmt_list` is the list of concurrent statements in the code; and `subprogram list` is the list of subprograms (functions and procedures) in the design.

IV. CORE SEMANTICS

After the core syntax of the language is defined, the core semantics is created to interpret expressions written following the syntax of the language. A `vhdl_state` is a record consisting of the following fields (we omit the types below):

`state_sp`	current value for signals/ports
`state_var`	current value for variables
`state_eff_val`	effective values for signals/ports
`state_dr_val`	driving values for signals/ports
`next_flag`	flag for the nearest next statement
`exit_flag`	flag for the nearest exit statement

This definition is inspired by the dynamic model in [5]. We distinguish the current value, effective value, and driving value of signals/ports. In the VHDL LRM [1], the effective value is "the value obtainable by evaluating a reference to the signal within an expression". Taking a cue from [5], the effective value of a signal/port is computed using the driving values contributed by every process statement that drives the signal. The driving value of a signal is defined as "the value that the signal provides as a source of other signals" [1]. In [5], the driving value of a signal/port, contributed by every process statement that drives the signal, is computed by passing the initial value of the signal through the list of sequential statements of the process. These will be detailed in the semantics.

The operational semantics for if statements is straightforwardly modeled as conditional statements in Isabelle/HOL. While loops, however, requires some care to accommodate `next` and `exit` in loops. The `next_flag` and `exit_flag` in the state are both of type `name × bool`, the former records the identifier of the loop, the latter is set to true when a next/exit statement is executed. The execution of a loop, where `p` is the current process statement, `s` is the current sequential statement, `subps` are the subprograms in the VHDL design, and `state` is the current state, is modelled in Figure IV.

The **if** part means that there is an exit flag active for this loop, so we reset flag to false and change nothing else in the state, i.e., exit this loop. The first **else if** indicates that an exit flag is active but is not for this loop, that is, we need to exit an outer level loop. So we exit the current loop by simply

```
"exec_loop_stmt p s subps state = (
case s of (sst_l n c ssl) => (
  if snd (exit_flag state) ∧
    (fst (exit_flag state) = n)
  then state(|exit_flag := (' ' ' ',False)|)
  else if snd (exit_flag state) then state
  else if snd (next_flag state) ∧
    (fst (next_flag state) = n)
  then rec_loop p s
    (state(|next_flag := (' ' ' ',False)|))
  else if snd (next_flag state) then state
  else rec_loop p s state))"
```

Fig. 3. The definition of exec_loop_stmt.

returning `state`. The second **else if** means that a next flag is active for the current loop, so we execute the loop again from beginning by invoking the function `rec_loop`, and reset the next flag. The third **else if** says that a next flag is active, but it is for an outer level loop. So we exit the current loop without resetting the next flag. In the **else** case, we execute the current loop. The function `rec_loop` first checks the loop condition, if the condition holds, then we sequentially execute the statements in `s` of process `p`, and go back to `exec_loop_stmt`. Note that a next/exit statement not only sets the flags, but also ignores the remaining statements in the loop, and calls `exec_loop_stmt`.

As mentioned earlier, in the core model we only support function calls of the form "v := function call". This allows us to model function calls and procedure calls in a similar way. For a function call `sst_fn n v spc`, where `n` is the name, `v` is the variable on the left hand side of the assignment, and `spc` is the function call, we first match `n` with the names of subprograms in `vhdl_desc`, and find the function to be called. Since all variables are globally visible in our model, we can pass arguments and return values via variable assignments. For example, for a function `f(x;y)`, which is called by `f(i,j)` with arguments `i,j`, we create assignments `x := i; y := j` and execute them before executing the function. We then execute the body of the function and obtain an expression `e` from the return statement. Lastly, we create an assignment `v := e`, which will be executed after the function execution is finished. Although rarely used in the LEON3 design, it is possible to define recursive functions, in which case function arguments (`i,j` in the above example) will be overwritten in nested function executions in our model. To solve this, we execute the function body by passing a copy of the current state as a parameter, thus we can retrieve the values of function local variables from the original copy of the current state.

In case of procedure calls, where there are no return values, we create a variable assignment for each `out` direction parameter and execute these assignments after the procedure execution is finished. For a procedure `p(x : in; y : out; z : out)` (we omit types here), which is called by `p(i,j,k)`, we execute an assignment `x := i` before

executing the procedure, and execute assignments `j := y;` `k := z` after executing the procedure.

Compared to the operational semantics for programming languages, a major difference in an operational semantics for VHDL is in the signal assignment statement, in which we assign the right hand side to the driving value of the signal. The field `state_dr_val` in a state has the type `sigprt =>` `conc_stmt => val option`, where `sigprt` is either a signal or a port, `conc_stmt` corresponds to a process, which is the only type of concurrent statement in the core model, and `val option` is either `Some` value or `None`. That is, each driving value of a signal is tied to a process that drives it. Due to the already rather involved syntax, the semantics for signal assignments considers a number of cases.

- Assignments for signals and ports of a record type are translated to assignments for each member in the record.
- If the left hand side is a signal/port `sp` which may or may not be a vector, and it does not specify a range, we consider the following cases:
  - If the right hand side is an expression `e`, we first evaluate the expression using a function `state_val_exp_t`, and then assign the value as the driving value of the signal/port for the current process. This is realised as follows:
    ```
    state(|state_dr_val :=
      (state_dr_val state)
      (sp := ((state_dr_val state) sp)
      (p := state_val_exp_t e state))|)
    ```
  - If the right hand side has the form `others =>` `e`, then we need to make a list (using the function `mk_list`) where each member is the value of `e`, and assign this list as the driving value of the left hand side for the current process. In this case, we replace the last line of the above case with below, where `vv` is the value of `e`, `length vl` is the length of the vector on the left hand side, and `val_list` is simply the constructor for vector values:
    ```
    (p := Some (val_list
      (mk_list vv (length vl)))))|)
    ```
- If the left hand side specifies a range, then the signal/port `sp` must be a vector. The sub-cases here are handled similarly as the above cases, but we need to make sure that only the elements in the range are modified, and the reminder of the vector stays unchanged.

We compute the effective value of a signal/port based on its driving values. This is implemented in Figure 4, where `sp` is a signal/port and `desc` is the VHDL model.

If a signal/port has no drivers, then its value is always the initial value, which must be its current value. If it has exactly one driver, then the effective value is the driving value. Otherwise, we resolve the driving values using a resolution function `rf`. Unresolved signals/ports have the value `None`.

Variable assignments are similar to signal/port assignments, except that variables do not have driving values and effective values, we only record the current value of variables.

```
let drivers = get_drivers sp desc state in
if drivers = [] then
  (state_sp state) sp
else if List.length drivers = 1 then
  Some (hd drivers)
else
  case (fst (snd desc)) sp of Some rf =>
    Some (rf drivers)|None => None
```

Fig. 4. The algorithm to obtain effective value from driving value.

V. SEMANTICS FOR SIMULATION

In a simulation cycle, we execute all active processes in a sequential order. This order should have no effect on the outcome. A process is active if there is a signal/port in its sensitivity list that has been changed since the last execution, i.e., its current value differs from its effective value. We then compute new effective values and check active signals after this round of computation. The function `update_sigprt` copies the effective values of signals/ports to their current values. After a round of execution, if a process's sensitivity list has an active signal/port, this process is then resumed and executed again. The cycle ends when all the processes' sensitivity lists do not have any active signals/ports. This is realised below, where `sps` is a list of active signals/ports.

```
function resume_processes where
"resume_processes desc sps state = (
  let state1 =
    exec_proc_all (snd (snd desc))
            sps state;
    state2 = comp_eff_val
    (env_sp (fst desc)) desc state1;
    act_sp1 = active_sigprts desc state2;
    state3 = update_sigprt
    (env_sp (fst desc)) desc state2 in
  if has_active_processes desc act_sp1 then
    resume_processes desc act_sp1 state3
  else state3)"
```

Executing a simulation cycle consists of checking the active signals/ports in each process, and executing a process if it has active signals/ports. This is modeled as follows:

```
definition exec_sim_cyc where
"exec_sim_cyc desc state ≡
  let act_sp = active_sigprts desc state in
  if has_active_process desc act_sp then
    resume_processes desc act_sp state
  else state"
```

The semantics for simulation is a straightforward recursive function:

```
fun simulation where
"simulation 0 desc state = state"
|"simulation n desc state =
  simulation (n-1) desc
  (flip_clk (exec_sim_cyc desc state))"
```

Since most designs use a clock signal to synchronise certain processes, we simulate the flip of a clock by the function `flip_clk`.

Example:: The VHDL code below demonstrates the difference between VHDL semantics and common semantics for programming languages.

```
process (M, N)
begin
  M <= 1; N <= 2; X <= M + N;
  M <= 3; Y <= M + N;
end
```

Suppose the value of `M` and `N`, before the process is executed, are both 0. Since each signal/port only has one driving value from each process, the second assignment of `M` overwrites the driving value of `M` from this process. At the end of this assignment sequence, the driving values of `M,N,X,Y` are respectively 3, 2, 0, 0. Note that the old values (which are the current effective values) of `M,N` are used in the assignment of `X,Y`. The driving values only become effective after the process suspends. Then, the effective values of `M,N` have been changed from 0s to 3, 2 respectively, triggering the process to resume and execute again. After the second execution finishes, the final effective values of `M,N,X,Y` are 3, 2, 5, 5, and the process does not have any active signals, thus this simulation cycle ends with `X,Y` having the same value.

VI. COMPONENTS

Architectures with components is widely-used in industrial designs and is the key to support compositional verification. Extending the core model, a VHDL design with components, corresponds to a list of pairs `(name × vhdl_desc)`, where `name` is a string identifier and `vhdl_desc` is the model for the component. Like in the ACL2 model [7], we handle components by giving each component a state. The state for an architecture with components is defined inductively as below:

```
datatype vhdl_arch_state =
arch_state "(name × vhdl_state ×
(compo_port_map × vhdl_arch_state) list"
```

Here, each component in the architecture corresponds to a `(compo_port_map × vhdl_arch_state)` pair, the former of which is a mapping from component ports to the outer-level architecture ports, the latter is the state for the component. The simulation of an architecture with components is captured by the following functions, whose types are omitted:

```
function (sequential)
    sim_arch and sim_comps where
"sim_arch 0 descs state = state"
|"sim_arch n descs state = (
let this_desc = get_desc descs state in
case this_desc of Some d => (
  case state of arch_state s =>
    if (snd (snd s)) = [] then
      sim_arch (n-1) descs
      (arch_state ((fst s),
      (simulation 1 d (fst (snd s))),[]))
    else
      let new_cl = pass_input_all_comps
            descs state (snd (snd s));
        sim_cl = sim_comps descs new_cl;
        output_s =
          get_comp_results_state descs
          (arch_state ((fst s),
          (fst (snd s)),sim_cl));
        ns = arch_state ((fst s),
          (simulation 1 d
          (state_of_arch output_s),
          (comps_of_arch output_s)));
      in sim_arch (n-1) descs ns)
 |None => state)"
|"sim_comps descs [] = []"
|"sim_comps descs (x#xs) =
  ((fst x),(sim_arch 1
  descs (snd x)))#(sim_comps descs xs)"
```

If `(snd (snd s)) = []`, then this architecture does not have component instances, thus we only have to simulate it as in the core model for 1 cycle. Otherwise, we first pass the input from the outer architecture to each component, obtaining a new list of component states `new_cl`. Each component is then simulated for 1 cycle, yielding a new list of component states `sim_cl`. Next, the output of each component is passed to the outer architecture, giving a new state `output_s` for the outer architecture. Finally, the outer architecture is simulated for 1 cycle, giving the next state `ns`.

VII. COMPLEX SYNTAX

Most formal models for VHDL apply on elaborated code or some simplified syntax, and use external software to convert more complicated syntax to the syntax accepted by the model. However, this route may lead to a low confidence on the correctness of the formal method, because the external software may not be formalised and may contain errors. To partially-overcome this, we provide a layer to extend our model with more complicated syntax. As this layer is formalised as a part of our formal model, we can verify the correctness of the translation in the future. Having this layer also improves the extensibility of our model: we only show a few treatments here, but more can be added if one wants to adopt our model in other situations.

In addition to the core sequential statements, we further support more complicated `if` statements with optional `elsif` parts; `case` statements; and `for` loops. The new sequential statement type is called `seq_stmt_complex`. These new language constructs are defined as follows:

```
|ssc_if name condition
  "seq_stmt_complex list"
  "elseif_complex list"
  "seq_stmt_complex list"
|ssc_case name expressoin
  "when_complex list"
  "seq_stmt_complex list"
|ssc_for name expression
  discrete_range
  "seq_stmt_complex list"
```

where

```
elseif_complex = ssc_elseif condition
  "seq_stmt_complex list"
when_complex = ssc_when choices
  "seq_stmt_complex list"
```

In the extended `if` syntax, the first and last `seq_stmt_complex list` are the "if" part and "else" respectively, and the `elseif_complex list` is the "else if" part. The `case` statement matches the `expression` with the `choices` (which is a list of expressions) in the `when_complex list`, and executes the corresponding list of sequential statements when a match is found. If no matches are found, the "others" part, which is the last part of the syntax, is executed. The `for` statement executes the list of sequential statements repeatedly while incrementing the `expression` within the `discrete_range`. The translation from the above syntax to the core syntax is straightforward and is not discussed here.

We add two types of concurrent statements which are widely-used in the LEON3 design: concurrent signal assignments and generate statement. They have the following forms respectively, where `conc_stmt_complex` is the type of the new concurrent statement syntax:

```
|csc_ca name sp_clhs
  "casmt_rhs list" asmt_rhs
|csc_gen name gen_type
  "conc_stmt_complex list"
```

The left hand side `sp_clhs` of the assignment can either be a `sp_lhs` or a `spl`. The right hand side `asmt_rhs` is the same as the right hand side of sequential assignments. In the middle part, each `casmt_rhs` is of the form

```
as_when asmt_rhs condition,
```

which corresponds to "asmt_rhs **when** condition **else**" in the VHDL syntax. As in [5], a concurrent signal assignment is translated to a process with signal assignments nested in `if` statements. Consider the following concurrent signal assignment:

```
s <= x when i > 0 else
     y when j = 5 else z
```

We translate this assignment to a process statement as below, where we put signals `i`, `j` in the sensitivity list of the process:

```
thisproc: process (i,j) begin
  if (i > 0) then s <= x;
  elsif (j = 5) then s <= y;
  else s <= z;
  end if;
end process thisproc;
```

We consider two types (of `gen_type`) of generate statements: `for` generate, and `if` generate:

```
for_gen expression discrete_range
|if_gen expression
```

Unlike the usual elaboration process, we translate a generate statement to a list of process statements. For an `if` generation, we evaluate the `expression` and create a list of process statements which correspond to `conc_stmt_complex list` if the expression is evaluated to be true. The translation of `for` generations are more tricky. For example, if the expression is e and the `discrete_range` is `1 to 10`, then we need to create 10 process statements for each member of `conc_stmt_complex list`, and globally replace e with the corresponding iteration number in the process statement. For example, consider the generate statement below, where `p1`, `p2` are two process statements:

```
thisgen: for i in (0 to 9) generate begin
  p1; p2;
end generate thisgen;
```

We need to generate 10 process statements based on `p1`: `p1[0/i]`, ⋯, `p1[9/i]`, where `[y/x]` means that x is globally replaced by y. Similarly, we generate 10 process statements based on `p2`.

We also provide abbreviations for our syntax to ease the translation process. Following is a small portion of the div32 unit in the LEON3/GRLIB source code [26].

```
divcomb : process (r, rst, divi, addout)
...
begin
  ...
    case r.state is
    when "000" =>
      v.cnt := "00000";
      if (divi.start = '1') then
        v.x(64) := divi.y(32);
        v.state := "001";
      end if;
  ...
  end process;
```

In our Isabelle/HOL model, this piece of code is given in Figure VII.

```
(''divcomb'':
 PROCESS ((splist_of_spl r)@[sp_p rst]@
 (splist_of_spl divi)@[sp_s addout])
 BEGIN [
...
('''': CASE (exp_of_spl (r s.''r_state'')) IS [
 (WHEN
 [elrl [(val_c (CHR ''0'')),
 (val_c (CHR ''0'')),
 (val_c (CHR ''0''))]] => [
('''': (clhs_v (lhs_v (var_of_vl
(v v.''v_cnt''))))) :=
(rhs_e (elrl [(val_c (CHR ''0'')),
(val_c (CHR ''0'')),
(val_c (CHR ''0'')),(val_c (CHR ''0'')),
(val_c (CHR ''0''))]))),
('''': IF (bexpr (exp_of_spl
 (divi s.''divi_start'')) [=]
 (el (CHR ''1'')))
 THEN [
 ('''': (clhs_v (lhs_va (var_of_vl
 (v v.''v_x'')) ((en 64)
 DOWNTO (en 64)))) :=
 (rhs_e (exp_nth (exp_of_spl
 (divi s.''divi_y'')) (en 32)))),
 ('''': (clhs_v (lhs_v (var_of_vl
 (v v.''v_state''))))) :=
 (rhs_e (elrl [(val_c (CHR ''0'')),
 (val_c (CHR ''0'')),
 (val_c (CHR ''1''))]))))
] [] ELSE [] END IF)]),
...
] END PROCESS),
```

Fig. 5. The code of divcomb in Isabelle/HOL.

It is easy to observe the resemblance between our model and the actual VHDL code. In the above case, most of the conversion is purely syntactical, except that we use `v.x(64 downto 64)` to access the 64th element in the vector `v.x`, as opposed to the original code `v.x(64)`.

VIII. EXPERIMENT AND TESTING

We use the Isabelle/HOL code export feature to automatically extract executable OCaml code for our model. This enables us to run our model as a VHDL simulator for testing purposes.

For small scale examples, we have tested the VHDL code for the factorial function in [6]. This design consists of two processes: `mult` models a multiplier, and `doit` controls the computation. The next tested design is the power function given in [7]. Similar to the factorial design, the power function design has a process for multiplication and a process which models a finite state machine to control the computation using the multiplier process. We have also tested a variant of the power function design in [7] that contains two entities, one for computing multiplication, the other one uses the multiplication entity as a component and computes the power of its inputs.

A larger tested example is the div32 unit in the LEON3/GRLIB source code [26]. This unit implements a SPARCv8 compliant 64-bit by 32-bit division, which leaves no remainder and uses the non-restoring algorithm. The VHDL code features most of the concepts captured in our model, including (operations on) records, concurrent assignments, signal and variable assignments, vectors, arithmetic and logical operations, if and case statements, process and generate statements, etc.

The all the above tested examples, our Isabelle/HOL VHDL model successfully processes the VHDL code and generates executable code in OCaml. We have then performed extensive testing on the generated OCaml program using a large number of input parameters, including corner cases. In all the tested cases, the executable program yields correct outcome of the arithmetic functions.

IX. CONCLUSION

This paper describes a formal model of the VHDL language in Isabelle/HOL. Our model is composed of a core of the most important syntax and semantics, and various extensions of the core model that handle subprogram calls, components etc. for large and modular designs. The formalisation is coded in Isabelle/HOL, which means that this model can be used to formally prove properties (such as correctness) for VHDL designs. Our model is carefully crafted to support the code export feature of Isabelle/HOL. This leads to an executable OCaml program generated from the formal model. The program can be seen as a VHDL simulator that strictly complies with the syntax and semantics defined in the model. We have tested our model through this program by running design components of the LEON3 processor and checking results.

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