

```
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39
     □module FullAdder(
40
           input x,
41
           input y,
42
           input z,
43
           output s,
44
           output c);
45
46
           wire w1, w2, w3;
47
           HalfAdder half_adder_1(x, y, w1, w2);
48
49
           HalfAdder half_adder_2(w1, z, s, w3);
50
           or G1(c, w2, w3);
51
52
       endmodule
53
     □module Adder4BitStructural(
54
55
           input[3:0] a,
56
           input[3:0] b,
           output[3:0] s);
57
58
59
           wire[4:0] c;
60
           FullAdder full_adder_0(a[0], b[0], c_in, s[0], c[1]); FullAdder full_adder_1(a[1], b[1], c[1], s[1], c[2]); FullAdder full_adder_2(a[2], b[2], c[2], s[2], c_out); FullAdder full_adder_3(a[3], b[3], c[3], s[3], c[4]);
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63
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55
       endmodule
66
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```

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•
                                                            calculator.v
 module sevensegmentdecoder(input[3:0] x, output reg[6:0] segments);
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9
             always @(x)
                  ways @(x)
case (x)
0: segments = 7'b1000000;
1: segments = 7'b1111001;
2: segments = 7'b0100100;
3: segments = 7'b0110000;
4: segments = 7'b0011001;
5: segments = 7'b0010010;
6: segments = 7'b0100000;
7: segments = 7'b1111000;
8: segments = 7'b00000000;
9: segments = 7'b00100000;
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14
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31
                       default: segments = 7'bxxxxxxx;
                   endcase
        endmodule
        module calculator(input[3:0] a, input[3:0] b, output[6:0] |segments);
             wire[3:0] s;
             Adder4BitStructural adder(a,b,s);
             sevensegmentdecoder decoder(s, segments);
        endmodule
      □module HalfAdder(
             input x,
             input y, output s,
32
33
34
             output c);
             xor G1(s, x, y);
and G2(c, x, y);
35
36
37
        endmodule
38
39
      □module FullAdder(
40
             input x,
<
```