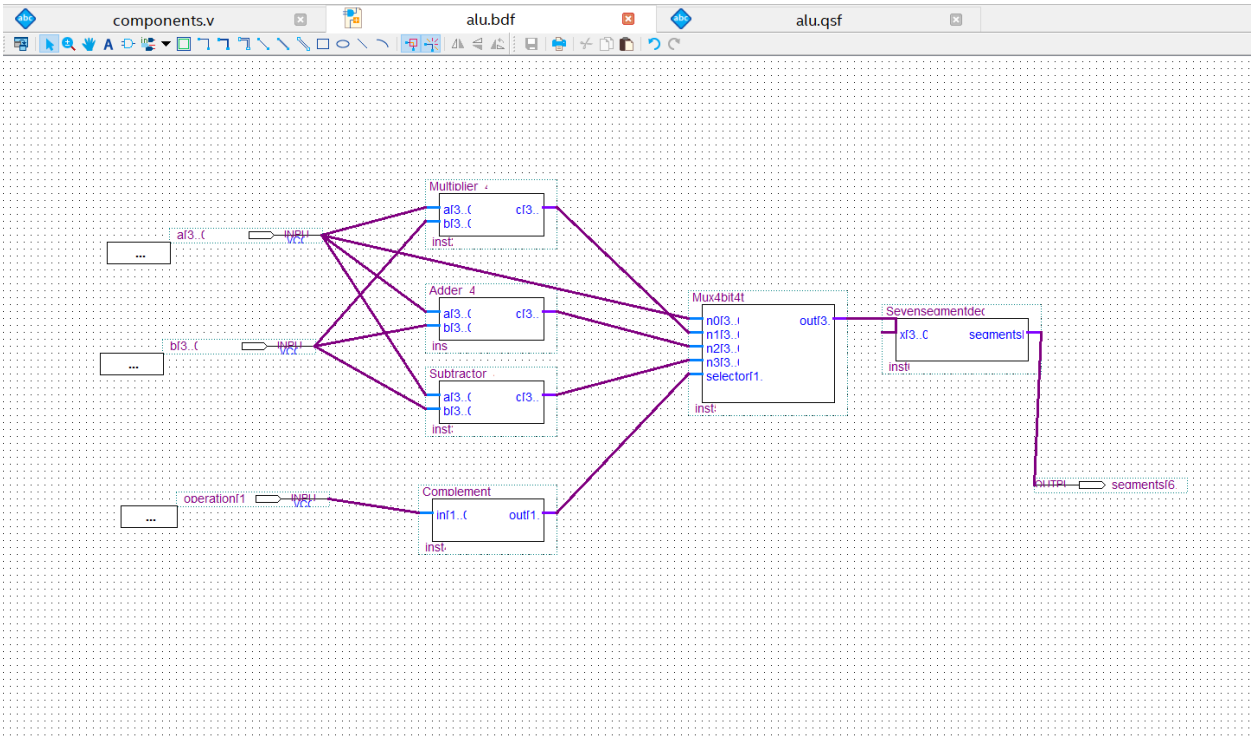

alu.qsf

```
#
# ------------------------------------------------------------------------- #


set_global_assignment -name FAMILY "Cyclone IV E"
set_global_assignment -name DEVICE EP4CE115F29C7
set_global_assignment -name TOP_LEVEL_ENTITY alu
set_global_assignment -name ORIGINAL_QUARTUS_VERSION 19.1.0
set_global_assignment -name PROJECT_CREATION_TIME_DATE "13:03:14  MARCH 17, 2022"
set_global_assignment -name LAST_QUARTUS_VERSION "19.1.0 Lite Edition"
set_global_assignment -name PROJECT_OUTPUT_DIRECTORY output_files
set_global_assignment -name ERROR_CHECK_FREQUENCY_DIVISOR 256
set_global_assignment -name VERILOG_FILE components.v
set_global_assignment -name PARTITION_NETLIST_TYPE SOURCE -section_id Top
set_global_assignment -name PARTITION_FITTER_PRESERVATION_LEVEL PLACEMENT_AND_ROUTING -section_id Top
set_global_assignment -name PARTITION_COLOR 16764057 -section_id Top
set_global_assignment -name BDF_FILE alu.bdf
set_global_assignment -name MIN_CORE_JUNCTION_TEMP 0
set_global_assignment -name MAX_CORE_JUNCTION_TEMP 85
set_location_assignment "<PIN_NAME>" -to "<signal_name>"

set_location_assignment PIN_AA23 -to a[0]
set_location_assignment PIN_AA22 -to a[1]
set_location_assignment PIN_Y24 -to a[2]
set_location_assignment PIN_Y23 -to a[3]
set_location_assignment PIN_AB28 -to b[0]
set_location_assignment PIN_AC28 -to b[1]
set_location_assignment PIN_AC27 -to b[2]
set_location_assignment PIN_AD27 -to b[3]
set_location_assignment PIN_M23 -to operation[0]
set_location_assignment PIN_M21 -to operation[1]
set_location_assignment PIN_G18 -to Sevensegmentdecoder[0]
set_location_assignment PIN_F22 -to Sevensegmentdecoder[1]
set_location_assignment PIN_E17 -to Sevensegmentdecoder[2]
set_location_assignment PIN_L26 -to Sevensegmentdecoder[3]
set_location_assignment PIN_L25 -to Sevensegmentdecoder[4]
set_location_assignment PIN_J22 -to Sevensegmentdecoder[5]
set_location_assignment PIN_H22 -to Sevensegmentdecoder[6]

set_instance_assignment -name PARTITION_HIERARCHY root_partition -to | -section_id Top
```

```
module Adder_4bit (input[3:0] a, input[3:0] b, output[3:0] c);
   assign c = a + b;

endmodule

module Subtractor_4bit (input[3:0] a, input[3:0] b, output[3:0] c);
   assign c = a - b;

endmodule

module Multiplier_4bit (input[3:0] a, input[3:0] b, output[3:0] c);
   assign c = a * b;

endmodule

module Complement_2bit (input[1:0] in, output[1:0] out);
   assign out = ~in;

endmodule

module Mux4bit4to1 (input[3:0] n0, input[3:0] n1, input[3:0] n2, input[3:0] n3, input[1:0] selector, output reg[3:0] out);
   always @ (n0, n1, n2, n3, selector)
      case (selector)
         0: out = n0;
         1: out = n1;
         2: out = n2;
         3: out = n3;
      endcase

endmodule
```

components.v

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```
1  module Sevensegmentdecoder (input[3:0] x, output reg[6:0] segments);
2     always @(x)
3        case (x)
4           0: segments = 7'b1000000;
5           1: segments = 7'b1111001;
6           2: segments = 7'b0100100;
7           3: segments = 7'b0110000;
8           4: segments = 7'b0011001;
9           5: segments = 7'b0010010;
10          6: segments = 7'b0000010;
11          7: segments = 7'b1111000;
12          8: segments = 7'b0000000;
13          9: segments = 7'b0010000;
14
15          default: segments = 7'bxxxxxxx;
16       endcase
17
18 endmodule
19
20 module Adder_4bit (input[3:0] a, input[3:0] b, output[3:0] c);
21    assign c = a + b;
22
23 endmodule
24
25 module Subtractor_4bit (input[3:0] a, input[3:0] b, output[3:0] c);
26    assign c = a - b;
27
28 endmodule
29
30 module Multiplier_4bit (input[3:0] a, input[3:0] b, output[3:0] c);
31    assign c = a * b;
32
33 endmodule
34
35 module Complement_2bit (input[1:0] in, output[1:0] out);
36    assign out = ~in;
37
38 endmodule
```