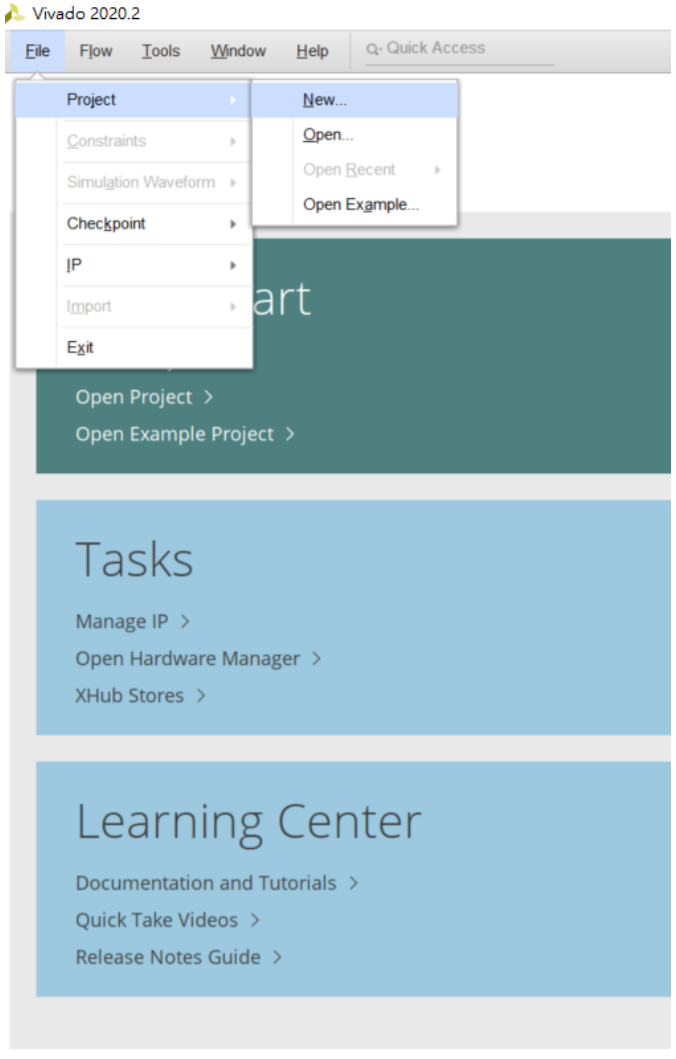
Lab0: Create a Project in Vivado and Verilog Practice

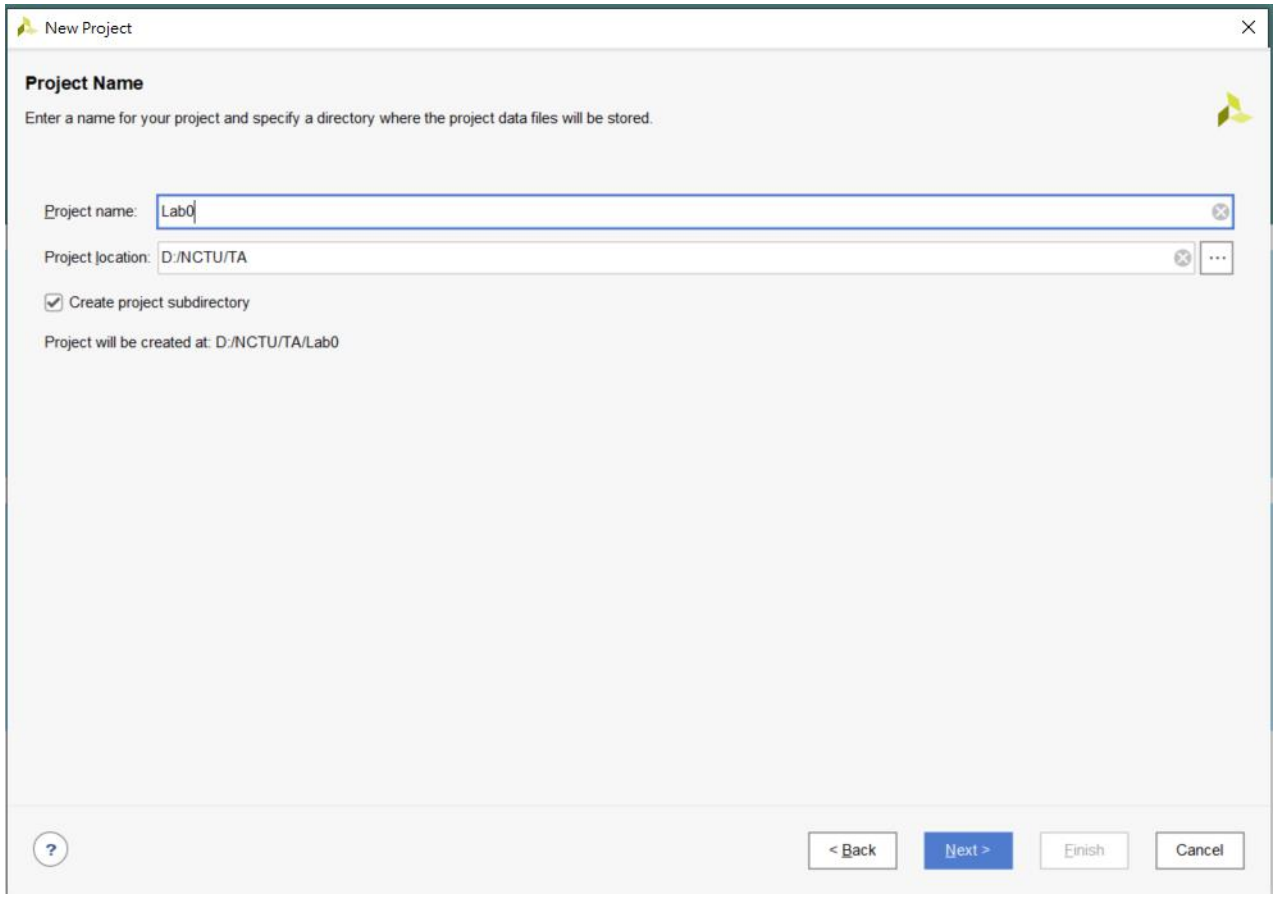
Step1

- Create a new project



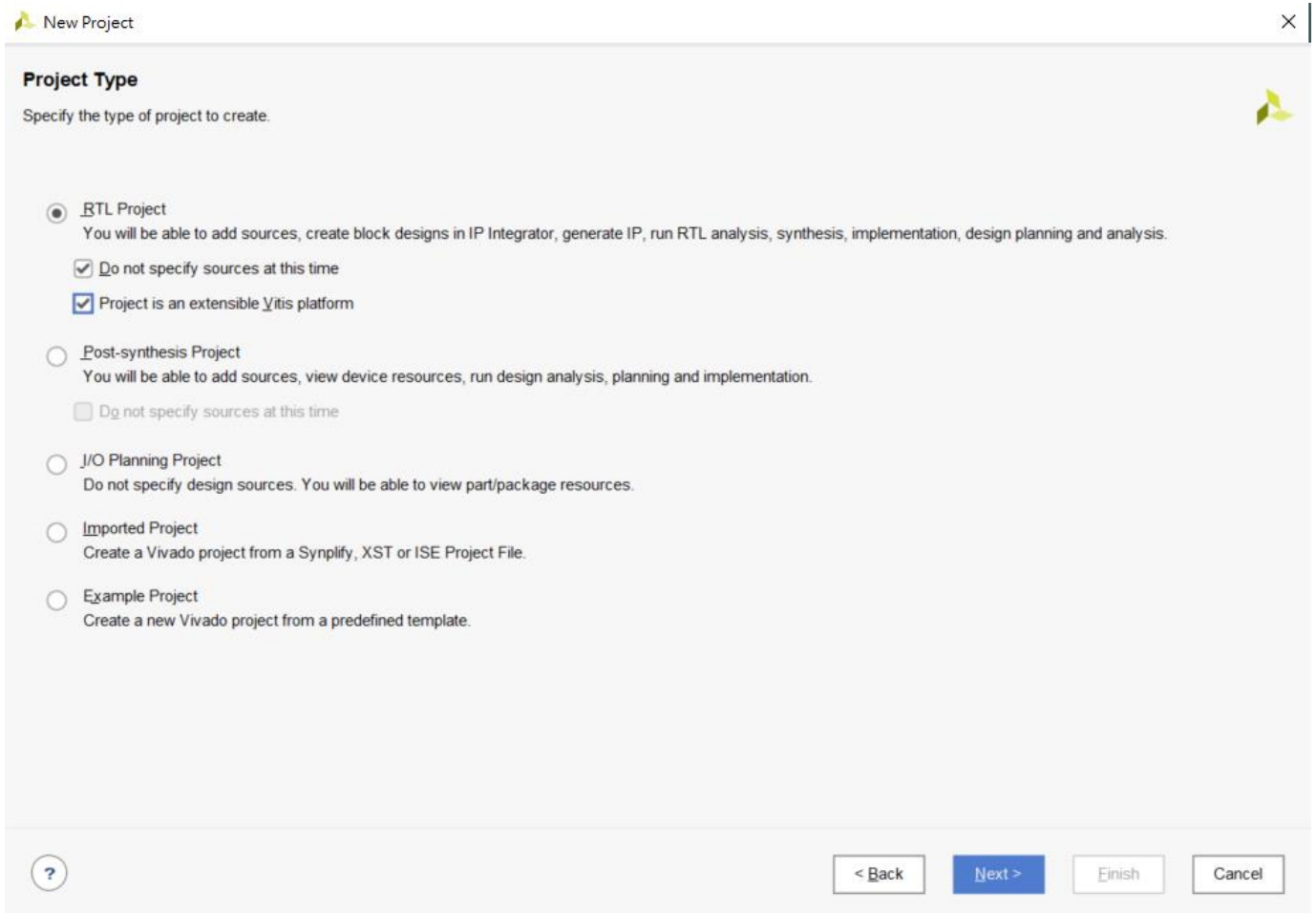
Step2

- Input project name and location



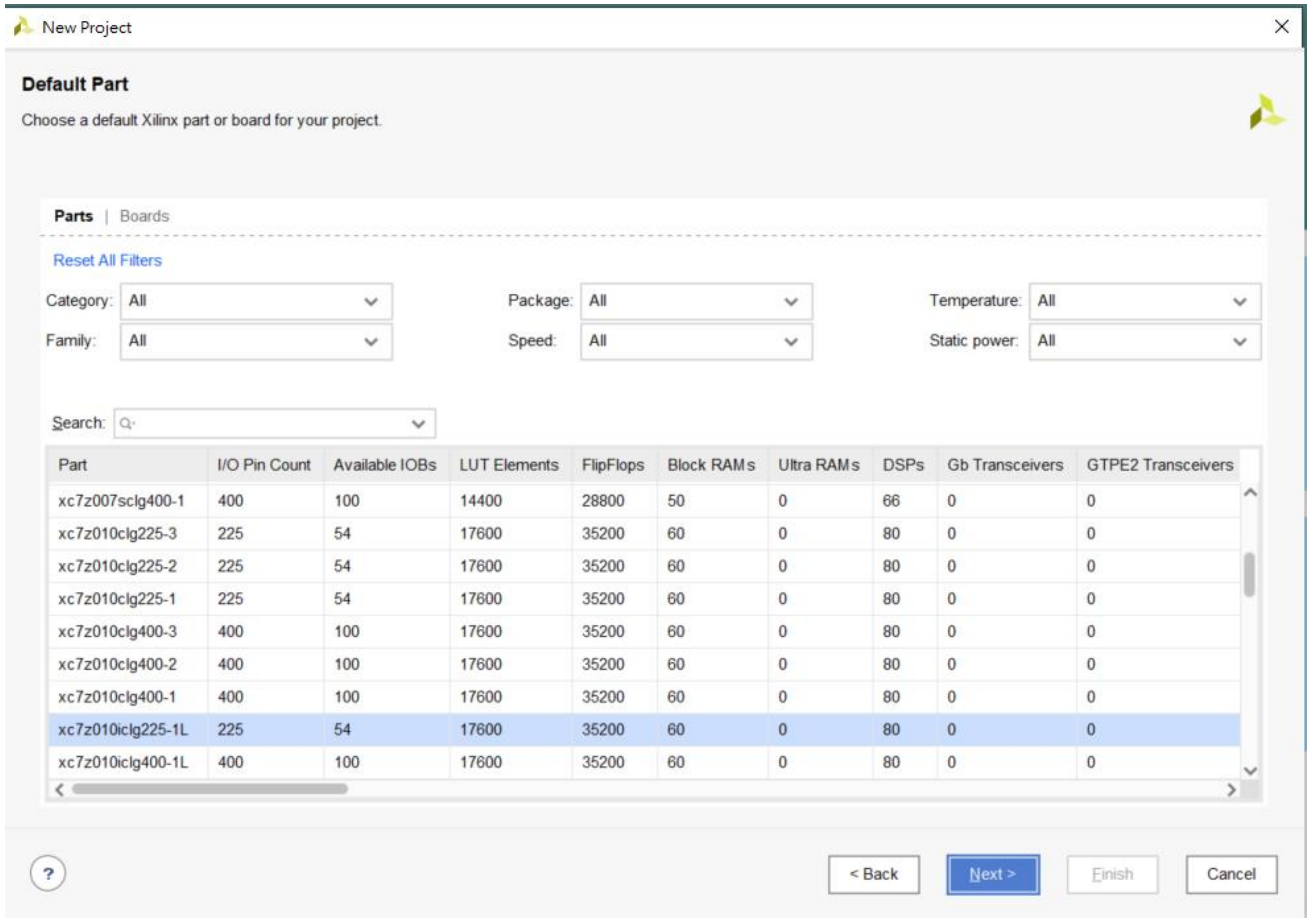
Step3

- RTL project

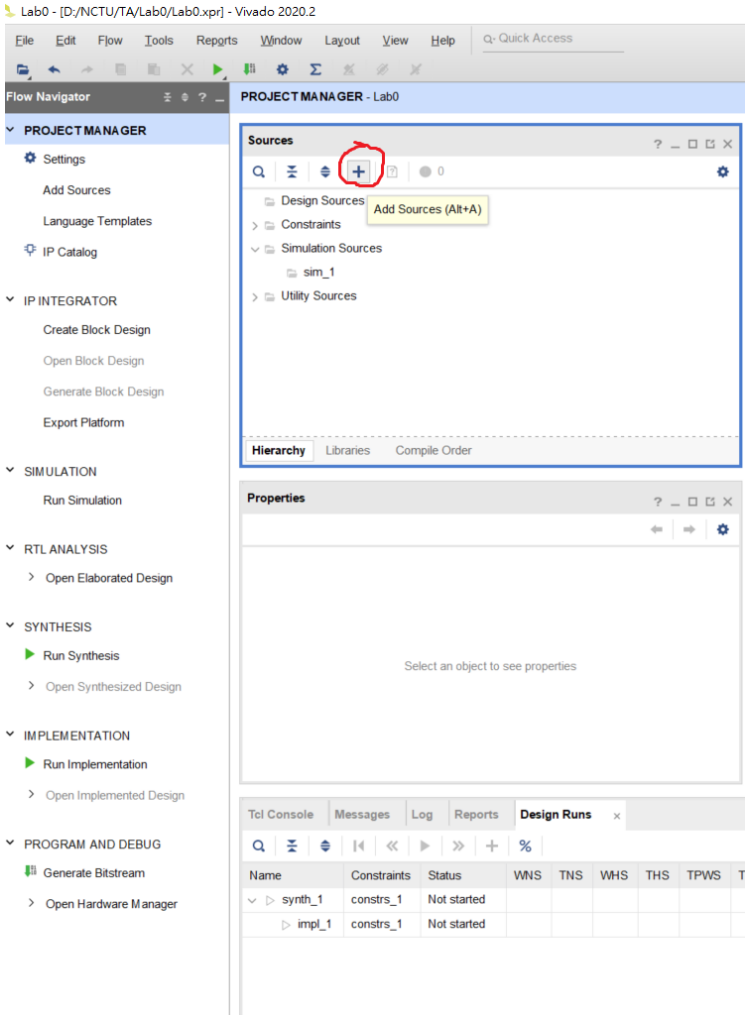


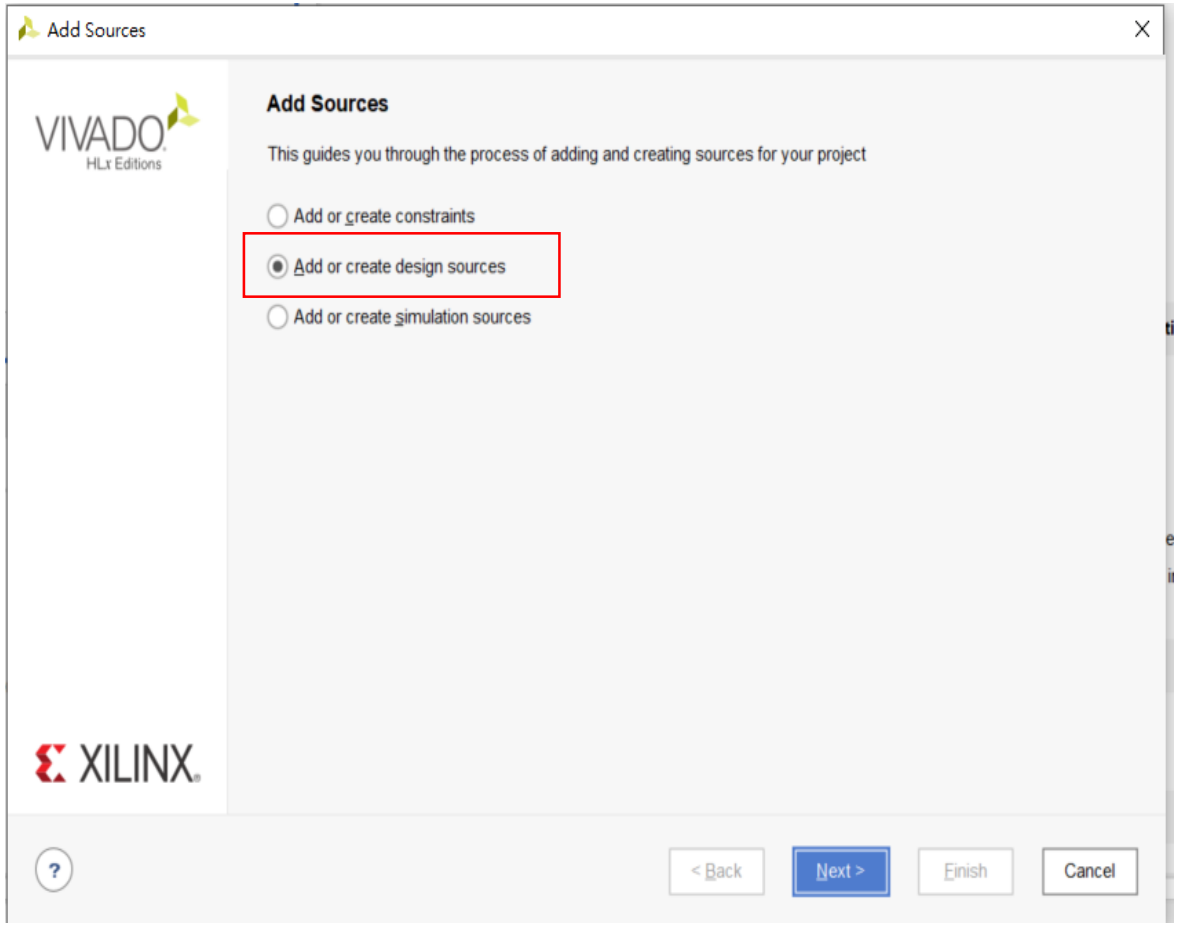
Step4

- Select parts or boards arbitrarily since we don’t need to implement the design on the FPGA.



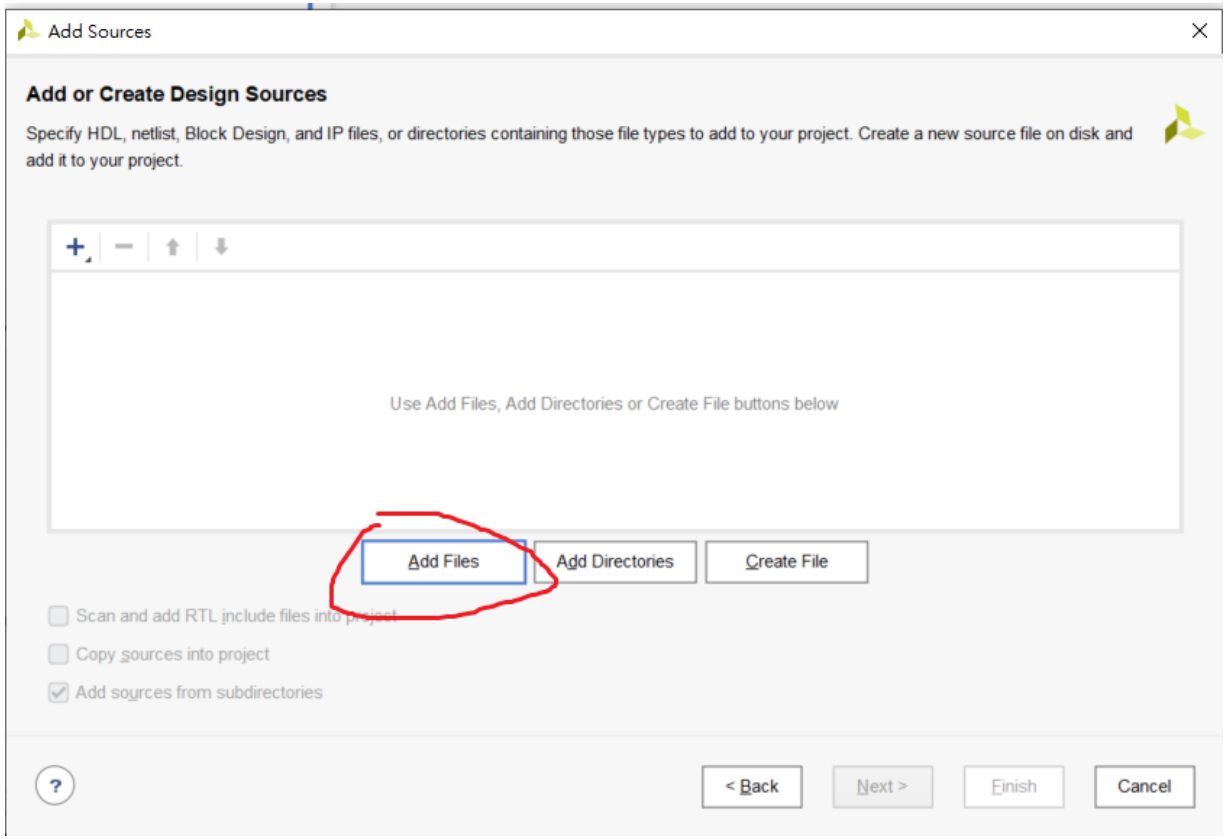
Add Source Files (.v files) Except testbench.v





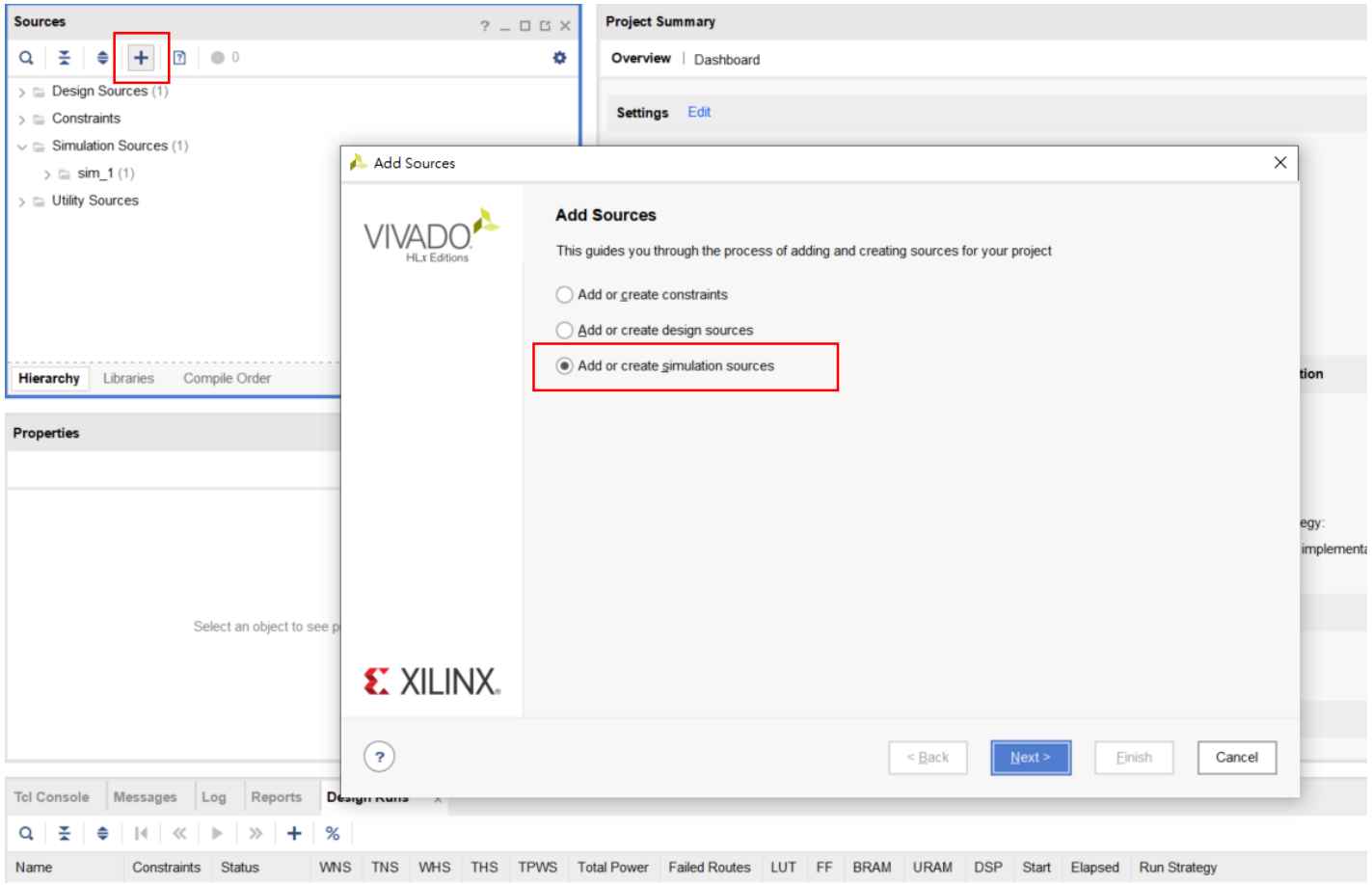
Add Source Files (.v files) Except testbench.v

- Add design sources (not including testbench.v) and finish.



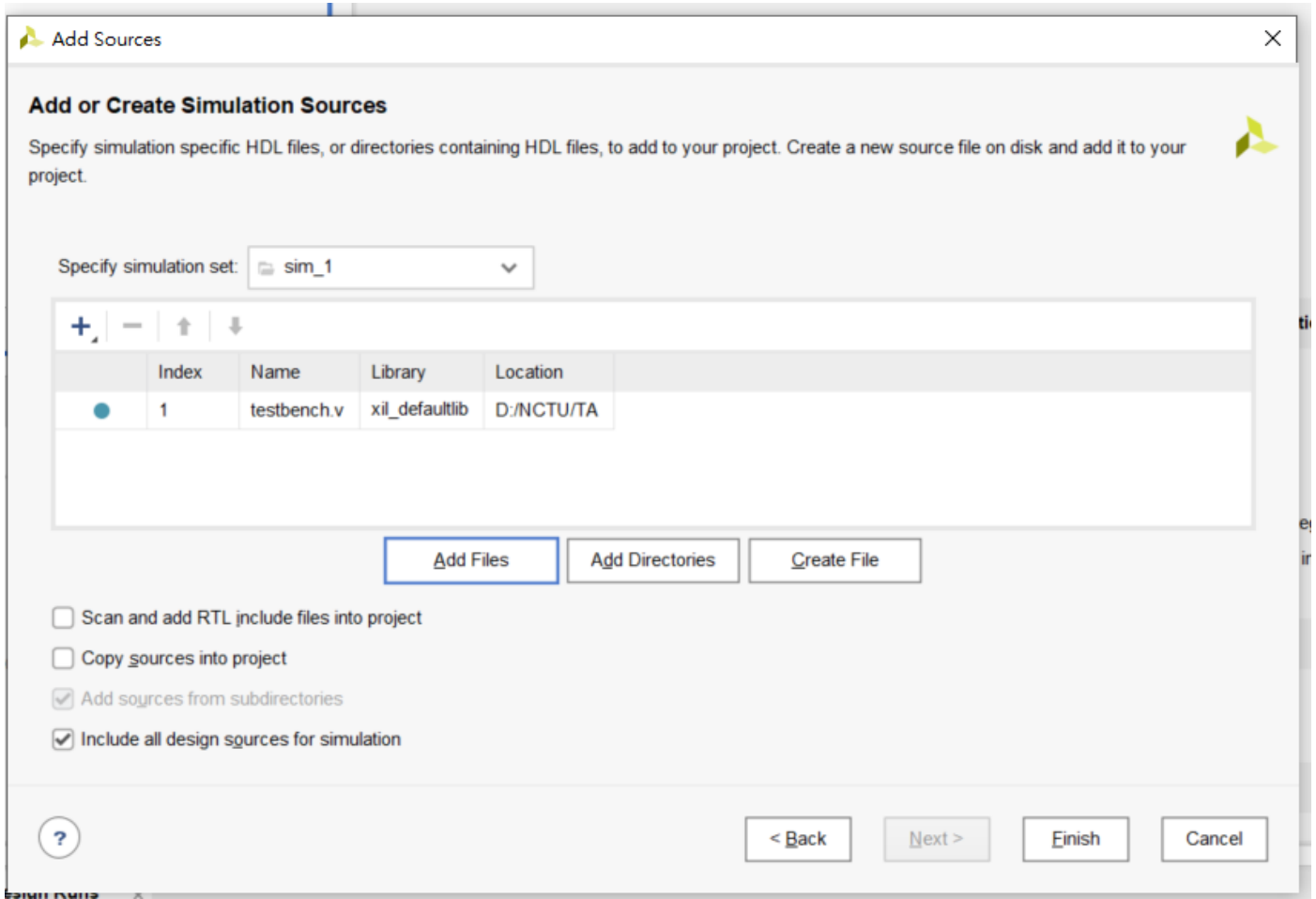
Add Simulation Sources

- Press add sources and select Add or create simulation sources



Add Simulation Sources

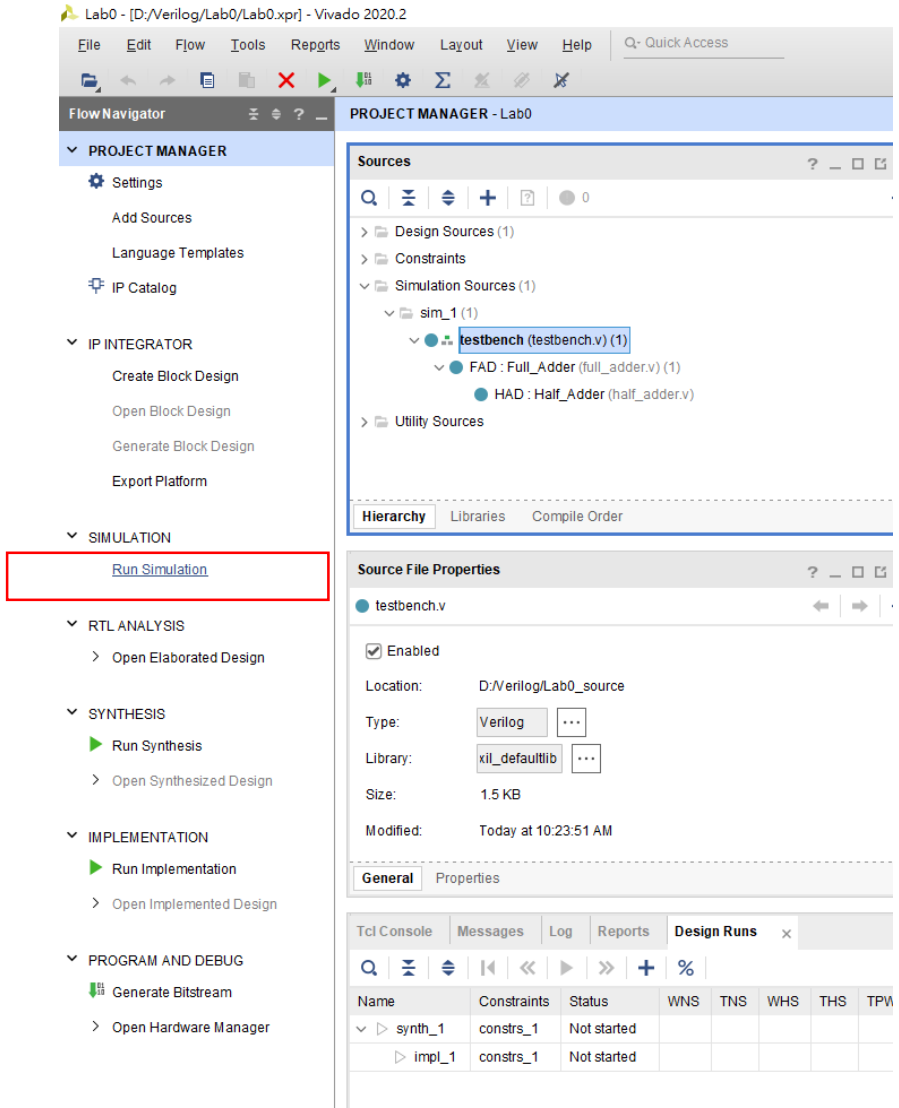
- Add testbench.v and finish

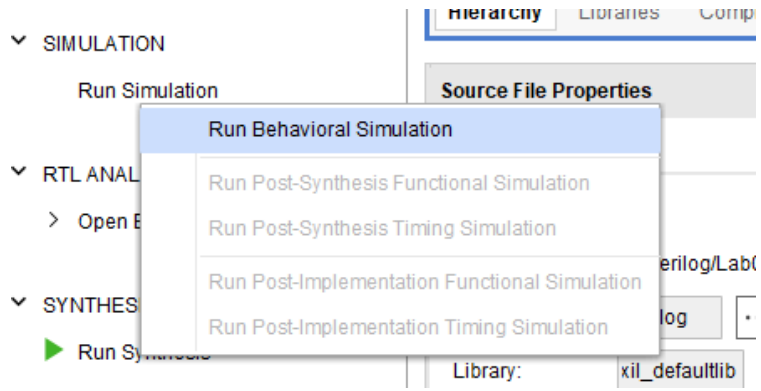


How to Run Simulation

- After adding testbench into project, you can execute the behavioral simulation. It can helps you debug with the signal waveform and check the correctness of your design.

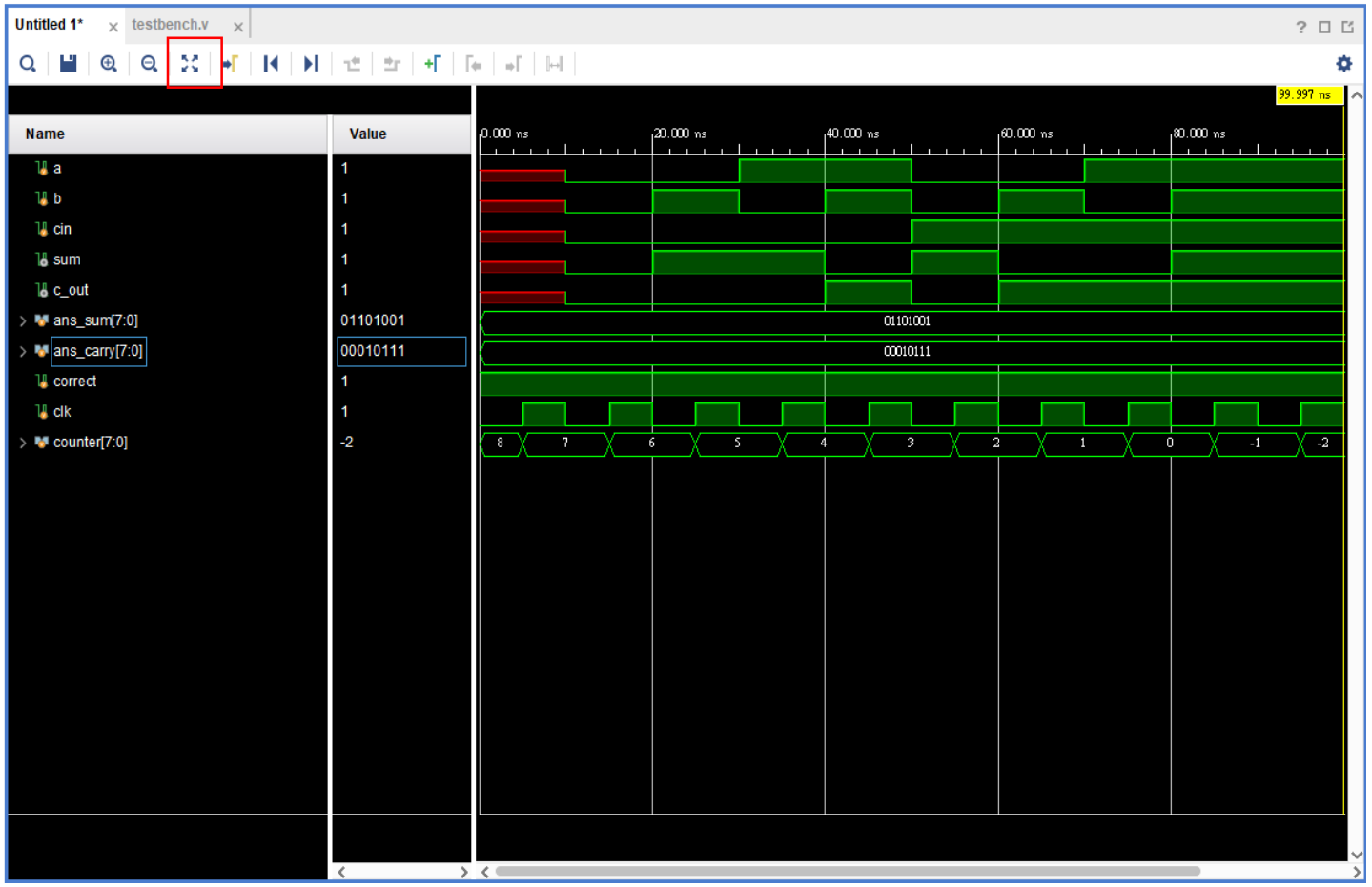
How to Run Simulation

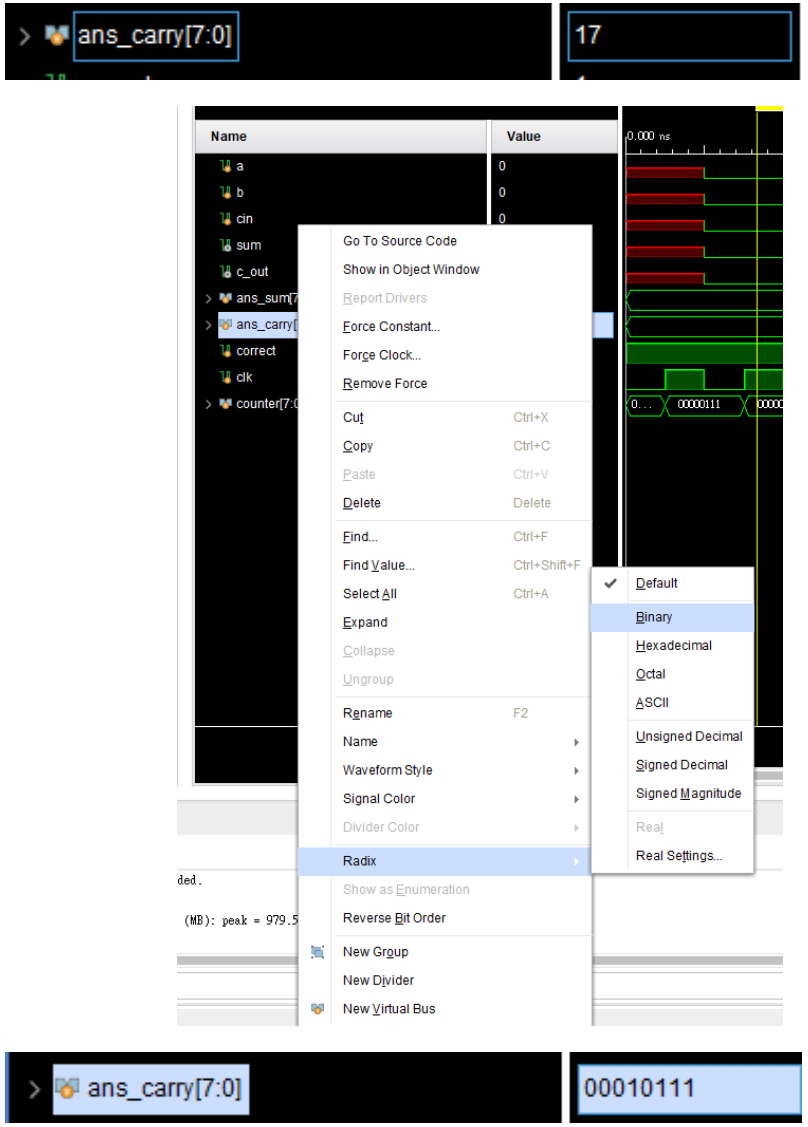




Useful Information

This bottom can make your waveform fit your screen size.



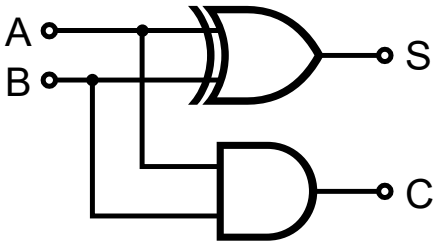


This function can help you change the radix of the signal

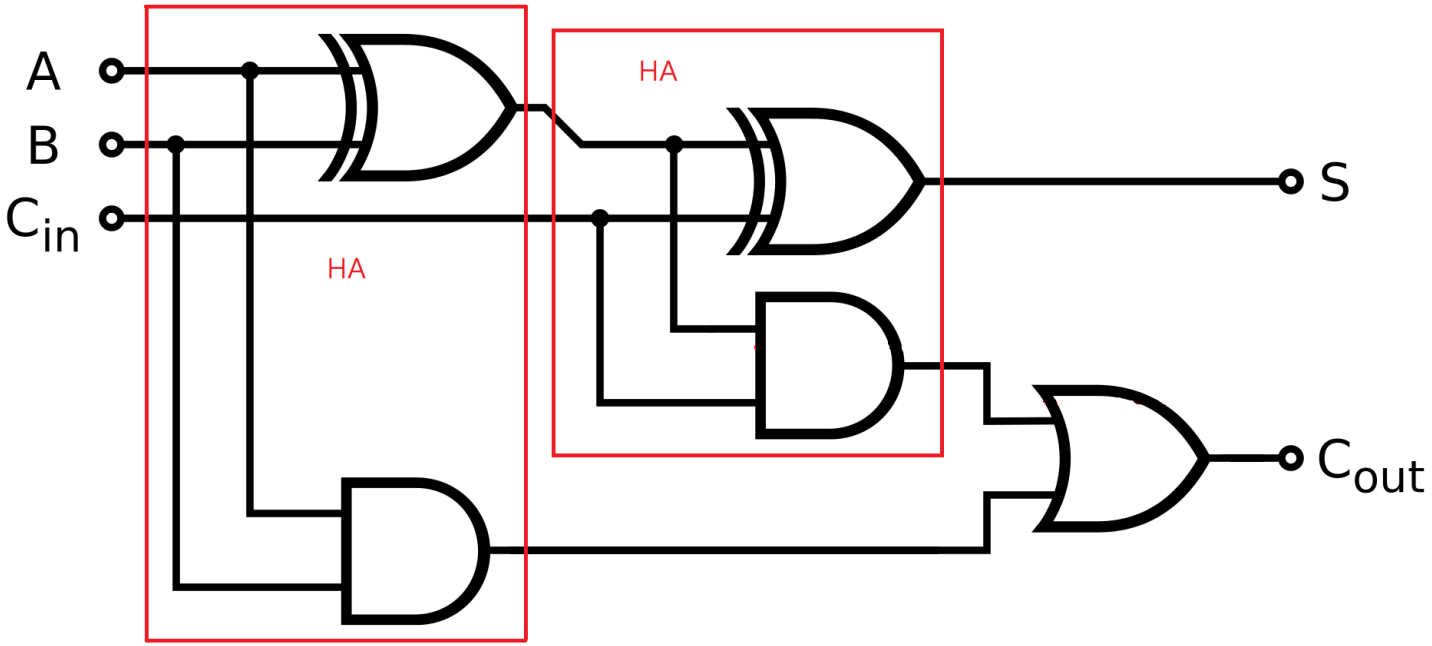
Lab0: Half Adder and Full Adder

- Implement the half adder and full adder without using ‘+’ operation.
- We want you to practice how to implement the signal connection with the given circuit. We will give you example design sources and testbench.v.

Half Adder Circuit and Full Adder Circuit



Half Adder

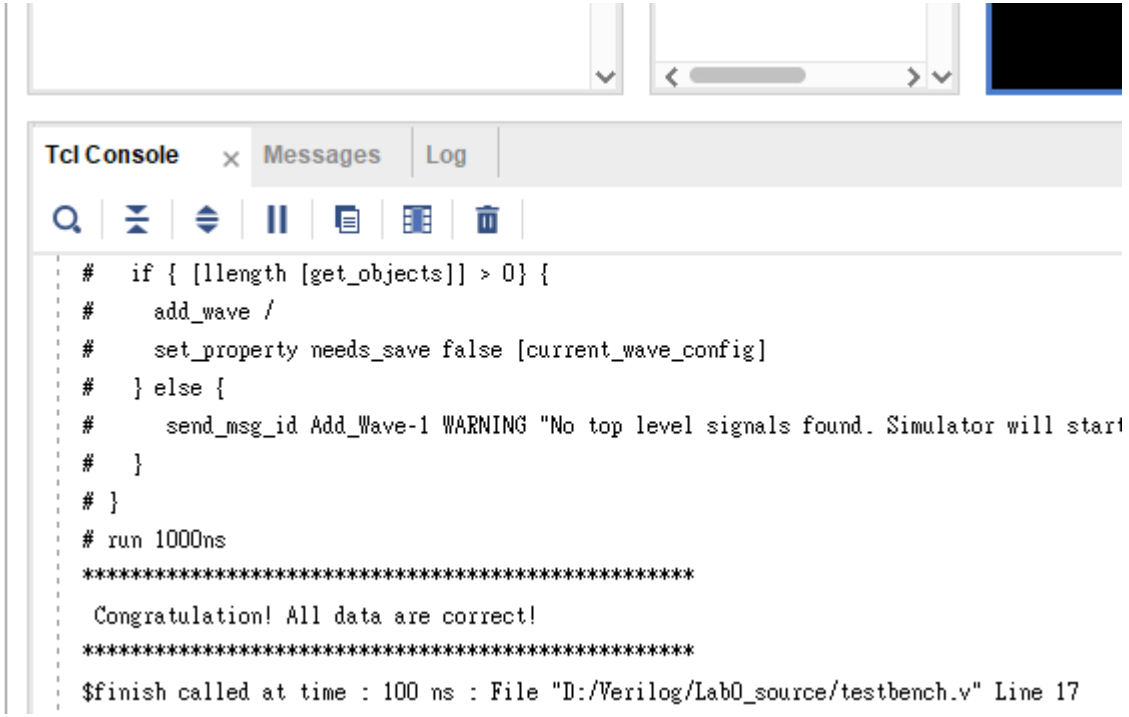


Full Adder

Source: wiki

Check Correctness

- We have enumerated all input cases in testbench.v.
- After simulation with our testbench.v, if your design is correct, you will see the message in the console.



Submission

- Due date: 2021/03/14 23:55
- Put your all design sources and testbench.v into one directory named “your_student_id” and zip the directory named “your_student_id.zip”. You only need to submit “your_student_id.zip”.
- If you have any question, feel free to ask on the Facebook discussion forum (prefer) or email to us. Thank you.