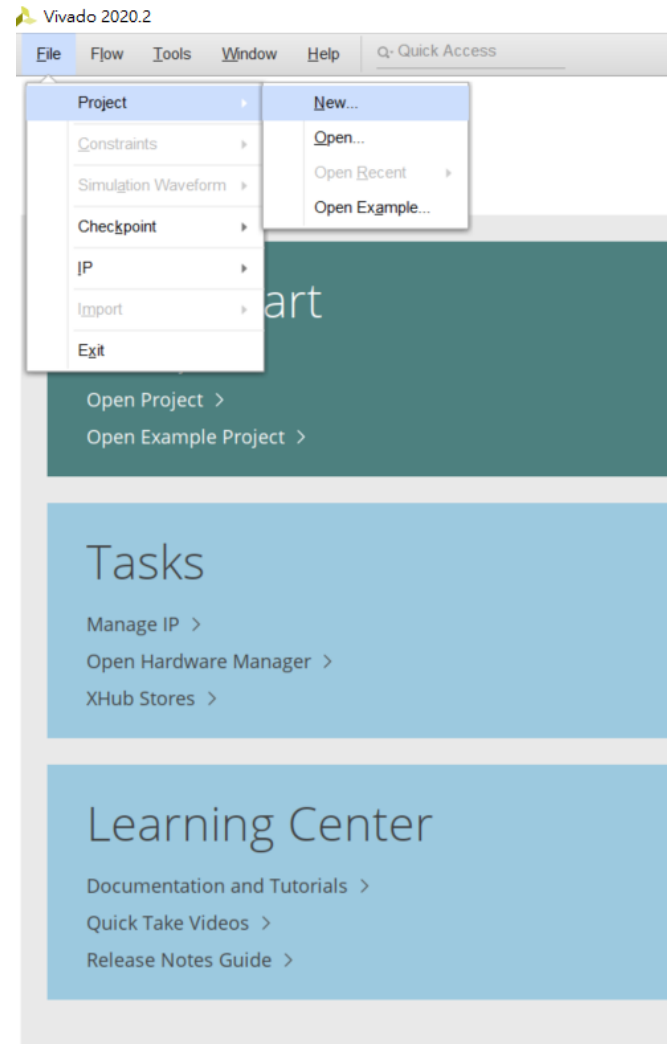


Lab0: Create a Project in Vivado and Verilog Practice

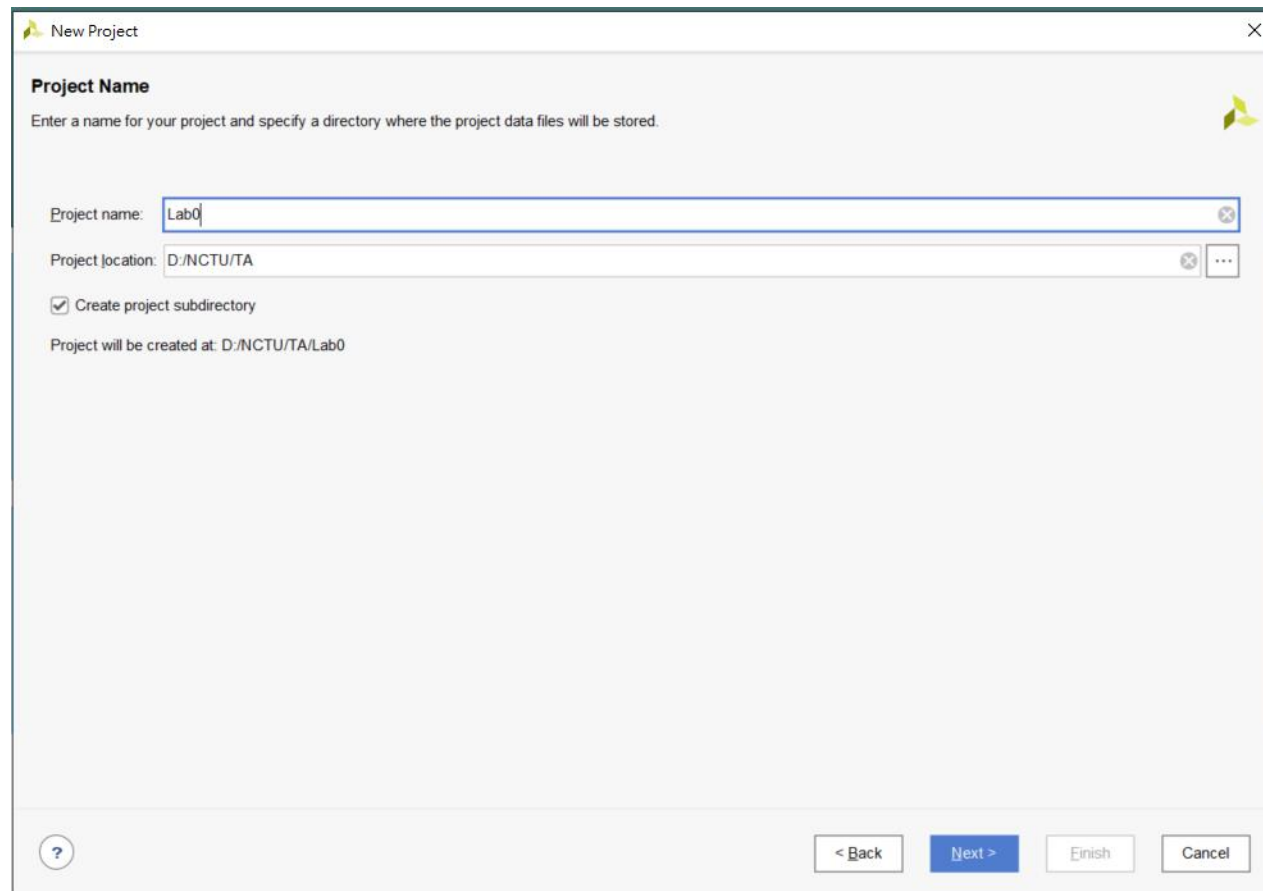
Step1

- Create a new project



Step2

- Input project name and location

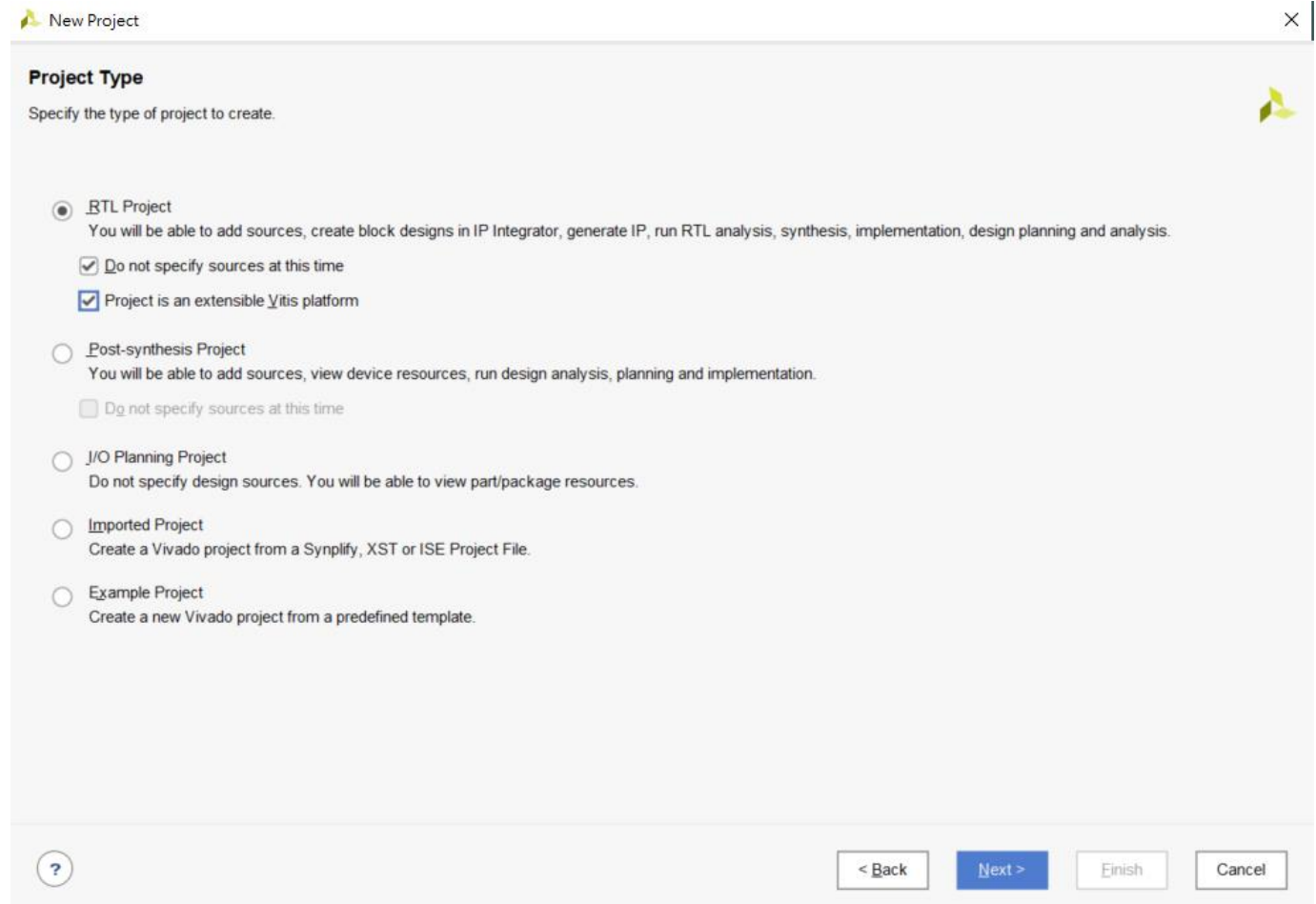


The screenshot shows a 'New Project' dialog box with the following elements:

- Title Bar:** 'New Project' with a close button (X) on the right.
- Section Header:** 'Project Name' with a small green logo icon on the right.
- Instruction:** 'Enter a name for your project and specify a directory where the project data files will be stored.'
- Project name:** A text input field containing 'Lab0'.
- Project location:** A text input field containing 'D:/NCTU/TA' with a browse button (three dots) on the right.
- Checkbox:** A checked checkbox labeled 'Create project subdirectory'.
- Summary:** 'Project will be created at: D:/NCTU/TA/Lab0'.
- Footer:** A row of buttons: a help button (question mark in a circle), '< Back', 'Next >' (highlighted in blue), 'Finish', and 'Cancel'.

Step3

- RTL project



New Project

Project Type

Specify the type of project to create.

☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
☒ Do not specify sources at this time
☒ Project is an extensible Yitis platform

☐ **Post-synthesis Project**
You will be able to add sources, view device resources, run design analysis, planning and implementation.
☐ Do not specify sources at this time

☐ **I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.

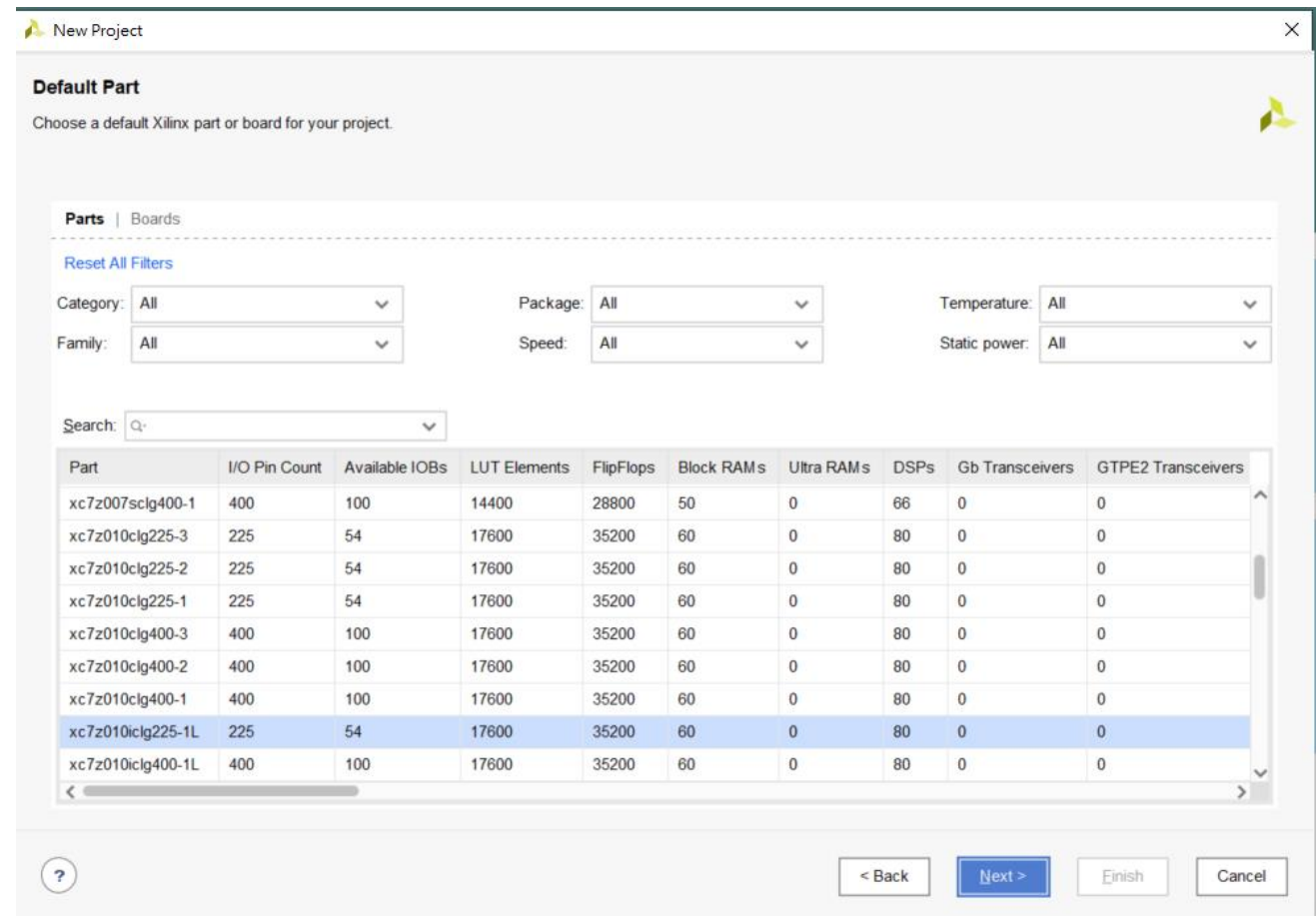
☐ **Imported Project**
Create a Vivado project from a Synplify, XST or ISE Project File.

☐ **Example Project**
Create a new Vivado project from a predefined template.

? < Back Next > Finish Cancel

Step4

- Select parts or boards arbitrarily since we don't need to implement the design on the FPGA.



New Project

Default Part
Choose a default Xilinx part or board for your project.

Parts | Boards

[Reset All Filters](#)

Category: All Package: All Temperature: All
Family: All Speed: All Static power: All

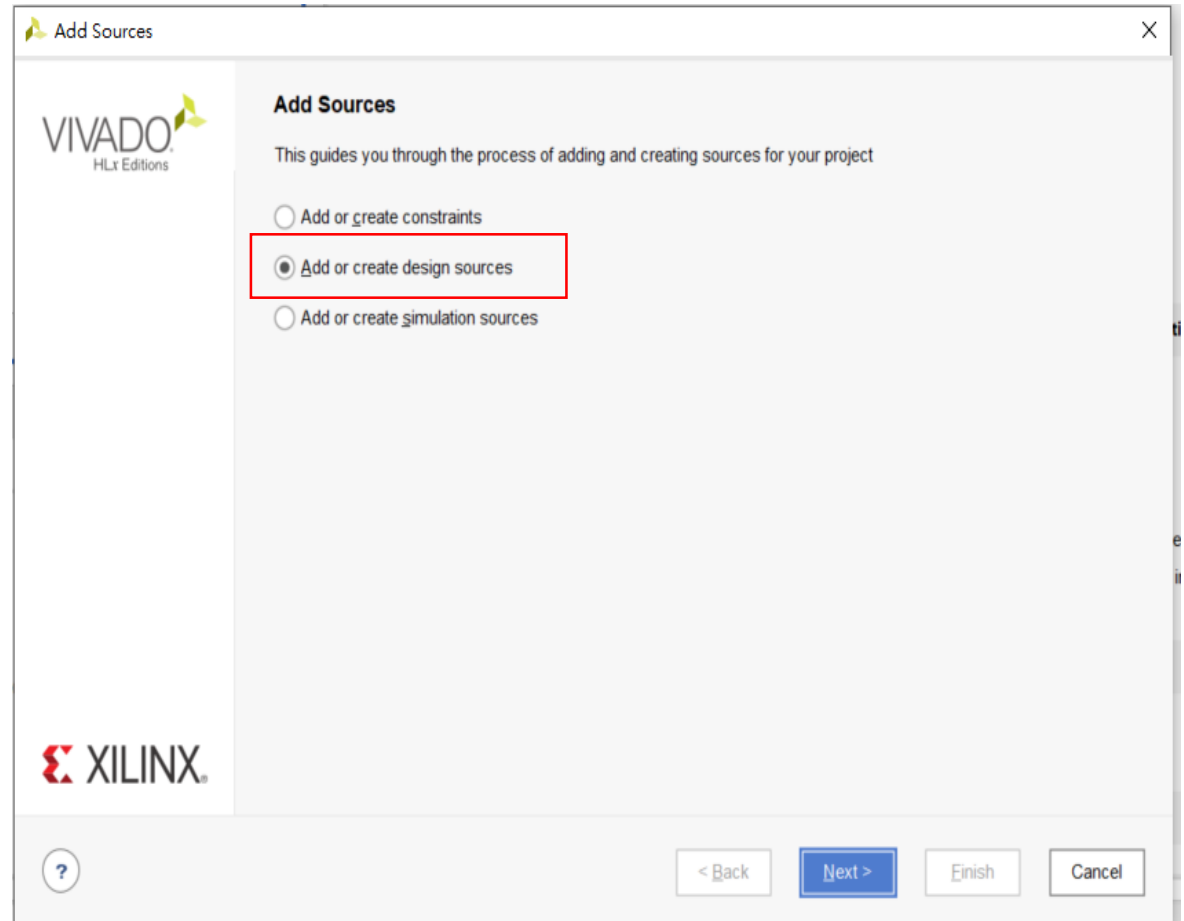
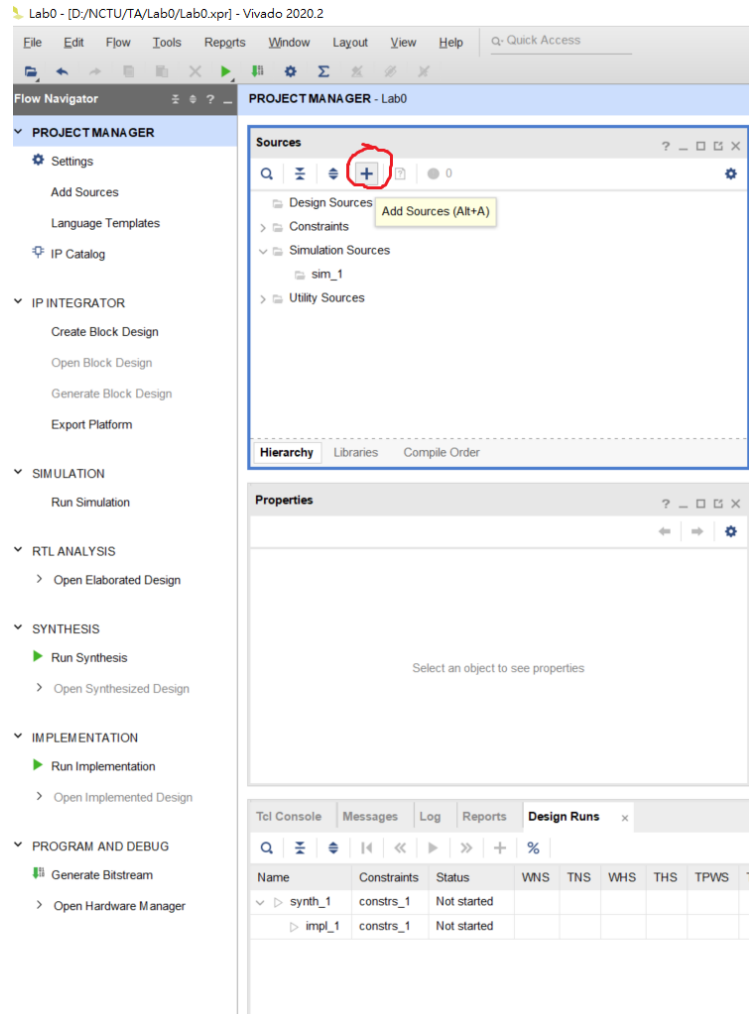
Search: Q

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAM s	Ultra RAM s	DSPs	Gb Transceivers	GTPE2 Transceivers
xc7z007sc1g400-1	400	100	14400	28800	50	0	66	0	0
xc7z010c1g225-3	225	54	17600	35200	60	0	80	0	0
xc7z010c1g225-2	225	54	17600	35200	60	0	80	0	0
xc7z010c1g225-1	225	54	17600	35200	60	0	80	0	0
xc7z010c1g400-3	400	100	17600	35200	60	0	80	0	0
xc7z010c1g400-2	400	100	17600	35200	60	0	80	0	0
xc7z010c1g400-1	400	100	17600	35200	60	0	80	0	0
xc7z010iclg225-1L	225	54	17600	35200	60	0	80	0	0
xc7z010iclg400-1L	400	100	17600	35200	60	0	80	0	0

< ? >

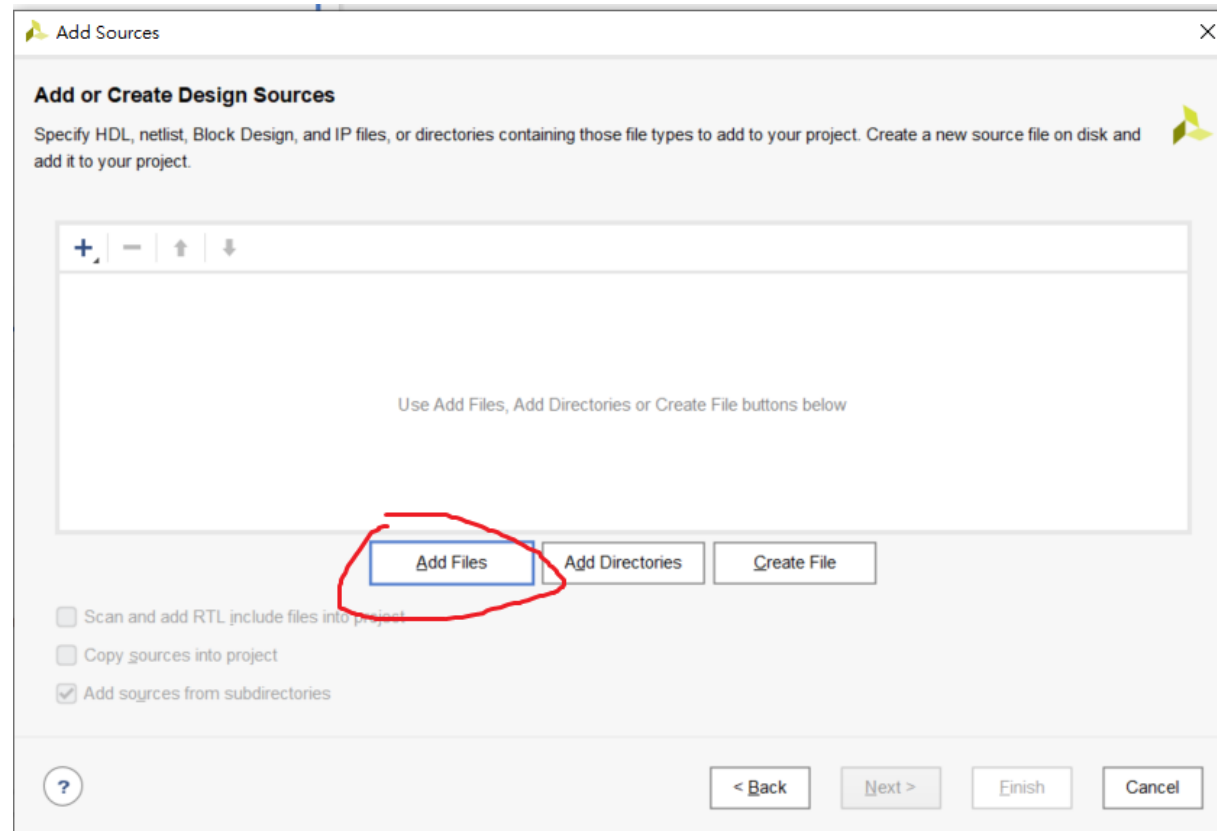
< Back Next > Finish Cancel

Add Source Files (.v files) Except testbench.v



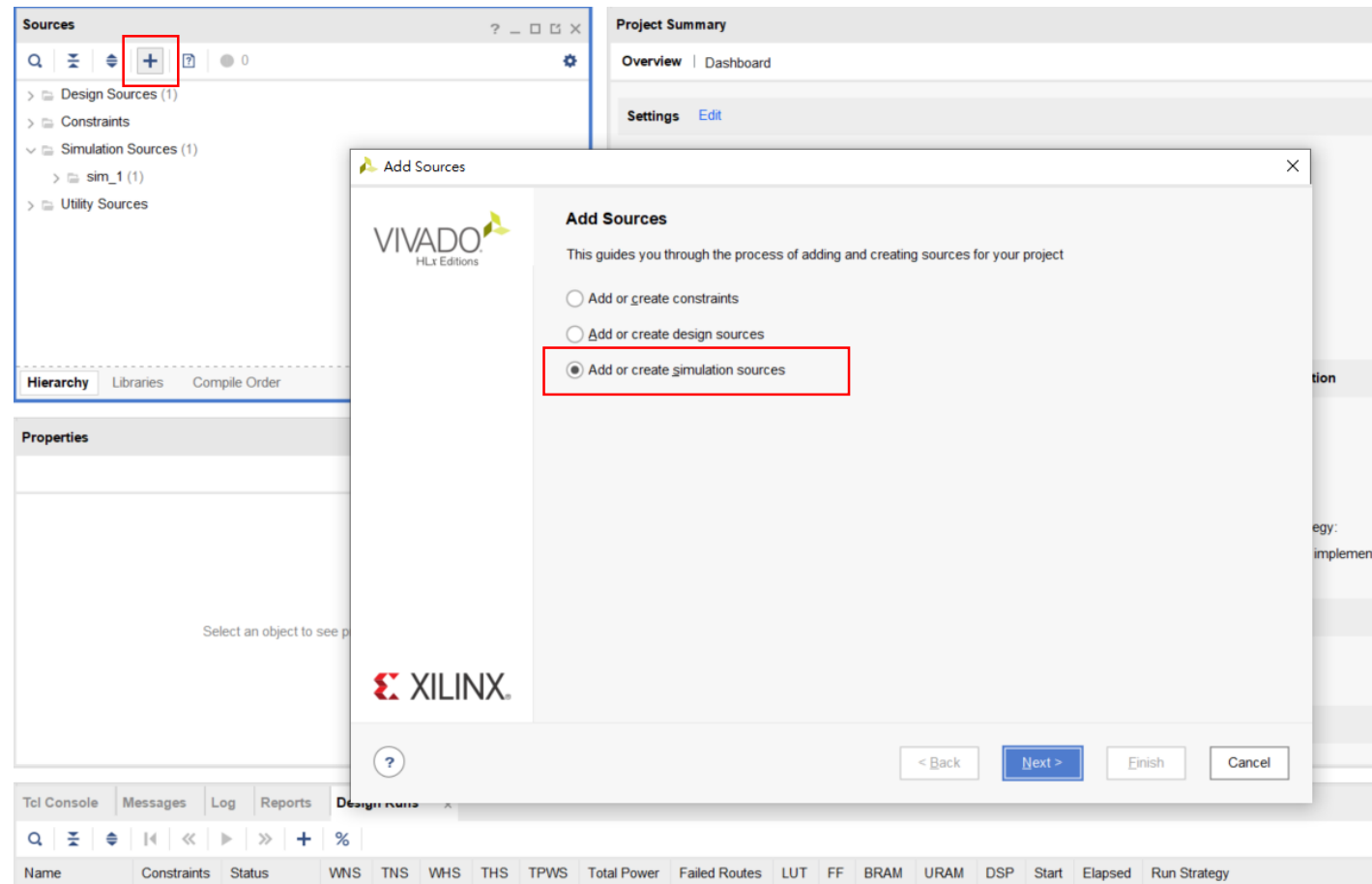
Add Source Files (.v files) Except testbench.v

- Add design sources (not including testbench.v) and finish.



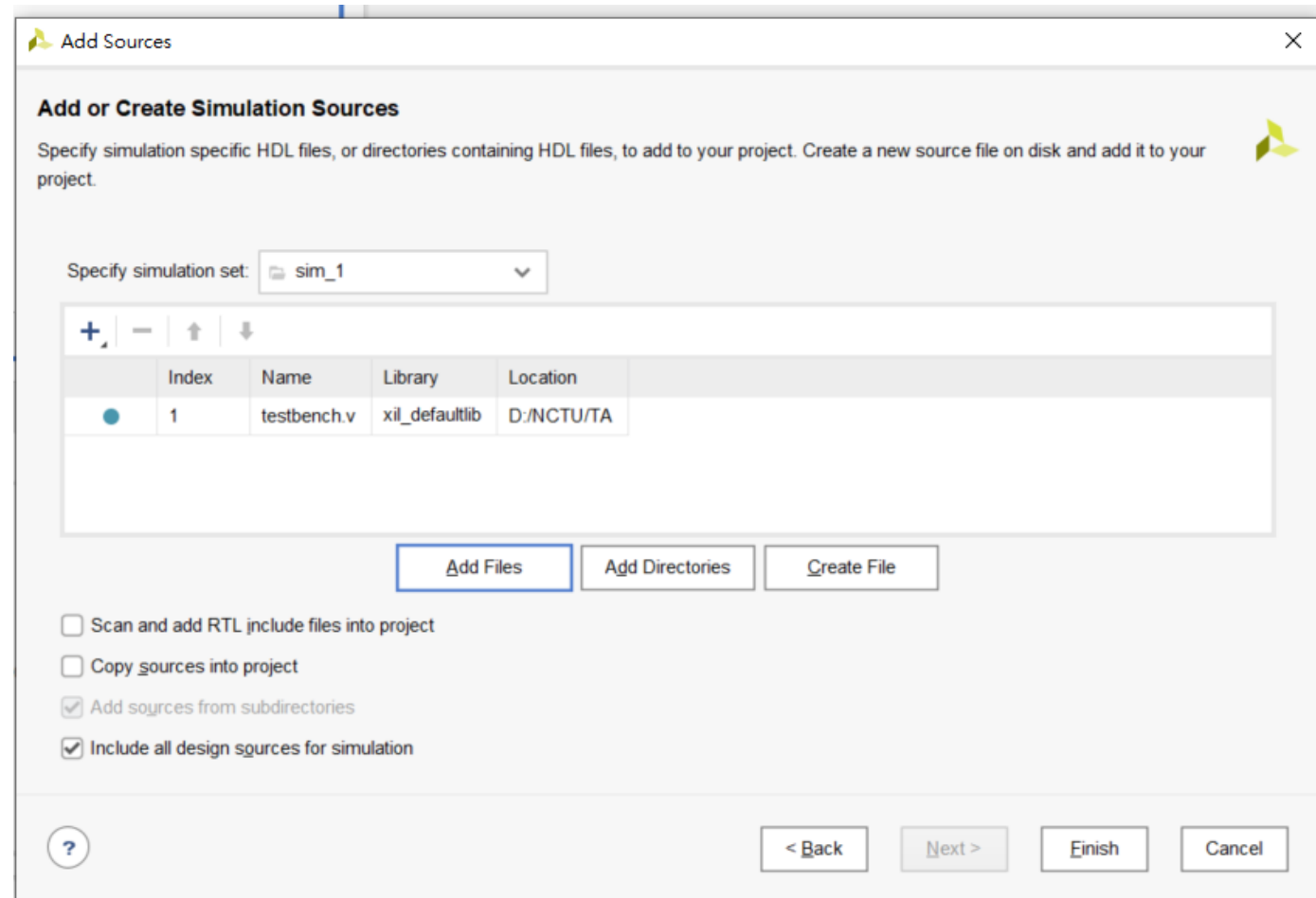
Add Simulation Sources

- Press add sources and select Add or create simulation sources



Add Simulation Sources

- Add testbench.v and finish



The image shows a screenshot of the 'Add Sources' dialog box in a software application. The dialog has a title bar with a yellow icon and a close button. The main area is titled 'Add or Create Simulation Sources' and contains instructions: 'Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.' Below this, there is a dropdown menu for 'Specify simulation set:' with 'sim_1' selected. A table with columns 'Index', 'Name', 'Library', and 'Location' is shown, containing one entry: '1', 'testbench.v', 'xil_defaultlib', and 'D:/NCTU/TA'. To the right of the table are buttons for '+', '-', '↑', and '↓'. Below the table are three buttons: 'Add Files', 'Add Directories', and 'Create File'. At the bottom, there are four checkboxes: 'Scan and add RTL include files into project' (unchecked), 'Copy sources into project' (unchecked), 'Add sources from subdirectories' (checked), and 'Include all design sources for simulation' (checked). At the very bottom, there is a help icon, a '< Back' button, a 'Next >' button, an 'Finish' button, and a 'Cancel' button.

Add Sources

Add or Create Simulation Sources

Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.

Specify simulation set: sim_1

	Index	Name	Library	Location
●	1	testbench.v	xil_defaultlib	D:/NCTU/TA

+ - ↑ ↓

Add Files Add Directories Create File

☐ Scan and add RTL include files into project

☐ Copy sources into project

☒ Add sources from subdirectories

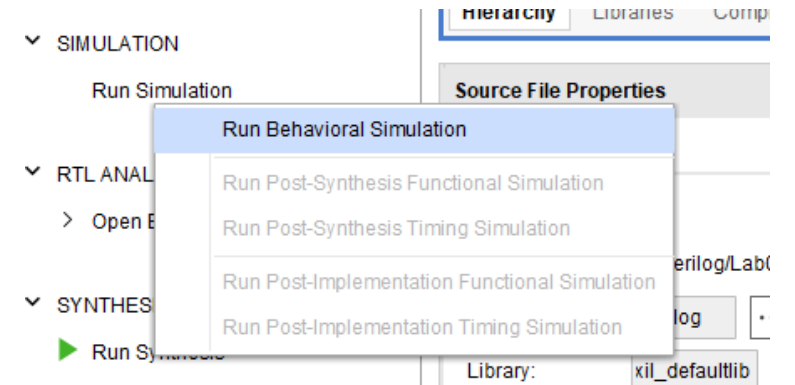
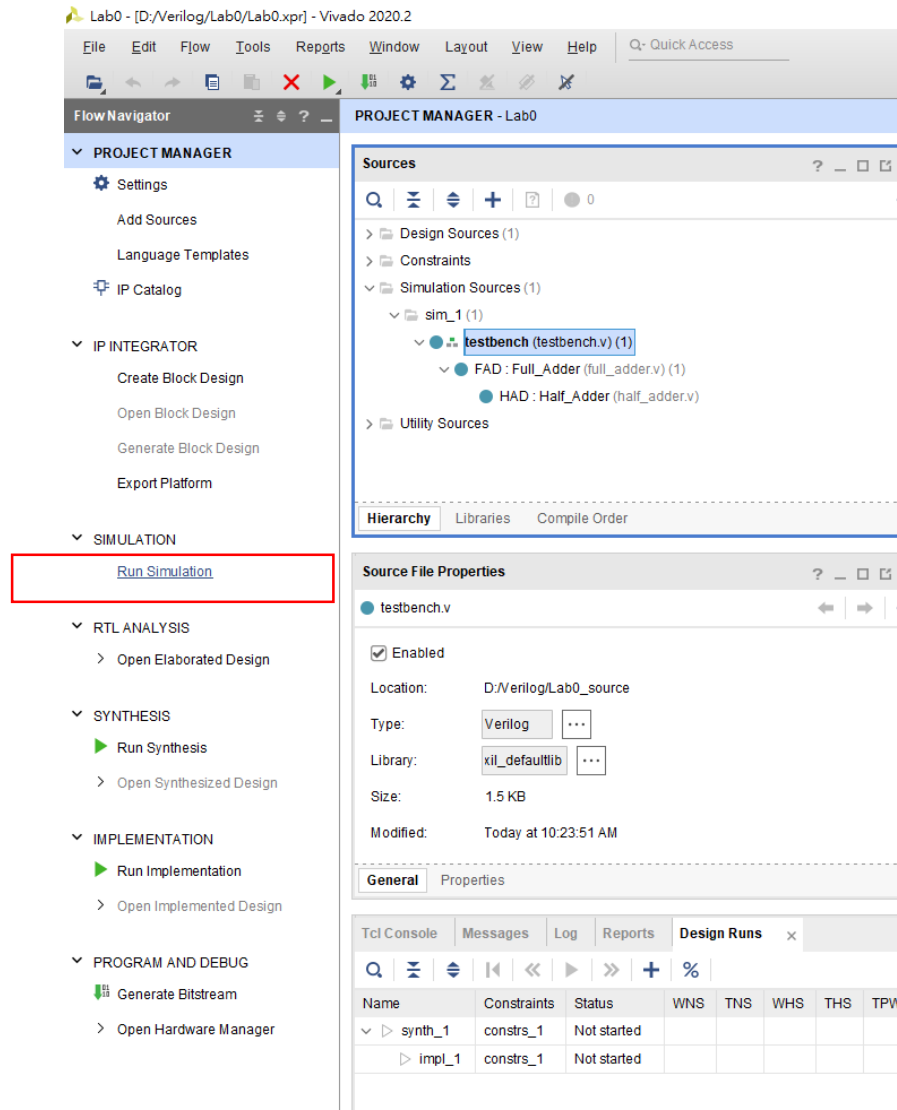
☒ Include all design sources for simulation

? < Back Next > Finish Cancel

How to Run Simulation

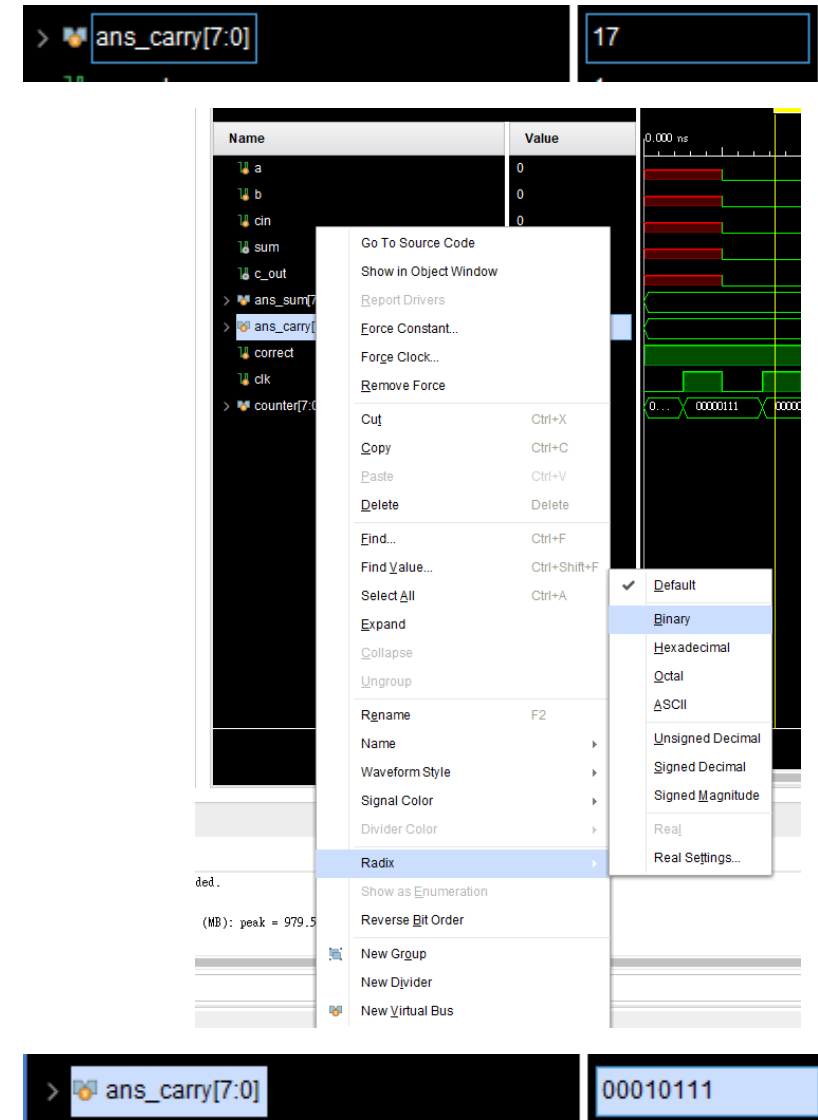
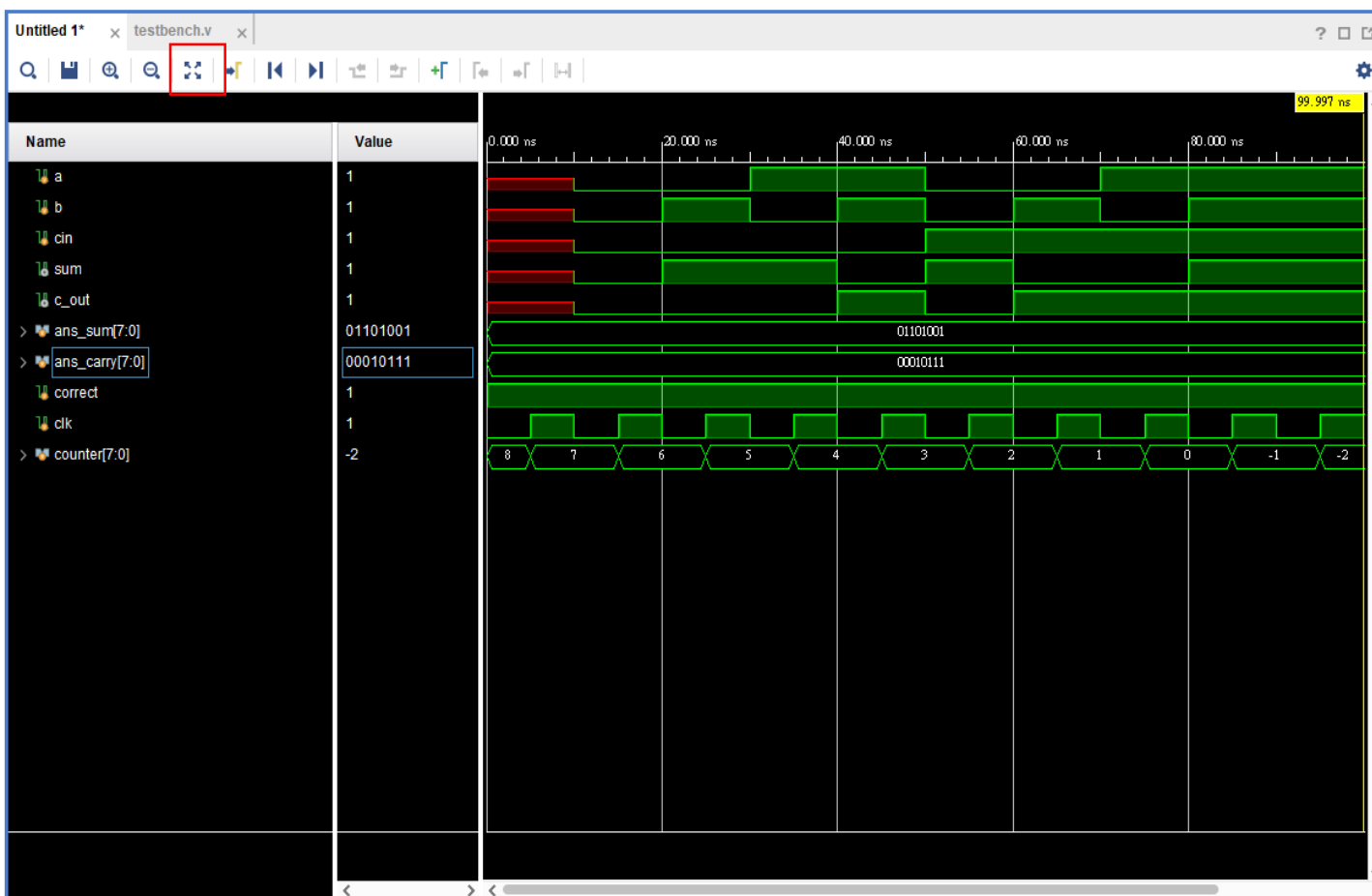
- After adding testbench into project, you can execute the behavioral simulation. It can help you debug with the signal waveform and check the correctness of your design.

How to Run Simulation



Useful Information

This bottom can make your waveform fit your screen size.

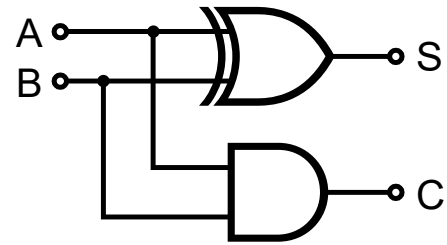


This function can help you change the radix of the signal

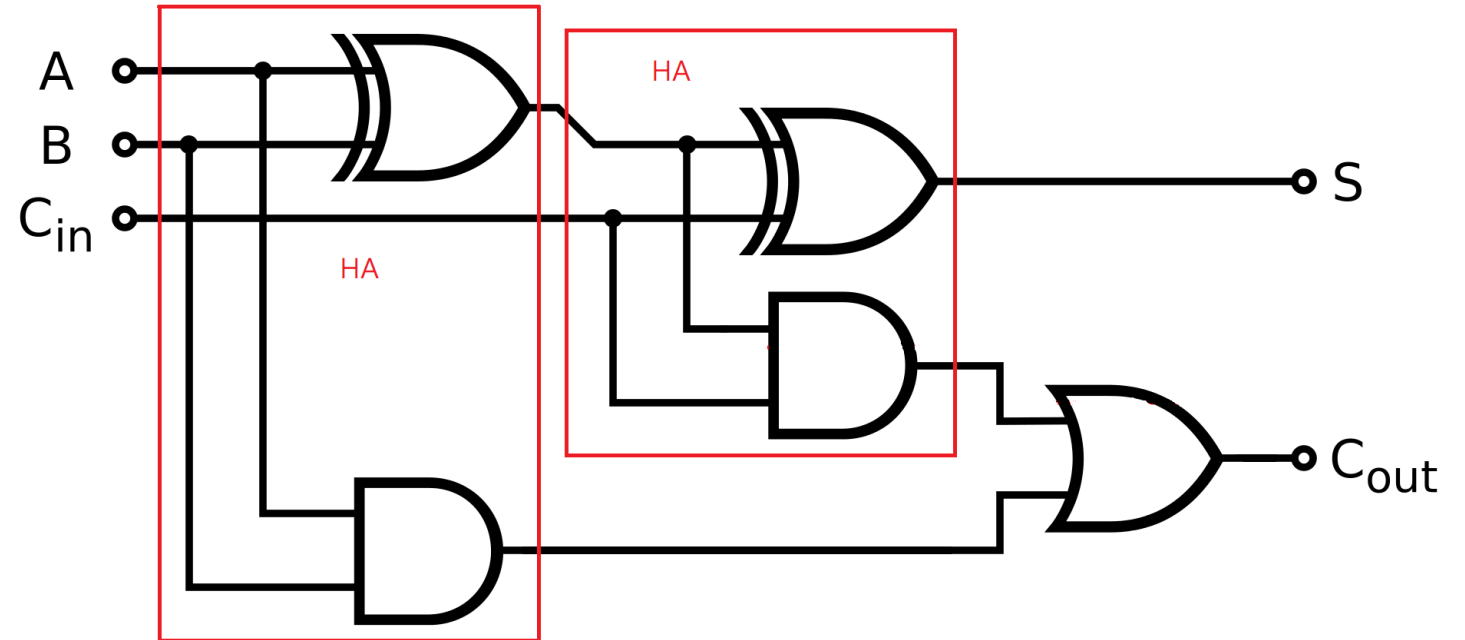
Lab0: Half Adder and Full Adder

- Implement the half adder and full adder without using '+' operation.
- We want you to practice how to implement the signal connection with the given circuit. We will give you example design sources and testbench.v.

Half Adder Circuit and Full Adder Circuit



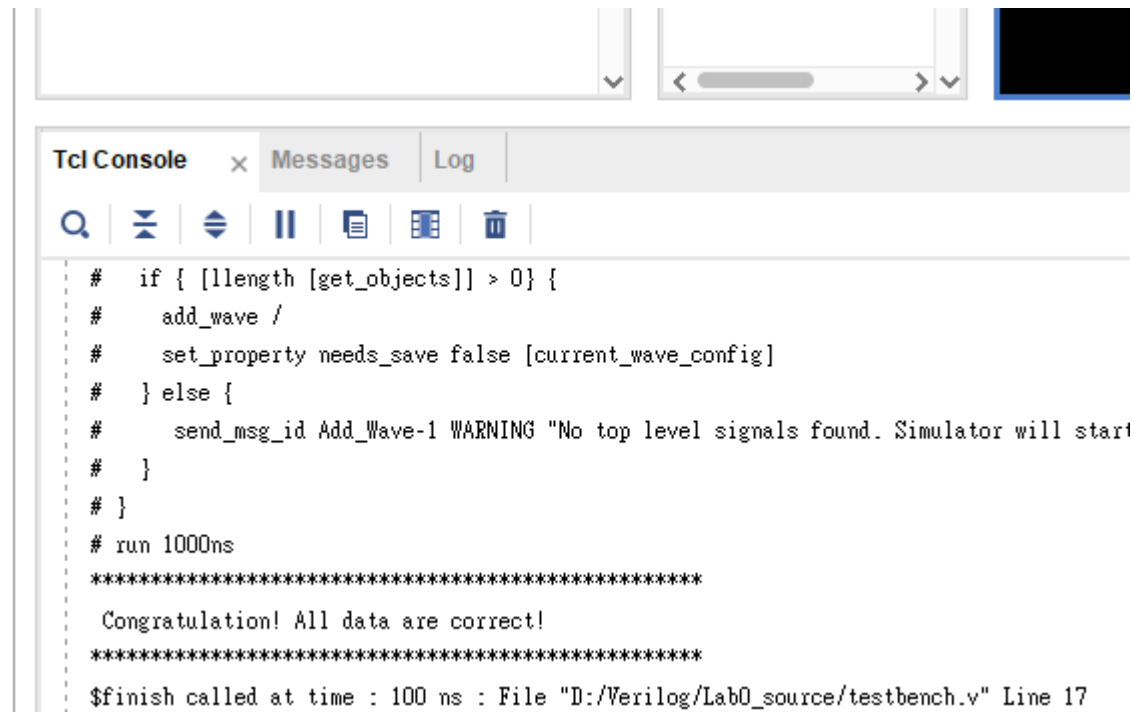
Half Adder



Full Adder

Check Correctness

- We have enumerated all input cases in testbench.v.
- After simulation with our testbench.v, if your design is correct, you will see the message in the console.



The screenshot shows a software interface with a 'Tcl Console' window. The window has tabs for 'Messages' and 'Log'. Below the tabs is a toolbar with icons for search, zoom, and other functions. The console displays the following text:

```
# if { [llength [get_objects]] > 0 } {  
#   add_wave /  
#   set_property needs_save false [current_wave_config]  
# } else {  
#   send_msg_id Add_Wave-1 WARNING "No top level signals found. Simulator will start  
# }  
# }  
# run 1000ns  
*****  
Congratulation! All data are correct!  
*****  
$finish called at time : 100 ns : File "D:/Verilog/Lab0_source/testbench.v" Line 17
```

Submission

- Due date: 2021/03/14 23:55
- Put your all design sources and testbench.v into one directory named “your_student_id” and zip the directory named “your_student_id.zip”. You only need to submit “your_student_id.zip”.
- If you have any question, feel free to ask on the Facebook discussion forum (prefer) or email to us. Thank you.