UNIT-3

MOSFET CONSTRUCTION, OPERATION, CHARACTERISTICS, AC EQUIVALENT CIRCUIT, MOSFET AS AN AMPLIFIER, CMOS INVERTER, NAND GATE AND NOR GATE, BASIC PRINCIPLES AND ADVANTAGES OF NEGATIVE FEEDBACK

INTRODUCTION:

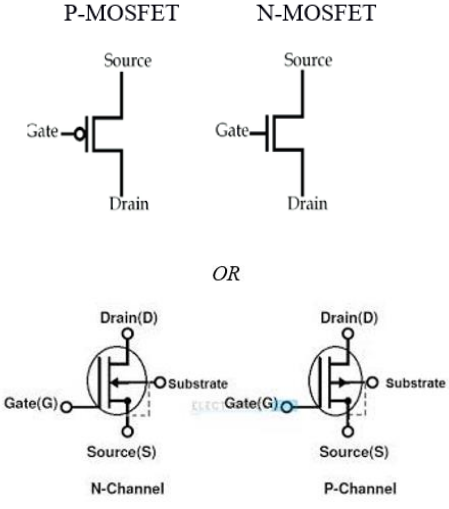
The field effect transistor (FET) is a three terminal device used for a variety of applications similar to BJT. There are certain similarities as well as a few differences between the two types of transistors i.e, BJT and FET. The primary difference being BJT is a current controlled device whereas FET is a voltage controlled device. Just as there are npn and pnp bipolar transistors there are n-channel and p-channel field effect transistors. However BJT is bipolar device where both charge carriers electrons and holes contribute to conduction whereas FET is a unipolar device where conduction is due to either electrons or holes. FET's one of the most important characteristic is it has high input impedance. Also FETs are more temperature stable than BJTs and FETS are usually smaller than BJTs making them particularly useful in integrated circuits (IC) chips.

Differences between BJT and MOSFET:

BJT	MOSFET
Current controlled device	Voltage controlled device
Bipolar	Unipolar
Less input impedance compared to MOSFET	High input impedance
Takes more area on an Integrated circuit	Less area on an Integrated circuit
More fabrication cost	Less fabrication cost
No terminals are interchangeable	Source and Drain terminals are interchangeable.
Gain is high	Gain is comparatively less
No terminals isolated	Gate terminal is isolated by SiO_2 layer

There are three types of FETs: Junction Field Effect Transistor (JFET), Metal-oxide Semiconductor Field Effect Transistor (MOSFET), and Metal Semiconductor Field Effect Transistor (MESFET).

Symbols of MOSFET:



CONSTRUCTION OF MOSFET:

MOSFET has become one of the most important devices used in the design and construction of integrated circuits. Its thermal stability and other general characteristics make it extremely popular in integrated circuit design. MOSFETs are further classified into depletion type and enhancement type which define the basic mode of operation. We study only enhancement type in our syllabus.

Enhancement type MOSFET construction: The basic construction of the n-channel enhancement MOSFET is shown in the Figure 1. It has three terminals namely source, gate and drain. A slab of p-type material is formed from a silicon base and is referred to as substrate. This substrate may be internally connected to the source terminal or can be used as a fourth terminal to externally control its potential level. Over the substrate two n type regions are formed as shown in Figure1. These regions form source and drain terminals which are connected through metallic contacts. Over this substrate a very thin layer of silicon dioxide is formed and a metallic contact is formed which becomes the gate terminal. The silicon dioxide (insulator/dielectric) layer is present to isolate the gate metallic platform from the region between the source and the drain. The built in potential between source and gate is referred to as threshold voltage(V_{th}).

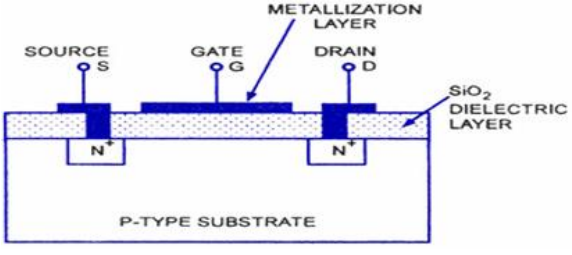


Figure 1: n- channel enhancement type MOSFET(Cross sectional view)

BASIC OPERATION AND CHARACTERISTICS:

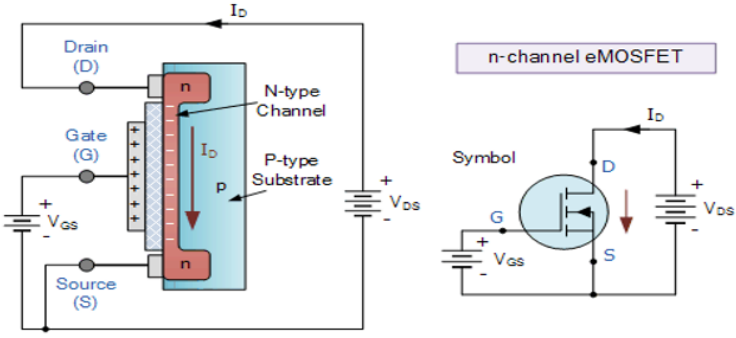


Figure 2: Bias conditions of n- channel enhancement type MOSFET

Operations of N-MOSFET are as follows:

Case 1: $V_{GS} < V_{th}$ and $V_{DS} > 0$: With V_{DS} some positive voltage and V_{GS} at 0V, There are two reverse biased pn junctions between n doped regions and p substrate to oppose any significant current flow between drain and source. Hence current in the device is effectively nil. Hence the device is in cut-off condition.

Eqn.1: $I_D = 0$

Device in Cut-off: $V_{GS} < V_{th}$

Case 2: $V_{GS} > V_{th}$ and $V_{DS} < V_{GS} - V_{th}$: With V_{DS} and V_{GS} set at some positive voltage, the positive potential at the gate will pressure the holes in the p-substrate (majority carriers) along the edge of sio2 layer to leave the area and enter into deeper regions of the p-substrate. However the electrons in the p substrate (minority carriers) will be attracted to the positive gate and accumulate in the region near the surface of sio2 layer. The sio2 layer's insulating properties will prevent

these electrons from getting absorbed at the gate terminal. As $\mathbf{V_{GS}}$ increases in magnitude, the concentration of electrons near the sio2 surface increases until eventually the induced n type region can support a measurable amount of current flow between source and drain. This n type region between source and drain is called channel. The level of $\mathbf{V_{GS}}$ that results in formation of the channel and hence significant increase in drain current (ID) is called threshold voltage (Vth).Figure 2 shows the formation of the channel between drain and source. Under this condition, the device will operate in linear or ohmic or triode region. Eqn.2 represents the N-MOSFET current equation in ohmic region, where K is a constant representing process parameter.

$$\text{Eqn.2:} \quad I_D = K[(V_{GS}-V_{th})V_{DS} - V_{DS}^2/2]$$

$$\text{Device in Linear or Ohmic: } V_{GS}-V_{th} > V_{DS}$$

Where K is the process parameter in A/V^2

Case 3: VGS>V_{th} and V_{DS}= V_{GS}-V_{th}: If VGS is held constant at some voltage greater than Vth and increase the level of $\mathbf{V_{DS}}$ the drain current will eventually reach a saturation level. The levelling off of ID is due to pinching off process as shown in the Figure 3 at the drain end of the induced channel since drain is more reverse biased than the source.

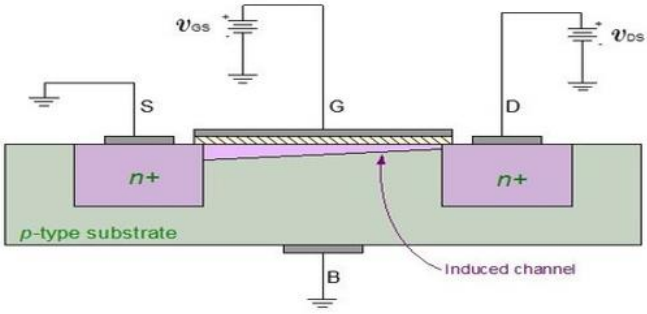


Figure 3: Pinch off proces

Also if V_{GS} is fixed and V_{DS} is increased, according to eqn 2, the gate will become less and less positive with respect to drain and hence there is reduction in channel width. Eventually the channel will be reduced to the point of pinch-off and a saturation region is established. The saturation level of V_{DS} is related to the level of applied V_{GS} by,

$$V_{DS\ sat} >= V_{GS}-V_{th}$$

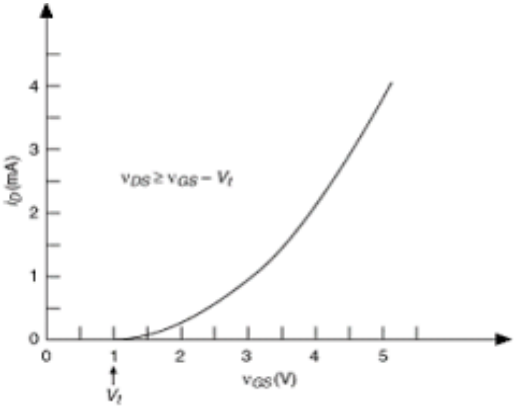
After pinch-off, further increase in VDS does not cause any increase in ID attaining saturation. The eqn 3 represents the N-MOSFET current equation in saturation region.

Eqn.3: $I_D = K/2.\ (V_{GS}-V_{th})^2$

Device in Saturation: $V_{DS}>= V_{GS}-V_{th}$

Where K is the process parameter in A/V^2

TRANSFER CHARACTERISTICS (I_D Vs V_{GS} for a fixed V_{DS}):



OUTPUT CHARACTERISTICS (ID Vs VDS for a fixed VGS):

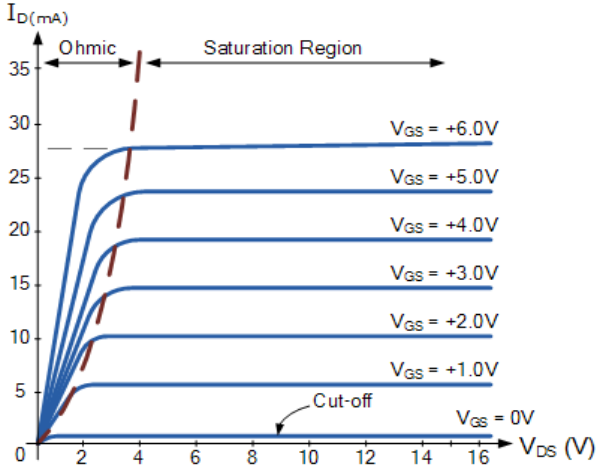


Figure 4: Drain characteristics

As shown in the Figure 4, there are three regions in the drain characteristics of MOSFET namely ohmic /triode region where $V_{GS} > V_{th}$ and I_D is increasing, saturation region where I_D gets saturated by increasing levels of V_{DS} and cut-off region where I_D is zero as $V_{GS} < V_{th}$.

MOSFET AS AN AMPLIFIER:

The Figure 6 shows N-MOSFET in voltage divider configuration used for amplification along with the DC-load line on its input characteristics.

Note: Circuit analysis is similar to BJT.

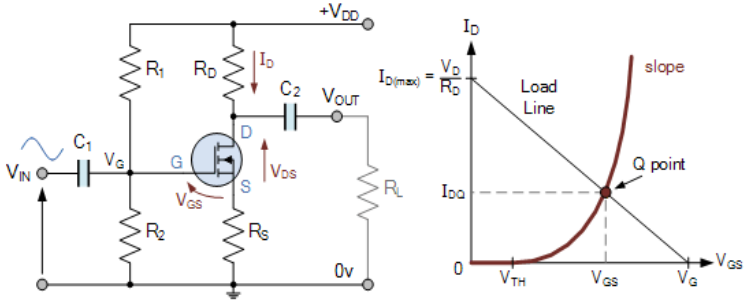


Figure 6: N-MOSFET as an amplifier

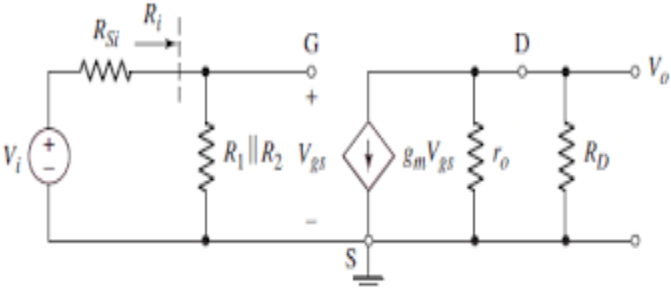


Figure 7: Small signal (AC) equivalent model of CS-amplifier

Input Impedance	Zi= R1||R2
Output Impedance	Z_0= r_o||R_D
Transconductance gm	K (V_{GS}-V_{th}) or 2I_D /(V_{GS}-V_{th}) or $\sqrt{2ID.K}$
r_{ds} for small value of V_{DS}	rds= 1/ K (V_{GS}-V_{th})
Gain (without load resistance)	Av= -gm*R_D
Gain (with load resistance)	Av= -gm*(R_D||R_L)

CMOS inverter: A very effective logic circuit with high input impedance, fast switching speeds, and lower operating power levels can be obtained by constructing p channel and n channel MOSFETS on a same substrate. This configuration is called complementary MOSFET arrangement. A complementary MOS (CMOS) inverter is implemented as the series connection of a p-device and an n-device, as shown in Figure 8. Note that the source and the substrate of the p - device is tied to the VDD rail, while the source and the substrate(VSS or GND) of the n-device are connected to the ground bus and drain terminals of both devices are connected to the output Vo.

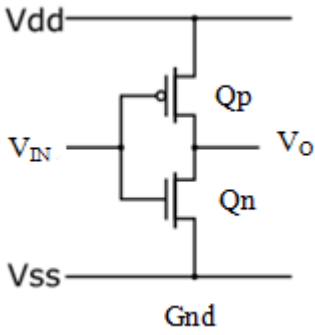


Figure 8:CMOS Inverter

An inverter is a circuit that inverts the applied signal. That is, if the logic levels of operation are 0V and 5V, an input level of 5V will result in output level of 0V and vice versa. For logic levels defined above, application of 5V at the input VIN, VGS of Qn=5V and Qn is on, resulting in low resistance between drain and source. Since VIN and VSS are at 5V, VGS of Qp=0V, and hence Qp is off. The resulting resistance level between drain and source is quite high for Qp. Hence Vo becomes 0V establishing inversion process. For an applied voltage VIN of 0V, VGSN=0V and Qn will be off and

VGSP=-5V, turning on the p channel MOSFET. The result is that Qp will present a small resistance , Qn a high resistance level, and Vo= 5V.

VIN	Qn	Qp	Vo
0V(LOW)	OFF	ON	5V(HIGH)
5V(HIGH)	ON	OFF	0V(LOW)

THE CMOS NAND GATE:

The schematic diagram of a 2-input CMOS NAND gate is shown in Figure.9. It can be seen that in this structure, the n-type driving transistors are connected in series while the p-type load transistors are connected in parallel. Transistors are a driven in n-type cum p-type pairs with one transistor ON while the other is OFF. A table of the conducting states of the transistors for all logic combinations of the inputs is given below.

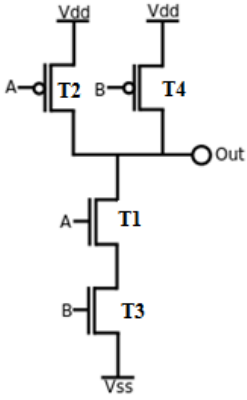


Figure 9 CMOS NAND gate

IN A	IN B	T_1	T_2	T_3	T_4	OUT
LO	LO	OFF	ON	OFF	ON	HI
LO	HI	OFF	ON	ON	OFF	HI
HI	LO	ON	OFF	OFF	ON	HI
HI	HI	ON	OFF	ON	OFF	LO

THE CMOS NOR GATE:

The schematic diagram of a 2-input CMOS NOR gate is shown in Figure.10. It can be seen that similar to NAND gate structure, the n-type driving transistors are connected in parallel while the p-type load transistors are connected in Series. Transistors are a driven in n-type cum p-type pairs with one transistor ON while the other is OFF. A table of the conducting states of the transistors for all logic combinations of the inputs is given below.

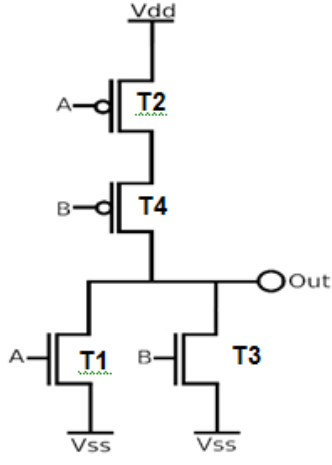


Figure 10 CMOS NOR gate

A	B	T1	T2	T3	T4	OUT
LO	LO	OFF	ON	OFF	ON	HI

LO	HI	OFF	ON	ON	OFF	LO
HI	LO	ON	OFF	OFF	ON	LO
HI	HI	ON	OFF	ON	OFF	LO

Negative Feedback

The block diagram of a feedback amplifier is shown in fig2.1.

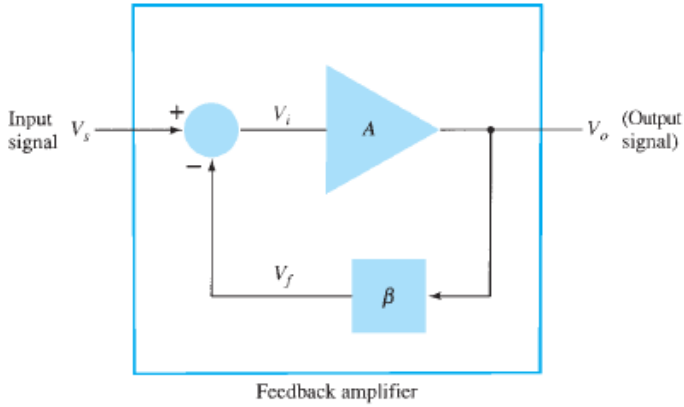


Fig2.1: Simple block diagram of feedback amplifier.

Gain with feedback:

$$A = \frac{V_o}{V_s} = \frac{V_o}{V_i}$$

If a feedback signal V_f is connected in series with the input, then

$$V_i = V_s - V_f$$

Since $$V_o = AV_i = A(V_s - V_f) = AV_s - AV_f = AV_s - A(\beta V_o)$$

then $$(1 + \beta A)V_o = AV_s$$

so that the overall voltage gain *with* feedback is

$$A_f = \frac{V_o}{V_s} = \frac{A}{1 + \beta A}$$

Gain stability with feedback:

$$\left|\frac{dA_f}{A_f}\right| = \frac{1}{|1 + \beta A|}\left|\frac{dA}{A}\right|$$

$$\left|\frac{dA_f}{A_f}\right| \cong \left|\frac{1}{\beta A}\right|\left|\frac{dA}{A}\right| \qquad \text{for } \beta A \gg 1$$

This shows that magnitude of the relative change in gain $\left|\frac{dA_f}{A_f}\right|$ is reduced by the factor $|\beta A|$ compared to that without feedback $\left(\left|\frac{dA}{A}\right|\right)$.

Advantages of negative feedback amplifiers:

1. Input impedance increases by a factor of 1+Aβ
2. Output impedance decreases by a factor of 1+Aβ
3. Bandwidth increases by a factor of 1+Aβ
4. Distortion decreases by a factor of 1+Aβ
5. Noise decreases by a factor of 1+Aβ
6. Stability of the gain improves by a factor of 1+Aβ