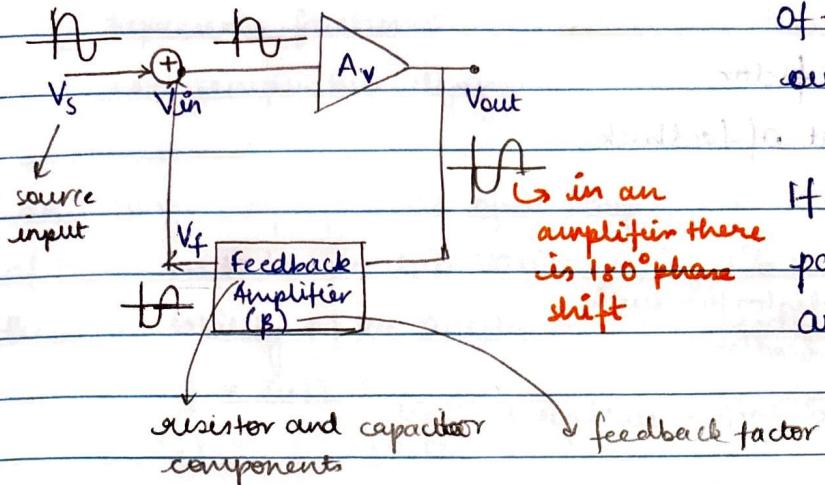


UNIT 2:

FEEDBACK AMPLIFIERS:



If the source signal and part of the feedback output are out of phase \rightarrow negative feedback

in an amplifier there is 180° phase shift

If the source signal and part of the feedback output are in phase \rightarrow positive feedback

$$A_v = \frac{V_{out}}{V_{in}} ; A_f = \frac{V_{out}}{V_s}$$

$$\beta = \frac{V_{out}}{V_{f\ out}}$$

feedback factor

$$V_{in} = V_s - V_f$$

$$A_f = \frac{V_{out}}{V_s} = \frac{V_{out}}{V_{in} + V_f} = \frac{V_{out}/V_{in}}{1 + \frac{V_f}{V_{in}}} = \frac{A_v}{1 + \beta \cdot A_v}$$

voltage series negative feedback

$$A_f = \frac{A_v}{1 + \beta \cdot A_v} \rightarrow \text{negative feedback}$$

$$A_f = \frac{A_v}{1 - \beta \cdot A_v} \rightarrow \text{positive feedback}$$

ADVANTAGES OF NEGATIVE FEEDBACK:

- (1) Stability of the gain improves by the factor $(1 + A_v \beta)$
- (2) Distortion reduced by $(1 + A_v \beta)$
- (3) noise decreases by $(1 + A_v \beta)$
- (4) Bandwidth increases by $(1 + A_v \beta)$
- (5) Z_{in} (input impedance) increases by $(1 + A_v \beta)$

(6) Output impedance decreases by $(1+A_V\beta)$

(7) It provides gain control.

$\beta \rightarrow$ feedback factor

$(1+A_V\beta) \rightarrow$ amount of feedback

FORMULAS:

$$(1) D_f = \frac{D}{1+A_V\beta}$$

distortion with
feedback

distortion without feedback

$$(2) A_N f = \frac{N}{1+A_B}$$

$$(3) BW_f = BW(1+A_B)$$

$$(4) Z_{inf} = Z_{in}(1+A_B)$$

$$(5) Z_{af} = \frac{Z_{af}}{1+A_B}$$

(Q) Prove that stability of the gain of an amplifier with negative feedback improves by a factor $(1+A_B)$, compared to that of amplifier without feedback, where A is the open loop gain, and β is the feedback factor.

$$(A) A_f = \frac{A}{1+A_B} \quad (\text{differentiate both sides w.r.t. } A)$$

$$\frac{d(A_f)}{dA} = \frac{1(1+A_B) - A(\beta)}{(1+A_B)^2} = 1$$

$$\frac{d(A_f)}{dA} = \frac{dA}{(1+A_B)^2} \quad (\text{divide both sides by } A_f)$$

$$\frac{d(A_f)}{dA} = \frac{1}{A_f} \circ \frac{dA}{(1+A_B)^2} \quad (\text{substitute } A_f)$$

$$\Rightarrow \frac{d(A_f)}{dA} = \frac{dA}{A_f(1+A_B)^2} \quad (\text{cancel out } dA})$$

$$\Rightarrow \frac{d(A_f)}{dA} = \frac{1}{A_f(1+A_B)^2} \quad (\text{cancel out } dA})$$

changes with temperature parameters

important relation for stability

Here ΔA_f represents fractional change in amplification with feedback.

A_f

ΔA_f represents fractional change in amplification without feedback. (This A is a temperature dependent parameter)

- (a) An voltage amplifier has open loop gain (A_f) of 500 and gain stability of 1% due to temperature variations. If 1% negative feedback is given then the gain stability of the amplifier with feedback is

$$(A) \Delta A_f = 0.12 \times \frac{1}{1 + 500(0.01)} \\ \approx 0.02 \\ \approx 2\%$$

- (b) An amplifier has gain of 60dB, bandwidth of 500kHz, distortion $\rightarrow 16\%$, input impedance 50k Ω , output impedance (Z_o) = 100 Ω . If 3% negative feedback is given, determine bandwidth, distortion, input impedance Z_{in} and gain of the amplifier with feedback.

$$(A) P_f = \frac{0.16}{1 + \frac{1000}{60 \times 0.03}} = 5.16 \times 10^{-3}$$

$$A_f = 20 \log_{10} \left(\frac{V_o}{V_i} \right)$$

$$BW_f = 500 \times 10^3 \left(1 + 1000 \times 0.03 \right) = 15500000 \approx 15.5 \text{ MHz}$$

$$Z_{in} = 50 \times 10^3 \left(1 + 1000 \times 0.03 \right) = 1550000 \approx 1.55 \text{ M}\Omega$$

$$Z_o = \frac{400}{1 + 1000 \times 0.03} = 12.9$$

$$A_f = \frac{A_v}{1 + \beta A_v} = \frac{1000}{1 + 0.03 \times 1000} = 32.25$$

- (c) An amplifier has an open loop gain of 8000, input impedance = 100k Ω ; Z_o = 10k Ω ; distortion = 15%; gain stability = 20%, bandwidth = 500kHz, noise = 1 pV. By giving negative feedback, the Z_{in} needs to be increased to 2.2M Ω . Determine the feedback factor required, also find gain, Z_{in}, Z_o, BW, N, D of the closed loop amplifier.

(A)

$$2 \cdot 2 \times 10^6 = 100 \times 10^3 (1 + 8000\beta)$$

$$2 \cdot 2 \times 10^6 = 1 + 8000\beta$$

$$100 \times 10^3$$

$$22 = 1 + 800\beta$$

$$21 = 800\beta$$

$$\beta = 21 = 2.625 \times 10^{-3}$$

8000

$$Z_{out} = 100 \times 10^3 (1 + 8000 \times 2.625 \times 10^{-3}) = 2200000$$

$$Z_0 = 10 \times 10^3$$

$$= 154.54 \times 10^3 = 154540 \Omega$$

$$1 + 8000 \times 2.625 \times 10^{-3}$$

$$BW = 500 \times 10^3 (1 + 8000 \times 2.625 \times 10^{-3}) = 11000000$$

$$N_f = 1 \times 10^{-6}$$

$$= 4.54 \times 10^{-8}$$

$$\beta_f = 0.15$$

$$= 6.89 \times 10^{-3}$$

$$d(A_f) = 0.20$$

$$= 9.09 \times 10^{-9}$$

$$A_f = 1 + 8000 \times 2.625 \times 10^{-3}$$

~~(3) $V_o = 10 \text{ mV}, A_f = 40 \text{ dB}, A_v = ??, \beta = 23$~~

$$A_v = V_{out} ; A_f = V_{out}$$

 V_{in} V_s 2.5 mV 0.001 mV

$$V_{out} = A_v \cdot V_{in} = A_v \cdot 10 \times 10^{-3}$$

$$A_f = \sqrt{10} \approx 3.16 \text{ (approx)}$$

$$100 = A_f = \frac{A_v \cdot 10 \times 10^{-3}}{4}$$

$$A_v = \frac{100 \times 4}{10 \times 10^{-3}} = 40 \times 10^3$$

$$= 4 \times 10^2$$

$$A_f = A_v \cdot (1 + \beta \cdot A_v)$$

$$(1 + \beta \cdot A_v)$$

$$\Rightarrow 100 + 100 \cdot \beta \cdot 4 \times 10^{-2} = 4 \times 10^{-2}$$

$$4 \times 10^{-2} - 100 = 4\beta$$

$$\beta = \frac{(4 \times 10^{-2} - 100)}{4} = -24.99$$

A

$$(1) V_{in} = 2 \times 10^{-3} V; V_{out} = 10 V; V_s = 200 \times 10^{-3} V$$

$$A_v = \frac{V_{out}}{V_{in}} = \frac{10}{2 \times 10^{-3}} = 5000 = 73.97 \text{ dB}$$

$$A_f = \frac{V_{out}}{V_s} = \frac{10}{200 \times 10^{-3}} = 50 = 33.97 \text{ dB}$$

The amount of feedback =

$$1 + AB$$

$$50 = \frac{5000}{1 + AB} \Rightarrow 50 + 50AB = 5000 \quad (1)$$

$$1 + \beta \cdot 5000 \quad 5000 \times 50 \times \beta = 5000 - 50$$

$$\beta = \frac{(5000 - 50)}{(5000 \times 50)} = 0.0198 \quad (2)$$

$$(5000 \times 50)$$

$$A_f = 20 \log_{10}(50) \quad (3)$$

$$A_f = 33.97 \text{ dB}$$

$$(3) V_i = 10 \text{ mV}; A_v = 40 \text{ dB}; \frac{V_o}{V_i} = A \cdot 10 \text{ mV}.$$

$$A_f = \frac{A}{1 + AB} \Rightarrow A_f = \frac{10 \text{ mV} \cdot A_v}{1 + AB} \Rightarrow A_f = 2.5 \text{ mV} \cdot A_v \quad (1)$$

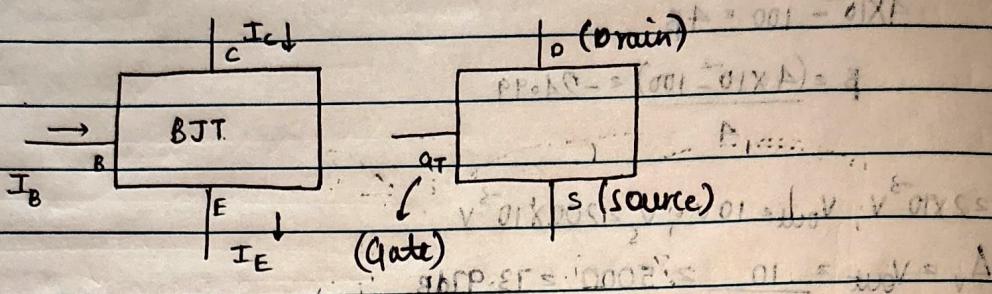
$$20 \log \left(\frac{A}{1 + AB} \right) = 40$$

$$\frac{A}{1 + AB} = 100$$

switch and amplifier
voltage controlled device while BJT \rightarrow current controlled

MOSFET: (Metal Oxide Semiconductor Field Effect Transistor)

An field effect transistor, either holes (or) electrons are responsible for conduction.



The comparison b/w BJT and MOSFET

= ~~BJT~~ ~~BJT to MOSFET~~

FIELD EFFECT TRANSISTOR

- | | |
|---------------------------------------|--|
| (1) BJT are current controlled device | (2) MOSFET are voltage controlled device |
| (2) Low input impedance | (2) High input impedance |
| (3) Bipolar device | (3) Unipolar device |
| (4) Larger size | (4) Smaller size |
| (5) Positive cost is more | (5) Lower cost |
| (6) Higher speed | (6) Lower speed |
| (7) Thermal runaway occurs | (7) Thermal runaway does not occur |
| (8) Less temperature stable | (8) More temperature stable |

CLASSIFICATION OF MOSFET

(1) Enhancement type MOSFET

(a) NMOS \rightarrow

(b) PMOS \rightarrow

(2) Depletion type MOSFET

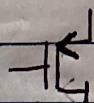
difference is Enhancement \rightarrow no channel

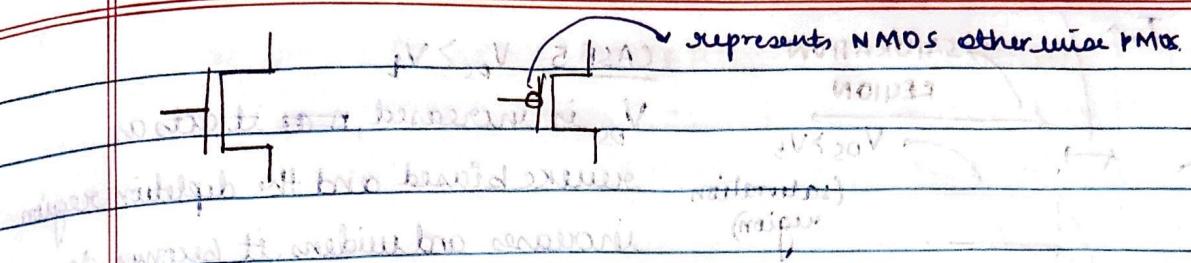
SYMBOLIC REPRESENTATION OF NMOS AND PMOS:

NMOS

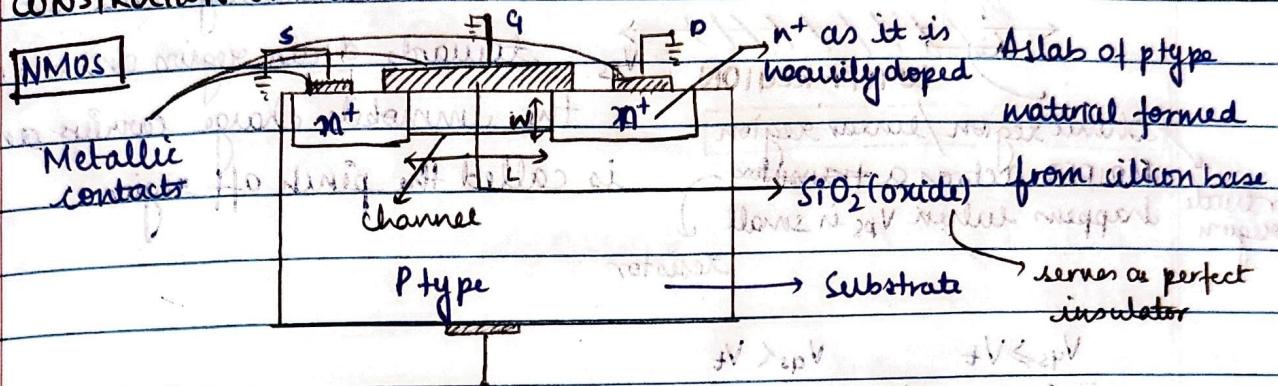


PMOS





CONSTRUCTION OF MOSFET:



CASE 1: When no external voltage is given ($V_{GS} = 0$)
It acts in cutoff region and is an open switch.

CASE 2: When V_{GS} has a small value ($|V_{GS}| < V_t$)

$I_d = 0$ as SiO_2 acts as a perfect insulator. There is a differentiation of the charge in the n^+ region and the ptype. (n^+ contains more e^- and ptype has more holes)

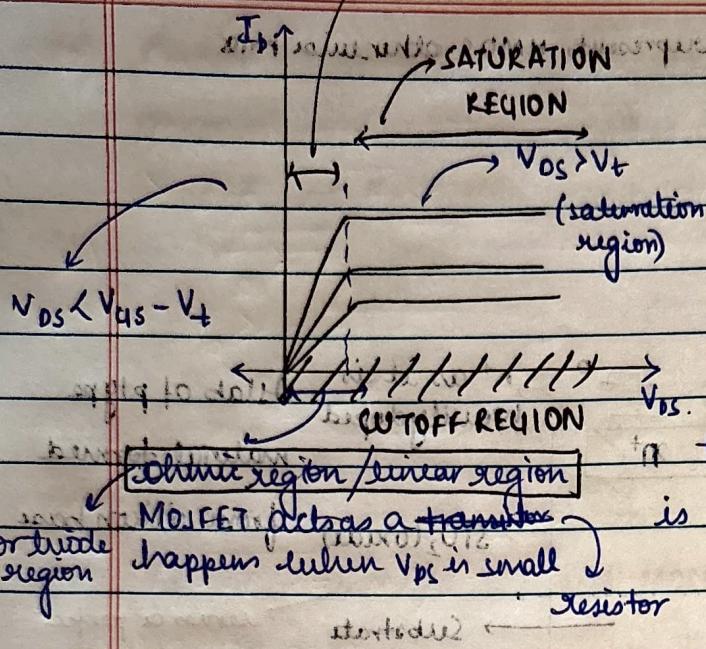
CASE 3: When $V_{GS} \geq V_t$ (threshold voltage)
 V_t is the threshold voltage specified by the manufacturer, and for the induction of the channel $V_{GS} = V_t$.

CASE 4: When V_{DS} has a small value. $(V_{DS} < V_{GS} - V_t)$
 I_D starts flowing from drain terminal to the source terminal. Dirⁿ of electron current is opposite to the conventional current. When V_{DS} is activated a channel which was induced when $V_{GS} = V_t$, allows I_D to flow through the device.

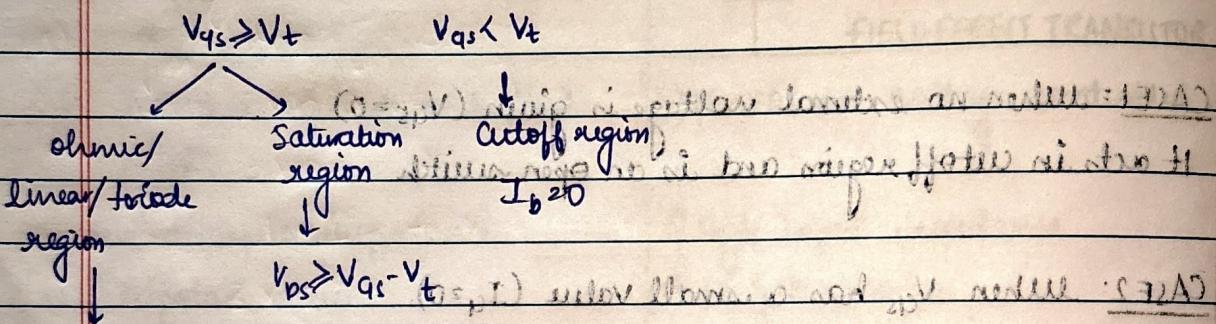
OUTPUT CHARACTERISTICS: I_D vs V_{DS} keeping input voltage is constant

saturation voltage of a diode
saturation voltage of a capacitor

OHMIC REGION

CASE 5: $V_{DS} > V_T$

V_{DS} is increased, so it acts as reverse biased and the depletion region increases and widens, it becomes deep towards source region and shallow towards drain region and it contains the immobile charge carriers and it is called the **pinch off region**.



$$\text{Ohmic region: } (I_D) = K [(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2]$$

$$\text{Saturation region: } (I_D) = K \left[\frac{V_{GS} - V_T}{2} \right]^2 \quad \text{where } K \text{ is the proportionality constant}$$

$$K = A/V^2 \quad \text{where } A \text{ is the area of the gate}$$

TRANSCONDUCTANCE:

$$g_m = K [V_{GS} - V_T], \text{ unit is Siemens/mho. } 25 \text{ mho} \approx 25 \text{ S}$$

LINEAR RESISTANCE: $R_{DS} = \frac{1}{g_m} = \frac{1}{K(V_{GS} - V_T)}$ value will increase as V_{GS} increases

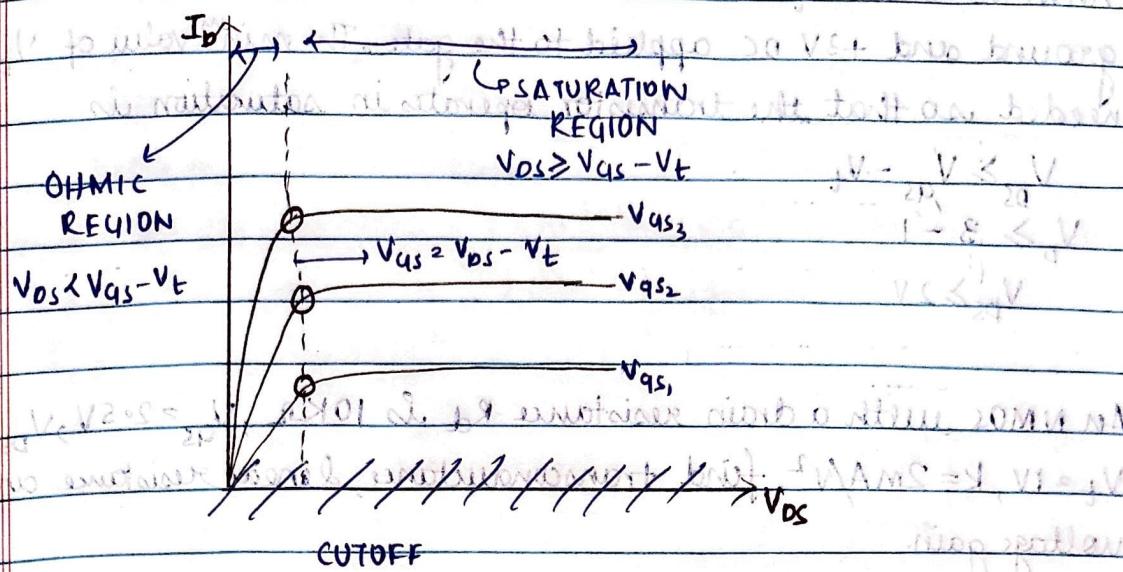
$$g_m = K [V_{GS} - V_T]$$

VOLTAGE GAIN: (N channel MOSFET) $A_V = -g_m \cdot R_{DS}$

$$A_V = -g_m \cdot R_{DS} \rightarrow (-) \text{ for } 180^\circ \text{ phase shift}$$

analogous to collector resistance

OUTPUT CHARACTERISTICS OF MOSFET



(Q) An NMOS having $V_t = 0.5V$, $K = 2\text{mA}/V^2$, $V_{GS} = 2V$; $V_{DS} = 1V$, $I_D = ?$

$$\begin{aligned}(A) \quad I_D &= K \left[(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \\ &= 2 \times 10^{-3} \left[1.5 \times 1 - \frac{1}{2} \times 1 \right] \\ &= 2 \times 10^{-3} [1.5 - 0.5] \\ &= 2 \times 10^{-3} \text{ A}\end{aligned}$$

(Q) An NMOS whose $V_t = 1V$, $K = 2\text{mA}/V^2$, is operating in saturation with $I_D = 4\text{mA}$, find V_{GS} and transconductance.

$$(A) \quad 4 \times 10^{-3} = 2 \times 10^{-3} [V_{GS} - 1]^2$$

$$\begin{aligned}&\Rightarrow 2 \times 10^{-3} = 2 \times 10^{-3} [3 - 1]^2 \\ &\Rightarrow g_m = 2 \times 10^{-3} \text{ mho.}\end{aligned}$$

(Q) An NMOS transistor, with $V_t = 1V$ is biased such that $V_s = 2V$, $V_g = 4V$. The maximum value of V_b allowed so that the transistor operates in ohmic region is

$$\begin{aligned}(A) \quad V_b - 2 &< 4 - 2 - 1 \\ &\Rightarrow V_b - 2 < 4 - 3 \\ &\Rightarrow V_b - 2 < 1 \\ &\Rightarrow V_b < 3V.\end{aligned}$$

(Q) An NMOS with $V_t = 1V$ has its source terminal connected to ground and +3V DC applied to the gate. The min^m value of V_b needed so that the transistor operates in saturation is

(A) $V_{DS} \geq V_{GS} - V_t$
 $V_b \geq 3 - 1$
 $V_{BS} \geq 2V$

(Q) An NMOS with a drain resistance R_d is $10\text{ k}\Omega$, $V_{GS} = 2.5V$, $V_{DS} = 4.5V$, $V_t = 1V$, $k = 2\text{ mA/V}^2$, find transconductance, linear resistance and voltage gain.

(A) $g_m = 2 \times 10^{-3} [2.5 - 1]$

$$= 2 \times 10^{-3} \times 1.5 \quad [V_{GS} - V_t] = 1, V_D = 0 = V_{DS}$$

$$R_{DS} = \frac{1}{3 \times 10^{-3}} \quad [1 - \frac{V_D}{V_{DS}}] = 1 \times 10^3 \quad [1 - \frac{0}{4.5}] = 10^3 \Omega$$

$$A_v = \frac{2 \times 10^{-3} \times 1}{3 \times 10^{-3}}$$

TUTORIAL:

(1) $V_t = 0.8V$; $k = 2\text{ mA/V}^2$

(a) $V_{GS} = 5V$; $V_{DS} = 2V$

$\rightarrow V_{DS} \leq V_{GS} - V_t \rightarrow$ ohmic region

$\rightarrow 2 \leq 5 - 0.8$

$1 \leq 4.2V$

$$I_D = K [V_{GS} - V_t] \cdot V_{DS} - \frac{1}{2} (V_{DS})^2$$

$$V_D = V_{DS} = 2 \times 10^{-3} [4.2 \times 1 - 0.8] = 1.2V$$

(c) $V_{GS} = 2V$; $V_{DS} = 1.2V$

$V_D = 1.2V$ \rightarrow cutoff region

(d) $V_{GS} = V_{DS} = 3V$

$V_t = 3 - 0.8$

$\geq 1.84\text{ mA}$

$E - A > C - V$

$I > C - V$

$N > C - V$

$$(2) V_t = 1V; I_d = 100 \times 10^{-6} A; V_{GS} = V_{BS} = 1.5V; V_{BS} > V_{GS} - V_t$$

$$I_p \rightarrow V_{GS} = 2.5V; V_{DS} = 1V$$

$$100 \times 10^{-6} = k [1.5 - 1]^2$$

$$100 \times 10^{-6} = \frac{2}{k} \times 0.5 \times 0.5$$

$$k = \frac{200 \times 10^{-6} \times 100}{25} = \frac{2 \times 10^{-4}}{25} = 0.8 \text{ mA/V}^2$$

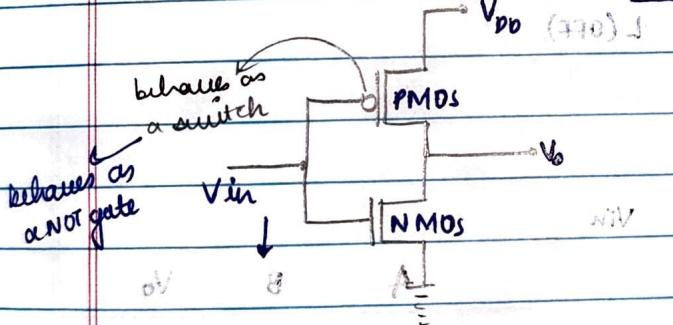
$$I_D = \frac{0.8 \times 10^{-3}}{2} [2.5 - 1]^2$$

$$= \frac{0.8 \times 10^{-3}}{2} \times 1.5 \times 1.5 = 0.9 \text{ mA}$$

$$V_{GS} = 3V; r_{ds} = \frac{10V}{0.8 \times 10^{-3} [3.25]} = 12.5 \text{ M}\Omega$$

CMOS INVERTER:

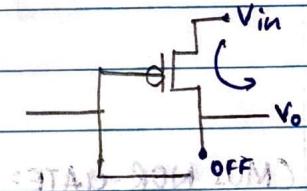
CASE 1: $V_{in} = \text{low}$.



NMOS = off

PMOS = on

$$V_o = V_{dd}$$



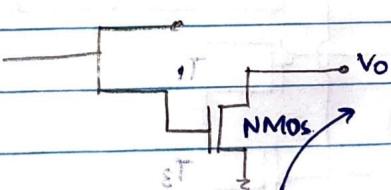
Equivalent circuit

CASE 2: $V_{in} = \text{high}$

① PMOS = off

② NMOS = on

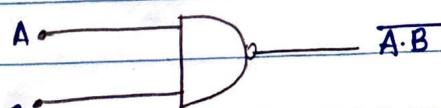
$$V_o = \text{Ground (0)}$$

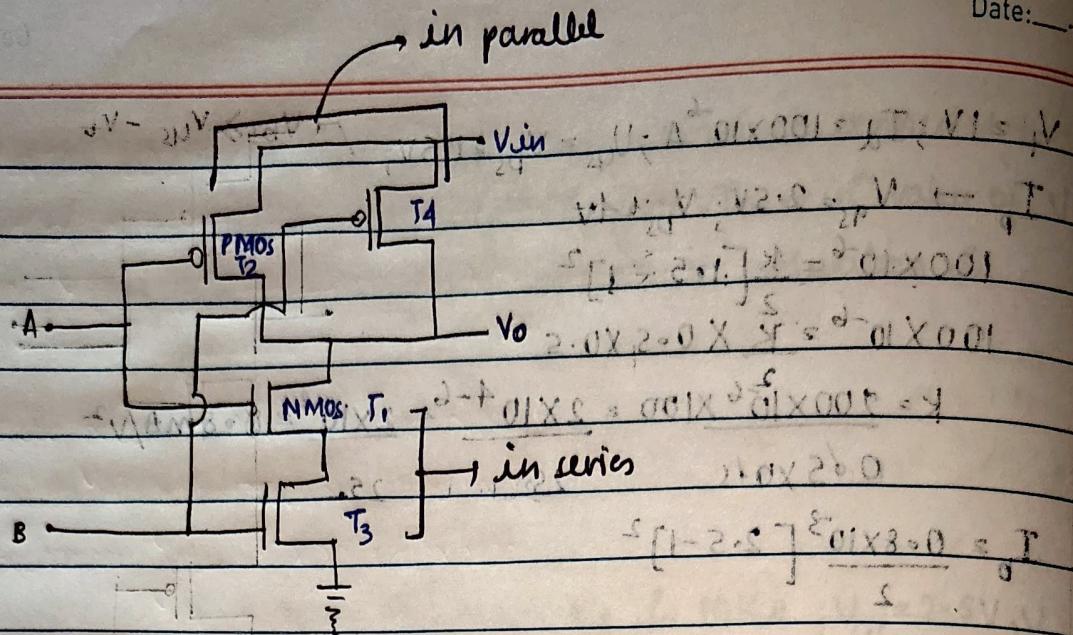


Equivalent circuit

CMOS NAND GATE:

A	B	V_o
0	0	1
0	1	0
1	0	0
1	1	0

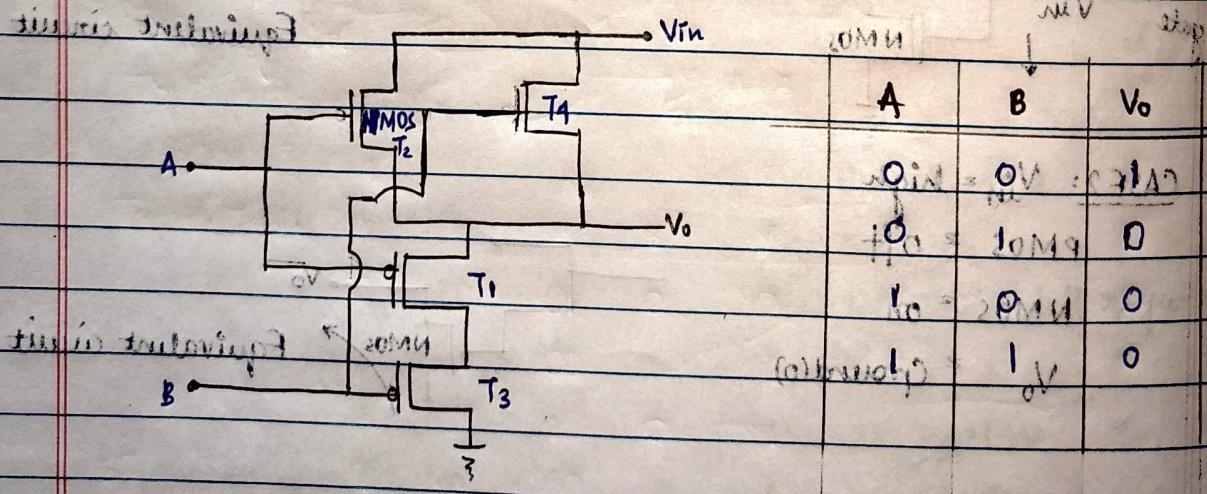




A	B	T ₁	T ₂	T ₃	T ₄	OUTPUT
Low	Low	L(OFF)	H(ON)	L(OFF)	H(ON)	V _{DD}
Low	High	L(OFF)	H(ON)	H(ON)	L(OFF)	V _{DD}
High	Low	H(ON)	L(OFF)	L(OFF)	H(ON)	V _{DD}
High	High	H(ON)	L(OFF)	H(ON)	H(ON)	0.

W/L = 1/2A
f₀ = 20MHz

CMOS NOR GATE:



MOSFET AS AN AMPLIFIER:

9.5

A

1

0

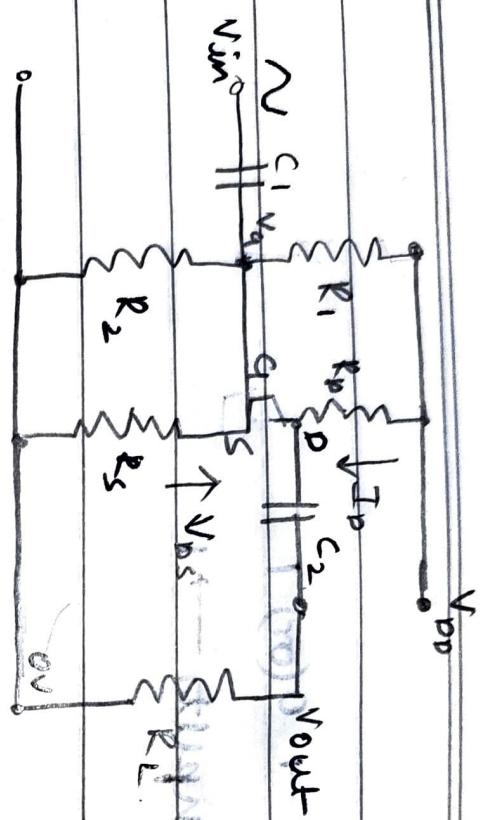
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NMOSFET as an amplifier

100K AND 10K FEEDBACK RESISTORS