



RV Educational Institutions
RV College of Engineering

Autonomous
Institution Affiliated
to Visvesvaraya
Technological
University, Belagavi

Approved by AICTE,
New Delhi

Academic year 2021-2022 (Even Sem)

Go, change the world

AKASHA

DEPARTMENT OF
ELECTRONICS AND COMMUNICATION ENGINEERING

Date	21.11.2023	Maximum Marks	100
Expt. Code	22EC13	Duration	90 Mins
Sem	I	Test-I	

BASIC ELECTRONICS (22EC13)
PHYSICS CYCLE

**CIE - I
SCHEME**

PART B				
1 a)	With the help of a block diagram elaborate on the working of regulated DC power supply	06	L2	CO1
1 b)	A DC Power supply output voltage drops from 15 V to 14.95 V when the ac source voltage falls by 10 %. The output also falls from 15V to 14.97 V when the load current is increased from 0 to maximum, Determine the source effect, load effect line regulation and load regulation	04	L3	CO2
2 a)	With the help of relevant input and output characteristic graphs elaborate on the working of BJT in common emitter configuration mode.	06	L2	CO1
2 b)	How does changes in V_{BE} , I_{CSO} (reverse saturation current) and β , cause the thermal runaway and shift in Q point in BJT? Briefly explain the reason.	04	L3	CO2
3 a)	Explain the working of RC Coupled amplifier and also Elaborate on the frequency response of RC coupled amplifier with relevant diagrams and equations	06	L2	CO1
3 b)	For the CE amplifier shown below in the figure 3.b, calculate R_1 , R_2 , R_F and R_C given that $V_{CC} = 24V$ and $R_L = 120k\Omega$	04	L3	CO2
<p>Figure 3. b) common Emitter Amplifier</p> <p><i>Inverted output</i></p> <p>$Q(V_E, I_E)$</p> <p>$V_{CE} = 0.3$</p>				
4 a)	A transistor circuit has $I_c = 3mA$ and $I_E = 3.03 mA$. Find β_{ac} for transistor used. Assuming no change in base current, find the new collector current when the transistor is replaced with new one with $\beta_{ac} = 70$.	04	L3	CO1
4 b)	The voltage divider bias circuit as shown in figure 4.(b) has $V_{cc} = 15 V$, $R_1 = 6.8 k\Omega$, $R_2 = 3.3 k\Omega$, $R_b = 900 \Omega$, $R_E = 900 \Omega$ and $R_L = 50$, $V_{BE} = 0.7 V$. Determine the levels of V_E , I_B , I_C , V_{CE} . Draw the DC load line and mark Q point on the load line.	06	L3	CO2



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5.a)	An amplifier having a power gain of 20dB delivers a power output of 40W to a load of 2KΩ. Calculate i) the input power needed and ii) the input voltage needed, if the voltage gain of the amplifier is 40dB	04	L3	CO2	
5.b)	With the help of relevant circuit diagram and equations elaborate on r_e . Transistor model.	06	L2	CO2	

Figure 4.(b) Voltage Divider Bias Network

$Z_i = B r_e$ *(problem)*
 $Z_o = r_o$
 $A_v = -r_o / r_e$

Academic year 2023-2024 (Odd Sem)

**DEPARTMENT OF
ELECTRONICS & COMMUNICATION ENGINEERING**

Date	28 th DEC 2023	Maximum Marks	50
Course Code	EC112AT	Duration	90 Min
Sem	I Semester	Test-2	
Basic Electronics			

**CIE - 2
SCHEME**

Sl. No.	Questions PART-B	4	1	1
1.a	An N channel MOSFET having $V_t=1V$ acts as a resistance of 500Ω for small values of V_{DS} , when $V_{GS}=3V$. i) If V_{GS} is changed to 6V, for small values of V_{DS} , what is the resistance offered by the MOSFET ii) When $V_{GS}=V_{DS}=4V$, determine the drain current. iii) Determine the trans conductance when $V_{GS}=V_{DS}=3V$.			
1.b	Draw the circuit diagram and explain the operation of a two input CMOS NOR gate.	4	1	1
2.a	Draw the structure of an N-channel MOSFET and explain its operation. Draw the output characteristics and mark the region of operation.	6	1	2
2.b	An amplifier needs an input voltage of 20mV to give a certain output power to the load. When negative feedback is provided to this amplifier, it needs 820mV to deliver the same power output. If the closed loop voltage gain of the amplifier is 32dB, determine the open loop voltage gain and the feedback factor.	4	2	3
3.a	Write the truth table for SUM and CARRYOUT of a full adder. From the truth table, obtain the expressions for the same and realize the full adder using 2 half adders.	6	2	2
3.b	Prove that gain stability of an amplifier with negative feedback improves by a factor of $(1+A\beta)$ compared to that of the amplifier without feedback, where A is the open loop gain and β is the feedback factor.	4	1	1
4.a	With a neat circuit diagram, illustrate the principle of operation of 3:8 Decoder.	6	2	2
4.b	Simplify the following expressions and realise using basic gates. $Y = A'BC + A'BC' + ABC' + AB'C'$	4	3	3
5.a	Simplify the logic expression using K map and implement the logic circuit using NAND Gate.	6	4	4
	$F = \sum m(0,1,2,3,5,7,8,9,,10,12,13)$			
5.b	Explain the operation of a 4-to-1 Multiplexer and write the logic expressions for its outputs. Also draw the logic circuit using basic gates to realize the Multiplexer.	4	1	1

BT-Blooms Taxonomy, CO-Course Outcomes, M-Marks

Marks Distribution	Particulars		CO1	CO2	CO3	CO4	L1	L2	L3	L4	L5	L6
	Test	Max Marks	12	18	14	6	18	16	10	6	-	-

Academic year 2023-2024 (Odd Sem)

DEPARTMENT OF
ELECTRONICS & COMMUNICATION ENGINEERING

Date	23 rd JAN 2024	Maximum Marks	50
Course Code	EC112AT	Duration	90 Min
Sem	I Semester	Test-3	

Basic Electronics

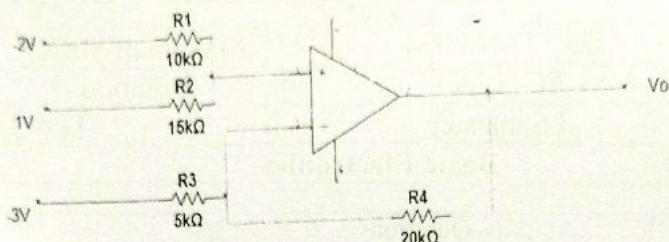
Sl. No.	Questions PART-B	M	BT	CO
1.a	List the characteristics of an ideal op-amp and indicate their typical values for a general purpose commercial op-amp.	4	2	2
1.b	Draw the circuit of an integrator using ideal op-amp & prove that it works as an integrator.	6	2	2
2.a	Draw the summer circuits, using two ideal op amps, and calculate the different resistor values to obtain $V_o = 2V_1 - 4V_2 + 6V_3$, where V_1, V_2, V_3 are the available inputs. Assume the value of feedback resistor as $10\text{ k}\Omega$.			
2.b	List Any 8 differences between Amplitude modulation & Frequency modulation.			
3.a	Draw the circuit of a Schmitt trigger using ideal op-amp and explain its operation along with the input / output waveform & relevant equations. Also draw its transfer characteristics.	6	1	2
3.b	With the help of a general block diagram explain the process in Communication system.	4	1	1
4.a	A non-inverting amplifier has input resistance $10\text{ k}\Omega$ and feedback resistance $60\text{ k}\Omega$ with load resistance $47\text{ k}\Omega$. Draw the circuit diagram & Calculate output voltage, voltage gain & load current when input voltage is 1.5 V .	5	3	3
4.b	Draw the circuit diagram of Instrumentation amplifier & explain its operation.	5	1	1
5.a	A carrier of 1 MHz with 400 W of its power is amplitude modulated with a sinusoidal signal of 2500 Hz . The depth of modulation is 75% . Calculate the sideband frequencies, the bandwidth, the power in the sidebands and the total power in the modulated wave.	5	3	3

**CIE-3
SCHEMES**



5.b

In the circuit shown below, determine the output voltage, V_o . Assume the op amps to be ideal.



5 | 4 | 3

BT-Blooms Taxonomy, CO-Course Outcomes, M-Marks

Marks Distribution	Particulars		CO1	CO2	CO3	CO4	L1	L2	L3	L4	L5	L6
	Test	Max Marks	13	16	15	6	15	14	16	5	-	-

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RV COLLEGE OF ENGINEERING®

(An Autonomous Institution affiliated to VTU)

I / II Semester B. E. Regular / Supplementary Examinations Feb-2024

Common to EC / ET / EI**BASIC ELECTRONICS***Time: 03 Hours**Maximum Marks: 100**Instructions to candidates:*

1. Answer all questions from Part A. Part A questions should be answered in first three pages of the answer book only.
2. Answer FIVE full questions from Part B. Question number 2 is compulsory. Choose any one full question from 3 or 4, 5 or 6, 7 or 8 and 9 or 10.

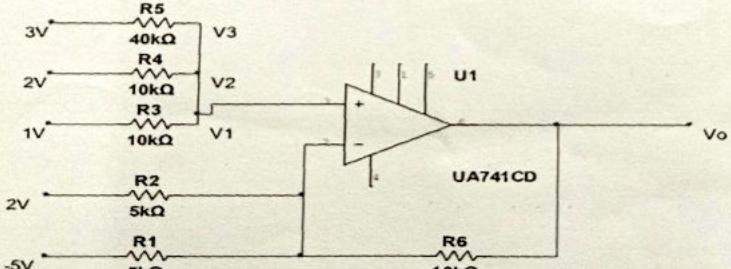
PART-A

1	1.1	A DC power supply has NO load voltage of 30V and a full load voltage of 25V at a full load current of 1A. Calculate the load regulation and its output resistance. <u>20V 25Ω</u> .	02
	1.2	In a NPN transistor, if the base emitter junction is reverse biased and the collector to base junction is reverse biased, the transistor is operating in the <u>Cut-off</u> region.	01
	1.3	An NPN transistor has $I_{co} = 25nA$, $I_B = 0$, $V_{CE} = 4V$ and $I_C = 20\mu A$. The value of β is <u>799</u> .	12 Q1 PET
	1.4	In a voltage divider circuit, for a silicon transistor having $\beta = 49$ has $R_E = 4K\Omega$ and $R_{th} = 60K\Omega$, $S(I_{co}) = \underline{12.3}$.	
	1.5	An amplifier has a voltage gain of 100 at 1kHz. The gain falls by 6dB at 1MHz. If the input is <u>3mW</u> at 2MHz, then the output voltage is _____.	
	1.6	The output of a cascaded chain of four amplifiers is 4V, when the input voltage is 0.5mV. If the voltage gains of the first, third and fourth stages are 28dB, 0dB and 12dB respectively, the voltage gain of the second stage in dB is <u>38.06 dB</u> .	02
	1.7	An N-channel MOSFET, having $V_t = 1V$, is biased such that $V_G = 4V$. The maximum value of V_D allowed, so that the device operates in ohmic region is <u>3V</u> .	01
	1.8	A MOSFET uses the electric field of a _____ to control the channel current. <u>Capacitor/dielectric</u>	01
	1.9	The open loop and closed loop gains of an amplifier are 66dB and 40dB respectively. The amount of negative feedback in dB is <u>26dB</u> .	01
	1.10	An amplifier without feedback has a gain of 100 and a bandwidth of 500kHz. If 5% negative feedback is given, then the bandwidth with feedback is <u>3 MHz</u> .	01
	1.11	$(AB' + AB + A'B) = \underline{A + B}$.	01
	1.12	If any one of the inputs of a EX-NOR gate is always connected to LOW, then the EX-NOR gate behaves as <u>Inverter/NOT gate</u> .	01

	The total number of gates required to implement 64:1 multiplexer is <u>71</u> .	01
1.14	An operational amplifier has a differential gain of 100 and a common mode gain of 0.1. The CMRR in dB is <u>100</u> .	01
1.15	The slew rate of an op amp used as a voltage follower is $5V/\mu s$. If the input voltage is $20\sin(6.28wt)$, the maximum frequency of the input so that the output is not distorted is <u>39.78 kHz</u> .	01
1.16	For an AM signal, the bandwidth is 10kHz and the highest frequency component present is 705kHz. The carrier frequency used for this AM signal is <u>700kHz</u> .	01
1.17	A 400W carrier is modulated to a depth of 75%. Assuming the modulating signal to be sinusoidal the total power in the amplitude modulated wave is <u>512.5W</u> .	01
1.18	A part of the transducer which responds to a change in the physical phenomenon is called <u>sensing/detecting element</u> .	01

PART-B

2	a Draw the block diagram of a DC power supply and explain the function of each block. b In a RC coupled CE amplifier, $R_1 = 90k\Omega$, $R_2 = 10k\Omega$, $R_E = 0.68k\Omega$, $R_C = 2.2k\Omega$, $V_{cc} = 16V$ and $\beta = 210$. Determine Z_i , Z_o and A_v of the transistor. Draw the re model for the same. c Explain the different operating regions of a transistor along with the applications and draw the output characteristics for transistor in common emitter configuration.	04 08 04
3	a With neat diagram explain the structure and working of N-channel enhancement type MOSFET. Draw the plot of I_D versus V_{GS} and I_D versus V_{DS} . Write the current equation at different regions of operation. b An N-channel MOSFET has a threshold voltage $V_t = 0.9V$ and $I_D = 0.75mA$, when $V_{GS} = V_{DS} = 2.5V$. Calculate: i) Drain current, if $V_{GS} = 4.1V$ and $V_{DS} = 4.0V$. ii) Drain to source resistance r_{ds} for small values of V_{DS} , if $V_{GS} = 4.9V$ iii) Trans conductance, g_m , if $V_{GS} = 4.9V$ c Explain the operation of CMOS NAND gate	07 05 04
	OR	
4	a Write the advantages of providing a negative series feedback to a voltage amplifier. b An amplifier has a gain of $60dB$, bandwidth of $30kHz$, distortion of 15% , input impedance of $5k\Omega$ and an output impedance of $1k\Omega$. If voltage series negative feedback of 3.9% is given to this amplifier, calculate the gain, input impedance, output impedance, distortion, bandwidth and amount of feedback for a closed loop amplifier. c Draw the circuit and explain the operation of a two input CMOS NOR gate along with the truth table.	04 06 06

5	a	The four variable function f is given in terms of min-terms as: $f(A, B, C, D) = \sum m(0, 1, 2, 3, 4, 6, 8, 9, 10, 11, 12, 14)$. Using the K -map minimize the function in the sum of products form and realize the expression using only <i>NAND</i> gates.	08
	b	Write the truth table for <i>SUM</i> and <i>CARRYOUT</i> of a full adder. From the truth table, obtain the logic expressions for the same and then realize the full adder using two half adders.	08
		OR	
6	a	A logic circuit has 3 inputs A, B and C and 2 outputs X and Y . Output X is 1, only when any two of the inputs are at 1 and Y is 1, only when any one of the inputs is at 1. Write the truth table and the logic expressions for X and Y . Also realize the logic circuit using basic gates.	08
	b	Explain the operation of 8:1 multiplexer along with the truth table and logic expression. Also draw the logic circuit to realise the multiplexer.	08
7	a	List at least eight important characteristics of ideal op-amp and indicate their typical practical values.	04
	b	Draw the circuit and design the values of different resistors of a summer circuit using 2 ideal op amps to get an output voltage $V_o = V_1 + 3V_2 + 5V_3 - 7V_4 - 9V_5 - 11V_6$ where V_1, V_2, V_3, V_4, V_5 and V_6 are available input voltages.	06
	c	Draw the circuit of a Schmitt trigger using an ideal op amp and explain its operation with necessary waveforms.	06
		OR	
8	a	Draw the circuit of a differentiator using an ideal op amp and derive the expression for the output voltage.	06
	b	Calculate the output voltage for the circuit in Fig. 8.b	
	c		
		Fig. 8.b	
	c	Explain the working of negative comparator with input output waveforms.	06 04
9	a	What is the need for modulation? Write eight differences between AM and FM.	08
	b	Explain the working of a piezoelectric transducer with relevant equations.	08
		OR	

10 a

A carrier signal of $1MHz$ with $400W$ of its power amplitude modulated with a sinusoidal signal of $2500Hz$. The depth of modulation is 75% . Calculate the sideband frequencies, the bandwidth, the power of the sidebands and total power in the modulated wave and sketch the frequency spectrum when amplitude of the carrier signal is $3V$.

08

b

With the help of a neat diagram, discuss the working principle of *LVDT*.

08



CIE I

Academic year 2022-2023 (Odd Sem)

DEPARTMENT OF
Electronics and Communication Engineering

Date	18/01/2023	Maximum Marks	60
Course Code	22EC13	Duration	120 Mins
Sem	I Semester	CIEI	

BASIC ELECTRONICS

Instructions to candidates:

- Part A must be answered within the first two pages of manuscript
- Assume the suitable data for missing values

PART-A

	M	BT	CO
1 The output characteristics of CB configuration exhibits variation in I_C due to variation in V_{CB} by maintaining _____ constant.	1	1	1
2 The current gain α of a transistor with $I_C = 5 \text{ mA}$ and $I_B = 100 \mu\text{A}$ is _____.	1	2	1
3 An NPN transistor has $I_{CO} = 25\text{nA}$, $I_B = 0$, $V_{CE} = 4\text{V}$ and $I_E = 20\mu\text{A}$. The value of β is _____.	2	3	2
4 In a voltage divider circuit for a silicon transistor having $\beta=49$ has $R_F = 4\text{K}\Omega$ and $R_{BE} = 60\text{K}\Omega$, then $S(I_{CO}) =$ _____.	1		
5 If a PNP transistor is operating as an open switch, its base emitter junction is biased.	1		
6 In an NPN transistor if $V_B = 3\text{V}$, $V_E = 2\text{V}$, $V_C = 1\text{V}$, the transistor is operating in region.	1	2	2
7 Three voltage amplifiers are cascaded to provide an overall gain of 10000. The first and the last stages have gains of 28dB and 20dB, then the gain of middle stage is _____.	2	3	4
8 The lower cut off frequency of an RC coupled amplifier is 400Hz. It has a voltage gain of 80 at 400Hz and has a bandwidth of 30KHz. The mid frequency gain of the amplifier is _____.	1	3	3

CIE Q1
SCHE

PART-B

1a	Draw the block diagram of a regulated DC power supply and explain the function of each block.	5	1	1
1b	For the bias circuit shown in the Fig.1b, Find the value of V_{CC} , R_B and β .	5	3	3

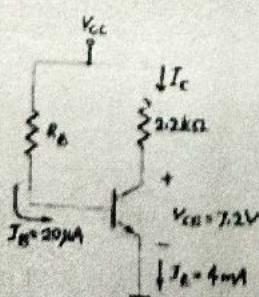


Fig. 1b

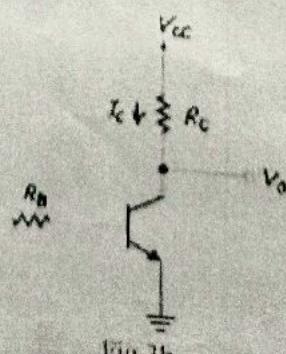


Fig. 3b



2a	Draw the input and output characteristics of a BJT in Common Emitter Configuration and briefly explain three regions of operation.	6	2	2
2b	An amplifier has a voltage gain of 200 at 1KHz. The gain falls by 6dB at 1MHz. If the input is a 2mV signal at 1MHz frequency, calculate the output voltage of an amplifier.	4	2	2
3a	Draw the circuit diagram of single stage RC coupled common emitter amplifier and explain the purpose of each component used. Also, sketch the frequency response.	5	2	1
3b	For the circuit shown in Fig.3b, $V_{CC}=10V$, $R_B=10K\Omega$, $R_C=1K\Omega$ and $\beta=50$. Find the value of V_{BB} so that BJT can be used as a switch.	5	3	4
4a	Explain Early effect and Thermal run-away in a BJT.	4	1	1
4b	Find the operating point of a silicon NPN transistor using voltage divider bias circuit for the following bias conditions: $R_1=150K\Omega$, $R_2=50K\Omega$, $R_E=3K\Omega$, $R_C=1K\Omega$, $\beta=100$, $V_{CC}=18V$.	6	3	4
5a	For the amplifier circuit shown in Fig.5a, draw the re-model and calculate input impedance Z_i , output impedance Z_o and voltage gain A_v .	6	3	3

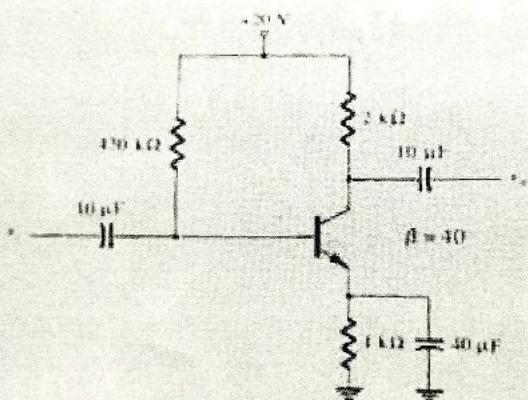


Fig. 5a

5b) Three amplifiers of voltage gains 18dB, 24dB and 40dB are cascaded to obtain the output voltage of 4V. Calculate the input voltage needed at every stage.

BT-Blooms Taxonomy, CO-Course Outcomes, M-Marks



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Semester: I
CIE 2

Course: Basic Electronics

Duration: 2 Hrs

Course Code: 22EC13

Date:

Maximum Marks: 50

Sl.No	PART-A	M	BT	CO
1	The bandwidth of an amplifier with negative feedback increase by a factor of $1 + AB$	1	1	1
2	If the amplifier gain in open loop is 46dB with 8% distortion. Find feedback factor if distortion is reduced to 2%. 1.5^4	1	3	2
3	An amplifier having open loop gain of 60dB and closed loop gain of 40dB. The amount of feedback in dB is $20dB$	1	2	3
4	An N channel enhancement MOSFET with a threshold voltage $V_t=2V$, has its source voltage, $V_s=3V$. If its gate voltage, $V_G=7V$, the minimum drain voltage, V_D , needed so that the device operates in saturation is $5V$	1	3	3
5	If any one of the inputs of an EX-NOR gate is always connected to HIGH, then the EXNOR gate behaves as <u>buffer</u>	1	2	2
6	In a 3 variable K-map, if all the cells contain 1's then the output is <u>1</u>	1	2	2
7	$B' + AB = B' + A$	1	2	3
8	MOSFET can be operated as amplifier in <u>saturation</u> region.	1	1	1
9	An N channel MOSFET with $V_t=1V$, $K=2mA/V^2$ has $V_{gs}=V_{ds}=4V$. The drain current of the transistor is $9mA$	1	3	3
10	The minimum number of NAND gates required to realize Half adder is <u>5</u>	1	2	2

Q. No		PART-B	M	BT	CO
1.	a.	Draw the structure and explain the operation of an N-channel enhancement type MOSFET. Draw its output characteristics and indicate three regions of operation.	06	2	1
	b.	Write any EIGHT differences between BJT and FET.	04	1	1
2.	a.	An amplifier has an open loop gain of 8000, input resistance=100kΩ, output resistance=10kΩ, distortion=15%, gain stability=20%, bandwidth=500kHz and noise=1μV. By giving suitable negative feedback the resistance needs to be increased to 2.2MΩ. Determine the feedback factor required. Also determine the gain, the output resistance, distortion, gain stability, bandwidth and noise of the closed loop amplifier.	06	3	3
	b.	Prove that the stability of the gain of an amplifier improves with negative feedback by a factor, $(1+A\beta)$, where A is open loop gain of the amplifier and β is the feedback factor. $\frac{dA_f}{A_f} = (1+A\beta)(1+1/\beta)$	04	1	2
3.	a.	An N channel MOSFET having $V_t=1V$ acts as a resistance of 500Ω for small values of V_{DS} , when $V_{GS}=3V$. i) If V_{GS} is changed to 6V, for small values of V_{DS} , what is the resistance offered by the MOSFET ii) When $V_{GS}=V_{DS}=4V$, determine the drain current. iii) Determine the trans conductance when $V_{GS}=V_{DS}=3V$.	06	3	4
	b.	Draw the circuit of a 2-input CMOS NAND gate and explain its working.	04	2	2
4.	a.	Starting from the logic expression, realize XNOR gate using minimum number of NAND gates.	04	3	3
	b.	Simplify the logic expression using K-map and implement the logic circuit using basic gates. $F(a,b,c,d)=\sum m(0,1,2,3,4,6,8,9,10,11,12,14)$	06	4	3
5.	a.	Write the truth table for SUM and CARRYOUT of a full adder. From the truth table, obtain the expressions for the same and realize the full adder using 2 half adders.	06	4	4
	b.	Simplify the following expressions using Boolean Algebra i) $Y=(A+B'+C')(A+B+C) = A+B'$ ii) $Y=AB+A'C+BC = AB + A'C$	04	3	3

BT-Blooms Taxonomy, CO-Course Outcomes, M-Marks

Marks Distribution	Particulars		CO1	CO2	CO3	CO4	L1	L2	L3	L4	L5	
	Quiz	Max Marks	2	4	4	-	2	5	3	-	-	
	Test	Max Marks	10	8	20	12	8	10	20	12	-	-

$$1+A\beta = 22 - 1$$

$$\beta = 0.2625\% - 0.5$$

$$\text{gain } A_f = 363 \cdot 63 = 51.21 \text{ dB} - 1$$

$$Z_{df} = 454.5 \text{ k}\Omega - 0.5$$

$$D_f = 0.681\% - 0.5$$

$$\frac{dA_f}{A_f} = 0.101\% - 0.5$$

$$\frac{A_f}{B_N} = 11 \text{ MHz} - 1$$

$$N_f = 0.045 \mu\text{V} - 1$$



Improvement
Test

Academic year 2022-2023 (ODD Sem)

DEPARTMENT OF
ELECTRONICS & COMMUNICATION ENGINEERING

Date	21-03-2023	Maximum Marks	60
Course Code	22EC13	Duration	110 Min
Sem	II Semester	Improvement Test	
Basic Electronics			

Sl. No.	Questions	M	BT	CO
1.	In a 3 to 8-line Decoder, with X_0 to X_3 as the inputs and Y_0 to Y_7 as the outputs, what should be the input code, so that Y_5 is HIGH and all other outputs are LOW.	1	1	1
2.	The output signal of an op-amp with slew rate of $2V/\mu s$ has a maximum amplitude value of 5V. Then the maximum frequency for undistorted output voltage is	1	1	3
3.	The circuit shown in Fig.1 uses 2:1 MUX works as _____ logic gate.	1	3	2
	 Fig.1			
	 Fig.2			
4.	An AM transmitter is $S(t) = 100(1 + 0.5\cos(31400t))\cos(6.28 \times 10^6 t)$ the frequencies of sidebands are _____ KHz and _____ KHz.	1	1	3
5.	An op amp has a differential gain of 2×10^4 and a CMRR of 86dB. Determine the output, if the differential input is $10\mu V$ and the common mode input is $10mV$.	2	2	3
6.	In the circuit shown in Fig. 2 $V_{CC} = 12V$ and $V_{EE} = -12V$, the output voltage Vo is = _____.	2	2	3
7.	List any 2 ideal characteristics of an op amp and compare the values with practical op amp.	2	1	3

PART-B

Sl. No.	Questions	M	BT	CO
1a	Explain the operation of 8:1 multiplexer with necessary truth table, logic expression and logic circuit.	6	1	2
1b	Explain the operation of 2 to 4 decoder with necessary truth table and logic expression.	4	1	2
2a	For the circuit shown in Fig 2a, Calculate output voltage at V_1 , V_2 and Vo . (Assume ideal op amps)	6	4	4

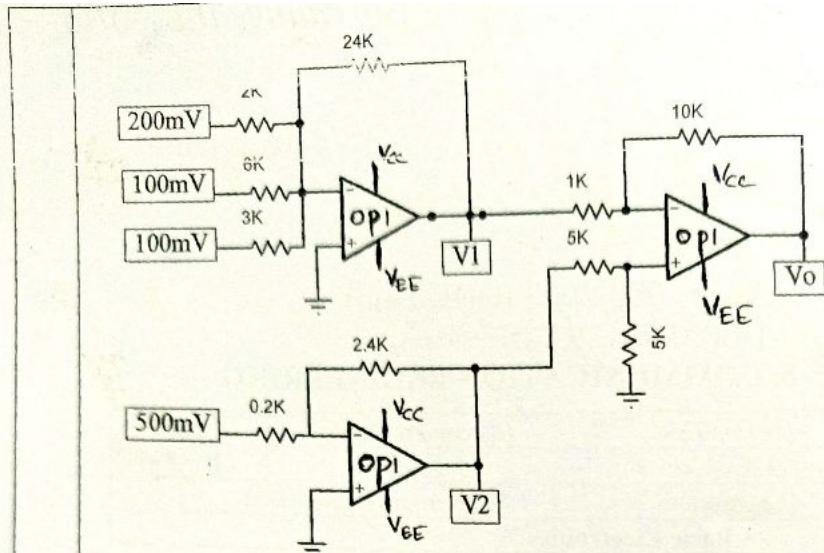


Fig.2a

2b	Draw the circuit of the Schmitt trigger and explain the operation of the circuit with neat waveforms.	4	2	3
3a	Design a summing amplifier to obtain V_o $V_o = 3V_1 + 4V_2 - 6V_3 - 8V_4 + 10V_5 - 12V_6 - 9V_7$ Assume that all the available inputs are positive.	6	4	4
3b	Draw the circuit of the Integrator and explain the operation of the circuit with neat waveforms.	4	2	3
4a	Given a signal $m(t) = A \sin 2\pi ft$ where $A=10\text{mV}$ and f is 1 KHz. Using Ideal Op-amps design the electronic circuitry required to generate an amplified sinusoidal signal $C_1(t) = 5\sin(2\pi ft)$ w.r.t $m(t)$. Also draw the designed circuit diagram:	6	4	4
4b	Draw the circuit of the Instrumentation amplifier and Derive the expression of Output voltage.	4	2	2
5a	The output voltage of an AM transmitter is given by $V_{AM}(t) = 200(1 + 0.4 \cos 12566.4t) \cos 6.283 \times 10^7 t$. Determine i) f_c and f_m iv) Sideband frequencies ii) Bandwidth v) Modulation index iii) Amplitude of the sidebands vi) The total power, if the load resistance is 10Ω .	6	2	1
5b	Write eight differences between AM and FM.	4	1	1

Marks Distribution	Particulars		CO1	CO2	CO3	CO4	L1	L2	L3	L4	L5	L6
	Test	Max Marks	10	14	08	5	5	26	14	-	-	-



RV COLLEGE OF ENGINEERING®
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I / II Semester B. E. Fast track Examinations Jan/Feb - 2023
Common to all Branches
ELEMENTS OF ELECTRONICS ENGINEERING

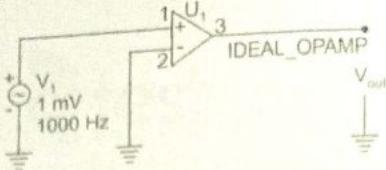
*Time: 03 Hours**Maximum Marks: 100**Instructions to candidates:*

1. Answer all questions from Part A. Part A questions should be answered in first three pages of the answer book only.
2. Answer FIVE full questions from Part B. In Part B question number 2, 7 and 8 are compulsory. Answer any one full question from 3 and 4 & one full question from 5 and 6.

PART-A

1	1.1	The reverse saturation current of a silicon diode is $2nA$ at $45^\circ C$. The reverse saturation current at $95^\circ C$ is ____.	01
	1.2	The ripple factor of a $50Hz$ full wave rectifier supplying a load of 470Ω in parallel with a capacitor of $307\mu F$ is ____.	01
	1.3	The maximum frequency at which a PN junction diode could be used as a Switch is limited by its ____.	01
	1.4	In a full wave bridge rectifier without any filter capacitor, using identical diodes with a forward resistance of 50Ω and the load resistance is 900Ω , the rectification efficiency is ____.	01
	1.5	In a transistor if β changes from 49 to 499, then α changes from ____ to ____.	01
	1.6	For an NPN transistor $V_E = 0.8V$, $V_B = 0.7V$ and $V_C = 0.7V$. The transistor is Operating in ____ region.	01
	1.7	The gain of RC coupled amplifier decreases at high frequencies because of ____.	01
	1.8	The open loop and closed loop gains are $100dB$ and $60dB$ respectively. The amount of feedback in dB= ____.	01
	1.9	MOSFET is a ____ Controlled device.	01
	1.10	An N channel enhancement MOSFET having $V_t=0.5V$, $K=2mA/V^2$ is biased such that $V_{gs}= 2V$ and $V_{ds}= 1V$, its $I_D=$ ____.	01
	1.11	In an AM system, the modulating frequency is $10KHz$ and the modulation is 0.9. The required bandwidth is ____.	01
	1.12	The total power delivered by an AM wave is $2640Watts$. If the modulation index=0.8, the power in each side band= ____.	01
	1.13	The minimum number of NAND gates required to realize XNOR gate is ____.	01
	1.14	The number of inputs is ____ than the number of outputs in a decoder.	01
	1.15	Draw the logic circuit to realize AND function using minimum number of NOR gates only.	02

1.16 What is the value of V_{out} of the following circuit given $V_{sat}=12V$?



1.17 A unity gain amplifier is also known as _____.

1.18 The output signal of an op-amp with slew rate of $3V/\mu sec$ has a maximum output of 20V. The maximum frequency at which the output is a faithful reproduction of the input is equal to _____.

02
01
01

PART-B

2 a Write the Shockley's diode current equation and plot the diode characteristics. From this equation, obtain the expression for the dynamic resistance r_d of the diode. 05

b A full wave bridge rectifier using ideal diodes is supplied from the secondary of a 10:1 transformer, whose primary is connected to 220V, 50Hz main supply. The output of the rectifier is connected to a load resistance of 220Ω in parallel with a capacitor filter C. Calculate the value of C required so that the ripple factor is 3%. Also determine:

- The dc output voltage
- The peak to peak ripple voltage
- The load regulation

c In a Zener regulator circuit, design the value of R so that circuit performs satisfactorily under all the given conditions. Given $P_d(\max)=6W$
 $I_{z\min}=10mA$, $V_z=12V$
 V_{in} varies from 22V to 28V
 R_L varies from 50Ω to 500Ω . 06

3 a Determine the operating point of the voltage divider biasing circuit of a silicon transistor shown in fig 3a. 06

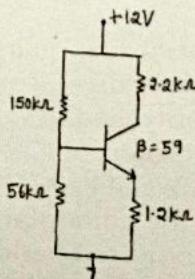


Fig 3a

b Explain the different operating regions of a transistor along with the applications and draw the output characteristics for transistor in CE configuration. 05

c An amplifier has a gain of 60dB, bandwidth of 30KHz, distortion of 15%, input impedance of $5K\Omega$ and an output impedance of $1K\Omega$. If voltage series negative feedback of 3.9% is given to the amplifier, calculate the gain, input impedance, output impedance, amount of feedback, bandwidth and distortion of the amplifier with negative feedback. 06

OR

4	a	In a common emitter amplifier, the transistor used has a $\beta=99$ and the dc emitter current, $I_E=2\text{mA}$, $R_1 = 10\text{K}\Omega$, $R_2 = 5\text{K}\Omega$ and $R_C = 2\text{K}\Omega$. Find the voltage gain, input impedance and output impedance and also draw the r_e model.	06
	b	Prove that gain stability of an amplifier with negative feedback improves by a factor of $(1+A\beta)$ compared to that of the amplifier without feedback, where A is the open loop gain and β is the feedback factor.	
	c	An amplifier needs an input voltage of 20mV to give a certain output power to the load. When negative feedback is provided to this amplifier, it needs 820mV to deliver the same power output. If the closed loop voltage gain of the amplifier is 32dB , determine the open loop voltage gain and the feedback factor.	
5	a	List out eight differences between BJT and MOSFET.	04
5	b	A carrier of 2MHz has 1kW of its power amplitude modulated with a sinusoidal signal of 2KHz . The depth of modulation is 60% . Calculate the sideband frequencies, the signal bandwidth, the power in the sidebands and the total power in the modulated wave.	06
	c	Explain the structure and operation of an N- channel enhancement MOSFET with a suitable diagram along with its output characteristics.	06
		OR	
6	a	Draw the circuit diagram and explain the operation of a two input CMOS NOR gate.	06
	b	An n-channel MOSFET has $V_t = 0.5\text{V}$ and drain current of 0.25mA when $V_{gs} = V_{ds} = 3\text{V}$. Find: (i) Drain current if $V_{gs} = 4\text{V}$ and $V_{ds} = 4.5\text{V}$. (ii) r_{ds} if $V_{gs} = 5\text{V}$ assuming V_{ds} to be very small. (iii) If the MOSFET is used as Common source amplifier with Drain resistance of $12\text{K}\Omega$, determine the voltage gain of the amplifier when $V_{gs}=6\text{V}$.	05
	c	Draw the block diagram of communication system and explain the function of each block	05
7	a	Write the truth table for the SUM and CARRY OUT of a full adder. From the truth table, obtain the logic expressions. From the logic expressions, realize full adder using two half adders.	06
7	b	Explain the operation of 1:4 demux with necessary truth table, logic expression and logic circuit.	05
	c	Simplify the following expression using 4-variable K-map and realize using basic gates. $f(a,b,c,d)=\Sigma(4,6,12,13,5,7,10)$	05

8 a

In the circuit of fig 8a, determine the output voltage V_o , assume the op-amp to be ideal.

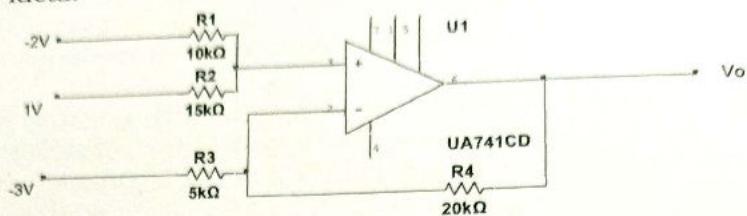


Fig 8a

b

Draw the circuit and calculate the values of different resistors of a summer circuit using two ideal op-amps to get $V_o = 2V_1 - 4V_2 + 6V_3$, Where $+V_1, +V_2, +V_3$ are the three available inputs.

c

Draw the circuit of a differentiator using an ideal op-amp and prove that it works as a differentiator.

06

05

05

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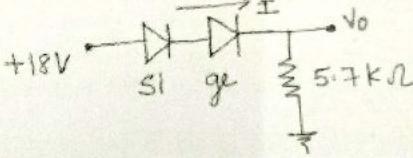
(An Autonomous Institution affiliated to VTU)

I / II Semester B. E. Regular / Supplementary Examinations Oct/Nov-2022

ELEMENTS OF ELECTRONICS ENGINEERING**COMMON TO ALL BRANCHES***Time: 03 Hours**Maximum Marks: 100**Instructions to candidates:*

1. Answer all questions from Part A. Part A questions should be answered in first two pages of the answer book only.
2. Answer FIVE full questions from Part B. In Part B question number 2 is compulsory. Answer any one full question from 3 and 4, 5 and 6, 7 and 8, 9 and 10.

PART A

1	1.1	The diffusion capacitance of a forward biased diode _____ with increase in forward current.	01
	1.2	The forward voltage of a diode with certain forward current at 55°C is 550mV. The forward voltage of the diode at same current at 35°C is _____.	01
	1.3	The filter capacitor used across the load of a rectifier circuit helps to decrease the output _____.	01
	1.4	In the circuit shown in figure 1.4, the diode current I is _____.	01
			
	1.5	Figure 1.4 In a transistor, if β changes from 99 to 999, then α changes from _____ to _____.	01
	1.6	For an NPN transistor $V_E = V_B = V_C = 0.7$, the transistor is operating in _____ region.	01
	1.7	The output voltage of a cascaded chain of three voltage amplifier is 2V. when the input is 0.5mV. If the gains of the first and the third stages are 28dB and 18dB respectively. The gain of the second stage is _____.	01
	1.8	The open loop and closed loop gains of the amplifier are 60dB and 38dB respectively. The amount of negative feedback is _____.	01
	1.9	MOSFET can be operated as amplifier in _____ region.	01
	1.10	An N-channel MOSFET with $V_t = 1V, K = 2mA/v^2$ has $V_{gs} = V_{ds} = 4V$. The drain current of the transistor is _____.	01
	1.11	The total power derived by an amplitude modulated wave is 2640 watts. If the modulation index = 0.8, the power in each sideband is _____.	01
	1.12	An amplifier has bandwidth of 45 KHz and the upper cut off frequency as 45.5 KHz. The lower cut off frequency is equal to _____.	01
	1.13	$\bar{B} + AB =$ _____.	01
	1.14	The minimum number of NAND gates required to realize Half adder is _____.	01

1.15 In the multiplexer circuit shown in figure 1.15, the output $Y =$

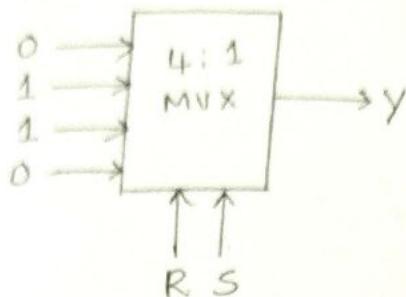


Figure 1.15

1.16 In a 4-variable k-map if all the cells contain 1's then the output is _____.

1.17 The CMRR of an opamp is 92dB. If its common mode gain = -6dB, then differential gain = _____.

1.18 The output of a comparator generates _____ wave.

1.19 The opamp has a common mode gain of 10 and CMRR of 106 dB. If the differential input is $0.5\mu V$ and the common mode input is $10mV$ the output voltage is _____.

1.20 The maximum operated frequency of an opamp is limited by its _____.

PART B

2 a Write the equation that represents V-I characteristics of a PN junction diode and discuss the temperature effects along with the graph. 05

b A full wave bridge rectifier drives a resistance of 270Ω in parallel with a filter capacitor, C . If ac input to the rectifier is $150\sin 628t$, calculate the capacitor value needed so that the ripple factor is 2%. Determine the following:

- (i) output dc voltage
- (ii) peak to peak ripple voltage
- (iii) The load regulation

c In the Zener regulator circuit of figure 2c, calculate the value of R so that the regulator performs satisfactorily for the given input voltage and load resistance variations. 05

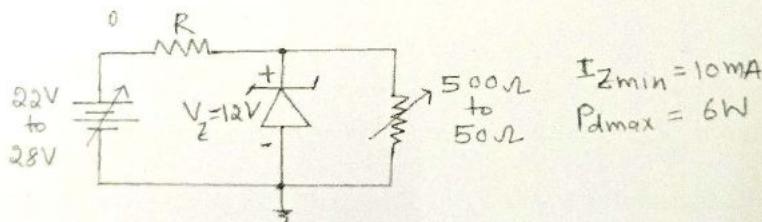


Figure 2c

3 a Mention any six advantages of negative feedback. 04

b Determine the minimum value of β required in the circuit of 3b, so that silicon transistor is in saturation.

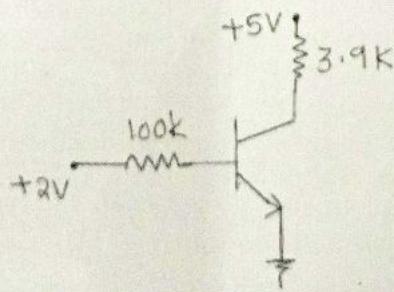
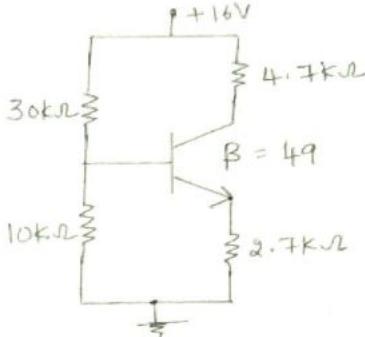
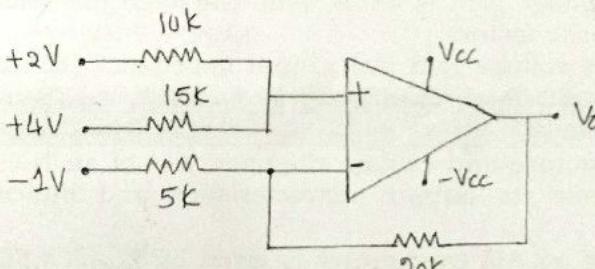


Figure 3b.

	c d	Explain the terms Early effect of thermal run Auray. Determine the operating point (V_{CE} , I_C) of the silicon transistor in the circuit of figure 3d.	•4
			•4
		Figure 3d	•4
		OR	
4	a b c d	Prove that the stability of the gain A_f of an amplifier with negative feedback improves by a factor of $(1+A\beta)$, compared to that of the amplifier without feedback, where A is the gain of the amplifier without feedback and β is the feedback factor. Draw the frequency response of an RC coupled amplifier and explain the effect of capacitors. An amplifier requires an input of 15mV to produce a certain output. To get the same output with negative feedback, the required input signal is 330mV. The closed loop voltage gain is 34dB. Find the open loop voltage gain of the amplifier and the feedback factor. Determine the voltage gain (A_v), Input impedance (Z_i) and output impedance (Z_o), Given : $R_1 = 10K\Omega$, $R_2 = 30K\Omega$, $\beta = 99$, $R_C = 2K\Omega$, $R_L = 4K\Omega$ and $I_C = 2mA$,	04 04 04 04
5	a b c	Draw the structure and explain the operation of an N-channel enhancement type MOSFET. Draw its output characteristics and indicate the three regions of operation. The output of an AM transmitter is given by $V_{AM}(t) = 50(1 + 0.6\cos 12560 t) \sin 628 * 10^4 t$. Determine, (i) The sideband frequencies (ii) Modulation index and bandwidth An n-channel MOSFET has $V_t = 1V$ and drain current $I_D = 1mA$ when $V_{gs} = V_{ds} = 3.5V$. Calculate, (i) Drain current if $V_{gs} = 3V$, $V_{ds} = 1.5V$ (ii) Drain to source resistance r_{ds} for small values of V_{ds} (iii) Transconductance $V_{gs} = V_{ds} = 4V$	06 04 06
		OR	
6	a b c	Draw CMOS NOR gate and explain its working. Given $V_t = 1V$, $V_{gs} = 2V$, $V_{ds} = 3V$, $K = 1.5mA/V^2$ and $R_d = 20K$. Calculate Transconductance (g_m) and voltage gain (A_v). Draw the block diagram of a communication system and explain each block.	06 05 05
7	a	Write the truth table for SUM and CARRYOUT of a half adder. From the truth table, obtain logic expression for the same and realize the half adder using minimum number of NAND gates.	06

	b	Explain the operation of 2:4 decoder and write the logic expressions for its outputs. Also draw the logic circuit to realize the decoder.	04
	c	Simplify the following Boolean expressions (i) $Y = (A + \bar{B} + C)(\bar{A} + B + C)(A + B)$ (ii) $Y = XY + XYZ + XY\bar{Z} + \bar{X}YZ$	06
		OR	
8	a	Explain the operation of 8:1 multiplexers with necessary truth table, logic expression and realize the same using basic gates.	06
	b	List any eight differences between RISC and CISC.	04
	c	Simplify the logic expression given below using Karnaugh map and realize the simplified expression using basic gates. $Y = \Sigma(0,1,4,5,7,10,11,13,14,15)$	06
9	a	List eight characteristics of opamp along with their ideal and typical values.	04
	b	Draw a circuit and calculate the values of different resistors of a summer circuit using two ideal op-amps to get $V_0 = 2V_1 - 4V_2 + 6V_3 - 8V_4$ where $+V_1, +V_2, +V_3, +V_4$ are the four available inputs.	06
	c	Draw the circuit of an instrumentation amplifier using three ideal op-amps and derive the expression for differential gain considering the condition $\frac{R_2}{R_1} = \frac{R_4}{R_3}$	06
		OR	
10	a	In the circuit of figure 10a, determine the output voltage V_o .	
			
		Figure 10a	
	b	Draw the circuit of an integrator using an ideal opamp and prove that it works as an integrator.	06
	c	Draw the circuit of a Schmitt trigger using an ideal opamp and explain its functioning with suitable waveforms.	05



DEPARTMENT OF
Electronics and Communication Engineering

Date	01/07/2022	Maximum Marks	60
Course Code	21EC25	Duration	120 Mins
Sem	II Semester	CIE1	

ELEMENTS OF ELECTRONICS ENGINEERING

Instructions to candidates:

- Part A must be answered within the first two pages of manuscript.
- Assume the suitable data for missing values

CIE / QP

PART-A

1	The diffusion capacitance of a forward biased diode _____ with decrease in the forward current.	1	1	1
2	The maximum frequency at which a PN-junction diode could be used as a switch is limited by its _____.	1	3	2
3	A Germanium diode has its maximum power dissipation of 1W at 50°C, with a de-rating factor of 25mW/°C. The power dissipation at 45°C is in Watt is _____.	1	2	3
4	The forward resistance of each diode in a full wave bridge rectifier is 50Ω the load resistance is 2KΩ. The load regulation of the rectifier in % is _____.	1	2	2
5	For the circuit shown in the Fig.1, V=_____ Volts. Assume a practical Silicon diode.	1		

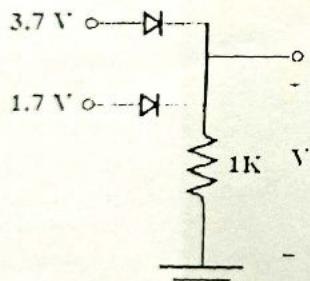


Fig. 1

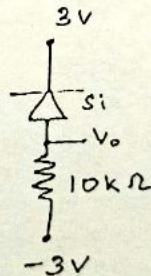


Fig. 2

6	In the given circuit in Fig.2, the diode is in _____ biasing state.	1	1	2
7	In a voltage divider circuit for a silicon transistor having $\beta=49$ has $R_E=4K\Omega$ and $R_{th}=60K\Omega$, $S(I_{co})=$ _____.	1	1	4
8	If a PNP transistor is operating as a open switch, its base emitter junction is _____ biased.	1	2	3
9	For an NPN transistor, if $I_{co}=4\mu A$, $I_B=0$, $V_{CE}=4V$ and $I_C=100\mu A$, then the value of β is _____.	1	3	4
10	In an NPN transistor if $V_B=3V$, $V_E=2V$, $V_C=1V$, the transistor is operating in _____ region.	1	3	2

PART-B

1.a	With the help of Schokley's equation draw the V-I characteristics of a PN junction diode and explain the changes in the characteristics with respect to the variation in temperature.	6	1	1
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Academic year 2021-2022 (Even Sem)

- b In the circuit shown in Fig.1b, determine the output ac voltage V_0 . Assume the temperature to be 27°C , $R1=2\text{K}\Omega$ and all the diodes are Si diodes.

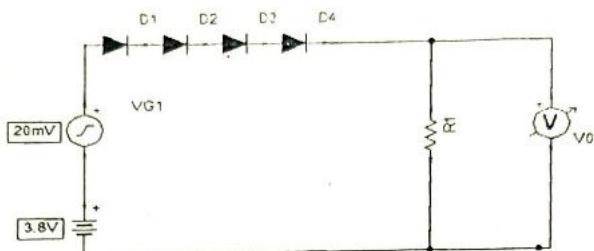


Fig. 1b

- 2a In a voltage regulator circuit design a value of source resistance R , so that the regulator operates satisfactorily for the given operating conditions. Assume fixed input and varying load conditions.

$V_{in}: 18\text{ V}$

R_L: 60Ω to 100 Ω

I_{ZMIN}: 10mA

P_{DZMAX}; 3W

Vo : 9V

- 2b Draw the block diagram of a regulated DC power supply and explain the function of each block.

- 3a Write the input, output waveforms of bridge rectifier with filter and derive the expression for i) Ripple factor ii) DC output voltage.

- b A full wave bridge rectifier drives a load resistance of 150Ω in parallel with a filter capacitor C . If the input to the rectifier is $150V$ at $100Hz$, calculate the quality factor.

- capacitor, C . If the ac input to the rectifier is 150V at 100Hz, calculate the capacitor value needed so that the ripple factor is 2%. Determine the output dc voltage, peak to peak ripple voltage and the load regulation.

- 4a Briefly explain the three regions of operation of a BJT. Draw and explain the input and output characteristics of a BJT in Common Emitter Configuration.

- b Find the operating point of a silicon NPN transistor using voltage divider bias circuit for the following bias conditions: $R_1=47\text{K}\Omega$, $R_2=10\text{K}\Omega$, $R_C=4.4\text{K}\Omega$, $R_E=1\text{K}\Omega$, $\beta=100$, $V_{CC}=12\text{V}$.

- 5a A 220V, 60Hz ac supply is connected to a full wave bridge rectifier through 5:1 transformer. The forward resistance of each diode used is 3Ω and the load resistance is 80Ω . Find i) DC load current ii) DC output voltage iii) RMS load current iv) Rectification efficiency v) Ripple factor.

- 5b Explain Early effect and thermal run-away in a BJT.

BT-Blooms Taxonomy, CO-Course Outcomes, M-Marks												
Marks Distribution	Particulars		CO1	CO2	CO3	CO4	L1	L2	L3	L4	L5	L6
	Test	Max Marks	12	9	16	14	18	14	28	-	-	-

* * * * *



Academic year 2021-2022 (Even Sem)

DEPARTMENT OF
ELECTRONICS & COMMUNICATION ENGINEERING

Date	19-08-2022	Maximum Marks	60
Course Code	21EC25	Duration	110 Min
Sem	II	CIE-2	

ELEMENTS OF ELECTRONICS ENGINEERING

Note: Part A should be answered in first two pages of answer scripts only.

PART A					
Sl. No.	Questions	M	BT	CO	
1.	For the proper operation of transistor as an inverter, the operating point should switch from _____ to _____ region.	1	2	2	-
2.	An amplifier has a voltage gain of 200 at 1KHz. The gain falls by 6dB at 1MHz. If the input is a 2mV signal at 1MHz frequency, the output voltage of amplifier is _____.	2	2	2	
3.	Three voltage amplifiers are cascaded to provide an overall gain of 30000. The first and the last stages have gains of 30dB and 20dB, then the gain of middle stage is _____ dB.	1	2	2	
4.	Enlist any two technical advantages of the negative feedback.	1	1	1	
5.	The open loop and closed loop gains of an amplifier are 62dB and 30dB respectively, the amount of negative feedback in dB is _____.	1	1	1	
6.	For N-Channel MOSFET, VS=3V and Vt=2V and VG=7V, the minimum value of VD required so that the device operates in saturation region is _____.	1	1	1	
7.	Number of MOSFETs required to realize 3 input CMOS NAND gate are _____.	1	1	1	
8.	The gain of RC coupled amplifier decreases at higher frequencies because of _____.	1	1	1	
9.	The final simplified expression for the function $AB + \bar{A}C + BC =$ _____	1	1	2	



Academic year 2021-2022 (Even Sem)

PART B

Sl. No.	Questions	M	BT	CO
1.a	Draw the circuit diagram of single stage RC coupled common emitter and explain the purpose of each component used. Also sketch a graph showing the frequency response of the amplifier.	5	1	1
1.b	In a common emitter amplifier, the transistor used has a $\beta=99$, $I_E=2\text{mA}$, $R_I=10\text{K}\Omega$, $R_2=5\text{K}\Omega$ and $R_C=2\text{K}\Omega$. Find the voltage gain, input impedance and output impedance.	5	3	3
2.a	Compare and contrast any six technical differences between BJT and MOSFET.	4	3	2
2.b	An amplifier has a gain of 60dB, bandwidth of 30KHz, distortion of 15%, input impedance of $5\text{K}\Omega$ and an output impedance of $1\text{K}\Omega$. If voltage series negative feedback of 3.9% is given to this amplifier, Calculate the gain, input impedance, output impedance, amount of feedback, bandwidth and distortion of the amplifier with negative feedback.	6	2	3
3.a	With the help of relevant sketches elaborate on the construction, working principle characteristics and equations on n-channel enhancement type of MOSFET.	5	3	2
3.b	An n-channel MOSFET has $V_t=0.5\text{V}$ and drain current of 0.25mA when $V_{gs}=V_{ds}=3\text{V}$. Find: (i) Drain current if $V_{gs}=4\text{ V}$ and $V_{ds}=4.5\text{V}$. (ii) r_{ds} if $V_{gs}=5\text{V}$ assuming V_{ds} to be very small. (iii) If the MOSFET is used as Common source amplifier with Drain resistance of $12\text{K}\Omega$, determine the voltage gain of the amplifier when $V_{gs}=6\text{V}$.	5	3	3
4.a	Draw the block diagram of communication system and explain the function of each stage.	5	1	1
4.b	A carrier of 1MHz with 400W of its power amplitude modulated with a sinusoidal signal of 2500Hz. The depth of modulation is 75%. Calculate the sideband frequencies, the bandwidth, the power of the sidebands and total power in the modulated wave and sketch the frequency spectrum when amplitude of the carrier signal is 3V.	5	2	3
5.a	Draw the circuit diagram and explain the operation of two input CMOS NOR gate.	6	1	2
5.b	Simplify the following Expressions 1. $Y = (A + \bar{B} + \bar{C})(A + \bar{B} + C)$ 2. $Y = \overline{BC} + \overline{AD}(\overline{AB} + \overline{CD})$	4	1	1

BT-Blooms Taxonomy, CO-Course Outcomes, M-Marks

Marks Distribution	Particulars		CO1	CO2	CO3	CO4	L1	L2	L3	L4	L5	L6
	Test	Max Marks	21	18	21	-	26	15	19	-	-	-



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Technological
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Academic year 2021-2022 (Even Sem)

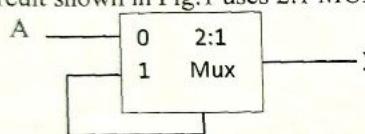
DEPARTMENT OF
ELECTRONICS & COMMUNICATION ENGINEERING

Date	21.09.2022	Maximum Marks	60
Course Code	21EC25	Duration	120 Min
Sem	II Semester	Improvement Test	

ELEMENTS OF ELECTRONICS ENGINEERING

Part A must be answered within the first two pages of manuscript.

PART A

Sl. No.	Questions	M	BT	CO
1.	In a 3-line to 8-line DECODER, with X ₂ , X ₁ , X ₀ as the inputs and Y ₀ to Y ₇ as the outputs, what should be the input code, so that Y ₅ is HIGH and all other outputs are LOW.	1	1	1
2.	If one of the inputs to a 2 input EX-NOR gate is always connected to logic 0, then it could be used as _____.	1	2	2
3.	The circuit shown in Fig.1 uses 2:1 MUX works as _____ logic gate.  Fig.1	2	3	2
4.	In the given in Fig.2, if c ₁ = 0 and c ₀ = 1 then the output M is _____.	2	3	2
5.	In the circuit shown in Fig. 3, the output voltage V _o is = _____.	2	2	3
6.	Op-amp is a _____ controlled voltage device.	1	1	3
7.	The output signal of an op-amp with slew rate of 2V/μs has a maximum amplitude value of 5V. Then the maximum frequency for undistorted output voltage is	1	1	3

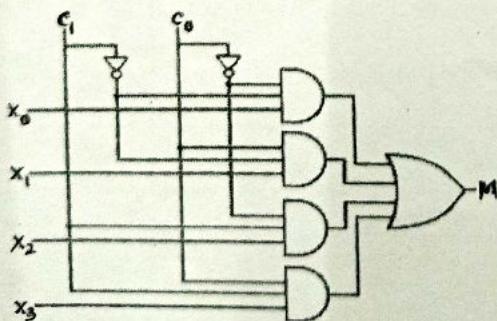


Fig.2

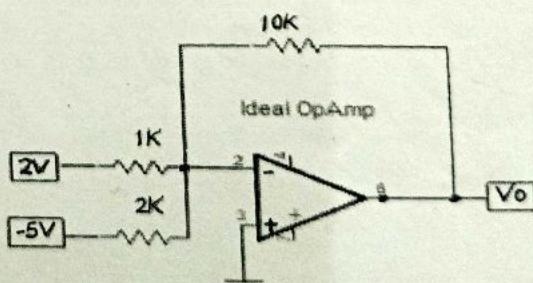


Fig. 3



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PART-B

Sl. No.	Questions	M	BT	CO
1a	Draw the truth table for SUM and CARRY OUT of a Full adder and obtain the logic expressions for the same. Realize full adder using two half adders.	6	2	1
1b	A bulb in a staircase has two switches, one switch being at the ground floor and the other one at the first floor. The bulb can be turned ON and also can be turned OFF by one of the switches irrespective of the state of the other switch. State the logic of switching of the bulbs.	4	3	1
2a	Realize an 8 to 3 line ENCODER with necessary truth table, logic expressions, logic circuit and explain its operation.	5	2	2
2b	Identify the logic expression realized in the circuit shown in Fig.4. Implement the same using minimum number of NOR gates only.	5	2	3
3a	Draw a circuit and calculate the values of different resistors of a summer circuit using two ideal op-amp to get the output $V_o = 3V_1 + 2V_2 + 5V_3 - 8V_4 - 10V_5 - 12V_6$, where V_1, V_2, V_3, V_4, V_5 and V_6 are the available inputs.	5	4	4
3b	Determine the simplified expression for the given function F using K map method. $F(A, B, C, D) = \sum m(0, 1, 2, 4, 5, 6, 7, 8, 10, 11, 12, 13, 14, 15)$	5	3	2
4a	Bring out eight difference between the RISC and CISC architectures.	5	1	3
4b	For the difference amplifier circuit shown in Fig.5, determine the output voltage V_o . Assume op amp used is ideal.	5	3	3
5a	Draw the circuit of an integrator using an ideal op-amp and prove that it works as an integrator.	5	2	2
5b	Draw the circuit of the Schmitt trigger and explain the operation of the circuit with neat waveforms.	5	2	3

Marks Distribution	Particulars		CO1	CO2	CO3	CO4	L1	L2	L3	L4	L5	L6
	Test	Max Marks	10	15	20	5	5	26	14	5	-	-