UNIT 1

Unit 1: Bipolar Junction Transistors

Semiconductor Diode- Review, Regulated Power Supply

Bipolar Junction Transistors- Transistor Construction and Operation, Load-Line Analysis, Operating Point, Fixed Bias, Voltage –Divider Bias Configurations, Bias Stabilization, Transistor Switching Networks, Amplification in the AC Domain, The r_e Transistor Model for CE Configuration, RC Coupled Amplifier, Gain, Input Resistance and Frequency Response, Cascaded Systems. Numerical Examples.

Reference Book:

"Electronic Devices and Circuit Theory", Robert L Boylestad, Louis Nashelsky, Prentice Hall India publication, 10^{th} Edition, 2009, ISBN: 978-317-2700-3.

Semiconductor Diode:

- A Semiconductor diode is created by diffusing one part of an intrinsic semiconductor with Acceptor impurities and the other part with Donor impurities, making one side P-type and the other side N-type. Thus we have here a junction of P-type and N-type regions in the same semiconductor material.

- In below Fig 1.1 p-type and n-type semiconductor materials are shown side by side representing a PN- junction.

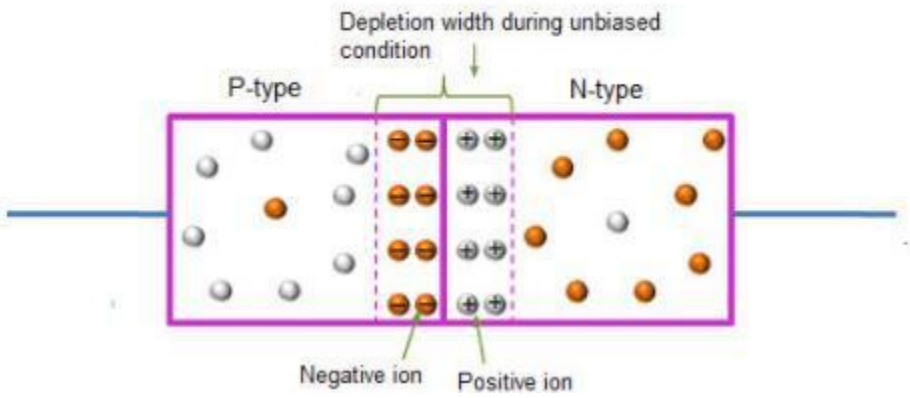


Fig 1.1: PN-junction diode

- Since holes and electrons are close together at the junction, some free electrons from the n-side are attracted across the junction from a region of higher carrier concentration.
- The free electrons crossing the junction create negative ions on the p-side by giving some atoms one more electron than their total number of protons.

- The electrons also leave positive ions(atoms with one fever electron than the number of protons)behind them on n-side.

Barrier Voltage:

- Before the diffusion process the n-type and p-type materials will be electrically neutral.

- When the negative ions are created on the p-side, the portion of the p-side close to the junction acquires a negative voltage. Similarly the positive ions created on the n-side give the n-side a positive voltage close to the junction.

- The negative voltage on the p-side tends to repel additional electrons crossing from the n-side and the positive voltage on the n-side tends to repel additional holes from the p-side.

- The initial diffusion of charge carriers creates a barrier voltage at the junction which is positive on n-side and negative on p-side.

- The magnitude of the barrier voltage for germanium is 0.3V and for silicon is 0.7V.

Depletion Region:

- Depletion region is also called space charge region.

- The movement of charge carriers across the junction leaves a layer on each side that is depleted of charge carriers.

- On the n-side, the depletion region consists of donor impurity atoms that having lost the free electron associated with them have become positively charged.

- On the p-side, the depletion region consists of acceptor impurity atoms that have become negatively charged by losing the hole associated with them.

- If the two blocks of semiconductor material have equal doping densities ,the depletion layer on each side have equal widths.

- If the p-side is more heavily doped than n-side the depletion region penetrates more deeply into the n-side in order to include an equal number of impurity atoms on each side of the junction.

- When the n-side is more heavily doped, the depletion region penetrates more deeply into the p-side.

- In equilibrium condition, the depletion region gets widened upto a point where further electrons or holes can cross the junction.

PN Junction diode operation and its V-I characteristics

PN Junction diode operation:

- The below Fig 1.2 shows the schematic arrangement of a PN junction diode and Fig 1.3 shows the symbol of a diode.

Fig 1.2: Schematic arrangement of PN junction diode

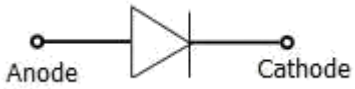


Fig 1.3: Symbol of PN junction diode

- The term Bias refers to the application of external voltage across the two terminals of the device to extract the response.

  The two different biasing conditions:

  1. Forward Bias
  2. Reverse Bias

- If a voltage applied across the diode has the same polarity across the diode it is considered as **Forward Biasing.**

- If a voltage applied across the diode has the reverse polarity across the diode it is considered as **Reverse Biasing.**

Forward Bias condition:

- A forward bias or ON condition is established by applying the positive potential to the p-type material and negative potential to the n-type material.

- The forward bias condition is shown in below fig 1.4.

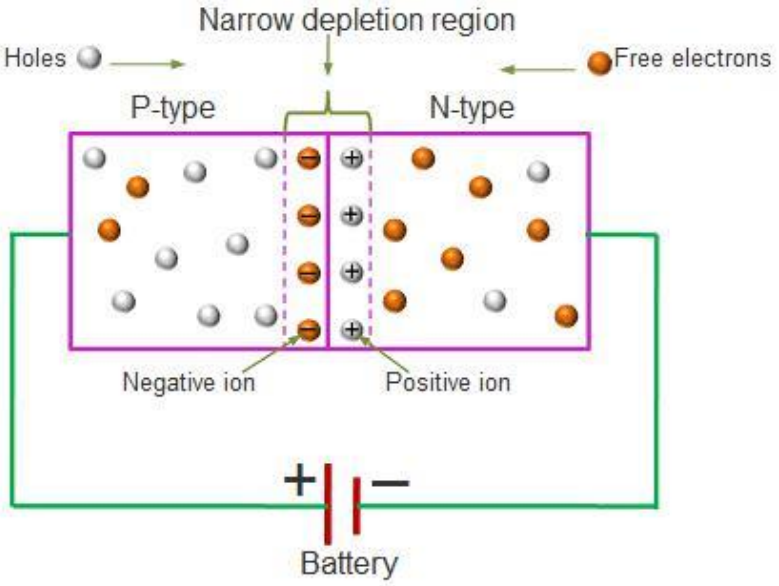


Fig 1.4: Forward biased PN junction

- The application of a forward biased potential will pressurize electrons in the n-type material and holes in the p-type material to recombine with the ions near the boundary and reduce the width of the depletion region.

- The minority flow of carrier flow of electrons from the p-type material to the n-type material and of holes from n-type material to p-type material has not changed in magnitude but the reduction in the width of the depletion region has resulted in a heavy majority flow across the junction

- An electron of the n-type material now experiences reduced barriers at the junction due to the reduced depletion region and a strong attraction for the positive potential applied to the p-type material.

- As the applied bias increase in magnitude the depletion region will continue to decrease in width until a flood of electrons can pass through the junction resulting in a exponential rise in current.
- Typically the voltage across the forward biased diode will be less than 1V.

- It is important to remember that in the forward biased condition, conduction is by majority current carriers(i.e. holes in p-type material and electrons in n-type material.)

- Increasing the battery voltage will increase the number of majority carriers arriving the junction and therefore increases the current flow.

- If the battery voltage is increased to the point where the barrier is greatly reduced a heavy current will flow and the junction may be damaged from the resulting heat.

Reverse Bias condition:

- A reverse bias or OFF condition is established by applying the positive potential to the n-type material and negative potential to the p-type material.

- The forward bias condition is shown in below fig1. 5.

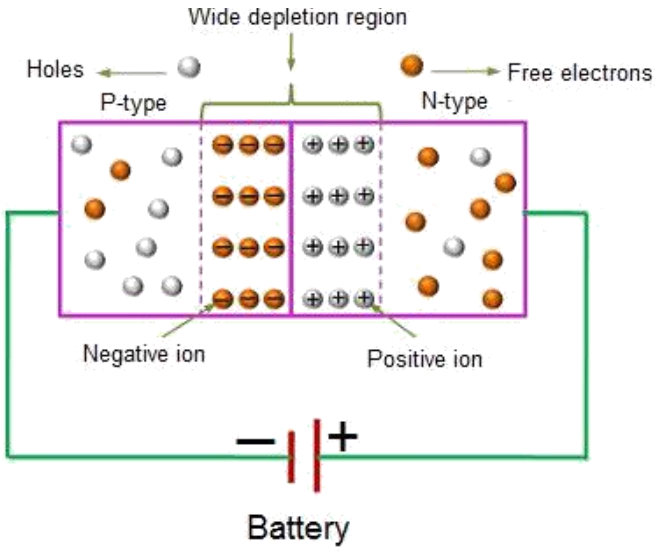


Fig 1.5: Reverse biased PN junction

- The number of uncovered positive ions in the depletion region of the n-type material will increase due to the large number of free electrons drawn to the positive potential of the applied voltage.
- Similarly the number of uncovered negative ions will increase in the p-type material. The net effect therefore is a widening of depletion region.
- This widening of the depletion region will establish a great barrier for the majority carriers to overcome effectively reducing the majority carrier flow to zero.
- The number of minority carriers, however entering the depletion region will not change, resulting in minority carrier flow.
- The current that exists under reverse bias conditions is called the reverse saturation current represented by I_s or I_o.
- when the reverse bias on the PN junction is increased, there is only a negligible increase in the reverse saturation current.
- Further increase in the reverse bias voltage reduces a special phenomenon called "**Junction Breakdown**".

Diode Current Equation:

- When a diode is subjected to bias there will be a current flow through the diode depending on bias conditions.
- Diode conducts when it is forward biased and there will be a large majority charge carriers crossing the junction resulting in large current.
- Diode stops conduction when it is reverse biased and there will be only minority charge carriers crossing the junction resulting in a reverse saturation current.
- The equation relating pn junction current and voltage levels is called Shockley equation and is represented as

$$I_D = I_o[e(^{V_D}/\eta V_T) - 1]$$

Where

I_o - Reverse Saturation Current

V_D - Applied bias voltage across the diode

η - Constant that depends on material

V_T - Thermal voltage called voltage equivalent of temperature

$$V_T = KT/q$$

where

K-Boltzman's constant=$1.38*10^{-23}$ J/K

T- Absolute Temperature=(273+T°c)K

q-change of electron=$1.6*10^{-19}$ C

By substituting the above values V_T can be obtained as $V_T = T/11600$

V-I characteristics of PN junction Diode:

- A complete analysis of PN junction shows that in the forward biased condition , the diode current I_D varies exponentially with applied voltage V
- Where as in the reverse biased condition, the diode current I_D is almost constant irrespective of the applied voltage and is almost equal to I_o.
- The relation between the current through the diode and the voltage across the diode is given by diode equation.
- The diode behavior based on the diode current equation is illustrated in below fig 1.6.

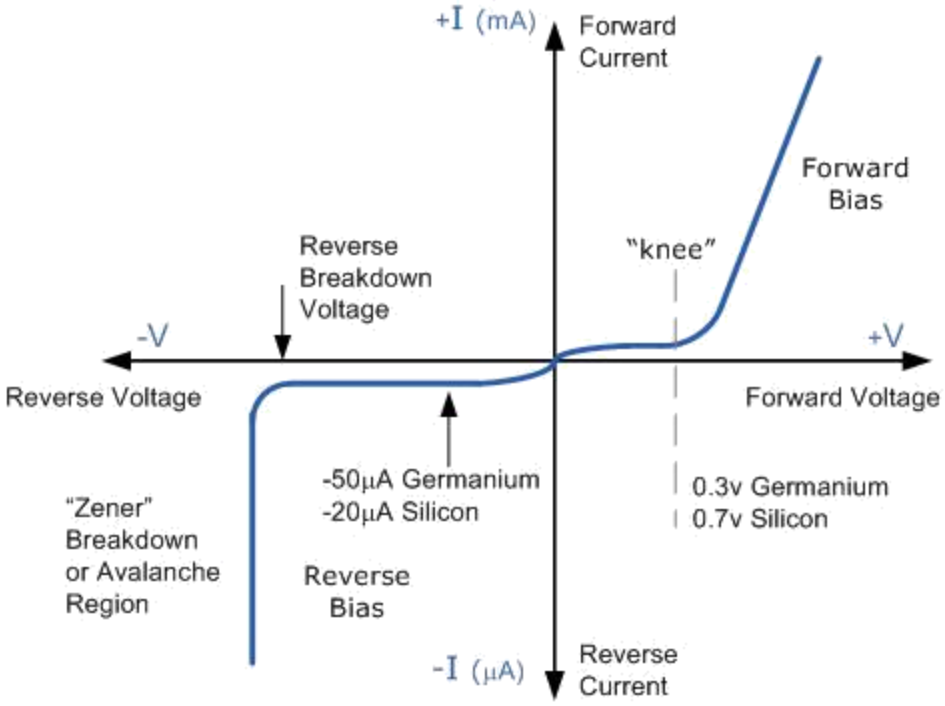


Fig 1.6: V-I Characteristics of PN junction diode

The figure 6 indicates the VI characteristics for a germanium diode and a silicon diode.

- From the curve it is clear that cut-in voltage Vγ for a germanium diode is 0.3V and for a silicon diode is 0.7V.

- It is evident from the diode current equation that diode current is sensitive to the device temperature.

- In the forward bias region for a given voltage ,diode current reduces with increase in temperature and the current shifts to the left.

- In reverse bias condition, the diode current increases i.e. I_0 doubles for every 10^o c rise in temperature.

Dynamic or AC resistance r_d:

- Suppose in addition to a dc current a small ac signal is super imposed in a diode circuit. The resistance that the diode offers to this signal is called AC resistance.
- The varying input will move the operating point up and down and thus defines a specific change in current and voltage.
- If there is no varying signal the point of operation would be the Q-point appearing on figure determined by the applied dc levels.
- The term Q-point is derived from the word "Quiescent" which means "Still or unvarying".

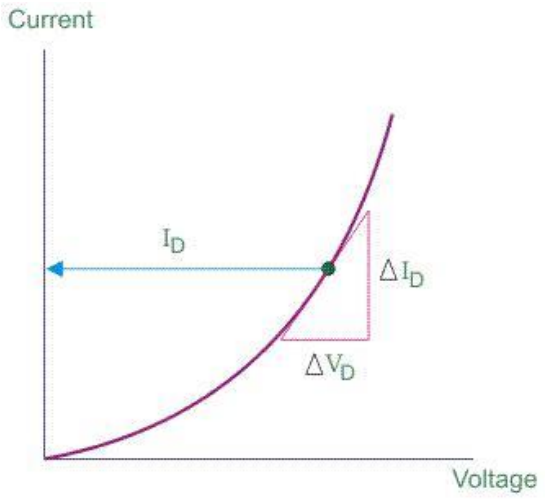


Fig 1.7: Defining the dynamic or AC resistance

- A straight line drawn tangent to the curve through the Q-point as shown on figure will define a particular change in voltage and current that can be used to determine the AC or dynamic resistance.
- r_d is given as

$$r_d = \Delta V_D / I_D$$

where signifies the finite change in the quantity.

Expressing r_d in terms of V_T and I_D

$$\text{WKT} \quad I_D = I_o[e^{V_D/\eta V_T} - 1]$$

Differentiate I_D w.r.t V_D

$$d I_D/ d V_D = d (I_o[e^{V_D/\eta V_T} -1])/ d V_D$$

$$d I_D/ d V_D = I_o[e^{V_D/\eta V_T} *1/ \eta V_T - 0]$$

$$d I_D/ d V_D = I_o e^{V_D/\eta V_T} * 1/ \eta V_T$$

$$d I_D/ d V_D = I_D/ \eta V_T$$

WKT $r = V/I$

Therefore $d V_D/ d I_D = \eta V_T/ I_D$

put $\eta = 1$ & $V_T = 26mV$, we get

$$r_d = 26mv/I_D = V_T/ I_D$$

Regulated Power Supply:

The Fig 1.8 shows the block diagram of regulated DC power supply. The AC voltage is connected to the primary of the transformer. The transformer steps down to the AC voltage for the desired DC output. Pulsating DC voltage means a unidirectional voltage containing large vary in component called ripple in it.

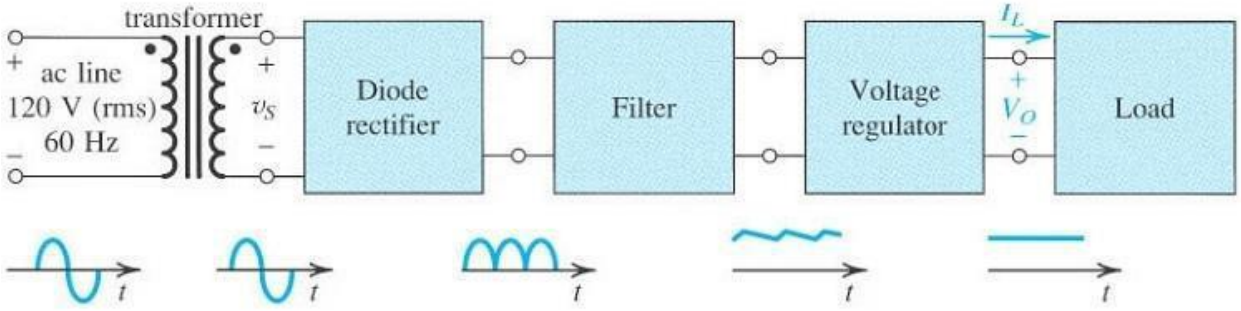


Fig 1.8: Regulated Power Supply

To reduce the ripple, filter is used after the rectifier circuit, which reduces the ripple content in the pulsating DC and tries to make it smoother. But still the output of filter contains some ripples and this output is called unregulated DC.

A circuit used after the filter is a regulator circuit which is not only makes the dc voltage smooth and almost ripple free but it also keeps the dc output voltage constant though

input dc voltage varies under certain conditions. The regulator also keeps dc voltage constant under variable load conditions. The output of the regulator is pure DC and to which the load can be connected.

Power Supply Performance parameters:

The DC output voltage in a DC Supply varies due to two parameters:

- Line Regulation
- Load Regulation

The input to the unregulated power supply i.e. rectifier circuit is 230V AC supply. This is called Line Voltage. The Line Voltage may change under different load conditions.

A +/- 10% variation in the AC supply voltage V_s also called as Line voltage is very common. There is some variation in the DC output voltage when the line voltage varies. The output voltage change ΔV_0 due to a change in the line voltage is called source effect.

Source Effect= ΔV_0 for a 10% change in V_s

The source effect expresses as a % of DC output voltage V_0 is called Line Regulation.

Line Regulation = =(ΔV_0 for a 10% change in V_s)/V_0 x100

For a good DC power supply ΔV_0 should be very small.

Ideally ΔV_0 should be equal to 0. Therefore Line Regulation is 0% for an ideal.

The load regulation is the change in the regulated output voltage when the load current is changed from minimum (no load) to maximum (full load). The DC output voltage V_0 is a function of load current I_L. If the load current I_L increases V_0 decreases and vice-versa.

The output voltage change ΔV_0 due to the load current change I_{Lmax} is called the load effect.

Load effect= ΔV_0 for ΔI_{Lmax}.

The load effect expressed as a percentage of the output voltage V_0 is called the load regulation.

$$\text{Load regulation} = (\Delta V_0 \text{ for } \Delta I_{L\max}.)/V_0 \times 100$$

BJT operation and characteristics

Bipolar junction transistor (BJT): It is a semiconductor device similar to pn diode. It is a three layer device consisting of either two n-type and one p-type (npn) or two p-type and one n–type material (pnp) with two junctions and three terminals. The terminals are Emitter (E), Base(B) and Collector(C). The two junctions are Emitter – Base (EB) junction and Collector – Base (CB) junction. The emitter layer is heavily doped, base is lightly doped and collector is moderately doped. Both holes and electrons contribute to the flow of current and hence the name bipolar junction transistor. The schematic and the symbol are shown in Fig 1.9.

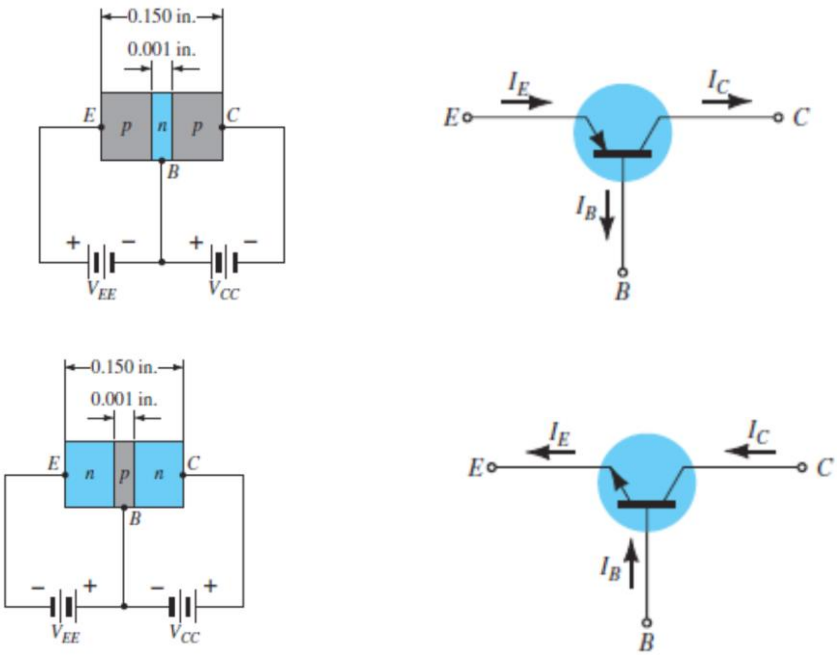


Fig 1.9. Transistor schematic and symbol

Transistor operation: As seen in Fig 1.10 a large number of majority carriers (holes which constitute the emitter current I_E) will diffuse across the forward bias p-n junction into the n–type material.

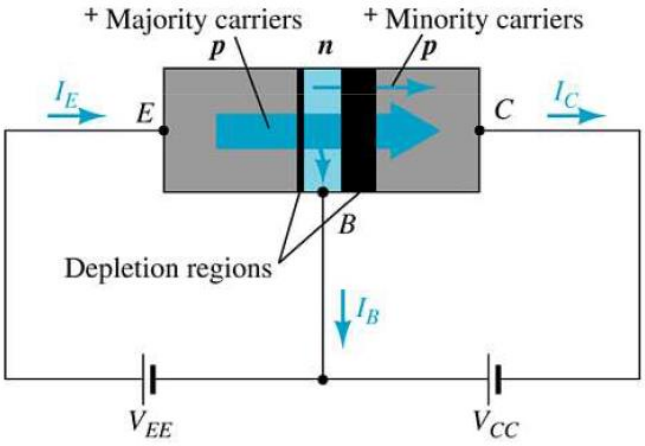


Fig 1.10: Transistor operation (pnp)

Since n-type is very thin and has a low conductivity, very small number of these carrier will take this path of high resistance to the base terminal and this constitutes the base current I_B. A large number these majority carriers will diffuse across the reverse bias junction into the p- type material to the collector terminal and constitute the collector current I_C .

Therefore $I_E = I_B + I_C$

The collector current however comprises of two components the majority and minority carriers. The minority current is called the leakage current and the symbol is $I_{CO.}$

ie, $I_C = I_{Cmajority} + I_{CBOminority}$

I_C is measured in mA and I_{CBO} is measured in µA or nA. I_{CBO} is similar to reverse saturation current (I_S) in a diode. To describe the behavior of the device, 2 sets of characteristics are required.

1. Input (I/P) characteristics
2. Output(O/P) characteristics

Relation between α and β

Common base dc current gain $\alpha = I_C/I_E$

Common emitter dc current gain, $\beta = I_C/I_B$

Since $I_E = I_B + I_C$, dividing this equation by I_C gives

$I_{E/} I_C = I_{B/} I_C + I_{C/} I_C$

$I_{E/} I_C = I_{B/} I_C + 1$

$1/\alpha = 1 + 1/\beta$ (since $\alpha = I_C/I_E$ and $\beta = I_C/I_B$)

$1/\alpha = (\beta + 1)/\beta$

$\alpha = \beta/1+\beta$

$\alpha(1+\beta) = \beta$

$\alpha + \alpha\beta = \beta$

$\alpha = \beta - \alpha\beta$

$\alpha = \beta(1-\alpha)$

$\beta = \alpha/(1-\alpha)$

The 3 main regions of operation of a transistor are:-

1. Cutoff region
2. Saturation region
3. Active region

1 Cutoff region: Here the two junctions EB and CB are reverse biased. In this region the device behaves as an open switch.

2 Saturation region: Both the junctions are forward biased. In this region the device acts like a closed switch.

3 Active region: Here the EB junction is forward biased and CB junction is reverse biased. In this region the BJT is used as an amplifier.

Note: When EB junction is reverse biased and CB junction is forward biased, this region is called as inverse active region. The operation in this region is generally not used in practice.

The transistor can be configured as an amplifier in 3 ways, depending on the common terminal between the input and the output.

1. Common Base configuration (CB)
2. Common Emitter configuration (CE)
3. Common Collector configuration(CC)

Common Base configuration (CB)

Base is common to both input and output sides of the configuration as shown in fig 1.11. In this mode E and B are the input terminals and C and B are the output terminals.

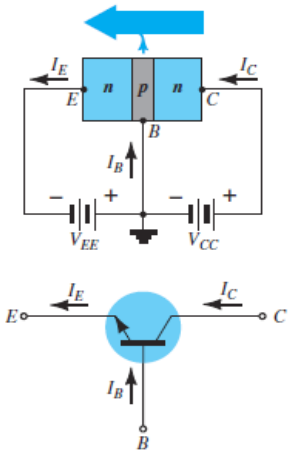


Fig 1.11: CB configuration

Input characteristics: A plot of the variation of i/p emitter current I_E with variation in the EB voltage V_{BE} (i/p) for different values of collector base voltage V_{CB} (o/p) is the i/p characteristics. To obtain the i/p characteristics, V_{CB} is kept constant ,V_{BE} is varied and value of I_E is recorded. The active region is the region normally employed for linear amplification. After the cut in voltage V_{BE} = 0.7 V, I_E increases with small increase in V_{BE} voltage as seen in Fig 1.12.

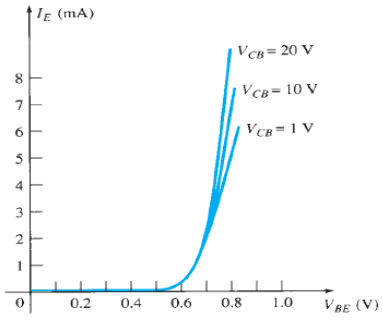


Fig 1.12: Input characteristics for CB mode

Output characteristics: Relates to o/p current I_C to the o/p voltage V_{CB} for various levels of input current I_E as shown in Fig 2.5. The three region of interest are :-

Active region:- The active region is defined by the biasing arrangements EB –FB and CB—RB. This is the normal operating region of the transistor. At lower end of the active region the emitter current is zero, and the collector current is due to the reverse saturation current which is very small.

Cut off region:- EB—RB,CB—RB. Region where collector current is zero.

Saturation region: EB—FB, CB—FB. The region of the characteristics to the left of V_{CB} is 0.

Early Effect. The effect of increase in reverse voltage reducing the effective base width is called base width modulation or early effect.

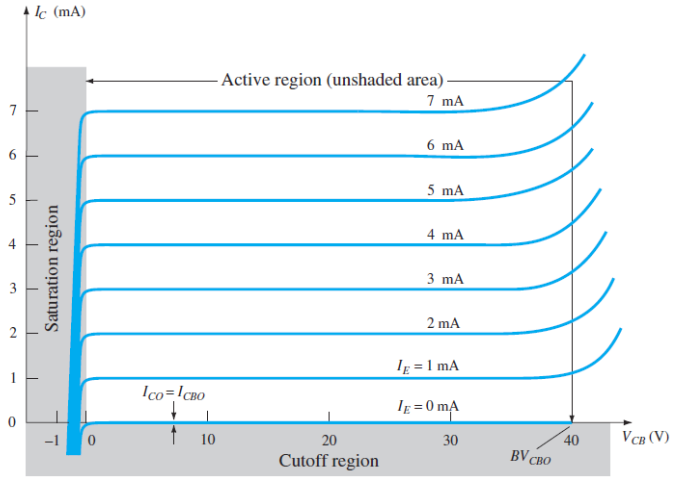


Fig 1.13: Output characteristics for CB mode

Common Emitter configuration (CE)

Emitter is common to both i/p and o/p terminals as shown in fig 1.14.

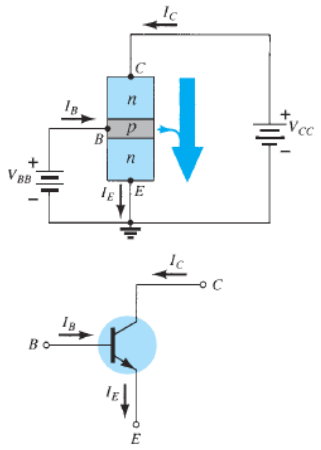


Fig 1.14: CE configuration

Input characteristics: A plot of the variation of i/p base current I_B with variation in the EB voltage V_{BE} (i/p) for different values of collector emitter voltage V_{CE} (o/p) is the i/p characteristics as seen in Fig 1.15.To obtain the i/p characteristics, V_{CE} is kept constant, V_{BE} is varied and value of I_B is recorded. For fixed value of $V_{BE,}$ I_B decreases with increase in $V_{CE.}$ This is due to the fact that with increase in $V_{CE,}$ the depletion region of the reverse bias collector base junction widens, reducing base width.

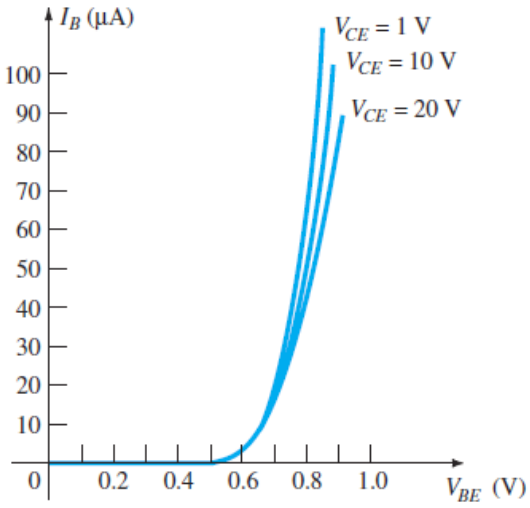


Fig 1.15: Input characteristics for CE mode

Output characteristics: Relates to o/p current I_C to an o/p voltage V_{CE} for various levels of input current I_B as seen in Fig 1.16. The three region of interest are :-

Active region:-In this region, the collector current responds more readily to any input signal since I_C is more sensitive. So the transistor can be used as an amplifier. The characteristics are not horizontal lines due to fixed I_B, the magnitude of I_C increases with increases in V_{CE} due to early effect.

The collector current I_C can be derived in active region as before.

In common base mode

$I_C = -\alpha I_E + I_{CO}$

$I_C = \alpha(I_B + I_C) + I_{CO}$

$I_C = \alpha I_B + \alpha I_C + I_{CO}$

$I_C(1-\alpha) = \alpha I_B + I_{CO}$

$I_C = \alpha I_B/(1-\alpha) + I_{CO}/(1-\alpha)$

Substituting $\beta = \alpha/(1-\alpha)$ and $1/(1-\alpha) = 1+\beta$ yields

$Ic = \beta I_B + I_{CO}(1+\beta)$

Cutoff region: the region to the right of the $V_{CE} = 0$ and below $I_B = 0$ is the cutoff region.

If $I_B = 0$ then $I_C = I_E = (1+\beta)Ico$.

Saturation region: This region lies extremely close to the zero voltage axis, where all the curves merge and fall rapidly towards the origin. In this region I_C is almost independent of I_B.

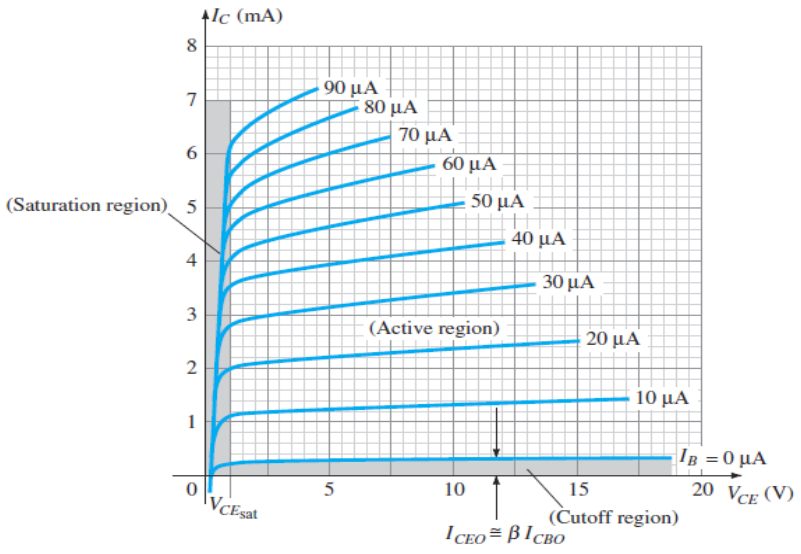


Fig 1.16: Output characteristics for CE mode

BJT Biasing

Biasing is necessary to keep the transistor in the active region by making the EB junction FB and CB junction RB. Transistor biasing is the establishment of suitable dc values such as I_C, V_{CE}, I_B and V_{BE} by using a single dc source. When BJT is properly biased, faithful amplification will takes place. As in CB and CE modes, two dc sources were used but in order to make biasing circuit simple, stable and economical single supply is used. There are 2 different types of biasing circuits

1. Fixed bias or base resistor bias
2. Voltage divider bias or self bias

Fixed Bias Configuration

- **DC load line:** Biasing is application of external dc voltages of correct polarity and magnitude across the two junctions of the transistor. Since dc biasing is essentially required for proper operation of the transistor. If the transistor is to be used as an amplifier then the device should be operated in active region. Similarly if the device is required to be operated as an electronic switch then it should be operated in saturation and cut off regions.

- **Operating point:** Consider the common emitter circuit as shown below. The transistor EB junction is forward biased by external dc voltage V_{BB} and CB junction is reverse biased by V_{CC}. When the signal is zero, there exists dc collector current I_C and the output voltage V_{CE}. Consider the common emitter circuit as shown in Fig 1.17.

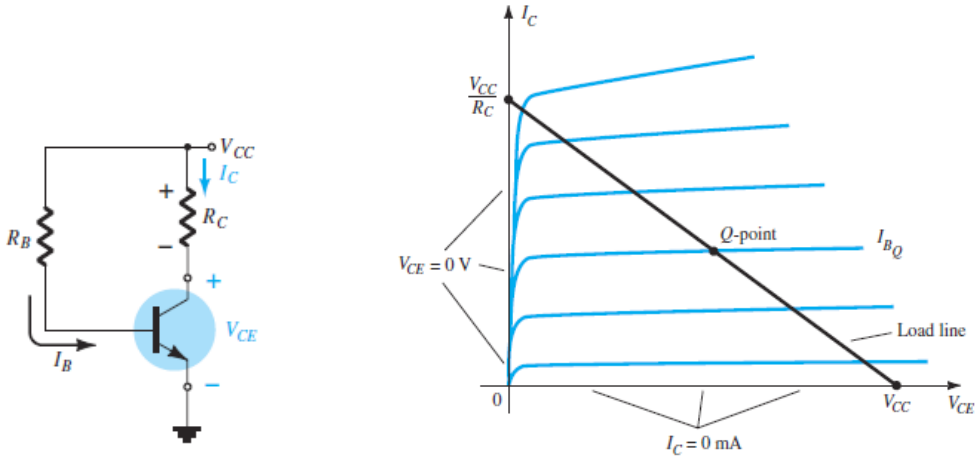


Fig 1.17: Fixed bias circuit and Load line analysis

By applying KVL to the o/p circuit

$V_{CC}=I_CR_C+V_{CE}$

$V_{CE}=V_{CC} - I_CR_C$

Therefore $I_C= (-1/R_C) V_{CE} + V_{CC}/R_C$

The above equation represents a straight line with the slope of $(-1/R_C)$. To draw the DC load line on the o/p characteristics, two points are required. In the below equation if $V_{CE}=0$,

$I_C=(-1/R_C) V_{CE} + V_{CC}/R_C$,

then $I_C= V_{CC}/R_C$……(a)

Similarly if $I_C=0$ then $V_{CC}=V_{CE}$……. (b)

Using (a) and (b) a straight line is drawn on the output characteristics. The line between (a) and (b) is called dc load line. The word dc indicates that only dc condition is considered with no input signal. During the operation of the transistor for fixed values of V_{CC} and R_C, the values of V_{CE} and I_C at different values of I_B are given by the intersection of load line with I_B lines as shown in figure. The intersection points on the load line are called operating point or quiescent point (Q-point). Usually Q point is said typically near the middle of dc load line for faithful amplification. If Q point is placed in saturation or cutoff, results in distortion in the o/p w/f.

Selection of Q-point

When a line is drawn joining the saturation and cut off points, such a line can be called as **Load line**. This line, when drawn over the output characteristic curve, makes contact at a point called as **Operating point**. This operating point is also called as **quiescent point** or simply **Q-point**. There can be many such intersecting points, but the Q-point is selected in such a way that irrespective of AC signal swing, the transistor remains in the active region.

The fig 1.18 shows how to represent the operating point.

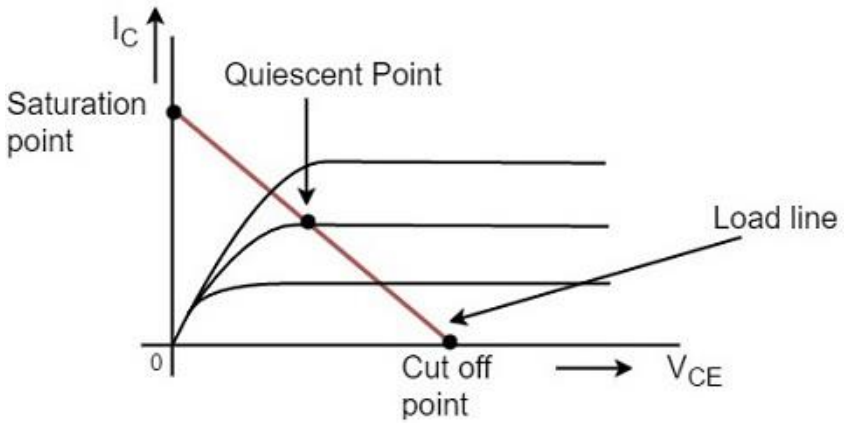


Fig 1.18: Regions of operations of CE configuration

The operating point should not get disturbed as it should remain stable to achieve faithful amplification. Hence the quiescent point or Q-point is the value where the Faithful Amplification is achieved.

Faithful Amplification

The process of increasing the signal strength is called as Amplification. This amplification when done without any loss in the components of the signal, is called as Faithful amplification. Faithful amplification is the process of obtaining complete portions of input signal by increasing the signal strength. This is done when AC signal is applied at its input.

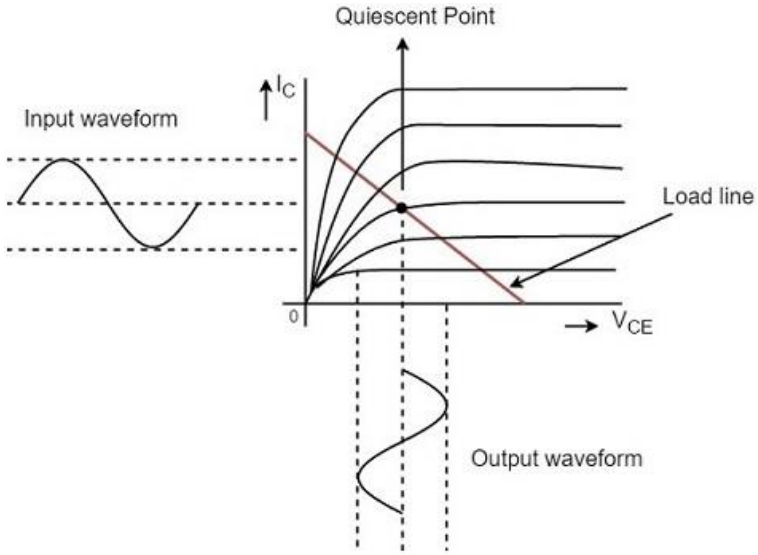


Fig 1.19: Operating point is in the middle of active region

In the above graph fig 1.19, the input signal applied is completely amplified and reproduced without any losses. This can be understood as Faithful Amplification. The operating point is so chosen such that it lies in the active region and it helps in the reproduction of complete signal without any loss. If the operating point is considered near saturation point, then the amplification is as shown in fig 1.20.

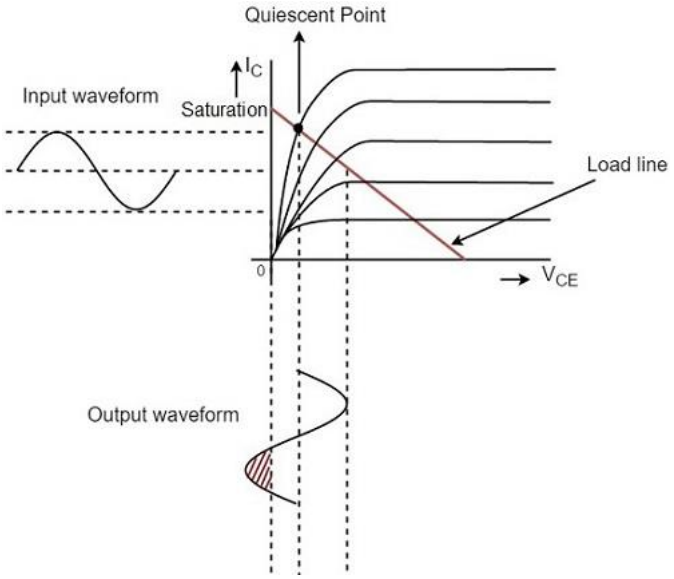


Fig 1.20: Operating point is considered near saturation point

If the operation point is considered near cut off point, then the amplification is shown in fig 1.21.

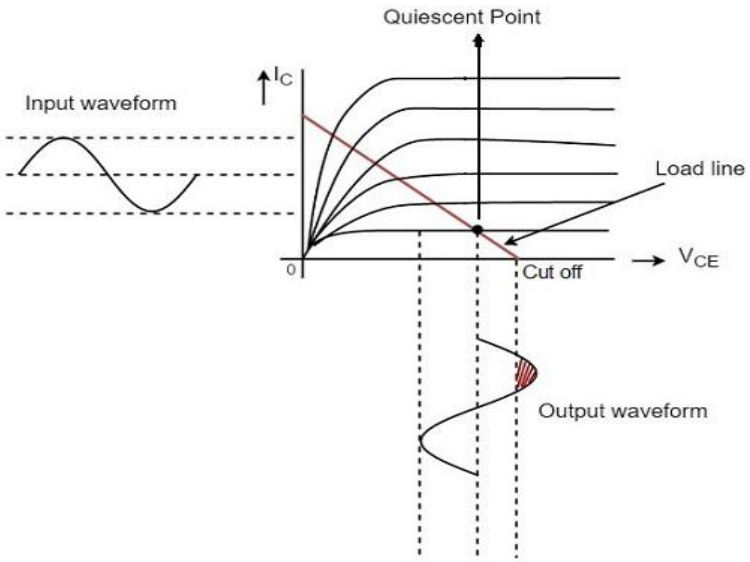


Fig 1.21: Operating point is considered near Cutoff point

Hence the placement of operating point is an important factor to achieve faithful amplification. But for the transistor to function properly as an amplifier, its input circuit (i.e., the base-emitter junction) remains forward biased and its output circuit (i.e., collector-base junction) remains reverse biased.The amplified signal thus contains the same information as in the input signal whereas the strength of the signal is increased.

To ensure faithful amplification, the following basic conditions must be satisfied.

- Proper zero signal collector current
- Minimum proper base-emitter voltage (V_{BE}) at any instant.
- Minimum proper collector-emitter voltage (V_{CE}) at any instant.

The fulfilment of these conditions ensures that the transistor works over the active region having input forward biased and output reverse biased.

Voltage Divider Biasing

This is the most widely used biasing circuit. In this method two resistors are connected across the supply V_{CC} which in turn provides biasing. This biasing circuit is called voltage divider biasing because the supply voltage V_{CC} is divided by the voltage divider network formed by R_1 and R_2 as shown in Fig 1.22. The voltage drop across R_2 will FB the EB junction resulting in the base current and hence the collector current.

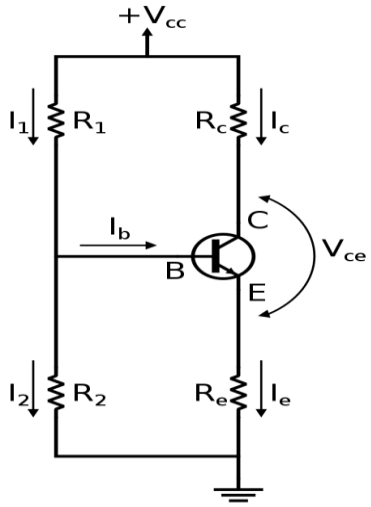
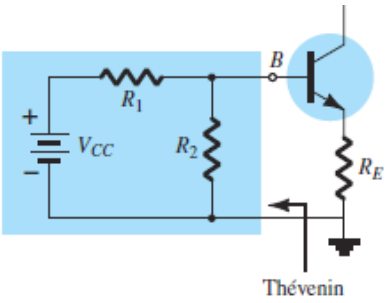


Fig 1.22. Voltage divider circuit.

The voltage divider circuit consisting of R_1 and R_2 can be replaced with its Thevenin's equivalent circuit. R_1 and R_2 should be replaced by Thevenin's resistance R_T in series with the Thevenin's voltage V_T as shown in Fig 1.23.The Thevenin's resistance R_T can be determined by setting the dc supply to zero where R_T is the parallel combination of R_1 and R_2. Similarly the Thevenin's voltage V_T can be determined as



$$V_T = (R_2 V_{CC})/ (R_1+R_2)$$

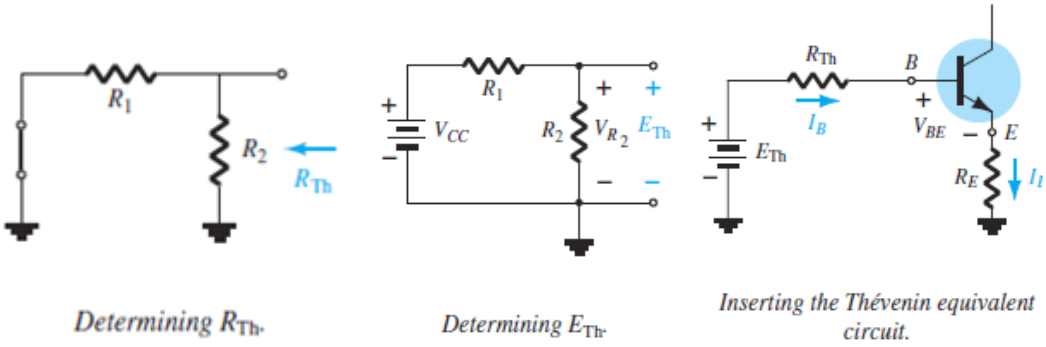


Fig 1.23. Steps to get Thevenin's equivalent circuit

By applying KVL to the base circuit in the Fig 1.23,

$$I_B = (V_T - V_{BE}) / (R_T + R_E(\beta+ 1))$$

Once I_B is determined, I_C can be calculated by $I_C = \beta I_B$

In order to find V_{CE} , KVL is applied to collector circuit

$$V_{CE} = V_{CC} - I_C (R_C + R_E) - I_B R_E$$

Bias Stability

The process of making the operating point independent of temperature changes or variation in transistor parameters is known as stabilization. Once stabilization is done, I_C and V_{CE} become

independent of temperature variations. A good biasing circuit always ensures the stabilization of the operating point.

Stability factor(S)

The rate of change of collector current I_C w.r.t the collector leakage current I_{CO} at constant β and I_B is called stability factor. Every circuit has three stabilization factors, one each with respect to I_{CO}, V_{BE} and β. At present only $S(I_{CO})$ is considered.

Stability factor $SI_{CO} = dI_C/ dI_{CO}$ at constant β & V_{BE}

The general expression for stability factor:

In active region the basic relationship between I_C and I_B is

$$I_C = \beta I_B + (1+ \beta) I_{CO}$$

Differentiate w.r.t I_C considering β constant

$$S = 1+ \beta / 1- \beta \, dI_B/dI_{CO}$$

Considering for the fixed bias circuit,

$$I_B = (V_{CC}-V_{BE})/R_B$$

$$S = 1+ \beta / 1- \beta \, dI_B/dI_{CO}$$

Therefore for the fixed bias circuit $SI_{CO} = 1+ \beta$

Similarly considering for the voltage divider circuit

$$I_B = (V_T - V_{BE}) / (R_T + R_E(\beta+ 1))$$

$$S = 1+ \beta / 1- \beta \, dI_B/dI_{CO}$$

Therefore for the voltage divider circuit

$$SI_{CO} = (1+ \beta) (R_T+R_E)/(R_T+(1+ \beta)R_E)$$

Thermal runaway:-

The collector current in BJT is

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

I_{CO} is dependent on temperature. The flow of I_C produces heat within the transistor. This raises the transistor temperature and if no stabilization is done the collector leakage current also increases. If leakage current increases, I_C increases by $(1+\beta)$ I_{CO} .This I_C will raise the temperature of the transistor, which in turn will cause I_{CO} to increase. This effect is cumulative and in a matter of seconds, the I_C may become very large causing the transistor to burn out. The self-destruction of an un stabilized transistor is known as thermal runaway.

re-model

Common-Emitter BJT transistor

Fig 1.24(a) below shows the common emitter transistor and Fig 1.24(b) is the re model for the configuration of (a).

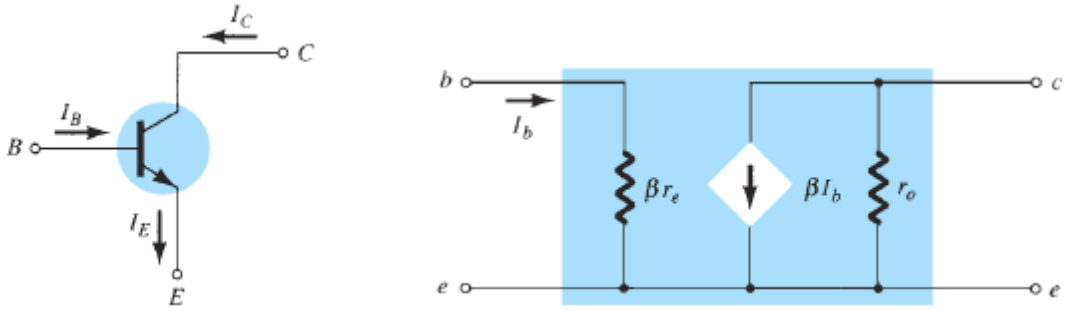


Fig 1.24(a) CE Configuration b)re-model of CE configuration

For the CE configuration the input terminals are base and emitter terminals and the output terminals are collector and emitter terminals. The base and emitter are replaced by a diode, the collector and base terminals are replaced by a current controlled source. For the ac response the diode is replaced by its equivalent ac resistance.

Input impedance $Z_i = V_{be}/i_b = \beta r_e$ if $\beta >> 1$

Output impedance $Z_o = V_o/I_o = r_o$

Voltage gain $A_v = V_o/V_i = -r_o/r_e$

Current gain $A_I = i_c/i_b = \beta$

Comparison of CE, CB &CC configurations

	CE	CB	CC
Zi	β re	re	β(re +R_E)
Zo	r_o	r_o	re
Av	- r_o / re	r_o / re	~1
A_I	B	A	(1+β)

Amplifiers

An amplifier is an electronic circuit that amplifies or magnifies or strengthens the amplitude of input signal without any distortion. Basic amplifier circuit is shown in Figure 1.25.

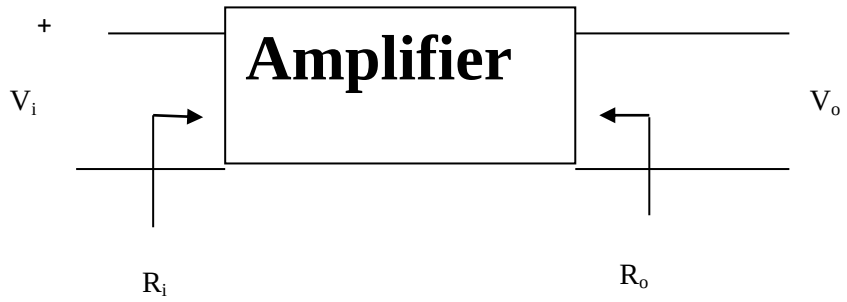


Figure 1.25: Basic Amplifier Circuit

Let us assume a small sinusoidal signal is applied to the amplifier at the output of the amplifier the signal must remain sinusoidal in waveform and the frequency of the signal must remain same as the input.

The ratio of output voltage to the input voltage of the amplifier is called the gain of the amplifier which is denoted by A_V.

The ratio of output current to the input current is called the current gain of the amplifier which is denoted as A_I.

Decibels:

The term bel is derived from the name of scientist Alexander Graham bell. It was found that the bel was too large for the unit of measurement, so the decibel (dB) is defined such that 10 decibels = 1 bel. Gain is generally expressed in dB because the ear responds to the sound intensities on a logarithmic scale rather than linear scale. It is easy to express the gain in dB rather than actual numbers

Voltage gain = A_V = (o/p voltage) / (i/p voltage)

$A_V = Vo / Vi$

Current gain = A_I = (o/p current) / (i/p current)

$A_I = Io / Ii$

Power gain = Ap = (o/p power) / (i/p power)

$A_P = Po / Pi$

Decibel power gain

$(A_P)dB = 10 \log(Po/Pi)$

$\Delta Po = 10 \log (P_2/P_1)$ dB

Decibel voltage gain

$(Ap)dB = 10 \log (P_o/P_i)$

Wkt $P_o = V_o^2 / RL$ and $Pi = V_i^2 /Ri$

$P_o/P_i = (V_o^2/RL) /(V_o^2/Ri) = V_0^2 / V_i^2$ if RL= Ri

$(A_P)dB = 10 \log (V_o^2 /V_i^2)$

(A_P) dB = $20 \log (V_o/V_i)$

Decibel voltage gain (A_V) dB = $20 \log (V_o/ V_i)$

Decibel current gain $(A_I)dB = 20 \log(I_o/I_i)$

(A_P) dB= $20 \log (I_o/I_i)$

Need for cascading of amplifiers:

The current gain or voltage gain obtainable from a single transistor amplifier stage is usually in adequate for most of the applications. Hence several amplifiers stage is connected in cascade.

The amplifiers are connected such that the output of one stage forms the input of the next stage. Such cascade amplifiers permit realization of any desired voltage or current.

In the cascading of amplifiers an important consideration is the choice of elements coupling one stage to the next one. Different coupling methods are used in the different type of cascade amplifier such as RC coupled amplifier and transformer coupled amplifier.

Cascaded stages: Figure 1.26 shows N amplifiers connected in cascade.

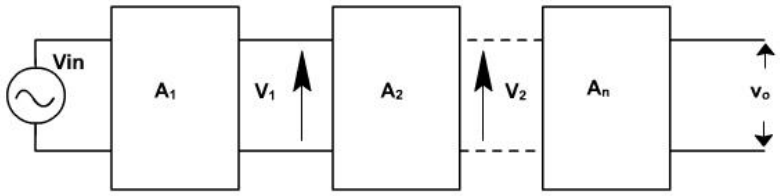


Fig 1.26: Amplifiers connected in cascade

Voltage of 1st stage $AV_1 = V_1/V_i$

Voltage of 2nd stage $AV_2 = V_2/V_1$

Voltage gain of Nth stage $AV_n = (V_o)/(V_{n-1})$

Overall voltage gain $AV = V_o/V_i$

$AV = V_o/V_{n-1} * ……..V_3/V_2 * V_2/V_1 * V_1/V_i$

$= AV_n * AV_2 * AV_3 * …….AV_n$

Overall voltage gain in dB

$(AV)dB = 20 \log (AV)$

$= 20 \log(AV_1 * AV_2 * AV_3 …….AV_n)$

$= 20 \log(AV_1) + 20\log(AV_2) + …….+ 20\log(AV_N)$

$(AV)dB = AV_1dB + AV_2dB + ……..+ AV_ndB$

RC Coupled CE Amplifier

The circuit diagram of RC coupled amplifier is shown in fig 1.27.

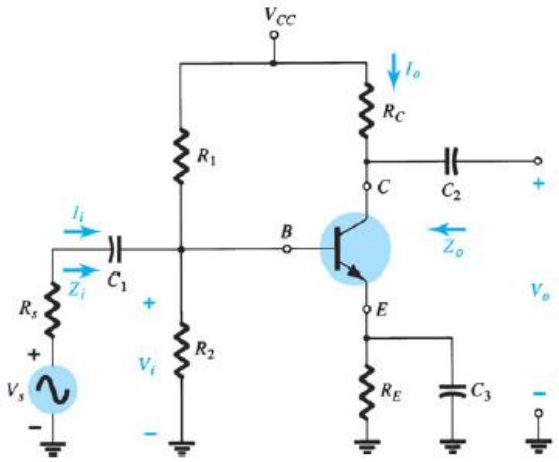


Fig 1.27: RC Coupled CE Amplifier

The resistors R1, R2, RC, RE forms the voltage divider biasing circuit. The values of resistors are chosen such that they set proper operating point for the CE amplifier. The operating point is chosen such that the device works in active region and it acts as an amplifier. In the fig 1.27, the coupling capacitors C1, C2 and bypass capacitor CE. The impedance of capacitor is given by XC = 1/2πfC. For dc signals f=0. The impedance XC = ∞. For DC signals capacitor acts as open circuit. In the circuit the signal source VS and the source is associated with source resistance RS. Note that source resistance RS is in parallel with R2 this reduces the bias voltage at the base of the transistor and this intern alters the collector current which is not desired. The dc signal which in the input of the source signal alters the biasing condition of the transistor. The capacitor C1 blocks any dc signals entering into the transistor. Similarly by connecting RL directly to the amplifier, the dc levels of VC and VCE will change which again alters the operating conditions of transistor. The output coupling capacitor C2 blocks dc signals entering the load or entering the next stage of the amplifier and it allows only ac signals to enter the next stage. The resistance RE provides bias stabilization to the transistor. But it also reduces the voltage gain of the amplifier. The bypass capacitor acts as a short circuit for ac signals and allows to create an ac ground in an amplifier without disturbing its Q-point.

Frequency response:

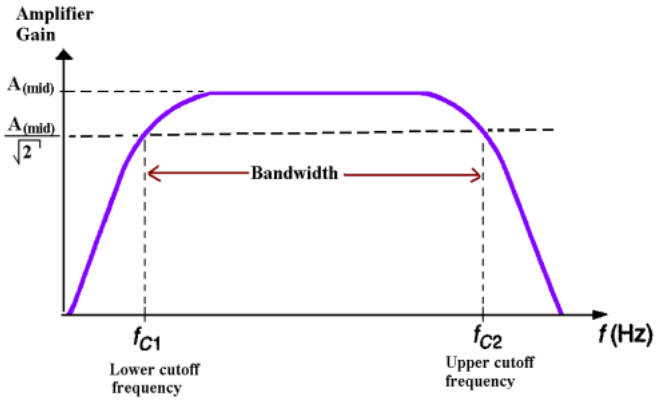


Fig 1.28: Frequency response of RC Coupled Amplifier

The frequency response of an RC coupled amplifier is shown in fig 1.28 can be divided into 3 regions:

1. Low frequency region: Reactance of a capacitor is given as XC = 1/2πfC

   At low frequencies XC increases, this increase in XC drops the signal voltage across the capacitor and in turn reduces the circuit gain.

2. Mid frequency region: As the frequency range increases, XC becomes very small and the voltage gain will be maximum and it will be almost constant for a certain range of frequencies.

3. High frequency range: At higher frequencies the voltage gain decreases due to the influence of junction capacitances of the transistor. At higher frequencies the reactance of junction capacitance falls. When the reactance becomes small enough, they provide shunting effect as they are in parallel with junctions. This reduces the current gain and in turn reduces the voltage gain.

Bandwidth (BW) of an amplifier:

Bandwidth of an amplifier is the difference between fC2(higher cutoff freq) and fC1 (lower cutoff freq)

BW of an amplifier = $f_H - f_L$.

The BW specifies the range of frequencies over which the gain does not deviate more than 70.7% of the maximum gain at mid frequency range. The two frequencies fC1 and fC2 are referred as half power frequencies or half power points or cut off frequencies. Because the gain or output voltage drops to 70.7% of maximum value and this represents a power level to one half the power at the reference frequency in mid frequency range.

Transistor as a switch

The application of transistors is not limited solely to the amplification of signals. Through proper design, transistors can be used as switches for computer and control applications. The

network of Fig.1.29 can be employed as an *inverter* in computer logic circuitry. Note that the output voltage *V C* is opposite to that applied to the base or input terminal. In addition, note the absence of a dc supply connected to the base circuit. The only dc source is connected to the collector or output side, and for computer applications is typically equal to the magnitude of the "high" side of the applied signal—in this case 5 V. The resistor R_B will ensure that the full applied voltage of 5 V will not appear across the base-to-emitter junction. It will also set the I_B level for the "on" condition.

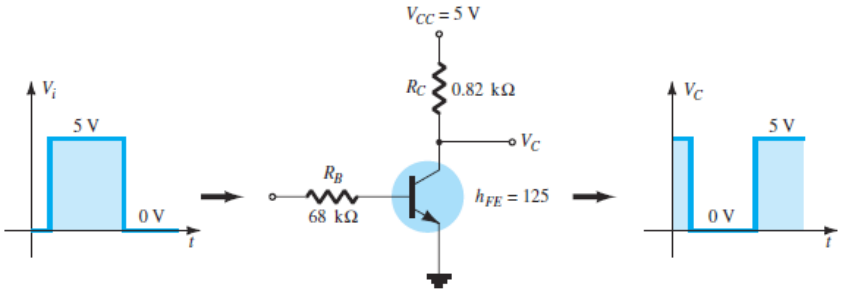


Fig. 1.29: Inverter circuit

Numerical Examples: Refer Tutorial - 1