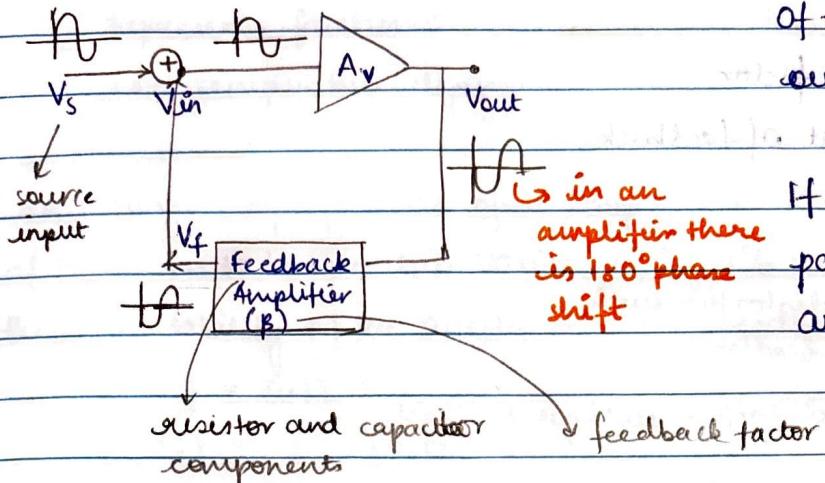


UNIT 2:

FEEDBACK AMPLIFIERS:



If the source signal and part of the feedback output are out of phase \rightarrow negative feedback

in an amplifier there is 180° phase shift

If the source signal and part of the feedback output are in phase \rightarrow positive feedback

$$A_v = \frac{V_{out}}{V_{in}} ; A_f = \frac{V_{out}}{V_s}$$

$$\beta = \frac{V_{out}}{V_{f\ out}}$$

feedback factor

$$V_{in} = V_s - V_f$$

$$A_f = \frac{V_{out}}{V_s} = \frac{V_{out}}{V_{in} + V_f} = \frac{V_{out}/V_{in}}{1 + \frac{V_f}{V_{in}}} = \frac{A_v}{1 + \beta \cdot A_v}$$

voltage series negative feedback

$$A_f = \frac{A_v}{1 + \beta \cdot A_v} \rightarrow \text{negative feedback}$$

$$A_f = \frac{A_v}{1 - \beta \cdot A_v} \rightarrow \text{positive feedback}$$

ADVANTAGES OF NEGATIVE FEEDBACK:

- (1) Stability of the gain improves by the factor $(1 + A_v \beta)$
- (2) Distortion reduced by $(1 + A_v \beta)$
- (3) noise decreases by $(1 + A_v \beta)$
- (4) Bandwidth increases by $(1 + A_v \beta)$
- (5) Z_{in} (input impedance) increases by $(1 + A_v \beta)$

(6) Output impedance decreases by $(1+A_V\beta)$

(7) It provides gain control.

$\beta \rightarrow$ feedback factor

$(1+A_V\beta) \rightarrow$ amount of feedback

FORMULAS:

$$(1) D_f = \frac{D}{1+A_V\beta}$$

distortion with
feedback

distortion without feedback

$$(2) A_N f = \frac{N}{1+A_B}$$

$$(3) BW_f = BW(1+A_B)$$

$$(4) Z_{inf} = Z_{in}(1+A_B)$$

$$(5) Z_{af} = \frac{Z_0}{1+A_B}$$

(Q) Prove that stability of the gain of an amplifier with negative feedback improves by a factor $(1+A_B)$, compared to that of amplifier without feedback, where A is the open loop gain, and β is the feedback factor.

$$(A) A_f = \frac{A}{1+A_B} \quad (\text{differentiate both sides w.r.t. } A)$$

$$\frac{d(A_f)}{dA} = \frac{1(1+A_B) - A(\beta)}{(1+A_B)^2} = 1$$

$$\frac{d(A_f)}{dA} = \frac{dA}{(1+A_B)^2} \quad (\text{divide both sides by } A_f)$$

$$\frac{d(A_f)}{dA} = \frac{1}{A_f} \circ \frac{dA}{(1+A_B)^2} \quad (\text{substitute } A_f)$$

$$\Rightarrow \frac{d(A_f)}{dA} = \frac{dA}{A_f(1+A_B)^2} \quad (\text{cancel out } dA})$$

$$\Rightarrow \frac{d(A_f)}{dA} = \frac{1}{A_f(1+A_B)^2} \quad (\text{cancel out } dA})$$

changes with temperature parameters

important relation for stability

Here $\frac{dA_f}{A_f}$ represents fractional change in amplification with feedback.

 A_f

$\frac{dA}{A}$ represents fractional change in amplification without feedback. (This A is a temperature dependent parameter)

- (a) An voltage amplifier has open loop gain (A_f) of 500 and gain stability of 1% due to temperature variations. If 1% negative feedback is given then the gain stability of the amplifier with feedback is

$$(A) \frac{d(A_f)}{A_f} = 0.12 \times \frac{1 + 500(0.01)}{1 + 500(0.01)} \approx 0.02 \approx 2\%$$

- (b) An amplifier has gain of 60dB, bandwidth of 500kHz, distortion $\rightarrow 16\%$, input impedance $50\text{ k}\Omega$, output impedance (Z_o) = $100\text{ }\Omega$. If 3% negative feedback is given, determine bandwidth, distortion, input impedance (Z_{in}) and gain of the amplifier with feedback.

$$(A) P_f = \frac{0.16}{1 + \frac{1000}{60 \times 0.03}} = 5.16 \times 10^{-3}$$

$$A_f = 20 \log_{10} \left(\frac{V_o}{V_i} \right)$$

$$BW_f = 500 \times 10^3 \left(1 + 1000 \times 0.03 \right) = 15500000 \approx 15.5 \text{ MHz}$$

$$Z_{in} = 50 \times 10^3 \left(1 + 1000 \times 0.03 \right) = 1550000 \approx 1.55 \text{ M}\Omega$$

$$Z_o = \frac{400}{1 + 1000 \times 0.03} = 12.9 \text{ }\Omega$$

$$A_f = \frac{A_v}{1 + \beta A_v} = \frac{1000}{1 + 0.03 \times 1000} = 32.25$$

- (c) An amplifier has an open loop gain of 8000, input impedance $= 100\text{ k}\Omega$; $Z_o = 10\text{ k}\Omega$; distortion $= 15\%$; gain stability $= 20\%$, bandwidth $= 500\text{ kHz}$, noise $= 1\text{ pV}$. By giving negative feedback, the Z_{in} needs to be increased to $2.2\text{ M}\Omega$. Determine the feedback factor required, also find gain, Z_{in} , Z_o , BW , N_D of the closed loop amplifier.

(A)

$$2 \cdot 2 \times 10^6 = 100 \times 10^3 (1 + 8000\beta)$$

$$2 \cdot 2 \times 10^6 = 1 + 8000\beta$$

$$100 \times 10^3$$

$$22 = 1 + 800\beta$$

$$21 = 800\beta$$

$$\beta = 21 = 2.625 \times 10^{-3}$$

8000

$$Z_{out} = 100 \times 10^3 (1 + 8000 \times 2.625 \times 10^{-3}) = 2200000$$

$$Z_0 = 10 \times 10^3$$

$$= 154.54 \times 10^3 = 154540 \Omega$$

$$1 + 8000 \times 2.625 \times 10^{-3}$$

$$BW = 500 \times 10^3 (1 + 8000 \times 2.625 \times 10^{-3}) = 11000000$$

$$N_f = 1 \times 10^{-6}$$

$$= 4.54 \times 10^{-8}$$

$$\beta_f = 0.15$$

$$= 6.89 \times 10^{-3}$$

$$d(A_f) = 0.20$$

$$= 9.09 \times 10^{-9}$$

$$A_f = 1 + 8000 \times 2.625 \times 10^{-3}$$

~~(3) $V_o = 10 \text{ mV}, A_f = 40 \text{ dB}, A_v = ??, \beta = 23$~~

$$A_v = V_{out} ; A_f = V_{out}$$

 V_{in} V_s 2.00×10^{-3} 0.001 $\text{A} = 10$

$$V_{out} = A_v \cdot V_{in} = A_v \cdot 10 \times 10^{-3}$$

$$A_f = \sqrt{10} \approx 3.16 \text{ (A)}$$

$$100 = A_f = \frac{A_v \cdot 10 \times 10^{-3}}{4}$$

$$A_v = \frac{100 \times 4}{10 \times 10^{-3}} = 40 \times 10^3$$

$$= 4 \times 10^2$$

$$A_f = A_v \cdot (1 + \beta \cdot A_v)$$

$$(1 + \beta \cdot A_v)$$

$$\Rightarrow 100 + 100 \cdot \beta \cdot 4 \times 10^{-2} = 4 \times 10^{-2}$$

$$4 \times 10^{-2} - 100 = 4\beta$$

$$\beta = \frac{(4 \times 10^{-2} - 100)}{4} = -24.99$$

A

$$(1) V_{in} = 2 \times 10^{-3} V; V_{out} = 10 V; V_s = 200 \times 10^{-3} V$$

$$A_v = \frac{V_{out}}{V_{in}} = \frac{10}{2 \times 10^{-3}} = 5000 = 73.97 \text{ dB}$$

$$A_f = \frac{V_{out}}{V_s} = \frac{10}{200 \times 10^{-3}} = 50 = 33.97 \text{ dB}$$

The amount of feedback =

$$1 + AB$$

$$50 = \frac{5000}{1 + AB} \Rightarrow 50 + 50AB = 5000 \quad (1)$$

$$1 + \beta \cdot 5000 \quad 5000 \times 50 \times \beta = 5000 - 50$$

$$\beta = \frac{(5000 - 50)}{(5000 \times 50)} = 0.0198 \quad (2)$$

$$(5000 \times 50)$$

$$A_f = 20 \log_{10}(50) \quad (3)$$

$$A_f = 33.97 \text{ dB}$$

$$(3) V_i = 10 \text{ mV}; A_v = 40 \text{ dB}; \frac{V_o}{V_i} = A \cdot 10 \text{ mV}.$$

$$A_f = \frac{A}{1 + AB} \Rightarrow A_f = \frac{10 \text{ mV} \cdot A_v}{1 + AB} \Rightarrow A_f = 2.5 \text{ mV} \cdot A_v \quad (1)$$

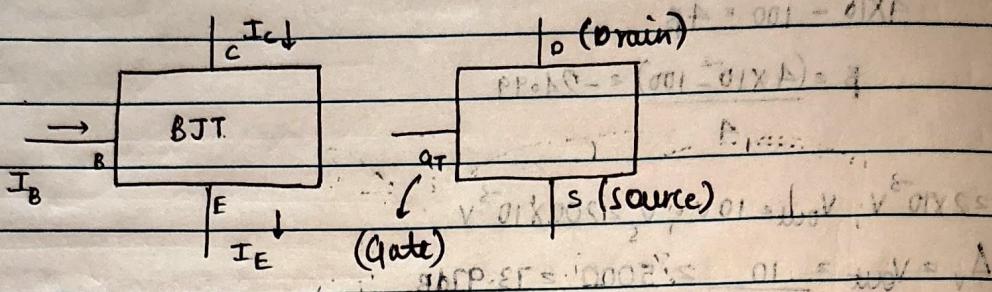
$$20 \log \left(\frac{A}{1 + AB} \right) = 40$$

$$\frac{A}{1 + AB} = 100$$

switch and amplifier
voltage controlled device while BJT \rightarrow current controlled

MOSFET: (Metal Oxide Semiconductor Field Effect Transistor)

An field effect transistor, either holes (or) electrons are responsible for conduction.



The comparison b/w BJT and MOSFET

= ~~BJT~~ ~~BJT to MOSFET~~

FIELD EFFECT TRANSISTOR

- | | |
|---------------------------------------|--|
| (1) BJT are current controlled device | (2) MOSFET are voltage controlled device |
| (2) Low input impedance | (2) High input impedance |
| (3) Bipolar device | (3) Unipolar device |
| (4) Larger size | (4) Smaller size |
| (5) Positive cost is more | (5) Lower cost |
| (6) Higher speed | (6) Lower speed |
| (7) Thermal runaway occurs | (7) Thermal runaway does not occur |
| (8) Less temperature stable | (8) More temperature stable |

CLASSIFICATION OF MOSFET

(1) Enhancement type MOSFET

(a) NMOS \rightarrow

(b) PMOS \rightarrow

(2) Depletion type MOSFET

difference is Enhancement \rightarrow no channel

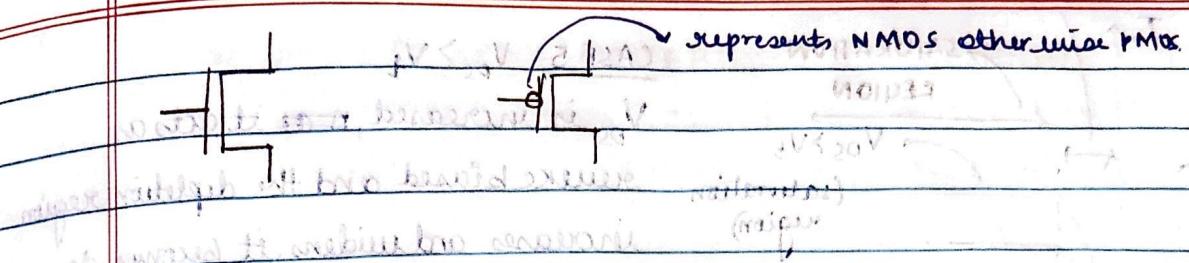
SYMBOLIC REPRESENTATION OF NMOS AND PMOS:

NMOS

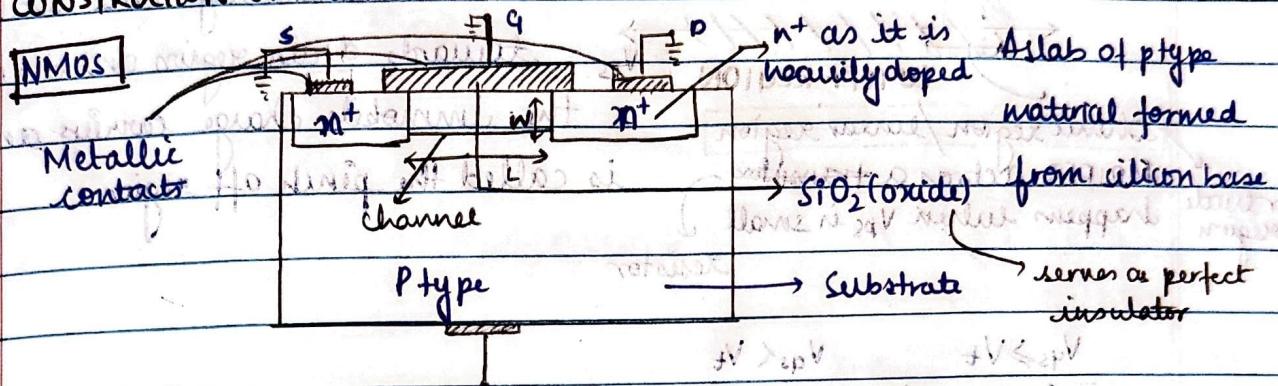


PMOS





CONSTRUCTION OF MOSFET:



CASE 1: When no external voltage is given ($V_{GS} = 0$)
It acts in cutoff region and is an open switch.

CASE 2: When V_{GS} has a small value ($|V_{GS}| < V_t$)

$I_d = 0$ as SiO_2 acts as a perfect insulator. There is a differentiation of the charge in the n^+ region and the p-type. (n^+ contains more e^- and p-type has more holes)

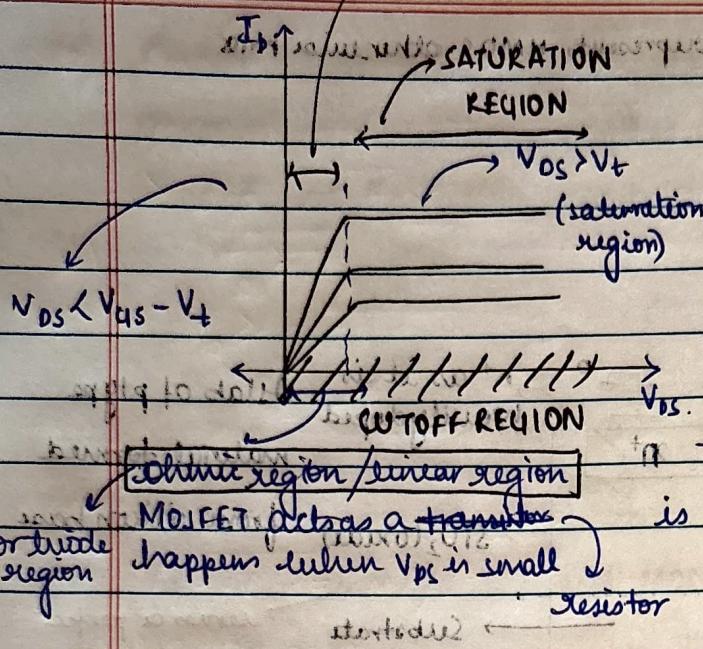
CASE 3: When $V_{GS} \geq V_t$ (threshold voltage)
 V_t is the threshold voltage specified by the manufacturer, and for the induction of the channel $V_{GS} = V_t$.

CASE 4: When V_{DS} has a small value.
 I_D starts flowing from drain terminal to the source terminal. Dirⁿ of electron current is opposite to the conventional current. When V_{DS} is activated a channel which was induced when $V_{GS} = V_t$, allows I_D to flow through the device.

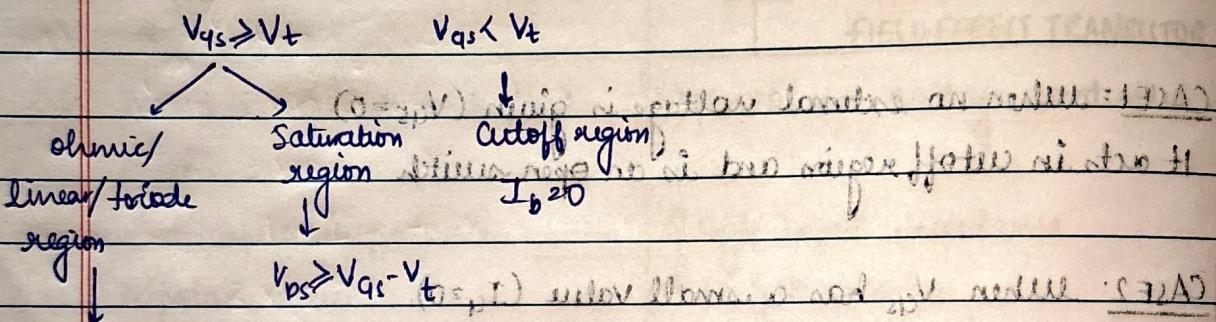
OUTPUT CHARACTERISTICS: I_D vs V_{DS} keeping input voltage is constant

Invertor characteristics of inverter

OHMIC REGION

CASE 5: $V_{DS} > V_T$

V_{DS} is increased, so it acts as reverse biased and the depletion region increases and widens, it becomes deep towards source region and shallow towards drain region and it contains the immobile charge carriers and it is called the **pinch off region**.



$$\text{Ohmic region: } (I_D) = K [(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2]$$

$$\text{Saturation region: } (I_D) = K \left[\frac{V_{GS} - V_T}{2} \right]^2 \quad \text{where } K \text{ is the proportionality constant}$$

$$K = A/V^2 \quad \text{where } A \text{ is the area of the gate contact}$$

TRANSCONDUCTANCE:

$$g_m = K [V_{GS} - V_T], \text{ unit is Siemens/mho. } 25 \text{ mho} \approx 25 \text{ S}$$

LINEAR RESISTANCE: $R_L = \frac{1}{g_m} = \frac{1}{K(V_{GS} - V_T)}$ value will increase as V_{GS} increases

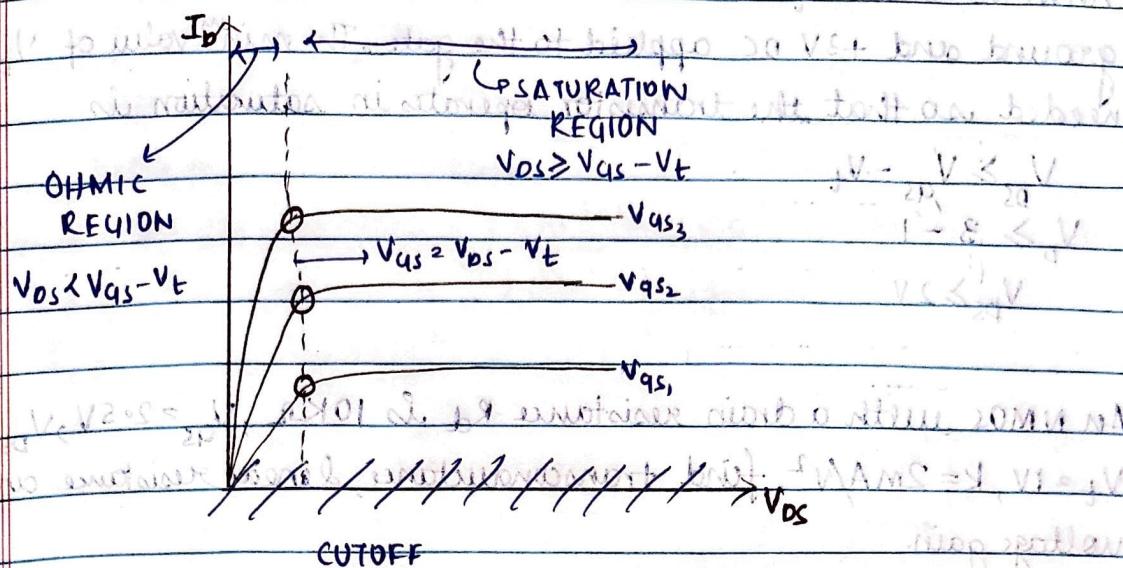
$$g_m = K [V_{GS} - V_T]$$

VOLTAGE GAIN: (N channel MOSFET) $A_V = -g_m \cdot R_{DS}$

$$A_V = -g_m \cdot R_{DS} \rightarrow (-) \text{ for } 180^\circ \text{ phase shift}$$

analogous to collector resistance

OUTPUT CHARACTERISTICS OF MOSFET



(Q) An NMOS having $V_t = 0.5V$, $K = 2\text{mA}/V^2$, $V_{GS} = 2V$; $V_{DS} = 1V$, $I_D = ?$

$$\begin{aligned}(A) \quad I_D &= K \left[(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \\ &= 2 \times 10^{-3} \left[1.5 \times 1 - \frac{1}{2} \times 1 \right] \\ &= 2 \times 10^{-3} [1.5 - 0.5] \\ &= 2 \times 10^{-3} \text{ A}\end{aligned}$$

(Q) An NMOS whose $V_t = 1V$, $K = 2\text{mA}/V^2$, is operating in saturation with $I_D = 4\text{mA}$, find V_{GS} and transconductance.

$$(A) \quad 4 \times 10^{-3} = 2 \times 10^{-3} [V_{GS} - 1]^2$$

$$\begin{aligned}&\Rightarrow 2 \times 10^{-3} = 2 \times 10^{-3} [3 - 1]^2 \\ &\Rightarrow g_m = 2 \times 10^{-3} \text{ mho.}\end{aligned}$$

(Q) An NMOS transistor, with $V_t = 1V$ is biased such that $V_s = 2V$, $V_d = 4V$. The maximum value of V_b allowed so that the transistor operates in ohmic region is

$$\begin{aligned}(A) \quad V_b - 2 &< 4 - 2 - 1 \\ &\Rightarrow V_b - 2 < 4 - 3 \\ &\Rightarrow V_b - 2 < 1 \\ &\Rightarrow V_b < 3V.\end{aligned}$$

(Q) An NMOS with $V_t = 1V$ has its source terminal connected to ground and +3V DC applied to the gate. The min^m value of V_b needed so that the transistor operates in saturation is

(A) $V_{DS} \geq V_{GS} - V_t$
 $V_b \geq 3 - 1$
 $V_{BS} \geq 2V$

(Q) An NMOS with a drain resistance R_d is $10K\Omega$, $V_{GS} = 2.5V$, $V_{DS} = 4.5V$, $V_t = 1V$, $k = 2mA/V^2$, find transconductance, linear resistance and voltage gain.

(A) $g_m = 2 \times 10^{-3} [2.5 - 1]$

$$= 2 \times 10^{-3} \times 1.5 \quad [V_{GS} - V_t] = 1, V_D = 0 = V_{DS}$$

$$R_{DS} = \frac{1}{3 \times 10^{-3}} \quad [1 \times 10^{-3} \times 10^4] = 100 \Omega$$

$$A_v = \frac{2 \times 10^{-3} \times 1}{3 \times 10^{-3}}$$

ANSWER: $V_{DS} = 4.5V$, $V_t = 1V$, $R_d = 10K\Omega$

TUTORIAL:

(1) $V_t = 0.8V$; $k = 2mA/V^2$

(a) $V_{GS} = 5V$; $V_{DS} = 2V$

$\rightarrow V_{DS} \leq V_{GS} - V_t \rightarrow$ ohmic region

$\rightarrow 2 \leq 5 - 0.8$

$2 \leq 4.2V$

$$I_D = K [V_{GS} - V_t] \cdot V_{DS} - \frac{1}{2} (V_{DS})^2$$

$$V_D = 2V, V_{GS} = 5V, V_t = 0.8V \Rightarrow 2 \times 10^{-3} \times [4.2 \times 1 - 0.8] = 1.2mA$$

(c) $V_{GS} = 2V$; $V_{DS} = 1.2V$

$V_D = 1.2V$ \rightarrow Cutoff region

(d) $V_{GS} = V_{DS} = 3V$

$$V_t = 0.8V$$

$$\rightarrow 3 - 0.8$$

$$\geq 2.2mA$$

$$E - A > C - V$$

$$1 > C - V$$

$$NE > V$$

$$(2) V_t = 1V; I_d = 100 \times 10^{-6} A; V_{GS} = V_{BS} = 1.5V; V_{BS} > V_{GS} - V_t$$

$$I_p \rightarrow V_{GS} = 2.5V; V_{DS} = 1V$$

$$100 \times 10^{-6} = k [1.5 - 1]^2$$

$$100 \times 10^{-6} = \frac{2}{k} \times 0.5 \times 0.5$$

$$k = \frac{200 \times 10^{-6} \times 100}{25} = \frac{2 \times 10^{-4}}{25} = 0.8 \text{ mA/V}^2$$

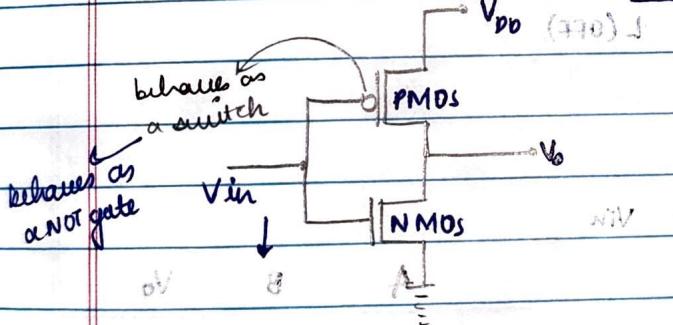
$$I_D = \frac{0.8 \times 10^{-3}}{2} [2.5 - 1]^2$$

$$= \frac{0.4}{2} \times 1.5 \times 1.5 = 0.9 \text{ mA}$$

$$V_{GS} = 3V; r_{ds} = \frac{10V}{0.8 \times 10^{-3} [3.5]} = 12.5 \text{ M}\Omega$$

CMOS INVERTER:

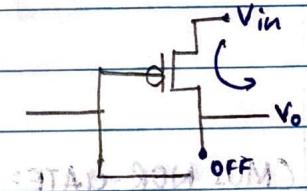
CASE 1: $V_{in} = \text{low}$.



NMOS = off

PMOS = on

$$V_o = V_{dd}$$



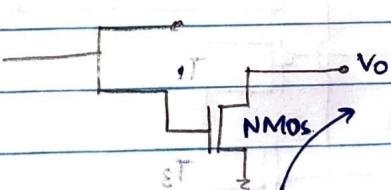
Equivalent circuit

CASE 2: $V_{in} = \text{high}$

① PMOS = off

② NMOS = on

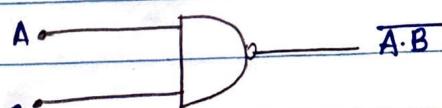
$$V_o = \text{Ground (0)}$$

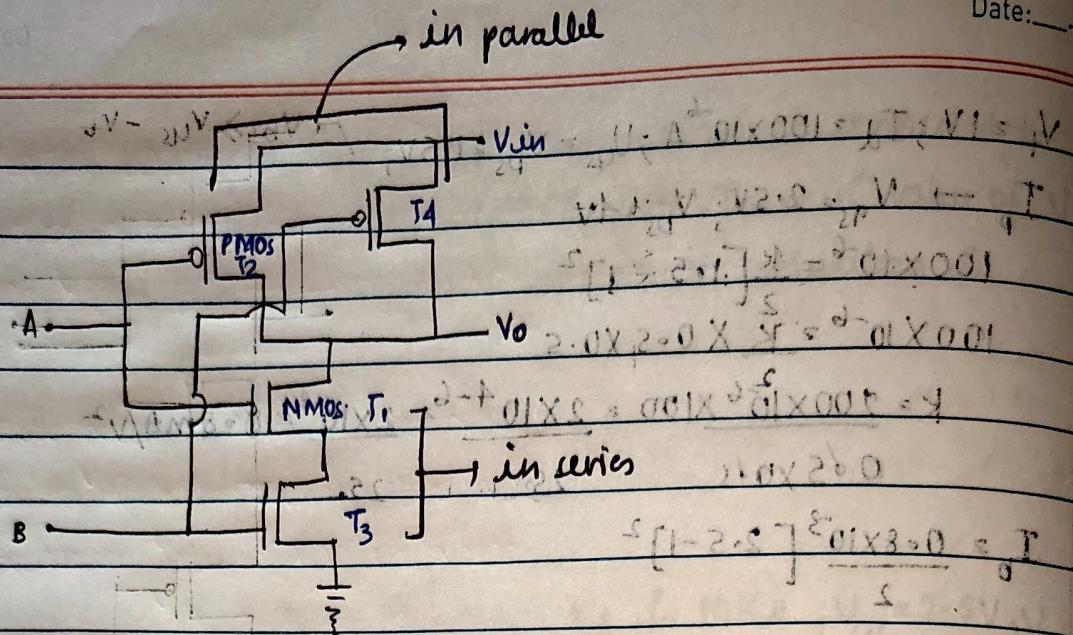


Equivalent circuit

CMOS NAND GATE:

A	B	V_o
0	0	1
0	1	0
1	0	0
1	1	0

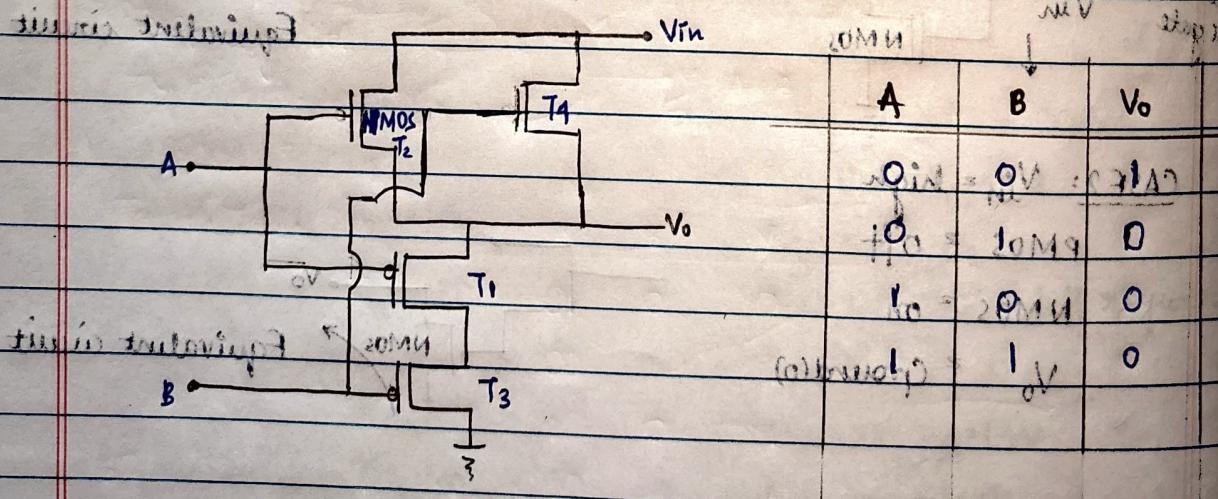




A	B	T ₁	T ₂	T ₃	T ₄	OUTPUT
Low	Low	L(OFF)	H(ON)	L(OFF)	H(ON)	V _{DD}
Low	High	L(OFF)	H(ON)	H(ON)	L(OFF)	V _{DD}
High	Low	H(ON)	L(OFF)	L(OFF)	H(ON)	V _{DD}
High	High	H(ON)	L(OFF)	H(ON)	H(ON)	0.

W/L = 1/2A
H₀ = 20MHz

CMOS NOR GATE:



MOSFET AS AN AMPLIFIER:

9.5

A

1

0

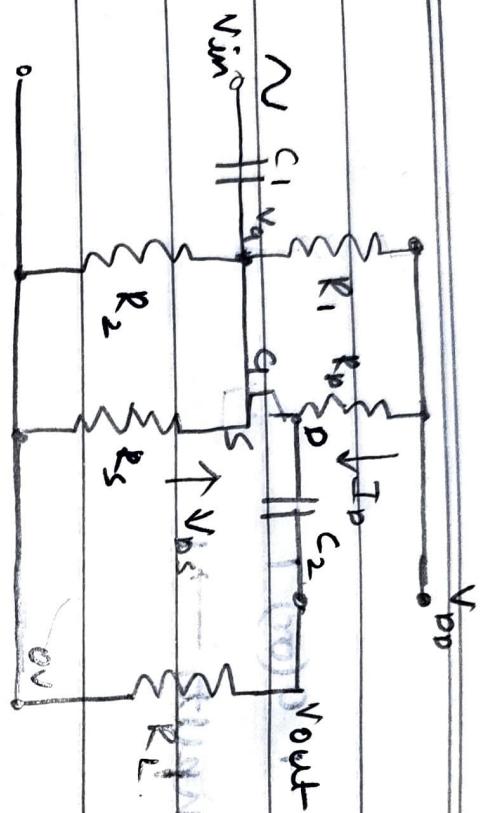
0

0

0

apsara

Date: _____



NMOSFET as an amplifier

10k and 10k + 10k

DIGITAL LOGIC → logic gates

- analog → continuous while digital → 0 (off) / 1
- XOR → like inputs → 0; unlike inputs → 1

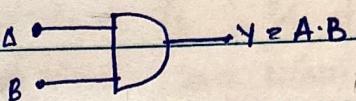
Basic gates → AND, OR and NOT

Universal gates → NAND and NOR

Exclusive gates → XOR and XNOR

(1) logic expression: $A \cdot B$ (AND) $A \cdot B = Y$

Logic symbol:

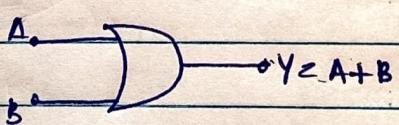


Truth table :

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

(2) logic expression: $A + B = Y$

Logic symbol:



Truth Table :

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

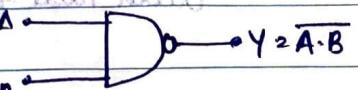
(3) logic expression: $\bar{A} = Y$

Logic symbol:



Truth Table:

	A	B	Y
0	-	1	1
1	-	0	0

(4) logic expression: $Y = \overline{A \cdot B}$ logic symbol: 

NOT of NOT

Y	A	B	A	B	Y	A	B	A
1	0	0	0	0	1	1	0	0
1	0	1	0	0	1	1	0	1
1	1	0	0	1	1	1	0	1
0	0	0	1	1	0	0	1	1
1	1	0	1	1	0	0	0	0

(5) logic expression: $Y = \overline{A + B}$ logic symbol: 

NOT of OR

 $\overline{A \cdot A} = \overline{A + A}$

Truth table:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0
0	1	0
0	0	1

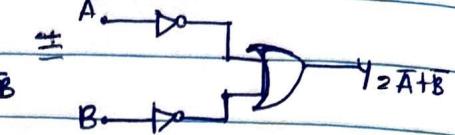
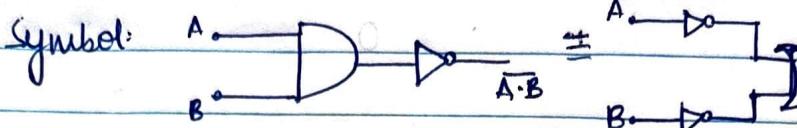
1st LAW: Complement of the product is equal to sum of the individual components1st LAW: $A \cdot B = \overline{\overline{A} + \overline{B}}$ 2nd LAW: Complement of the sum is equal to product of the individual components2nd LAW: $\overline{A + B} = \overline{A} \cdot \overline{B}$

step may give step for writing

(Q) Prove the 1st LAW:

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

Symbol:

 $\overline{A} = Y$ indicates true signal

Truth table for LHS:

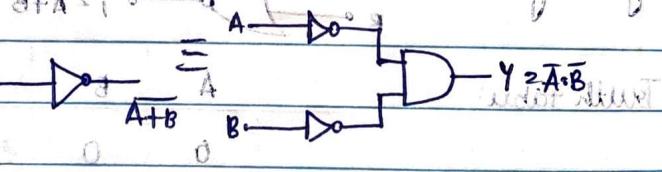
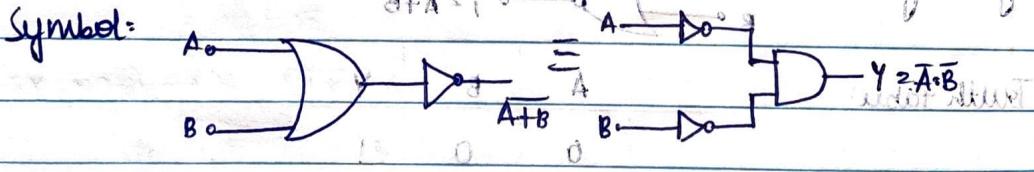
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0
		0

A	B	\overline{A}	\overline{B}	$Y = \overline{A} + \overline{B}$
0	0	1	1	1
0	1	1	0	1
1	0	0	1	1
1	1	0	0	0
		1	1	1

(Q) Prove the 2nd LAW:

$$\overline{A + B} = \overline{A} \cdot \overline{B}$$

Symbol:



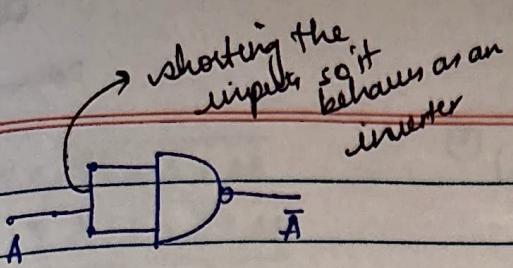
Truth table for LHS:

A	B	Y
0	0	1
0	1	0
1	0	0

Truth table for RHS:

A	B	Y
0	0	1
0	1	0
1	0	0

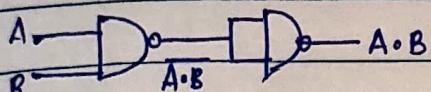
- (*) REALISATION OF BASIC GATES USING UNIVERSAL GATES : TFA
- Realisation of NOT gate using NAND gate



$$A \bar{A} = 1 \quad (1)$$

$$A \cdot (\bar{A} \cdot \bar{A}) = A \cdot 0 = 0 \quad (2)$$

(2) Realisation of AND gate using NAND gate.

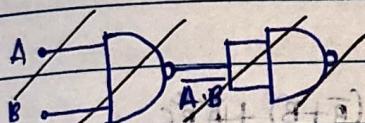


$$A \bar{A} \bar{B} = A \cdot B \quad (3)$$

$$(A \bar{A}) \bar{B} = A \cdot B \quad (4)$$

$$A \cdot B$$

(3) Realisation of OR gate using NAND gate



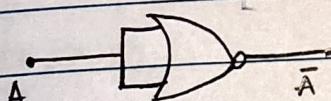
$$A \bar{A} \bar{B} + \bar{A} \bar{B} \bar{A} + \bar{A} \bar{B} = A + B \quad (1)$$

$$[A \bar{A} + \bar{A} \bar{B}] \bar{A} =$$

$$[A \bar{A} + \bar{A} \bar{B}] \bar{A} =$$

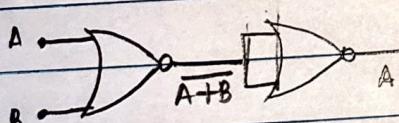
$$[A + B] \bar{A} =$$

(4) Realisation of NOT gate using NOR gate



$$A \oplus A = 0 \quad (5)$$

(5) Realisation of AND gate using NOR gate



$$A \bar{A} \bar{B} =$$

$$A \oplus \bar{A} = V \leftarrow (01)X$$

(6) $\bar{A} = A$

$$(\bar{A} + X)\bar{Y} + (\bar{A} + Y)\bar{X} =$$

$$\bar{Y}X + (\bar{A} + Y)X =$$

$$(\bar{A} + \bar{Y}X + Y)X =$$

$$(\bar{A} + \bar{Y}A + YA) = V \quad (6)$$

$$[(\bar{A} + \bar{Y}) + YA]A =$$

$$[(\bar{A} + Y) + YA]A =$$

$$[(\bar{A} + Y) + YA]A =$$

$$[(\bar{A} + Y) + YA]A =$$

BOOLEAN LAWS:

$$\bar{\bar{A}} = A$$

AND LAWS:

$$\bar{0} = 1$$

$$A \cdot 0 = 0$$

OR LAWS: $(\bar{A} + A)(A + \bar{A}) = 1 \quad (7)$

$$\bar{1} = 0$$

$$A \cdot 1 = A$$

$$A + 0 = A$$

$$(\bar{A} + A) = A$$

$$A \cdot A = A$$

$$A + 1 = 1$$

$$A \cdot \bar{A} = 0$$

$$A + \bar{A} = 1$$

POSTULATES

(1) $A + AB$

$$A(I+A) \stackrel{!}{=} A(I) = A$$



(2) $A + \bar{A}B$

$$\downarrow A + AB + \bar{A}B$$

$$A + B(A + \bar{A})$$

$$A + B$$



stop Anna can stop DNA to multiplication

stop Anna can stop DNA to multiplication

(*) SIMPLIFICATION OF BOOLEAN EXPRESSION:

(1) $ABC + \bar{A}BC + \bar{A}BC$

$= \bar{A}[B\bar{C} + B\bar{C} + BC] \quad \text{MAM'S WAY: } \bar{A}\bar{C}(\bar{B} + B) + \bar{A}BC$

$\Rightarrow \bar{A}\bar{C} + \bar{A}BC$

$= \bar{A}[\bar{C} + BC]$

$\Rightarrow \bar{A}[\bar{C} + BC] \quad \text{stop Anna can stop DNA to multiplication}$

$\Rightarrow \boxed{A + AB = A + B}$

EX(OR) $\rightarrow Y = A \oplus B$

$= \bar{A}B + A\bar{B} \quad \text{stop Anna can stop DNA to multiplication}$

EX(NOR) $\rightarrow Y = \bar{A} \oplus \bar{B}$

$= \bar{A}\bar{B} + A\bar{B}$

(2) $Y = ABC + A\bar{B}C + A\bar{B}\bar{C}$

$\Rightarrow A[B\bar{C} + \bar{B}C + \bar{B}\bar{C}]$

$\Rightarrow A[C(B + \bar{B}) + \bar{B}\bar{C}]$

$\Rightarrow A[C + \bar{B}\bar{C}]$

$\Rightarrow A[C + B]$

(3) $f = XY + XYZ + XY\bar{Z} + X\bar{Y}Z$

$\Rightarrow XY[1 + \bar{Z}] + YZ[X + \bar{X}]$

$\Rightarrow XY[1 + \bar{Z}] + YZ$

$\Rightarrow Y[X + X\bar{Z} + Z]$

$\bar{Z} + \bar{Z} + \bar{Z}$

(4) $Y = (A+B)(A+\bar{B})(\bar{A}+B)$

$\Rightarrow (A+B)($

$A = 0 + A$

$0 = 0 \cdot A$

$I = I + A$

$A = I \cdot A$

$A = A + A$

$A = A \cdot A$

$I = \bar{A} + A$

$0 = A \cdot A$

$A = \bar{A}$

$I = \bar{0}$

$0 = \bar{1}$

$$\begin{aligned}
 @1) & Y = \overline{AB} + \overline{A} + AB \\
 & \Rightarrow \overline{A} + \overline{B} + \overline{A} + AB \\
 & \Rightarrow \overline{AB} + \overline{A} + B \\
 & \Rightarrow \overline{A} + \overline{B} + \overline{A} + B \\
 & = \overline{1 + 2\overline{A}}
 \end{aligned}$$

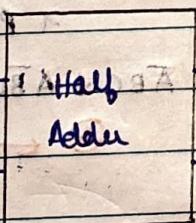
(2)

$$\begin{aligned}
 & Y = \overline{L + M + MN + LN} \\
 & Y = \overline{L \cdot \overline{M}} + \overline{M \cdot \overline{N}} \\
 & \Rightarrow \overline{M} \cdot (\overline{L} + \overline{N}) \\
 & \Rightarrow M + \overline{L} + \overline{N} \\
 & \Rightarrow M + \overline{L + N}
 \end{aligned}$$

$$\begin{aligned}
 @3) & Y = \overline{LM} + \overline{LN} + MN + \overline{LN} \\
 & \Rightarrow \overline{LM} + N(\overline{L} + M) + \overline{LN} \\
 & \Rightarrow \overline{L}(\overline{M} + N) + N(\overline{L} + M) \\
 & \Rightarrow (\overline{L} + M)(\overline{L} + N)
 \end{aligned}$$

0	0	0	0	0
M($\overline{L} + N$) + LN			0	0
M($\overline{L} + N$) + LN			1	0
M \overline{L} + MN + LN			1	0
0M \overline{L} + LN(M+1)			0	1
M \overline{L} + LN			1	0
1	0	0	1	1
1	1	1	1	1

HALF ADDER



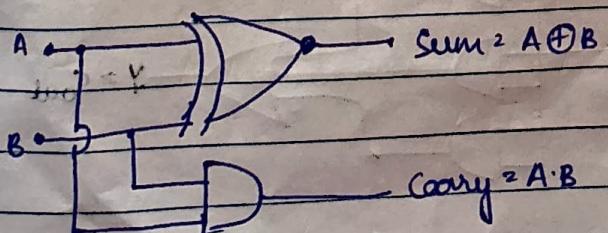
- if output depends on the previous state \rightarrow sequential logic circuit
- if output is independent on the previous state \rightarrow combinational logic circuit.

$$1+0 = (1)_2$$

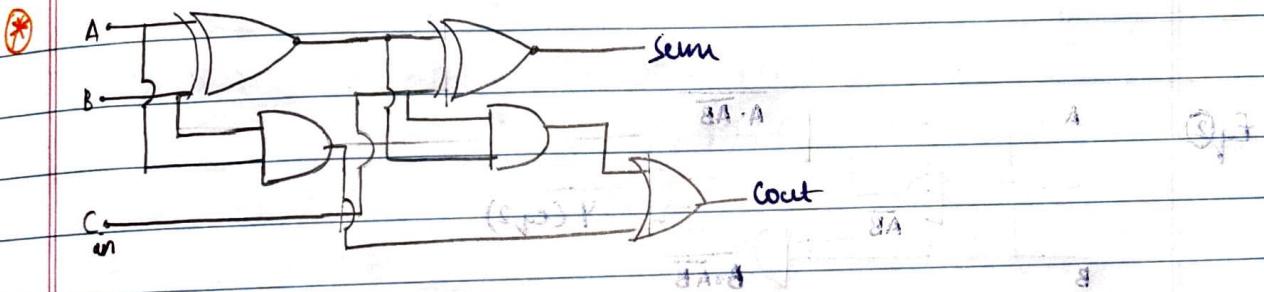
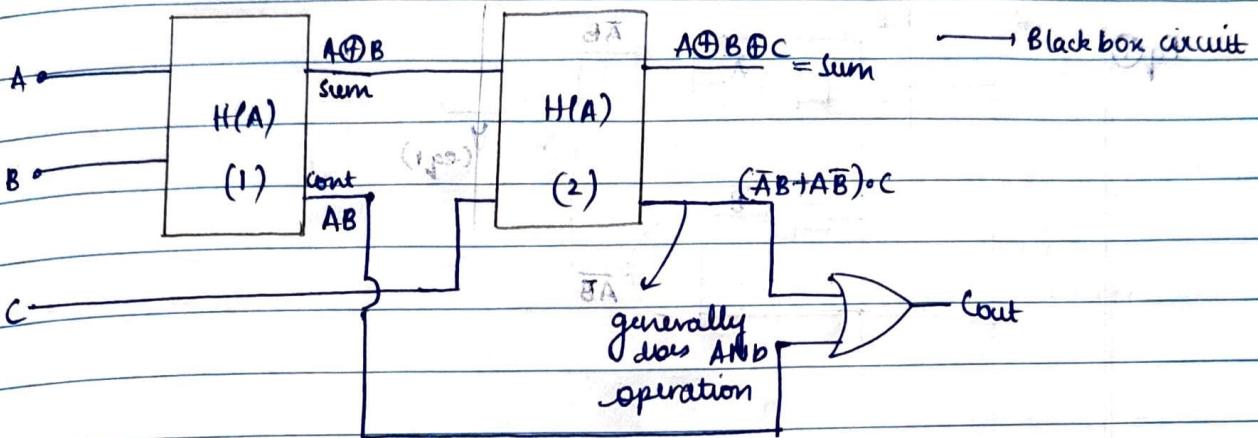
	A	B	Sum	Carry
0+1 = (1) ₂	0	0	0	0
0+0 = (0) ₂	0	1	1	0
1+1 = (10) ₂	1	0	1	0
	1	1	0	1

$$\text{Sum} = A \oplus B$$

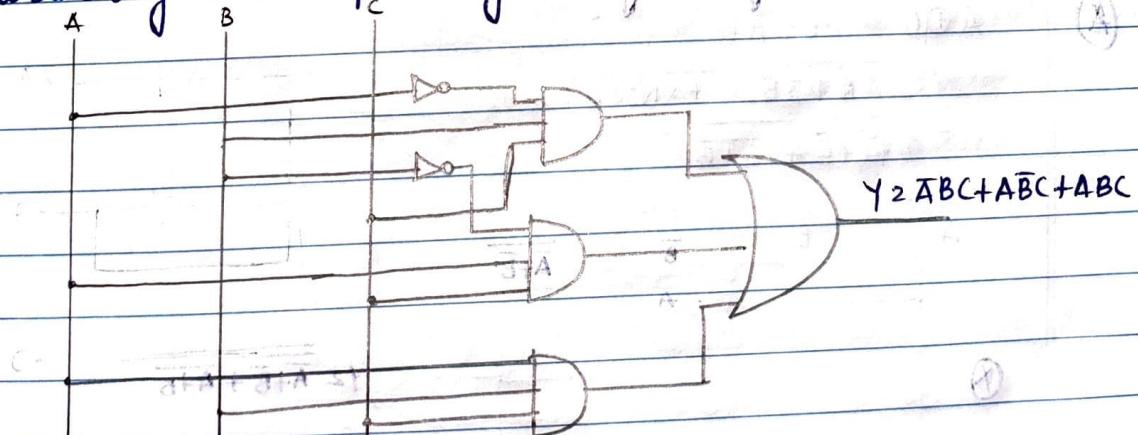
$$\text{Carry} = A \cdot B$$



REALISATION OF FULL ADDER USING TWO HALF ADDERS BY



(Q) Draw the logic circuit for the given expression: $Y_2 = \overline{ABC} + \overline{ABC} + ABC$



REALISATION OF XOR USING NAND GATES (minimum NAND gates)

$$Y = AB + A\bar{B}$$

$$\Rightarrow \overline{AB} + \overline{A\bar{B}}$$

$$\Rightarrow \overline{AB} \cdot \overline{A\bar{B}} \quad \text{--- ① need 5 NAND gates}$$

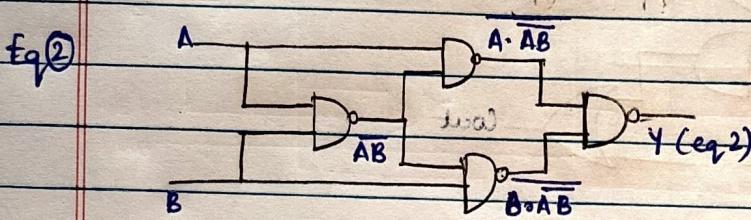
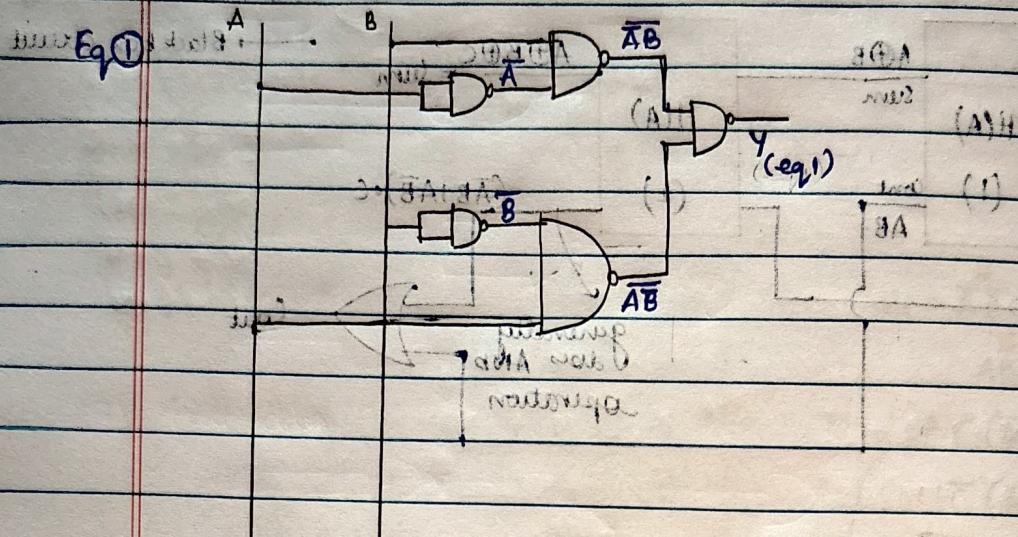
$$\Rightarrow (\overline{A} + B) \cdot (\overline{A} + \overline{B})$$

$$\Rightarrow (\overline{A} + AB) \cdot (\overline{B} + AB)$$

$$\Rightarrow \overline{\overline{A} + AB} \cdot \overline{\overline{B} + AB}$$

Taking double complement

Y₁ A · AB + B · AB \Rightarrow ② 1 NAND gate required



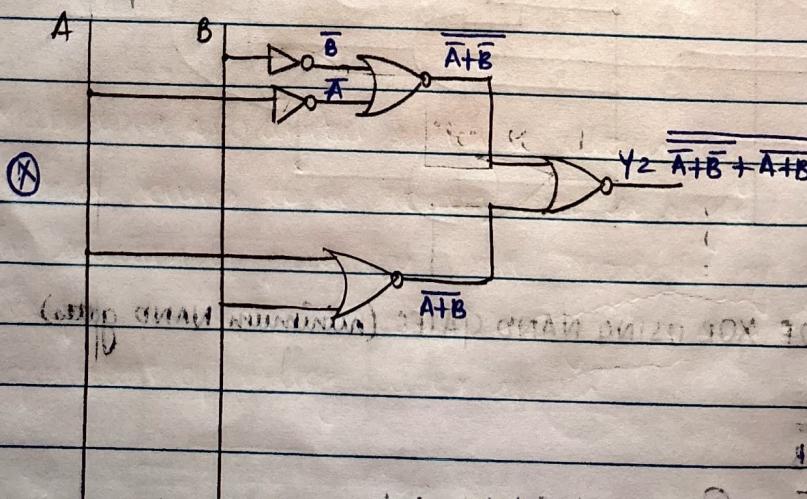
Q (a) Realise XOR using NOR gates.

$$(A) A \oplus B \Rightarrow A\bar{B} + \bar{A}B$$

$$Y_2 \overline{AB + \bar{AB}} = \overline{\text{EX-NOR}} = \text{EX-OR}$$

$$\overline{A + B} + \overline{A + B}$$

~~ABC + ABC + ABC + ABC~~



Q (a) Realise XNOR using minimum NAND gates.

(A)

$$\text{minimum width grid} \quad (\bar{A} + B) \cdot (A + \bar{B}) =$$

$$(\bar{A}B + A\bar{B}) =$$

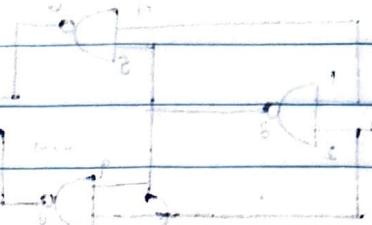
$$Y = \overline{AB + \overline{A}\overline{B}}$$

$$\Rightarrow (\overline{A}\overline{B}) \cdot (\overline{A}B) \rightarrow 5 \text{ gates required}$$

A

B

(X)



Author: Nitin (S)

(Q) Realise XNOR using NOR gates. (minimum) \rightarrow 4 gates

$$(A) Y = AB + \overline{A}\overline{B}$$

$$\Rightarrow \overline{\overline{A} + B} + \overline{A + \overline{B}}$$

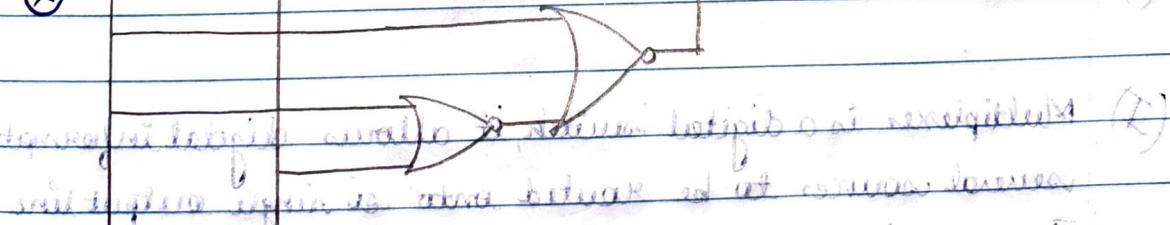
$$\Rightarrow \overline{B + \overline{A}B} + \overline{A + \overline{A}B}$$

$$\Rightarrow (\overline{A + B} + B) + (\overline{A} + \overline{A}B)$$

A

B

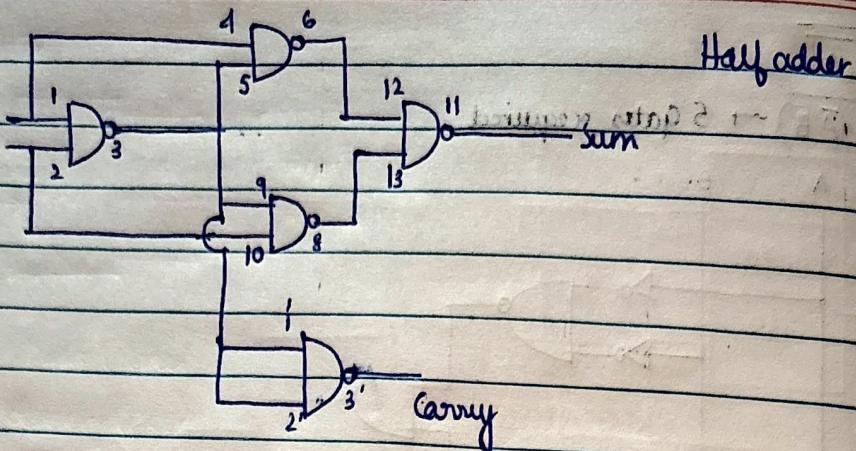
(X)



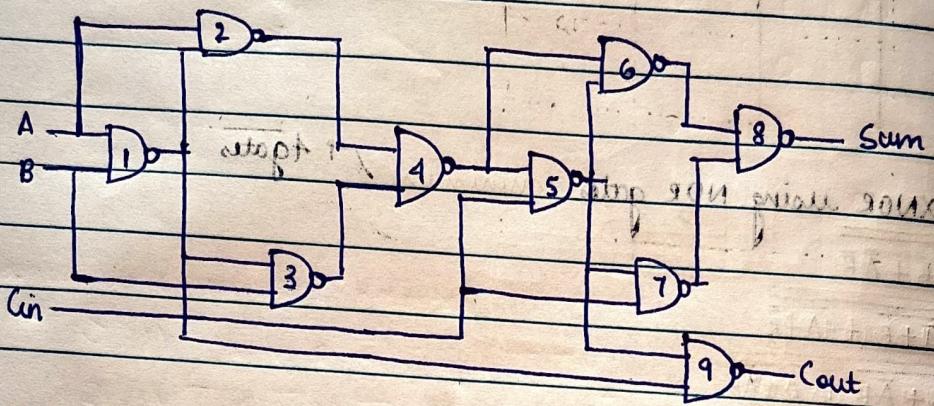
(Q) Realise half adder using only NAND gates. (in column form tabularly)

(Q) Realise full adder using only NAND gates

(1)



(2) Full adder.

**COMBINATIONAL LOGIC CIRCUITS:**

(1) Multiplexer → acts as a digital switch.

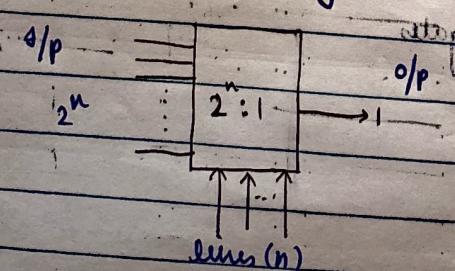
(2) Demux → receiver part of communication

(3) Encoder

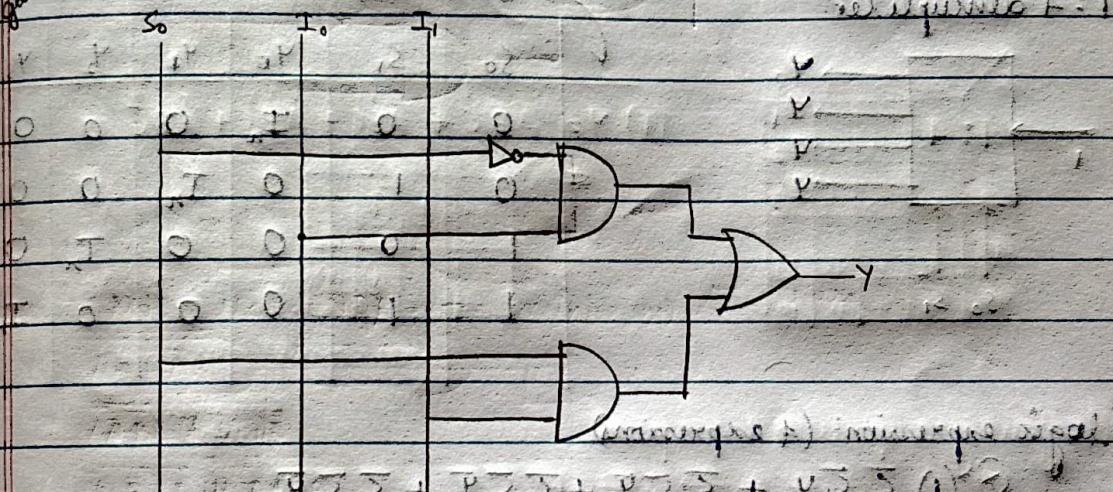
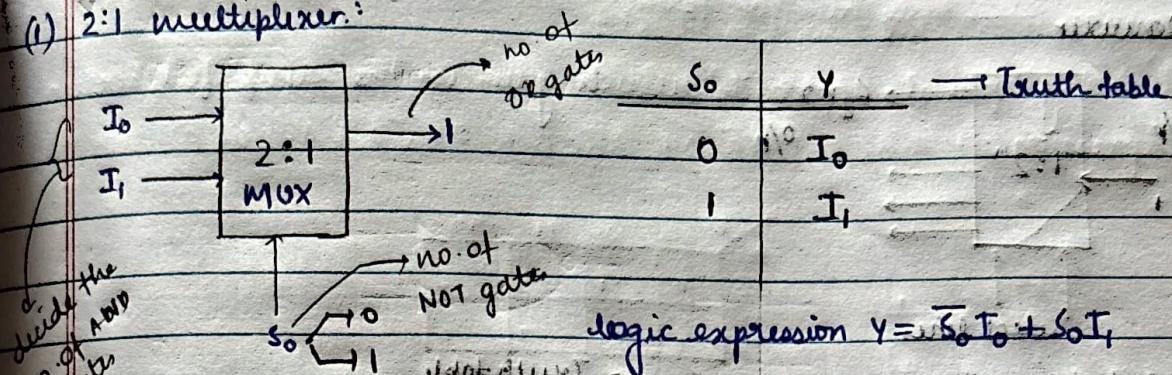
(4) Decoder

(5)

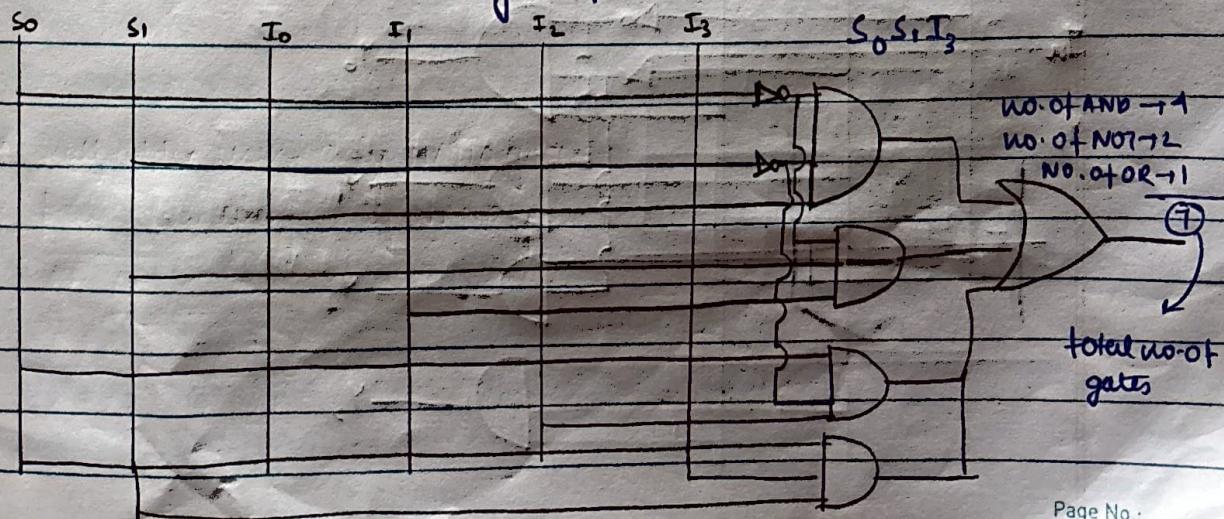
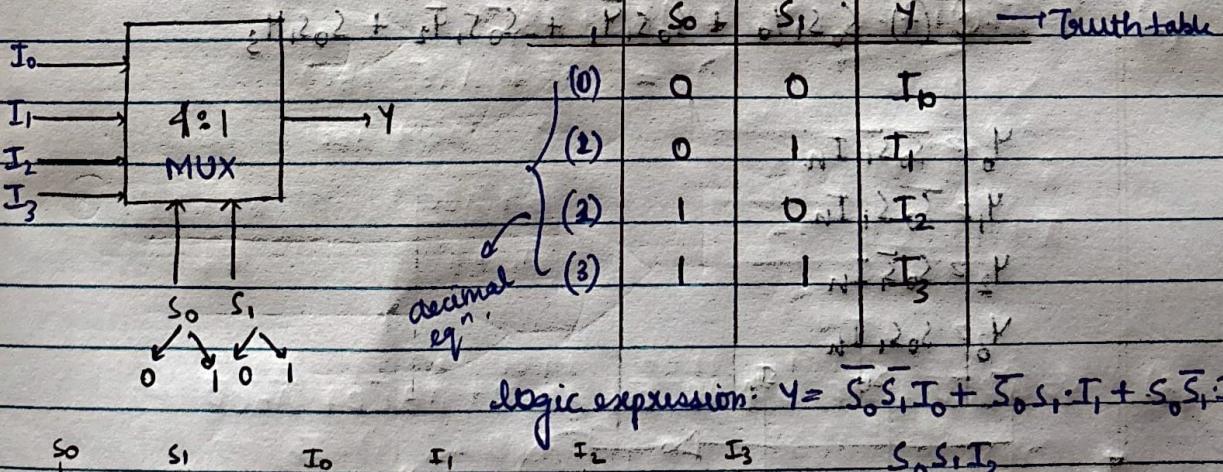
Multiplexer is a digital switch, it allows digital information from several sources to be routed onto a single output line. The selection of particular input is controlled by a set of select lines. Therefore, multiplexer is called many to one and it provides digital equivalent of analog selector switch.



(1) 2:1 multiplexer:

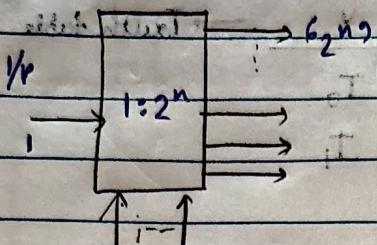


(2) 4:1 multiplexer:



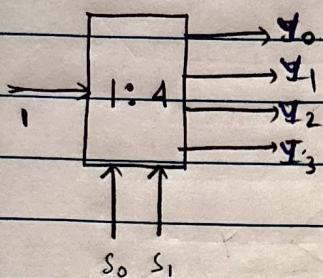
(II)

Demuxer



To select lines & minimize signal.

(i) 1:4 demultiplexer.



Truth-table

S_0	S_1	Y_0	Y_1	Y_2	Y_3
0	0	I_n	0	0	0
0	1	0	I_n	0	0
1	0	0	0	I_n	0
1	1	0	0	0	I_n

Logic expression: (4 expressions)

$$\textcircled{1} \quad (1) \bar{S}_0 \bar{S}_1 Y_0 + \bar{S}_0 S_1 \bar{Y}_1 + S_0 \bar{S}_1 \bar{Y}_2 + S_0 S_1 \bar{Y}_3$$

$$\textcircled{2} \quad \bar{S}_0 S_1 \bar{Y}_0 + \bar{S}_0 S_1 Y_1 + S_0 \bar{S}_1 \bar{Y}_2 + \bar{S}_0 S_1 \bar{Y}_3$$

$$\textcircled{3} \quad S_0 \bar{S}_1 \bar{Y}_0 + S_0 \bar{S}_1 Y_1 + S_0 S_1 \bar{Y}_2 + S_0 S_1 Y_3$$

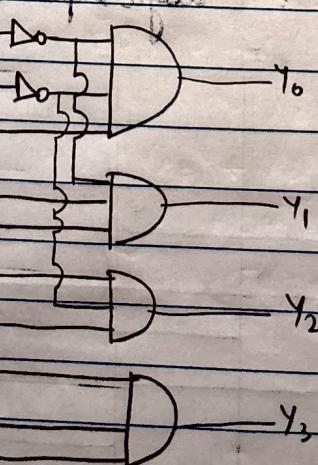
$$\textcircled{4} \quad S_0 S_1 \bar{Y}_0 + S_0 S_1 Y_1 + S_0 \bar{S}_1 \bar{Y}_2 + S_0 \bar{S}_1 Y_3$$

$$Y_0 = \bar{S}_0 \bar{S}_1 I_n$$

$$Y_1 = \bar{S}_0 S_1 I_n$$

$$Y_2 = S_0 \bar{S}_1 I_n$$

$$Y_3 = S_0 S_1 I_n$$



Home

188 → demux.

Tutorial 1

 $B + A\bar{B}$
 $B + \bar{B}A$

(i)(a) $y = ((\bar{A}\bar{B} + ABC) + A(B + \bar{A}\bar{B}))$

⇒ $\bar{A}(B + C) + A(A + B)$

⇒ $\bar{A}\bar{B} + AC + A + AB$

⇒ $\bar{A}\bar{B} + AC + A$

⇒ $AB + AC \cdot \bar{A}$

⇒ $A(B + C) \cdot \bar{A} = 0$

(b) $y = AB + \bar{AC} + \bar{ABC}(AB + C) \quad \exists A = Y(1)$

⇒ $AB + A + \bar{C} + ABC + ABC$

⇒ $(AB + A) + \bar{C}$

⇒ $\bar{A} + B + \bar{C}$

(c) $y_2 = \bar{ABC} + \bar{ABC} + \bar{ABC} + \bar{ABC}$

⇒ $\bar{A}\bar{B} + \bar{A}\bar{B}C + \bar{ABC} + \bar{ABC}$

⇒ $\bar{B}(\bar{A} + \bar{AC}) + \bar{ABC}$

⇒ $\bar{B}(\bar{A} + \bar{C}) + \bar{ABC}$

⇒ $\bar{AB} + \bar{BC} + \bar{ABC}$

⇒ $\bar{AB} + \bar{C}(B + AB)$

⇒ $\bar{AB} + \bar{C}(\bar{A} + \bar{B})$

⇒ $\bar{AB} + \bar{AC} + \bar{CB}$

(d) $y = (\bar{A} + \bar{B} + C) \cdot (\bar{A} + \bar{B} + \bar{C}) \cdot (\bar{A} + B)$

⇒ $(\bar{A} + \bar{B} + C + (\bar{A} + \bar{B} + \bar{C}) + (\bar{A} + B))$

⇒ $(\bar{A} \cdot B \cdot \bar{C} + A \cdot B \cdot C + A \cdot \bar{B})$

⇒ $(B(\bar{AC} + A\bar{C}) + A\bar{B}) + 03A + 03\bar{C} + A\bar{C} + 03\bar{A} + 03\bar{C} \quad (5)$

⇒ $(B(1) + A\bar{B})$

⇒ B

(e) $y = AB + \bar{A}C + \bar{BC}$

→ Karnaugh

KMAPS: → only have SOP form

It is a graphical approach which gives us the simplified Boolean expression

	A	'2'
B	0	0 1
1	2 3	

	A	'2'
B' C	00 01 11 10	
0 1 3 2	1 5 7 6	

	CD
AB	00 01 11 10
00	0 1 3 2
01	4 5 7 6
11	12 13 15 14
10	8 9 11 10

$$(1) Y = \frac{0}{\bar{A}\bar{B}C} + \frac{0}{\bar{A}BC} + \frac{0}{ABC} + \frac{1}{\bar{A}\bar{B}C} + \frac{1}{\bar{A}BC} + \frac{1}{ABC}$$

sum of product form

$$\Rightarrow A \quad \begin{matrix} BC \\ 00 01 11 10 \end{matrix}$$

Pair $Y = \bar{A}C$

$$\begin{matrix} A \\ 0 \\ 1 \end{matrix} \quad \begin{matrix} 0 \\ 1 \\ 3 \\ 2 \end{matrix}$$

Pair $Y = AB$

If you group two 1 → pair
 " " " four 1 → quartet
 " " " 8 1 → octet

you cannot pair 3 and 7
redundant gap

$$(2) Y = \frac{1}{\bar{A}\bar{B}C} + \frac{1}{\bar{A}\bar{B}C} + \frac{1}{\bar{A}BC} + \frac{1}{ABC} + \frac{1}{\bar{A}\bar{B}C} + \frac{1}{\bar{A}BC}$$

	BC	$\bar{B}C$	$B\bar{C}$	BC
A	0	00 01	11 10	
A 1	0	0 0	0 1	

$$\Rightarrow (\bar{A}\bar{B}) + A(\bar{B}\bar{C} + \bar{B}C)$$

$$= \bar{A}\bar{B} + \bar{A}BC \quad \bar{B}\bar{C} + BC$$

$$= (\bar{B} + \bar{A}BC) + (\bar{A} + \bar{B}\bar{C}) \cdot (\bar{B}\bar{C} + BC) = \bar{B}$$

F4

$$(3) Y = \frac{0}{\bar{A}\bar{B}\bar{C}\bar{D}} + \frac{0}{\bar{A}\bar{B}\bar{C}D} + \frac{0}{\bar{A}\bar{B}CD} + \frac{1}{\bar{A}\bar{B}C\bar{D}} + \frac{1}{\bar{A}\bar{B}CD} + \frac{1}{\bar{A}\bar{B}C\bar{D}}$$

$$\Rightarrow \bar{C}\bar{D} + \bar{C}D = \bar{C}(1) \cdot \bar{A}\bar{B}$$

	$\bar{A}\bar{B}$	00		0 1
$\bar{A}B$	0 1	00 01		0 1
AB 11	0 1	0 1		
$A\bar{B}$ 10	0	0 1		

$$= \bar{A}\bar{B}\bar{C}$$

$$\Rightarrow \bar{C}(AB) + \bar{A}\bar{B}\bar{C}$$

$$= \bar{B}\bar{C} + A\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D}$$

$$= \bar{C}(B + AD) + \bar{A}\bar{B}\bar{C}\bar{D}$$

$$(1) Y_2 = \overline{A}\overline{B}CD + A\overline{B}CD + \overline{ABC}\overline{D} + ABC\overline{D} + \overline{ABC}\overline{D} + A\overline{BC}\overline{D} + \overline{ABC}\overline{D} + \overline{ABC}\overline{D}$$

	CD	00	01	11	10
AB	00	01	11	10	
00	1	1	1	1	
01	1	1	1	1	
11	1	1	1	1	
10	1	1	1	1	

→ four corners will make a quadrangle

→ make another quadrant

$$(2) Y_2 = \overline{ABC}\overline{D} + A\overline{BC}\overline{D} + \overline{ABC}D + \overline{ABC}\overline{D} + A\overline{BC}\overline{D} + A\overline{BC}D + ABC\overline{D}$$

	CD	00	01	11	10
AB	00				
00					
01		1	1	1	1
11	1	1	1	1	1
10	1	1	1	1	1

SOF → m; POS → M

$$\Rightarrow f(A, B, C, D) = \sum m(0, 1, 4, 8, 9, 10)$$

	CD	00	01	11	10
AB	00	1	1		
00					
01		1			
11					
10		1	1	1	1

$$\overline{ACD} + ABD + \overline{BC}$$

$$\overline{BC} + \overline{ACD} + \overline{DAB}$$

$$(3) ny(w, x, y, z) = \sum m(0, 2, 6, 7, 8, 10, 14, 15)$$

	CD	00	01	11	10
AB	00	1	2	1	2
00		1	2	1	2
01		1	5	1	1
11		1	1	1	1
10		1	9	10	10