

MOSFET

Metal Oxide Semiconductor field Effect Transistor

The field Effect transistor abbreviated as (FET) is another semiconductor device like BJT which can be used as an amplifier or switch.

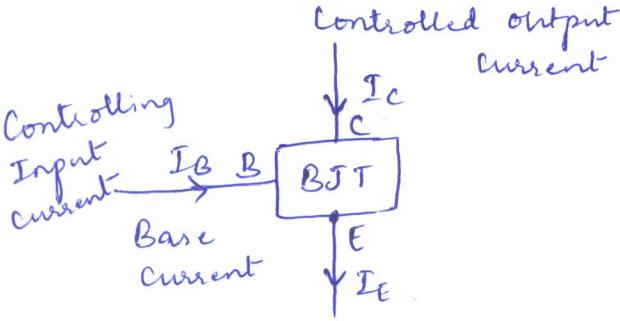
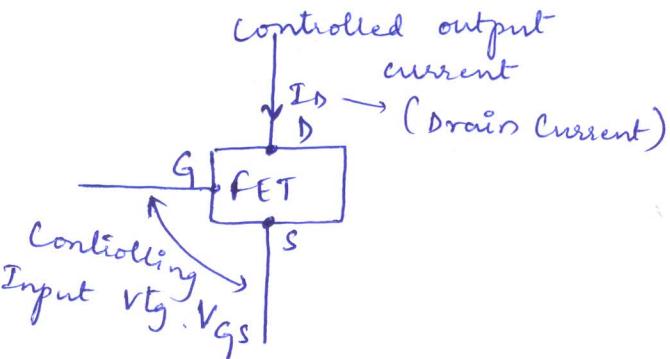
Like BJT, FET is also a three terminal device.

The three terminals of FET : (1) Drain (D)

(2) Source (S)

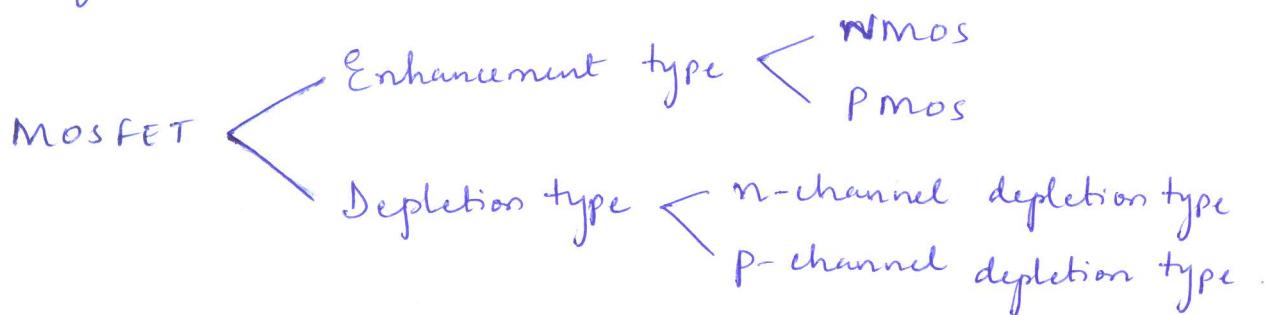
(3) Gate (G).

Comparison between Bipolar Junction transistor (BJT) & Field Effect transistor (FET) :-

Bipolar Transistor (BJT)	field Effect Transistor (FET)
(1) BJT : <u>Current controlled device</u>	(1) FET : <u>Voltage controlled device</u>
	
(2) Low Input Impedance	(2) High Input Impedance
(3) Bipolar device	(3) Unipolar device
(4) Larger size	(4) Smaller Size
(5) Cost is more	(5) Lower cost
(6) Higher Speed	(6) Lower Speed
(7) More Noise	(7) Lower Noise
(8) Thermal runaway occurs	(8) Thermal runaway does not occur
(9) Less temperature stable	(9) More temperature stable

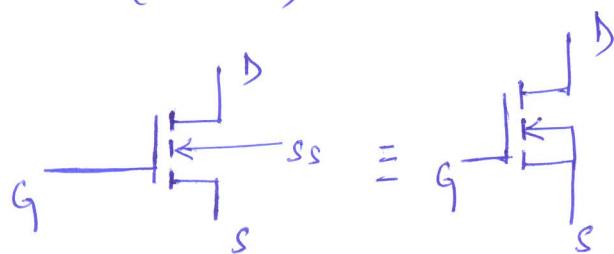
MOSFET :

MOSFET has become by far the most widely used electronic device, especially in the design of Integrated Circuits (IC's) which are circuits fabricated on a single silicon chip.

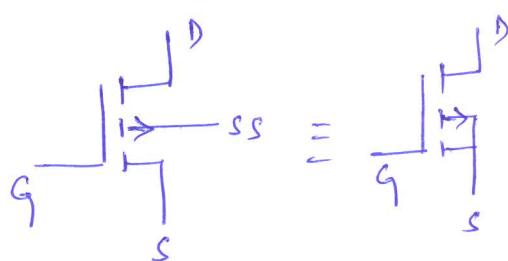


Symbolic Representation :-

(a) n-channel Enhancement type (nmos)

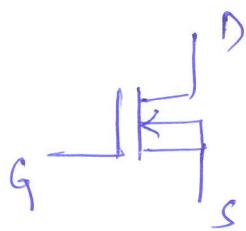


(b) p-channel Enhancement type (pmos)

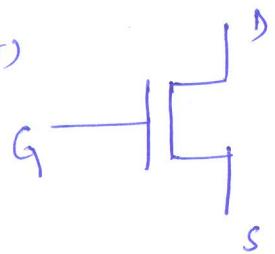


ss \Rightarrow Substrate

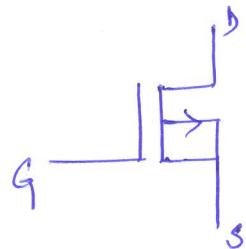
(c) n-channel Depletion type



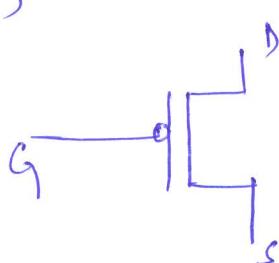
(OR)



(d) p-channel depletion type

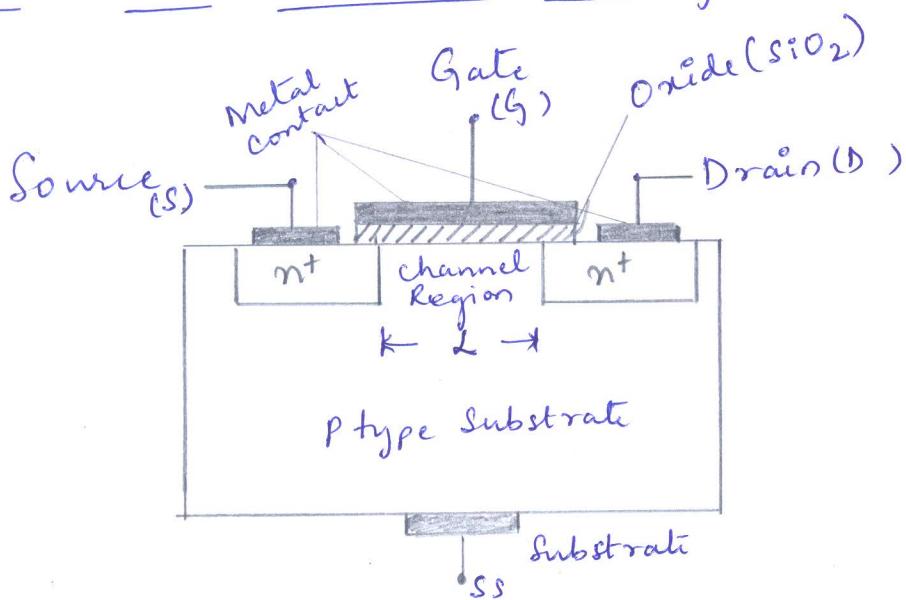


(OR)



✓ V X X

1.1. MOSFET Device Structure and Operation :-



* Shows the physical structure of n-channel Enhancement type MOSFET.

* A slab of p-type material is formed from a silicon base and is again referred to as substrate.

* The source and drain terminals are again connected through metallic contacts to n-doped regions (n⁺).

* Absence of Channel between two n-doped regions.
This is the primary difference between the depletion type & enhancement type MOSFET.

Depletion type MOSFET → Presence of channel in channel region.

Enhancement type MOSFET → Absence of channel in channel between source & drain regions.

* A thin layer of silicon dioxide (SiO₂), which is an excellent electrical Insulator, is grown on the surface of the substrate, covering the area between the source & drain regions.

* Metal is deposited on top of the oxide layer to form the Gate electrode of the device.

* Metal contacts are also made to the source region, drain region and the substrate

* MOSFETs are fabricated using a process known as silicon gate technology, in which a certain type of silicon called polysilicon, is used to form the gate electrode.

* It will be shown that the voltage applied to the gate controls current flow between source and drain.

This current will flow in longitudinal direction from drain to source in the region labeled 'channel region'.

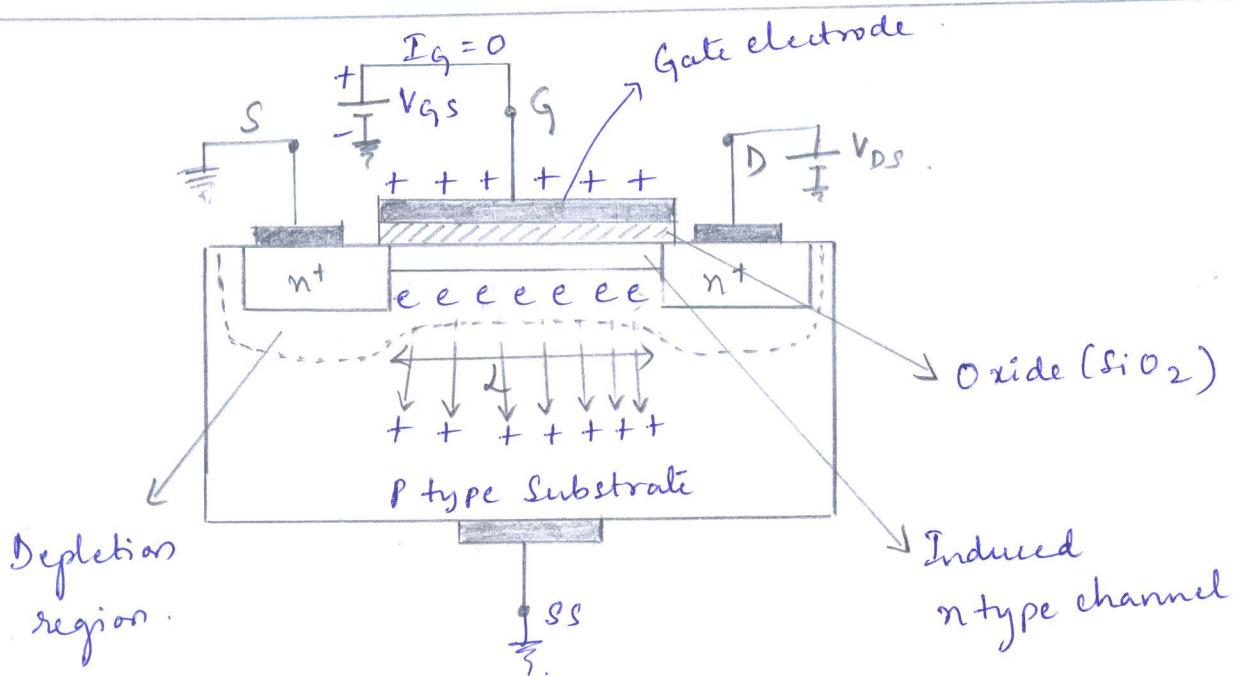
This region has length (L) and width (W) two important parameters of MOSFET.

1.1.(a) operation with No Gate Voltage.

With no bias voltage applied to the gate, two back-to-back diodes exist in series between drain and source. One diode is formed by the $p-n$ junction b/w n^+ drain region and p-type substrate and the other diode is formed by the $p-n$ junction between the p-type substrate and n^+ source region. These back-to-back diodes prevent current conduction from drain to source when a voltage V_{DS} is applied.

1.1.(b) Creating a Channel for current flow.

* As shown in fig 2. Here we have grounded the source & the drain and applied a positive voltage to the gate.



fig(2) : Enhancement type NMOS transistor with positive V_{TG} applied to the Gate

* Since the Source is grounded, the gate Voltage appears in effect between gate and source and thus it is denoted as V_{GS} .

* The positive Voltage on the gate causes, the free holes (which are positively charged) to be repelled from the region of the substrate under the gate (channel region). These holes are pushed downward into the substrate.

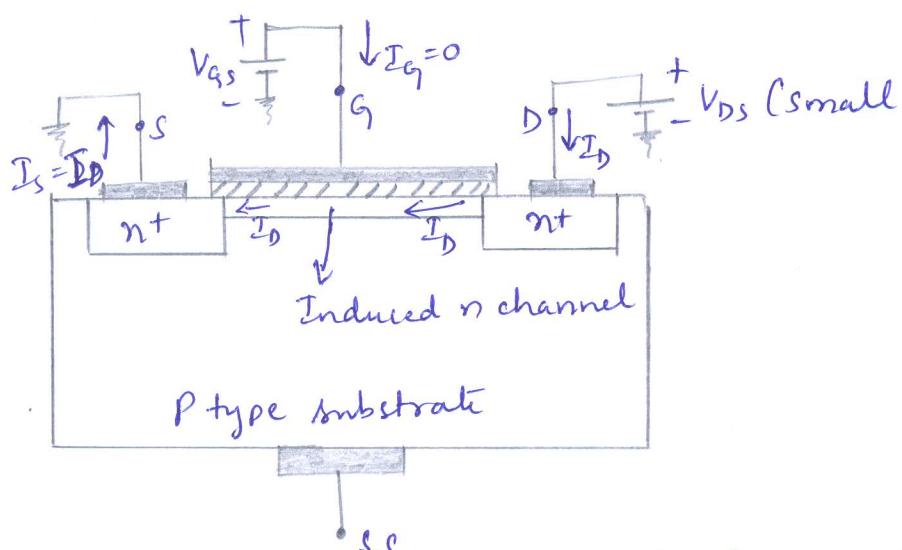
* The positive gate voltage attracts electrons from the n^+ source and drain regions (e^- are in abundance) into the channel region. length of the channel is L .

* Now if a Voltage is applied between drain and source, current flows through the induced n region, carried by the mobile electrons. As shown in fig(2)

* The induced n region thus forms a channel for current flow from drain to source. Thus the MOSFET is called an n-channel MOSFET or an NMOS Transistor which is formed in a p-type substrate

- * The value of V_{GS} at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called the threshold Voltage (V_t)
- * Thus the channel is created from drain to source, instant current will flow through the channel when a voltage V_{DS} is applied.

1.1.(c) Applying a small V_{DS} .



fig(3): NMOS Transistor, $V_{GS} > V_t$ & with a small V_{DS} .

- * We now apply a small positive voltage V_{DS} between drain and source as shown in fig(3).
- * The voltage V_{DS} causes the current I_D to flow through the induced 'n' channel. Current is carried by free electrons travelling from source to drain.
- * The current in the channel I_D will be from drain to source.

For $V_{GS} = V_t$ the channel is just induced and the current conducted is negligibly small.

for $V_{GS} > V_t$, more electrons are attracted into the channel. ($V_{GS} - V_t = V_{ov}$) \Rightarrow Overdrive Voltage.

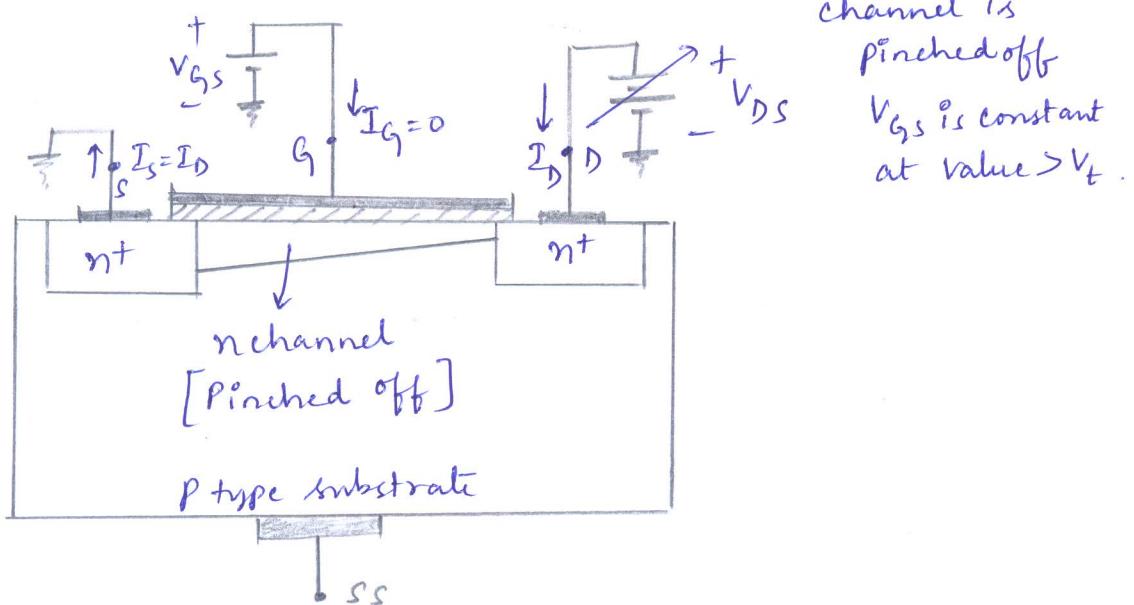
* It follows that current I_D is proportional to $V_{GS} - V_t$ & to the voltage V_{DS} that causes I_D to flow.

* The description above indicates that for the MOSFET to conduct, a channel has to be induced. Then increasing V_{GS} above the threshold voltage V_t enhances the channel. Hence the name Enhancement type MOSFET

Note : $I_S = I_D$ and $I_g = 0$

1.1.(d) Operation as V_{DS} is Increased

fig(4) : Enhancement nmos transistor, V_{DS} is increased,



* Next we consider the situation as V_{DS} is increased.

Let V_{GS} is held constant at a value greater than V_t .

V_{DS} appears as a voltage drop across the length of the channel.

* As we travel along the channel from source to drain the V_{tg} increases from 0 to V_{DS} .

Since the channel depth depends on this Voltage, the channel is no longer of Uniform depth, rather the channel will take tapered form.

* When V_{GS} is increased beyond threshold level, the density of free carriers in the induced channel will increase, as a result I_D will increase.

* However if we hold V_{GS} constant and increase the level of V_{DS} , the drain current eventually reaches Saturation level. As V_{DS} is increased the channel becomes more tapered and its resistance increases. Being deepest at the source end and shallowest at the drain end as shown in fig(4)

* When V_{DS} is increased to the value that reduces the voltage between gate and drain to V_t .

$$\text{ie } V_{GD} = V_t \quad \text{X.}$$

or $V_{GS} - V_{DS} = V_t$

or

$$V_{DS} = V_{GS} - V_t$$

The channel depth at the drain end decreases to almost zero and the channel is said to pinched off X.

* when V_{DS} is still more increased

$$V_{DS} \geq V_{GS} - V_t,$$

the drain current thus saturates at this value & the MOSFET is said to have entered the Saturation region of operation.

✓ $V_{DS} = V_{GS} - V_t$.
(Sat)

for every value of $V_{GS} \geq V_t$, there is a corresponding value of $V_{DS_{(sat)}}$. The device operates in saturation region.

* for $V_{DS} < V_{GS} - V_t$

$V_{DS} < V_{DS_{(sat)}}$, then device operates in triode region (ohmic).

* Expression for Drain Current (I_D) for N-channel MOSFET $(I_D - V_{DS})$ characteristic Eq :-

(1) Ohmic Region (Triode Region)

$$I_D = K \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

(2) Saturation region

$$I_D = \frac{k}{2} \left[V_{GS} - V_T \right]^2$$

(3) Cutoff Region

$$\underline{\underline{I_D = 0}}$$

Where K = Constant of Proportionality

SI unit is A/V^2

* Expression for Transconductance (g_m) for MOSFET :-

$$g_m = k (V_{GS} - V_T) \quad A/V \text{ (SI unit)}$$

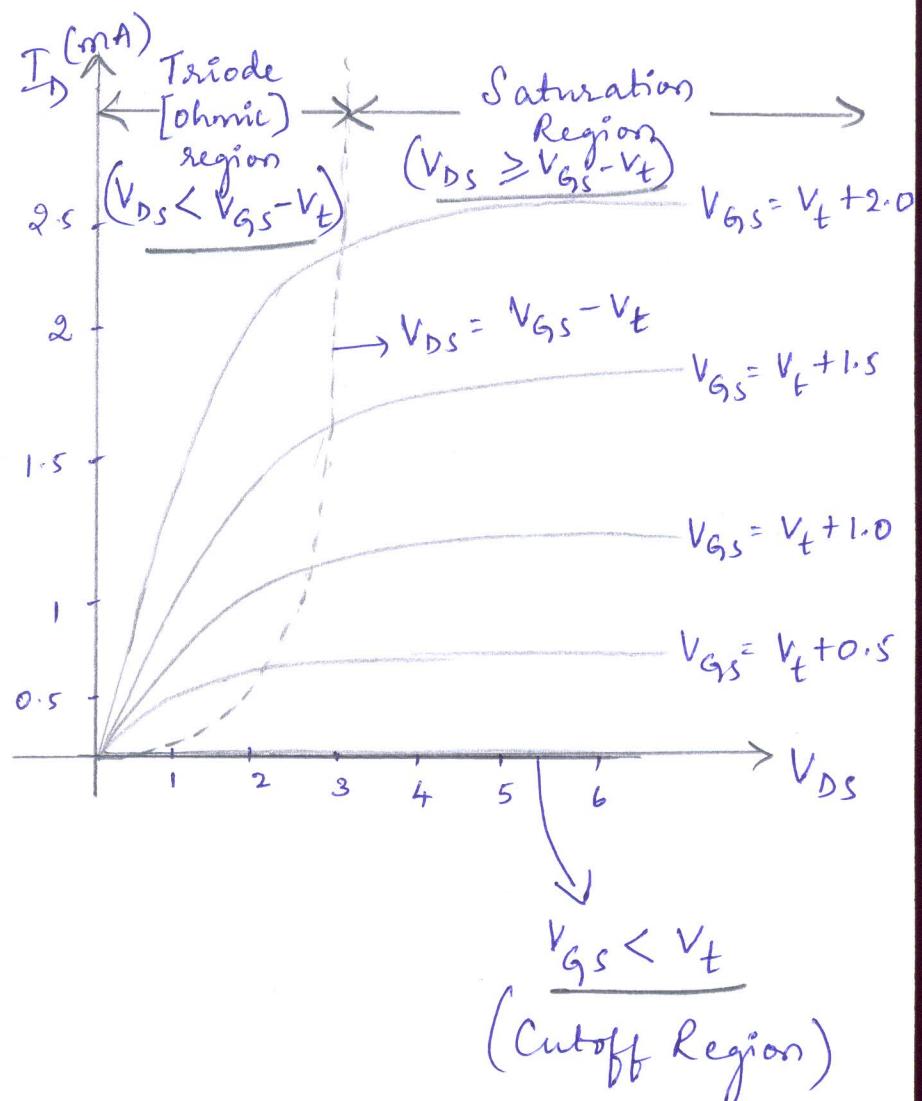
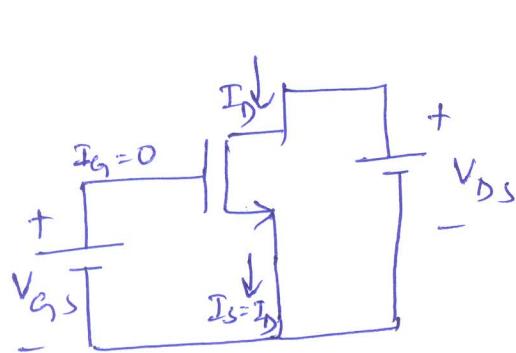
* Expression for linear resistance (r_{DS}) :-

$$r_{DS} = \frac{1}{k(V_{GS} - V_T)} = \frac{1}{g_m}$$

* Current - Voltage characteristics of MOSFET (OR)

[Output characteristics $\Rightarrow I_D - V_{DS}$ Characteristics]

The curve represents relationship between the drain current (I_D) and drain to source voltage (V_{DS}) for different values of V_{GS} .



MOSFET
Regions :-

Condition:

$$V_{GS} \geq V_t$$

Ohmic
(triode)

$$V_{DS} < V_{GS} - V_t$$

Saturation

$$V_{DS} \geq V_{GS} - V_t$$

$$V_{GS} < V_t$$

Cutoff region

The characteristic curve indicates that there are three distinct regions of operation:-

- (1) Saturation : MOSFET operates as an Amplifier region
- (2) Triode or ohmic region : MOSFET operates as an Closed Switch
- (3) Cutoff region : MOSFET operates as an open switch

* To operate MOSFET as a Switch :-

→ MOSFET operates in triode (ohmic) region, (Closed switch)
we must first Induce a channel,

$$V_{GS} \geq V_t \text{ (Induced channel)}$$

when V_{DS} is increased.

$$V_{DS} < V_{GS} - V_t .$$

→ MOSFET operates in cutoff region,

$$V_{GS} < V_t .$$

* To operate MOSFET as a Amplifier :-

MOSFET operates in Saturation region.

we must first Induce the channel,

$$V_{GS} \geq V_t \text{ (Induced channel)} \quad \begin{matrix} \nearrow \text{gate to drain} \\ \searrow V_{GD} \end{matrix}$$

By raising V_{DS} to value that results in V_{GD} falling below V_t .

$$V_{GD} \leq V_t \text{ (Pinched off)}$$

Condition can be expressed as,

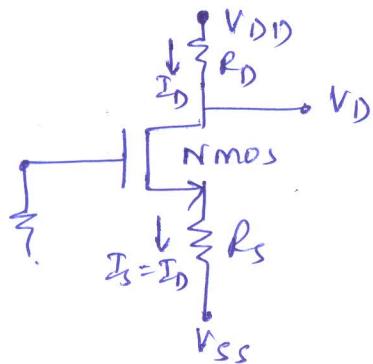
$$V_{DS} \geq V_{GS} - V_t \text{ (Pinched off channel).}$$

* The Boundary between triode & saturation region is,

$$\underline{V_{DS} = V_{GS} - V_t}.$$

MOSFET circuits at DC :-

①



Design Eqn:

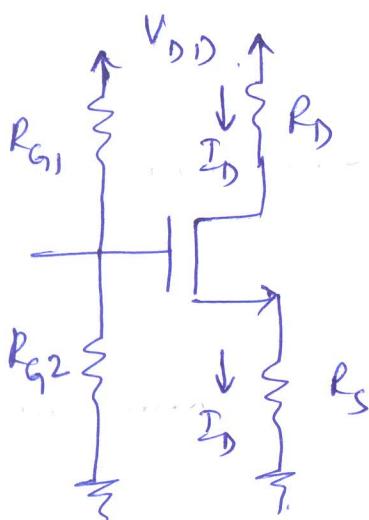
MOSFET in Saturation.

$$I_D = \frac{k}{2} (V_{GS} - V_t)^2 \quad \textcircled{1}$$

$$V_D = V_{DD} - I_D R_D \quad \textcircled{2}$$

$$R_{DS} = \frac{V_{DS}}{I_D} \quad \textcircled{3}$$

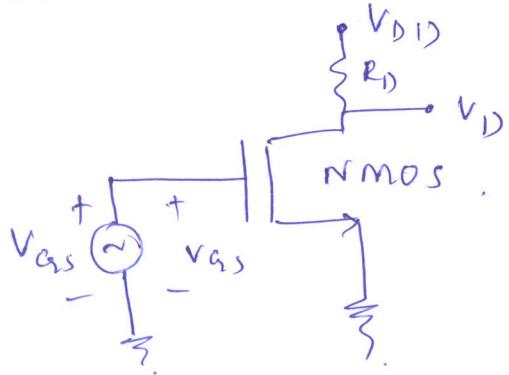
②



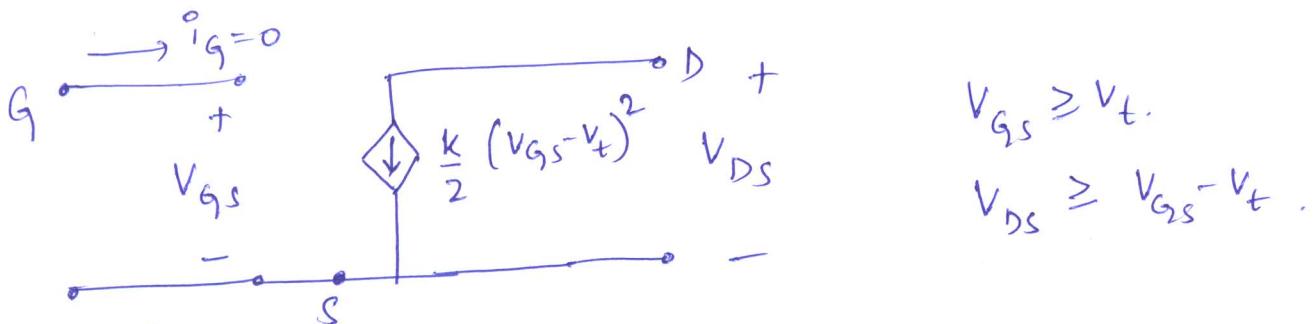
Voltage divider ckt,

$$V_G = \frac{V_{DD} \cdot R_{G2}}{R_{G1} + R_{G2}}$$

MOSFET AC Equivalent Ckt:



Equivalent model :- in saturation region.



Transconductance

$$g_m = k (V_{GS} - V_t), \quad A/V \quad (\text{SI unit of } g_m)$$

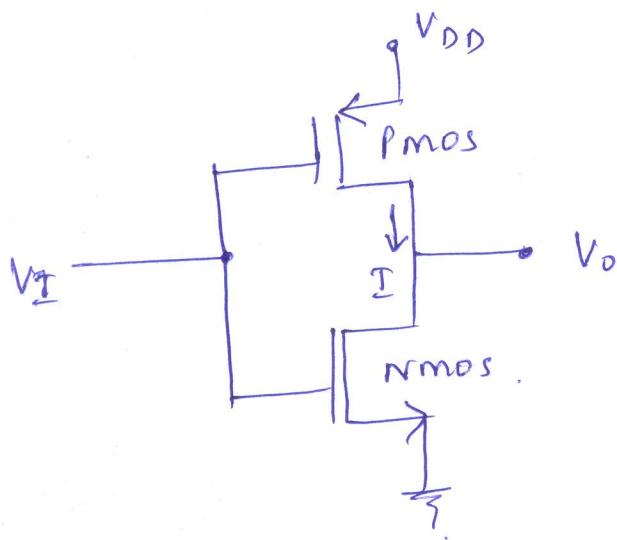
Voltage Gain :-

$$A_V = -g_m R_D$$

where R_D = drain resistance

Negative sign indicates Output is 180° out of phase with input (V_{GS}).

Cmos Inverter :-



Case 1 :- when V_I is low (0)

Pmos = ON

Nmos = OFF

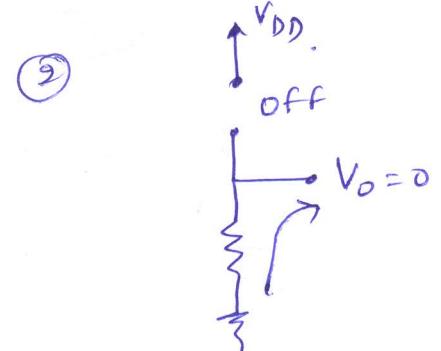
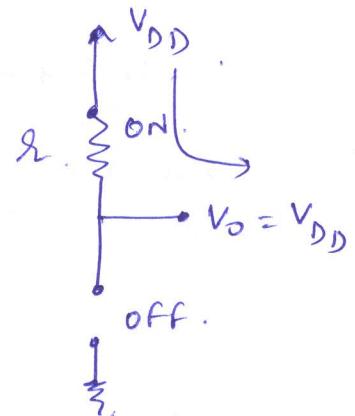
$$\therefore \underline{\underline{V_o = V_{DD}}}$$

Case 2 :- when V_I is High (1)

Pmos = OFF

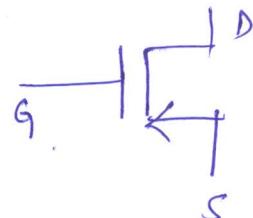
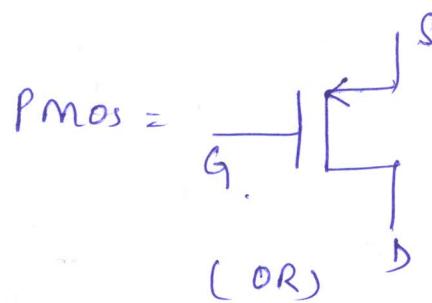
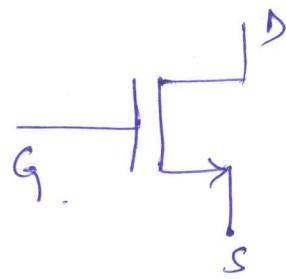
Nmos = ON

$$\therefore \underline{\underline{V_o = 0}}$$



Summary of MOSFET :-

(1) NMOS =



(2) MOSFET in Triode (ohmic) region :-

Conditions :

$$V_{GS} \geq V_t$$

$$V_{DS} \leq V_{GS} - V_t$$

Drain current (I_D) = $k \left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2 \right]$

(3) MOSFET operation in Saturation region :-

Conditions : $V_{GS} \geq V_t$

$$V_{DS} \geq V_{GS} - V_t$$

Drain current (I_D) = $\frac{k}{2} (V_{GS} - V_t)^2$

(4) Linear Resistance,

$$R_{DS} = \frac{1}{k(V_{GS} - V_t)} = \frac{1}{g_m}$$

(5) Operation in Cutoff:

Neglect ($\frac{W}{L}$)

$$V_{GS} \leq V_t.$$

(6) Transconductance (g_m):

$$g_m = \frac{I_d}{V_{GS}} = k \cdot \frac{W}{L} (V_{GS} - V_t) = k (V_{GS} - V_t)$$

(7) Voltage gain (A_v)

$$A_v = \frac{V_d}{V_{GS}} = -g_m R_D$$

where R_D = drain resistance.

$$(8) \quad g_m = \frac{1}{R_D}$$

(1) An N-channel Enhancement MOSFET having $V_t = 0.5V$
 $k = 2mA/V^2$, $V_{GS} = 2V$, $V_{DS} = 1V$, $I_D = \underline{2mA}$

~~$V_{DS} \geq V_{GS} - V_t$~~

Soln :- Here $V_{DS} \leq V_{GS} - V_t$

MOSFET is working in triode (ohmic) region.

~~$I_D = k \cdot \frac{W}{L}$~~

~~$\left[\frac{W}{L} = 1 \right]$~~

$$I_D = k \cdot \left[(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$I_D = 2m \left[(2 - 0.5) 1 - \frac{1}{2} (1) \right] = \underline{\underline{2mA}}$$

- 2 An N-mos tr, whose $V_t = 1V$, & $k = 2mA/V^2$ is operating in saturation with drain current = $4mA$.
find V_{GS} & transconductance (g_m).

Soln: $I_D = \frac{1}{2} \times k (V_{GS} - V_t)^2$ (for saturation)

$$\Rightarrow V_{GS} = \underline{\underline{3V}}$$

$$g_m = k (V_{GS} - V_t) = \underline{\underline{4mA/V}}$$

3. An Nmos transistor, with $V_t = 1V$, is biased such that $V_S = 2V$ & $V_G = 4V$. The max value of V_D allowed so that the transistor operates in ohmic region = 3V

$$V_{GS} = V_G - V_S = 2V$$

$$V_{DS}^{(ohmic)} = V_{GS} - V_t = 2 - 1 = 1V$$

$$V_{DS}^{(ohmic)} = V_D + V_S$$

$$V_D = V_{DS}^{(ohmic)} + V_S = 3V$$

- 4 for an Nchannel MOSFET, $V_S = 4V$, $V_G = 7V$, $V_{th} = 2V$, Min value of V_D regd so that device operates in saturation region = 5V

$$V_{GS} = V_G - V_S \\ = 7 - 4 = 3V$$

$$V_{DS(sat)} = V_{GS} - V_t = 3 - 2 = 1V$$

$$V_{DS(sat)} = V_D - V_S$$

$$\therefore V_D = V_{DS(sat)} + V_S = 1 + 4 = \underline{\underline{5V}}$$

- 5 for NMOS, $V_S = 4V$, $V_G = 9V$, $V_{th} = 2V$, find V_D in saturation region = 7V

- 6 An N-channel Enhancement MOSFET, with a threshold $V_t = 1V$, has its source terminal connected to ground and +3V DC V_{Gy} applied to the gate. The min value of V_D needed so that transistor operates in Satⁿ region = 2V

$$V_g = 3V, V_t = 1V, V_s = 0.$$

$$V_{GS} = V_g - V_s = 3V$$

$$V_{DS} = V_{GS} - V_t = 3 - 1 = 2V$$

(Sat)

$$V_{D_{(sat)}} = V_D - V_s$$

$$\therefore V_D = \underline{\underline{V_{DS} + V_s}} = 2V$$

- 7 An NMOS, with $V_t = 1V$, $k = 2mA/V^2$, $V_{GS} = 4V$, $V_{DS} = 4V$ then region of operation is Saturation region and drain current is 9mA = I_D

$$V_{DS} > V_{GS} - V_t \text{ so (Saturation region)}$$

$$I_D = \frac{1}{2} k (V_{GS} - V_t)^2 = \underline{\underline{9mA}}$$

- 8 For NMOS, $V_t = 0.8V$, Source terminal is grounded, drain $V_D = 1.9V$, DC V_{Gy} to gate = +2.5V Device is operating in Saturation region.

$$V_{GS} = V_g - V_s = 2.5V$$

$$V_{GS} - V_t = 1.7V \quad V_{DS} > V_{GS}$$

$$V_{DS} = V_D - V_s$$

$$V_{DS} = 1.9 - 0 = 1.9V$$

- 9 An N-channel mosFET, drain resistance = $10\text{ k}\Omega$,
 $V_{GS} = 2.5\text{ V}$, $V_{DS} = 4.5\text{ V}$, $V_t = 1\text{ V}$, $k = 2\text{ mA}/\text{V}^2$
 find transconductance (g_m) & VTG gain (A_V), R_{DS}

Soln :- $g_m = k (V_{GS} - V_t) = \underline{\underline{3\text{ mA/V}}}$

$$A_V = -g_m \times R_D$$

$$= \underline{\underline{-3\text{ mA} \times 10\text{ k}}} \quad \underline{\underline{}}$$

$$A_V = \underline{\underline{-30}}$$

$$R_{DS} = \frac{1}{g_m} \\ = \underline{\underline{0.33\text{ k}\Omega}}$$

- 10 for an N-channel mosFET, $V_S = 2\text{ V}$, $V_G = 5\text{ V}$ & $V_D = 4\text{ V}$.
 If $V_t = 0.7\text{ V}$ device is operating in ohmic region
 or
triode

- 11 An N-ch mosfet with drain resistance = $10\text{ k}\Omega$, $V_{GS} = 3.5\text{ V}$ &
 $V_{DS} = 5\text{ V}$. If $V_{th} = 1.5\text{ V}$ and $k = 3\text{ mA}/\text{V}^2$. Find
 g_m (transconductance) & VTG gain (A_V)

$$g_m = 6\text{ mA/V}$$

$$A_V = -60$$

- 12 N-channel Enhancement mosFET, $V_t = 0.8\text{ V}$, $k = 150\mu\text{A}/\text{V}^2$
 $\frac{W}{L} = 8$. If its $V_S = 2\text{ V}$, $V_G = 4\text{ V}$, $V_D = 3.6\text{ V}$, calculate
 drain current I_D .

$$V_{GS} = V_G - V_S = 2\text{ V}, \quad V_{DS} = V_D - V_S = 1.6$$

$$V_{DS} < V_{GS} - V_t$$

$1.6 < 1.2$ (ohmic region)

$$I_D = \frac{kW}{L} ((V_{GS} - V_t)V_{DS} - \frac{1}{2}(V_{DS})^2) = \underline{\underline{7.68 \times 10^{-4} \text{ A}}}$$