

Introduction

Junction Diode: Two terminal semiconductor device

"bipolar junction diode" \rightarrow Limited Application

(2D) Circuits

MOSFET & BJT: Three terminal semiconductor device

MOSFET: Metal Oxide Semiconductor
Field Effect Transistor

Numerous Applications

BJT: Bipolar Junction Transistor

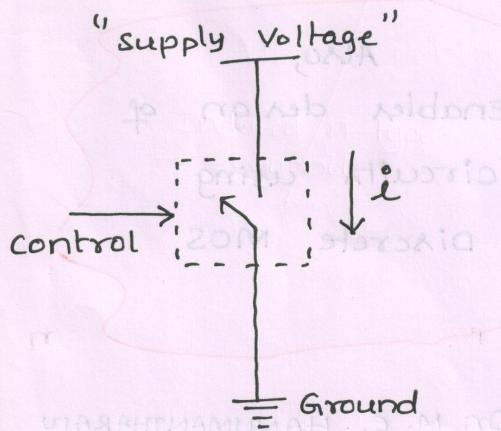
signal Amplification

Range

Digital Logic & Memory

Basic Principle

The voltage between the two terminals is used to control the current flow in the third terminal



Controlled Source

$i = \text{current}$ $\begin{cases} 0 \\ \text{Large value} \end{cases}$

MOSFET versus BJT

Both have unique features

&
Applications

UNIT 1
MOSFET :

MICROELECTRONIC
CIRCUITS NOTES

BMSIT

Bangalore

→ More widely used electronic device



→ In the Design of "Integrated circuits" (ICs)

ICs: circuits fabricated on a single silicon chip

→ MOSFET requires small area on silicon IC

→ Manufacturing process: Relatively simple

→ Operation requires: comparatively little power

→ High Density (> 200 million): VLSI

→ used to implement both Analog and Digital circuits & Mixed signal Design

Objectives : "Develops high degree of familiarity of MOSFETs"

★ physical structure

Operation

Terminal characteristics

Circuit Models

Applications

Amplifier

Digital logic

Also,
Enables design of
circuits using
Discrete MOS

Dr. M. C. HANUMANTHARAJU

Associate Professor

BMSIT, Bangalore

MOSFET : Device structure & physical operation

①

Metal oxide Semiconductor Field Effect Transistor or IGFET

Size : Small

process : simple

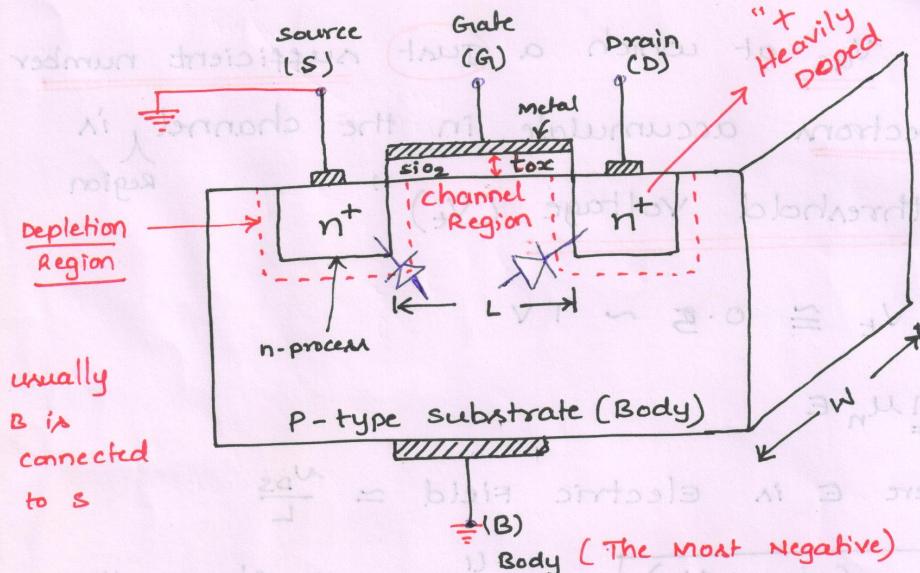
→ silicon gate Technology

Name derived from physical structure

very large scalers IC

★ n - channel enhancement-type MOSFET

"Most widely used"



usually
B is
connected
to S

L : channel

= Length

(0.1 to 3 μm)

W : channel

= Width

(0.2 to 100 μm)

tox : oxide

= thickness

(2 to 50 nm)

$$[1 \text{ nm} = 10^{-9} \text{ m}$$

$$= 0.001 \mu\text{m}$$

A voltage is applied to gate (G) to control the current flow between S and D

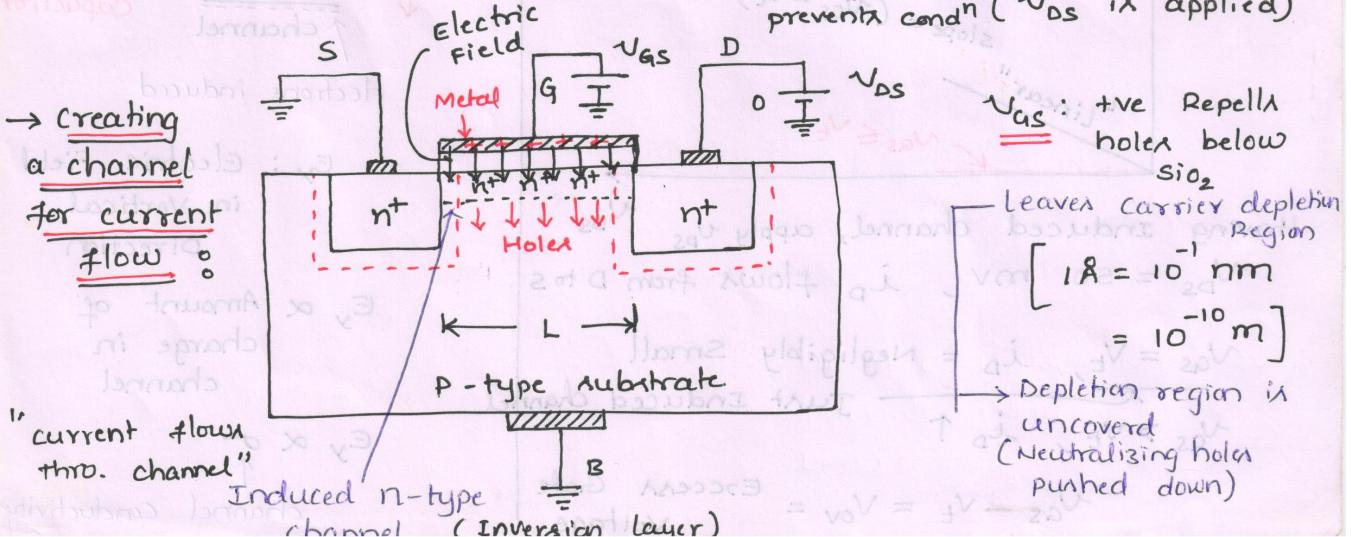
s → D (longitudinal direction)

★ Operation

→ No gate bias (zero bias) ⇒ back-to-back diodes, $i_D = 0$

(High resistance = $10^{12} \Omega$)

↓ prevents cond'n (V_{DS} is applied)



V_{GS} : +ve Repells holes below

SiO_2

Leaves carrier depletion Region

$$[1 \text{ Å} = 10^{-10} \text{ m}$$

$$= 10^{-10} \text{ m}$$

→ Depletion region is uncovered (Neutralizing holes pushed down)

①

Apply a positive V_{GS}

⇒ pushes holes down to the substrate

⇒ deplete the holes under SiO_2

Further increase V_{GS} : Attracts \bar{e} from S & D

⇒ Invert the P to n under SiO_2

"The value of V_{GS} at which a just sufficient number of mobile electrons accumulate in the channel in Region called the threshold voltage (V_t)"

$$V_t \approx 0.5 \sim 1 \text{ V}$$

$$i_D = j_n = qn\mu_n E$$

where E is electric field $\approx \frac{V_{DS}}{L}$

$$n \propto (V_{GS} - V_t)$$

* Applying a small V_{DS}

i_D

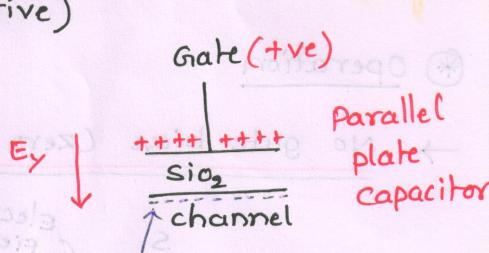
$$i_D \propto V_{OV}$$

$$\text{slope} = (V_{DS} - V_t)$$

"Linear"

\nwarrow

$N_{GS} \leq V_t$



electron induced

E_y : Electric field
in vertical direction

$E_y \propto$ Amount of charge in channel

$E_y \propto \sigma$
channel conductivity

Having induced channel, apply V_{DS}

$V_{DS} = 50 \text{ mV}$, i_D flows from D to S

$V_{GS} = V_t$, i_D = Negligibly Small

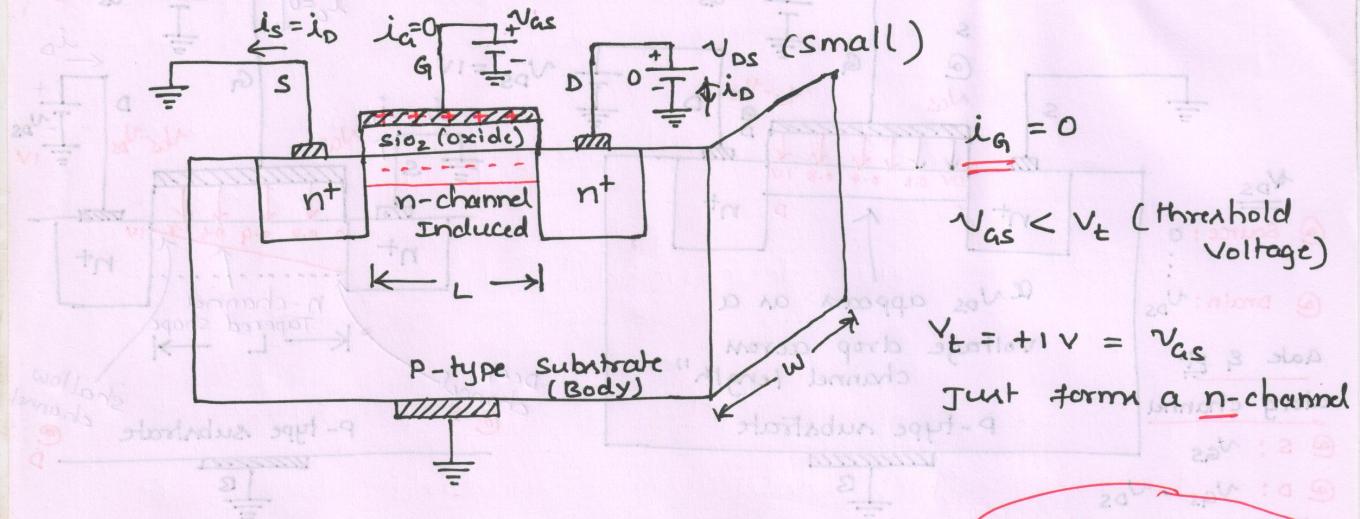
Just Induced channel

$V_{GS} > V_t$, $i_D \uparrow$

$$V_{GS} - V_t = V_{OV} = \text{Excess Gate Voltage}$$

n-channel enhancement-type MOSFET

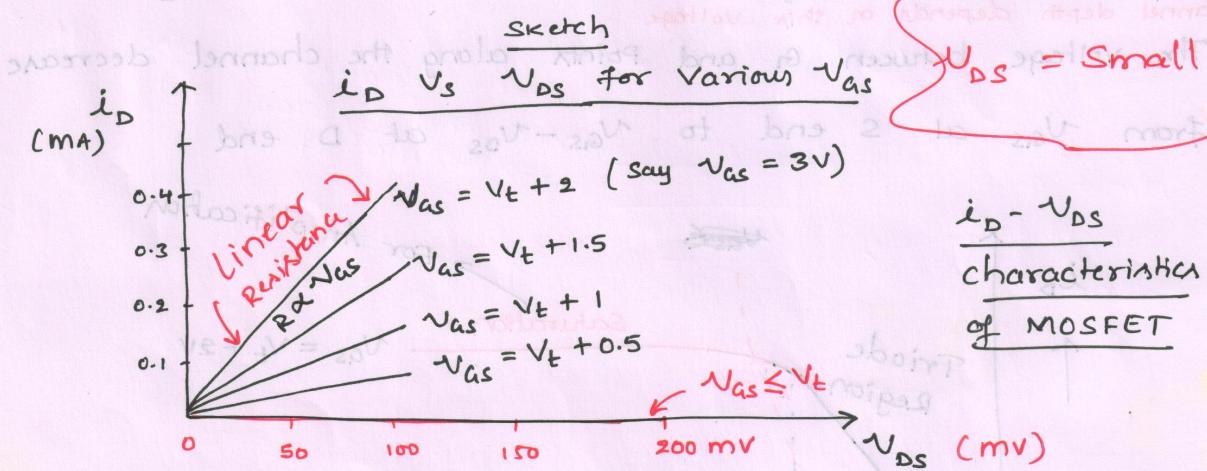
(2)



$$i_D = 0$$

$V_{GS} < V_T$ (threshold voltage)

$V_T = +1V = V_{GS}$
Just forms a n-channel



$i_D - V_{DS}$ characteristics of MOSFET

$V_{GS} \leq V_T, i_D = 0, \text{Resistance} = \infty$

$V_{GS} > V_T, V_{GS} = V_T + 0.5V, \text{Resistance} \downarrow$

Enhances the channel
hence, the name
Enhancement mode
operation

$$i_D = q_n \mu_n E_{\text{eff}} \frac{N_A}{L}$$

Effective Voltage for Inducing
electrons



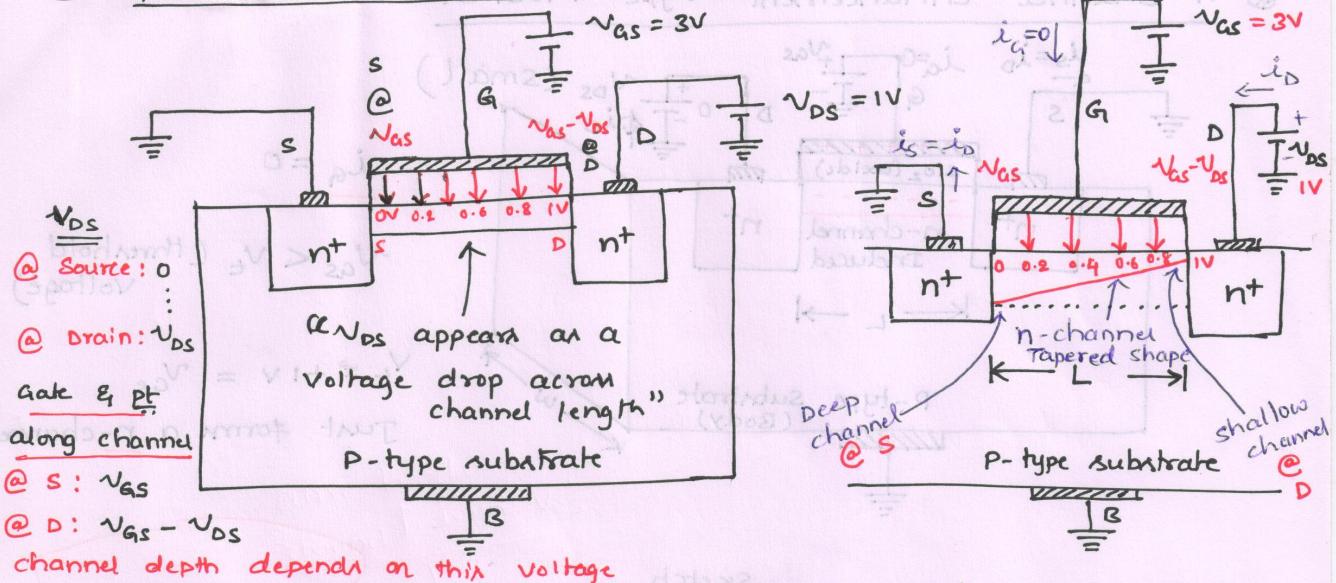
Dr. M. C. Hanumantharaju

Associate Professor

BMSIT, Bangalore

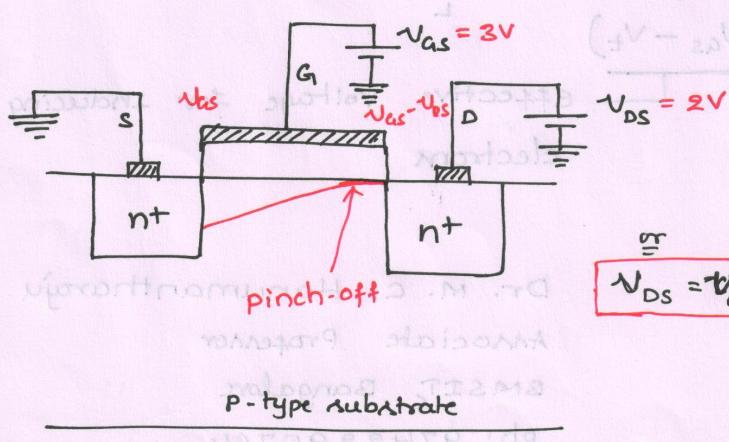
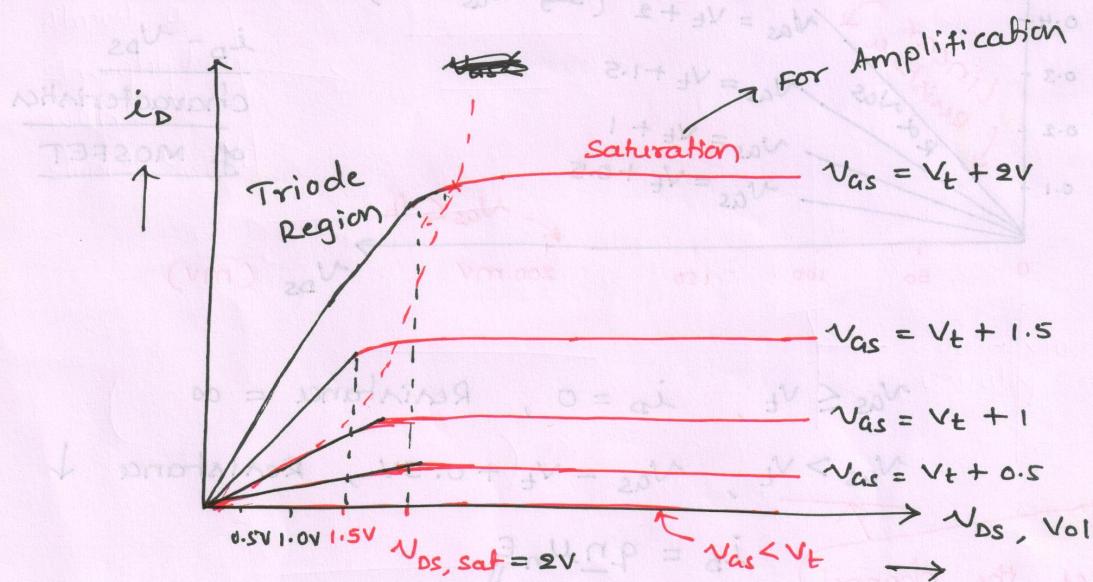
ph: 9742290764

* Operation As V_{GS} is Increased : $V_{GS} = \text{constant} > V_t$



The voltage between G and points along the channel decrease from V_{GS} at S end to $V_{GS} - V_{DS}$ at D end

from V_{GS} at S end to $V_{GS} - V_{DS}$ at D end

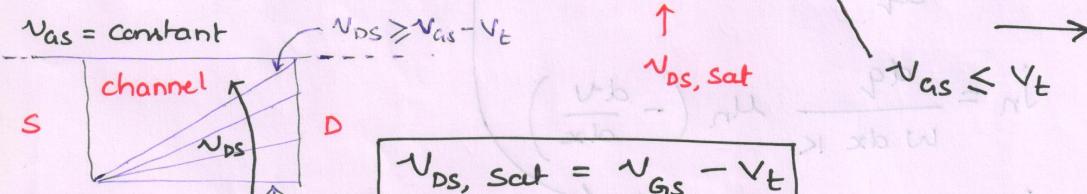
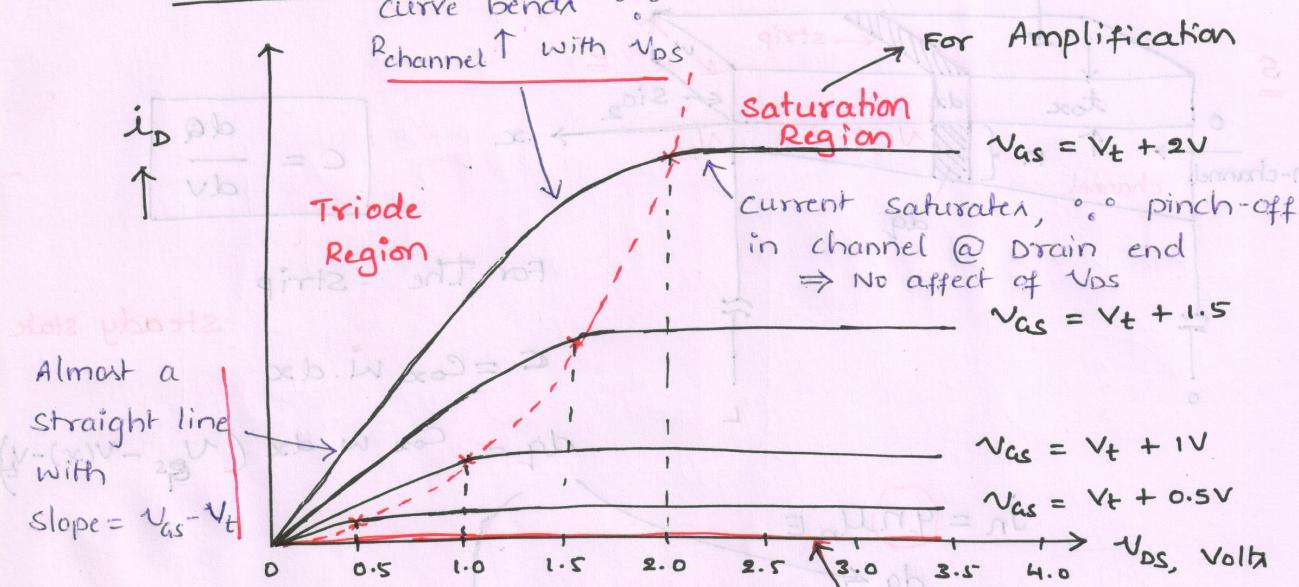


Eventually, when $V_{GD} = V_{GS} - V_{DS} = V_t$, the channel depth at D is almost zero
 \Rightarrow The channel is pinched off

$$V_{DS} = V_{GS} - V_t$$

$i_D - V_{DS}$ for enhancement MOSFET

(3)a



Effect of V_{DS}

$V_{DS} > V_{DS, \text{sat}}$: Device Operates in Saturation Region

(For every value of $V_{AS} \geq V_T$ there is a $V_{DS, \text{sat}}$)

$V_{DS} < V_{DS, \text{sat}}$: Triode Region

V_{AS}	V_{DS}	$V_{AS} - V_{DS}$
3	4	0
3	4	1
3	4	2
3	4	3
3	4	4

(pinch off)

* Derivation of the $i_D - V_{DS}$ relationship

Consider "Triode" region

Recall: A ϵ_f channel forms capacitor

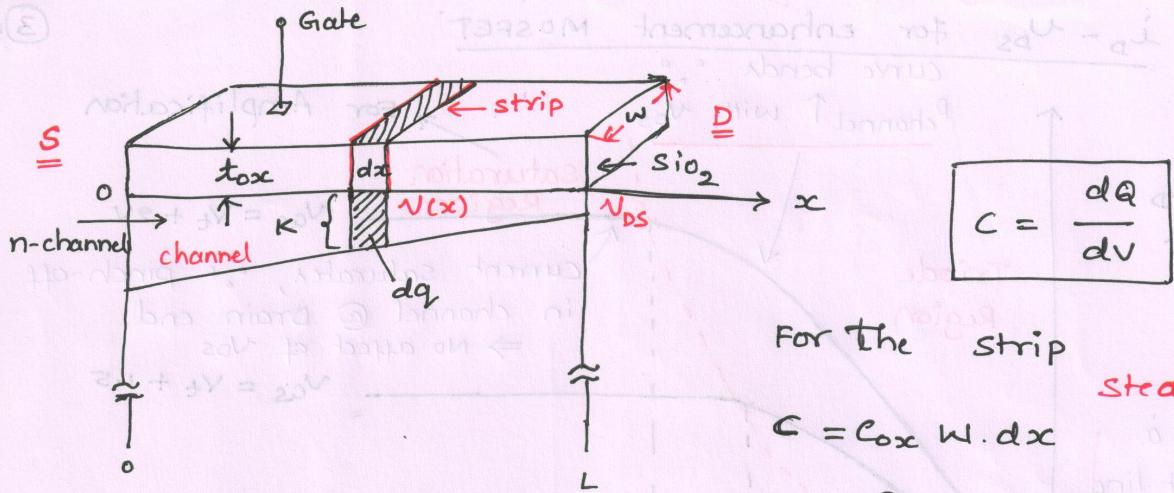
$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9 \epsilon_0}{10 \text{ nm}} = 3.45 \times 10^{-11} \text{ F/m}$$

$8.854 \times 10^{-12} \text{ F/m}$

(per unit area)

$$C_{ox} = 3.45 \times 10^{-3} \text{ F/m}^2 = 3.45 \text{ fF/}\mu\text{m}^2$$

(usually expressed)



$$C = \frac{dQ}{dV}$$

For The Strip

Steady state

$$C = C_{ox} W \cdot dx$$

$$dq = C_{ox} W dx (V_{GS} - V(x) - V_t)$$

$$j_n = q n \mu_n E$$

$$dq \leftarrow$$

$$j_n = \frac{dq}{W dx K} \mu_n \left(-\frac{dV}{dx} \right)$$

$$i_D = j_n \cdot K W = \frac{dq}{dx} \mu_n \left(-\frac{dV}{dx} \right)$$

$$i_D = \mu_n C_{ox} W (V_{GS} - V(x) - V_t) \frac{dV}{dx}$$

$$\int_0^L i_D dx = \mu_n C_{ox} W \int_0^L [(V_{GS} - V_t) - V(x)] \frac{dV}{dx} dx$$

$$i_D \cdot L = \mu_n C_{ox} W \left[(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$i_D = \frac{\mu_n C_{ox} W}{L} \left[(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

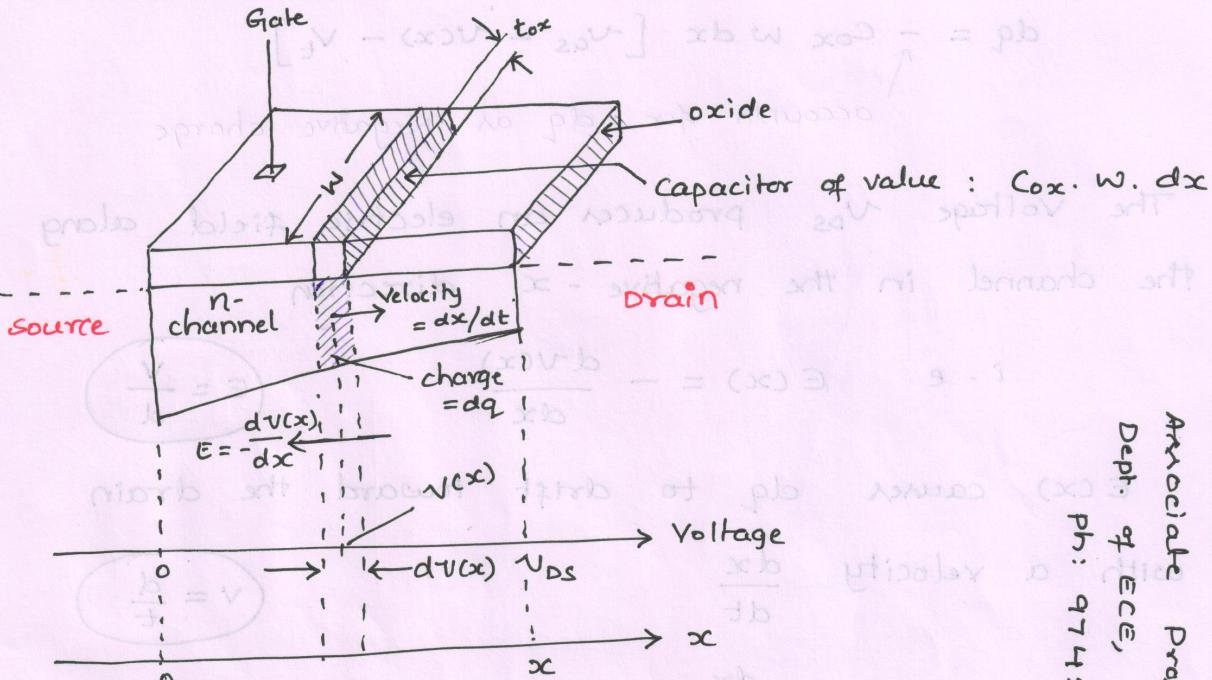
$$i_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

Aspect Ratio

\Rightarrow Triode Region

Derivation of $i_D - V_{DS}$ Relationship

(3b)



Derivation of $i_D - V_{DS}$ Relationship

Dr. M. C. Hanumantharaju
Associate Professor

Dept. of ECE,
BMSIT, Bangalore
Ph: 9742290764

Consider "Triode" Region

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9 \epsilon_0}{10 \text{ nm}} = 3.45 \times 10^{-11} \text{ F/m}$$

$$= 8.854 \times 10^{-12} \text{ F/m}$$

(Capacity per unit area)

$$C_{ox} = 3.45 \times 10^{-3} \text{ F/m}^2 = 3.45 \text{ fF}/\mu\text{m}^2$$

(usually expressed)

Consider infinitesimal strip of gate at distance x from Source

$$\text{Capacitance of the strip} = C = \underbrace{C_{ox} w \cdot dx}_{\text{Area of strip}}$$

To find charge stored on this strip:

Effective voltage between gate & channel at point x ,

$$dv = [V_{GS} - \underbrace{V(x)}_{\text{Voltage in the channel at point } x} - V_t]$$

Voltage in the channel at point x

Electron charge on the strip = $dq = C \cdot dV$, since $C = \frac{dq}{dV}$

$$dq = -C_{ox} W dx [V_{as} - V(x) - V_t]$$

accounts for dq as Negative charge

The voltage V_{as} produces an electric field along the channel in the negative $-x$ direction

$$\text{i.e } E(x) = -\frac{dV(x)}{dx}$$

$$E = \frac{V}{d}$$

$E(x)$ causes dq to drift toward the drain with a velocity $\frac{dx}{dt}$

$$v = \frac{d}{t}$$

velocity = $\frac{dx}{dt} = -\mu_n E(x)$: Relation b/w velocity & E

$$= \mu_n \frac{dV(x)}{dx}$$

\uparrow Mobility of electrons in the channel

(Depends on fabrication process technology)

The drift current resulting in

$$i = \frac{dq}{dt}$$

$$= \frac{dq}{dx} \times \frac{dx}{dt}$$

$$i = -\mu_n C_{ox} W [V_{as} - V(x) - V_t] \frac{dV(x)}{dx}$$

i : source-to-drain

$$i_D = -i$$

i_D : drain-to-source

$$i_D = \mu_n C_{ox} W [V_{as} - V(x) - V_t] \frac{dV(x)}{dx}$$

$$i_D \cdot dx = \mu_n C_{ox} W [V_{as} - V(x) - V_t] dV(x) \quad (3) c$$

$$\int_0^L i_D \cdot dx = \int_0^{V_{DS}} \mu_n C_{ox} W [V_{as} - V(x) - V_t] dV(x)$$

mu 21.0 : v polarisat 20M
mu 21.0 : dim
mu 21.0 : min
mu 21.0 : max

$$[x]_0^L \quad \text{constant in Steady state}$$

$$x = \int_0^L \quad \text{e.g. } V(x) = \int_0^{V_{DS}} \frac{[V(x)]^2}{2} \quad \text{Aspect ratio}$$

$$i_D = (\mu_n C_{ox}) \left(\frac{W}{L} \right) \left[(V_{as} - V_t) - \frac{1}{2} V_{DS}^2 \right]$$

Saturation: \rightarrow Expression for i_D in Triode Region

Substitute $V_{DS} = V_{as} - V_t$ in the above eqn to

obtain i_D in saturation

$$i_D = \frac{1}{2} (\mu_n C_{ox}) \left(\frac{W}{L} \right) (V_{as} - V_t)^2$$

\rightarrow Expression for i_D in Saturation Region

$$i_D = f(V_{as}, V_t)$$

$\mu_n C_{ox}$: Det. by process technology

(process transconductance Parameter)

\rightarrow Determines MOSFET transconductance

Denoted by, $K_n' = \mu_n C_{ox}$

$$\therefore i_D = K_n' \left(\frac{W}{L} \right) \left[(V_{as} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad \text{"Triode"}$$

$$i_D = \frac{1}{2} K_n' \left(\frac{W}{L} \right) [V_{as} - V_t]^2 \quad \text{"Saturation"}$$

Q 8

State-of-the-art in 2003

MOS Technology : $0.13 \mu\text{m}$

$L_{\min} : 0.13 \mu\text{m}$

$W_{\min} : 0.16 \mu\text{m}$

$t_{\text{ox}} : 2 \text{ nm}$

(P) Consider a process technology for which $L_{\min} = 0.4 \mu\text{m}$, $t_{\text{ox}} = 8 \text{ nm}$, $\mu_n = 450 \text{ cm}^2/\text{V.s}$, and $V_t = 0.7 \text{ V}$.

(a) Find C_{ox} and k'_n

(b) For a MOSFET with $\frac{W}{L} = \frac{8 \mu\text{m}}{0.8 \mu\text{m}}$, calculate

the values of V_{as} and V_{DSmin} needed to operate the transistor in the saturation region with a DC current $I_D = 100 \mu\text{A}$.

(c) For the device in (b), find the value of V_{as} required to cause the device to operate as a 1000Ω resistor for very small V_{DS} .

Solution

$$(a) C_{\text{ox}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}} = \frac{3.45 \times 10^{-11}}{8 \times 10^{-9}} = 4.3212 \times 10^{-3} \text{ F/m}^2$$

$$k'_n = \mu_n C_{\text{ox}} \\ = 450 \times 10^{-4} \times 10^{12} \left(\frac{\mu\text{m}^2}{\text{V.s}} \right) \times 4.3212 \times 10^{-3} \text{ F/m}^2$$

$$= 450 \times 10^8 \frac{\mu\text{m}^2}{\text{V.s}} \times 4.3212 \times 10^{-15} \text{ F/}\mu\text{m}^2$$

$$= 194 \times 10^{-6} \text{ F/V.s} = 194 \mu\text{A/V}^2$$

(b) In saturation region, $i_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) (V_{GS} - V_t)^2$ (4)

$$i_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) (V_{GS} - V_t)^2$$

$$100 = \frac{1}{2} \times 194 \times \frac{8}{0.8} (V_{GS} - V_t)^2$$

$$V_{GS} = 1.021 \text{ V}$$

$$V_{DS\min} = V_{GS} - V_t = 1.021 - 0.7$$

$$V_{DS\min} = 0.321 \text{ V}$$

(c) For MOSFET in triode region, $V_{DS} = \text{small}$

$$i_D = k_n' \frac{W}{L} (V_{GS} - V_{DS})$$

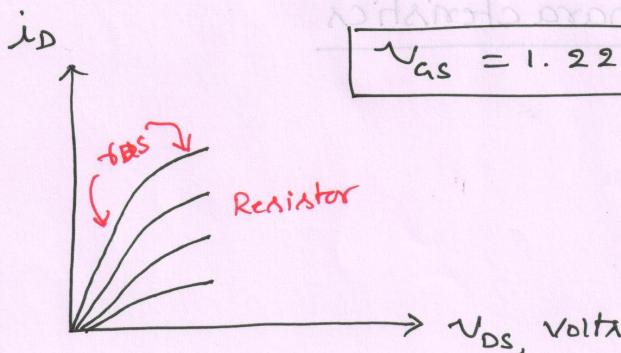
$$i_D = k_n' \left(\frac{W}{L}\right) [(V_{GS} - V_t) V_{DS}] \quad \text{Neglecting } \frac{V_{DS}^2}{2}$$

$$\gamma_{DS} = \frac{V_{DS}}{i_D} \quad | \quad V_{DS} = \text{small}$$

$$\gamma_{DS} = \frac{1}{k_n' \frac{W}{L} (V_{GS} - V_t)}$$

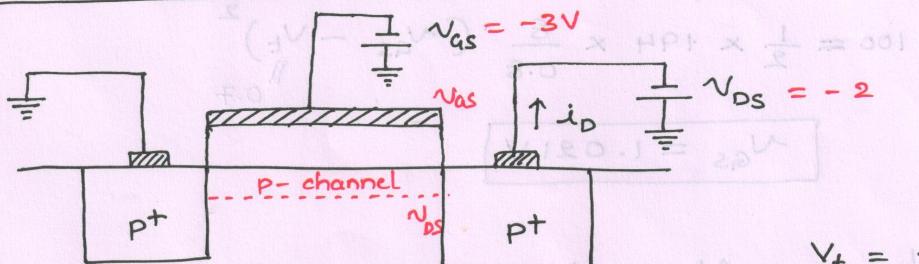
$$1000 = \frac{1}{194 \times 10^{-6} \times \frac{8}{0.8} (V_{GS} - 0.7)}$$

$$V_{GS} = 1.22 \text{ V}$$



(4) 4.2 & 4.3 : Home Work

The P-channel MOSFET



n-type substrate

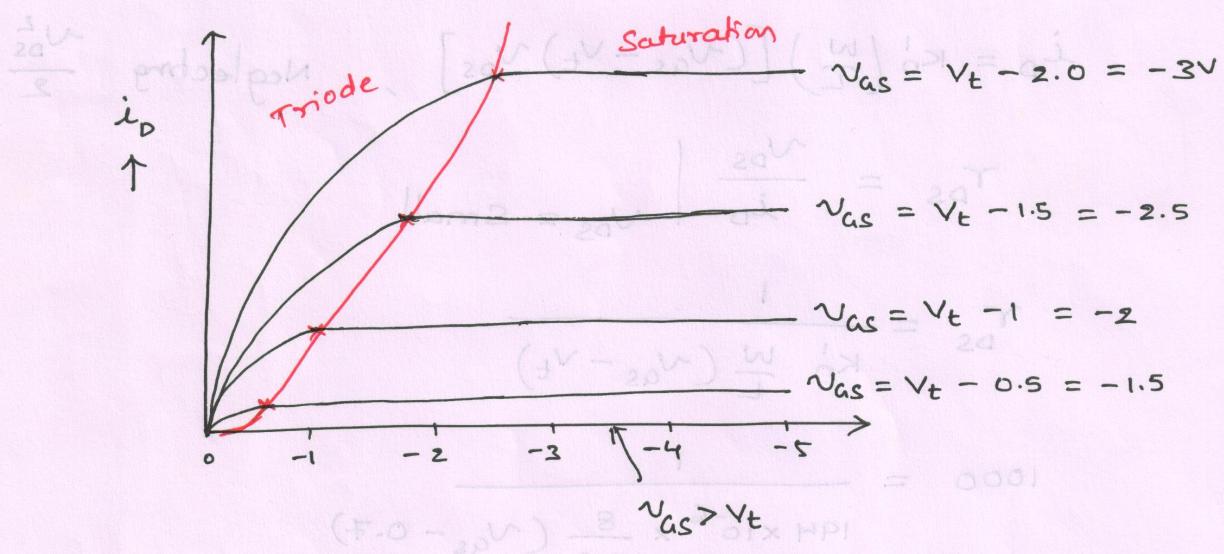
$$V_t = -1V$$

$V_{GS} = V_t$, just form
p-channel

$$V_{GS} - V_{DS} = V_t$$

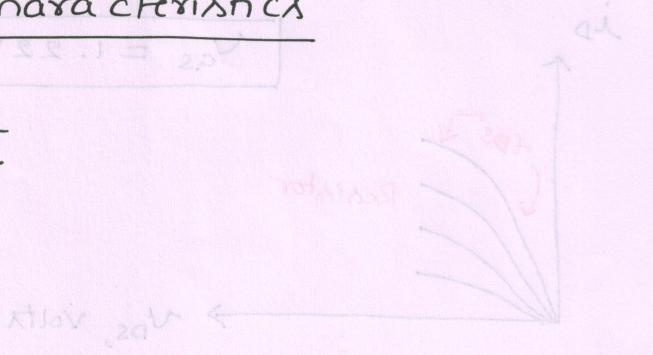
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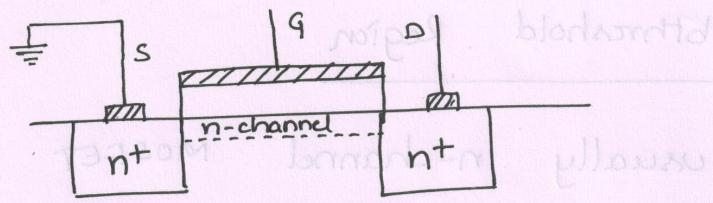
$$\text{Ex: } -3 - (-2) = -1V$$



4.2 current - voltage characteristics

4.2.1 circuit symbol





Dr. M. C. Hanumantharaju
Associate Professor
Dept. of ECE, BMSIT
Bangalore - 64

Ph: 9742290764

p-type body

Space indicates
gate is insulated

(a) n-channel enhancement type circuit symbol

Always
positive
to
source

(b) Modified symbol

Arrow is placed on Source end } shows bulk is shorted to source

(C) Simplified Symbol

* Complementary MOS

CMOS

The diagram illustrates a CMOS inverter circuit. It consists of two complementary metal-oxide-semiconductor (CMOS) transistors. On the left, there is an nMOS transistor with an n+ source/drain terminal and a poly gate. On the right, there is a pMOS transistor with a p+ source/drain terminal and a poly gate. Both transistors are positioned above a p-type body. Between the two transistors is a thick SiO_2 insulation layer. The entire structure is contained within an n-well region.

Fig 1 = (W) cross-section of a CMOS IC

Operating in Subthreshold Region

$V_{as} < V_t$, usually n-channel MOSFET
 do not conduct
 $i_D = 0$

NOT TRUE

→ For $V_{as} < V_t$, but close to V_t

i_D exists

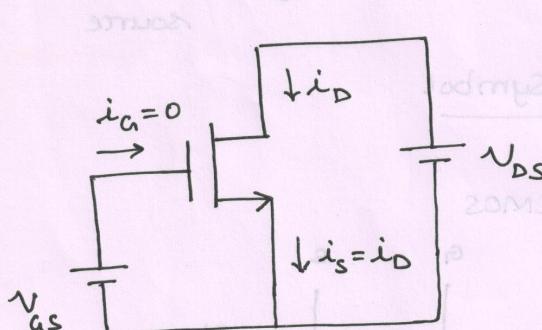
⇒ Subthreshold Region

$$i_D \propto e^{V_{as}}$$

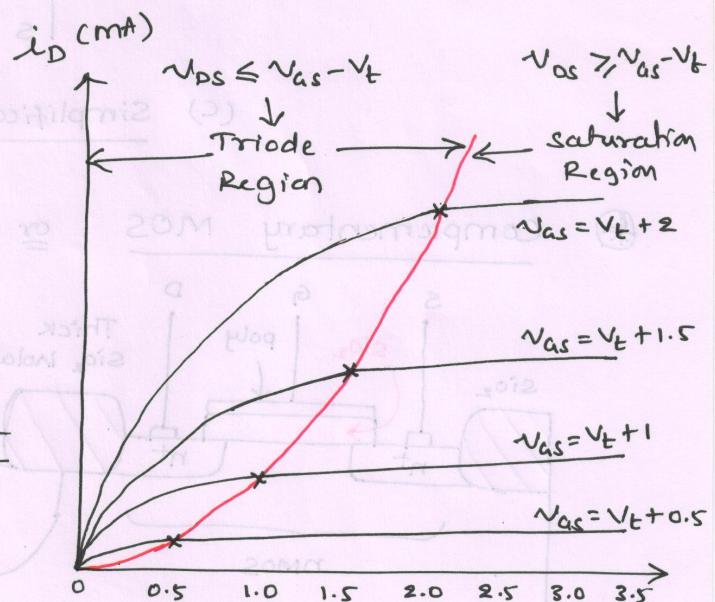
\cong III' to $i_C - V_{BE}$ in BJT

4.2.2

The $i_D - V_{DS}$ characteristics (static characteristics)



An n-channel enhancement MOSFET with V_{as} applied



$i - V_{DS}$ characteristics

with $k_n' \left(\frac{W}{L} \right) = 1 \text{ mA}$

$\rightarrow V_{DS}$ (V)

From characteristics:

(6)

Three distinct regions of operation

① The cut-off region } 'switch'

② The Triode region

③ The Saturation region } 'Amplifier'

① The cut-off region

$V_{AS} < V_t$, no channel, $i_D = 0$

② The triode region or Linear region

$V_{AS} \geq V_t$ [Induced channel]

$V_{GD} > V_t$ [continuous channel] MOSFET in triode Region

Ex: $V_{AS} = 3V$

$$V_{AS} - V_t = V_{OV} = 2V$$

$V_{DS,SAT} = 2V$ (if $V_{DS} = 1V$)
(min)

then, $V_{GD} = 1V$

$V_{DS} = 1V$ $V_{GD} = 1V$: continuous channel
 $V_{GD} > V_t$

cond'n explicitly stated

$$V_{DS} = 2V$$

$$V_{GD} = 0 < V_t$$

\Rightarrow channel is not continuous

$$V_{GD} < V_t$$

in terms of V_{DS}

$$V_{GD} = V_{AS} + V_{SD}$$

$$3V \geq 2V - 2V$$

or

$$V_{GD} = V_{AS} - V_{DS}$$

no baroring

$$3V - 2V \leq 2V$$

$$V_{AS} - V_{DS} > V_t$$

since $V_{GD} > V_t$

$$V_{DS} < V_{AS} - V_t$$

Continuous channel

$$i_D = k_n' \left(\frac{w}{L} \right) \left[(V_{AS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

→ Linear Equation

$$i_D \approx k_n' \left(\frac{w}{L} \right) [(V_{AS} - V_T) V_{DS}]$$

$$r_{DS} = \frac{V_{DS}}{i_D}$$

$V_{DS} = \text{small}$

$a = \text{constant}$ $V_{AS} = \text{constant}$

$$r_{DS} = \frac{k_n' \left(\frac{w}{L} \right) (V_{AS} - V_T)}{k_n' \left(\frac{w}{L} \right) V_{DS}}$$

→ Relation $r_{DS} \propto V_{DS}$

③ Saturation Region

$$V_{AS} \geq V_T \quad [\text{induced channel}]$$

$$V_{AS} \leq V_T \quad [\text{pinched-off channel}]$$

This condition can be alternatively expressed

in terms of $-V_{DS}$

$$\exists V > \text{Consider } V_{AD} = V_{AS} - V_{DS}$$

$$\text{since } V_{AD} \leq V_T \quad \Rightarrow \quad V_{AS} - V_{DS} \leq V_T$$

$$V_{AS} - V_{DS} \leq V_T$$

$$V_{DS} \geq V_{AS} - V_T \quad [\text{pinched off channel}]$$

$$\exists V - 20V > 20V$$

$$V_{DS} = V_{GS} - V_t \quad [\text{Boundary condition}]$$

(7)

Therefore, substituting this condition in linear current equation

$$i_D = \frac{1}{2} k_n' \left(\frac{w}{L} \right) (V_{GS} - V_t)^2$$

$$G \xrightarrow{i_G=0} +$$

$$V_{GS}$$

$$V_S = 20V$$

$$-$$

$$i_D = \frac{1}{2} k_n' \frac{w}{L} (V_{GS} - V_t)^2$$

$$\downarrow \frac{1}{2} k_n' \frac{w}{L} (V_{GS} - V_t)^2 V_{DS}$$

$$V_S = 20V$$

$$-$$

$$V_D = 20V$$

$$-$$

$$V_D = 20V$$

$$-$$

$$V_D = 20V$$

Large Signal Equivalent circuit Model for MOSFET in saturation

④ channel length modulation Effect

→ In saturation, i_D is independent of V_{DS}

Therefore, Incremental Resistance $= r_o = \frac{\Delta V_{DS}}{\Delta i_D}$

→ $w \cdot k \cdot T \quad V_{DS, sat} = V_{GS} - V_t$

As $V_{DS} > V_{DS, sat}$, pinch-off point moves

from drain towards source

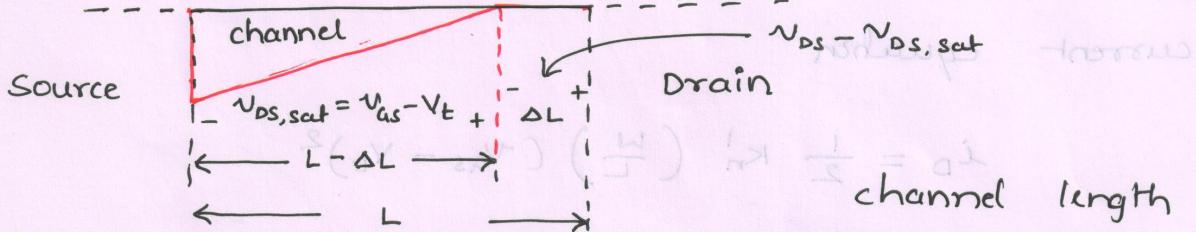
→ The channel length in effect reduced from L to

$L - \Delta L \Rightarrow$ phenomenon in "channel length modulation"

(F)

$$[n\text{-tubros}] \quad jV - 20V = 20V$$

resistors in n-tubros with per unit length property



Ex:

$$V_T = 1V$$

$$V_{DS} = 5V$$

$$V_{AS} = 4V$$

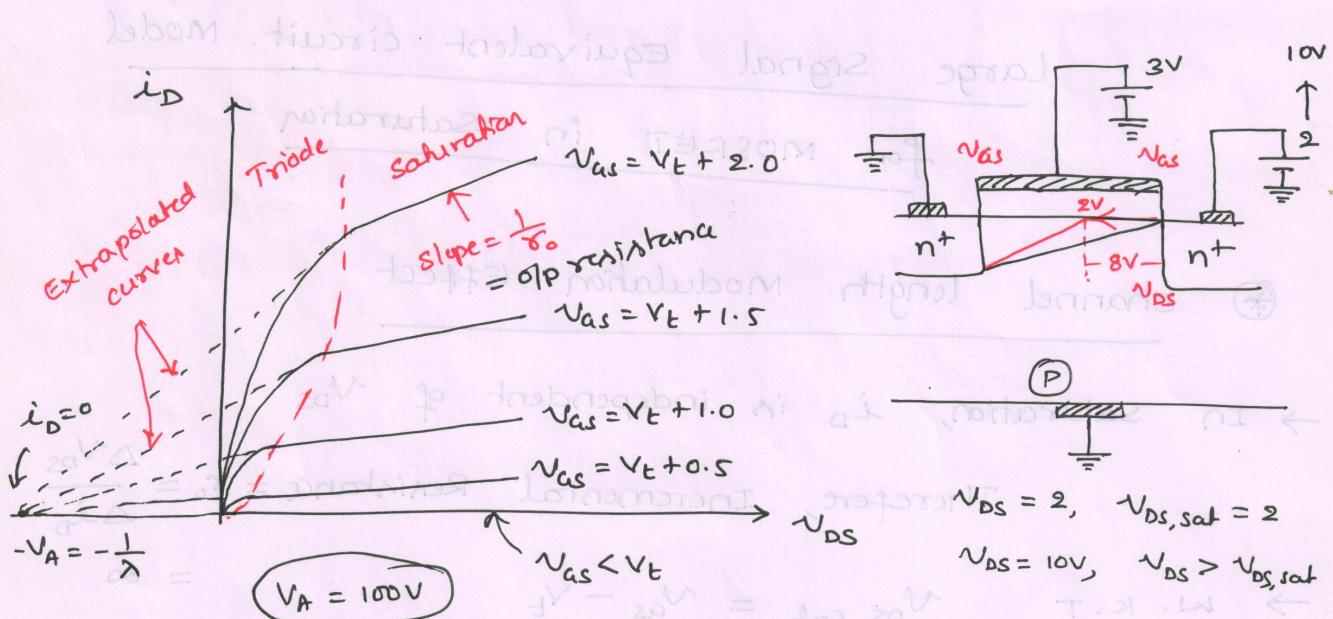
$$V_{OV} = 3V$$

$$V_{DS,sat} = 3V$$

$$\text{Additional } V_{DS} = 2V$$

Modulation = Early Effect

$$\text{Saturation current} = I_D = \frac{1}{2} K_n \frac{W}{L} (V_{AS} - V_T)^2$$



To account for I_D dependence on V_{DS} in saturation

replace L by $L - \Delta L$

$$I_D = \frac{1}{2} K_n \left(\frac{W}{L} \right) (V_{AS} - V_T)^2 = \frac{1}{2} K_n \frac{W}{(L - \Delta L)} (V_{AS} - V_T)^2$$

of L more number except in digital circuits etc

$$= \frac{1}{2} K_n \left(\frac{W}{L} \right) \times \frac{1}{\left(1 - \frac{\Delta L}{L} \right)} (V_{AS} - V_T)^2$$

"molti tuberosi digitali"

$$= \frac{1}{2} k_n' \left(\frac{w}{L} \right) \frac{\left(1 + \frac{\Delta L}{L} \right)}{\left(1 - \frac{\Delta L}{L} \right) \left(1 + \frac{\Delta L}{L} \right)} (V_{as} - V_t)^2$$

$$= \frac{1}{2} k_n' \left(\frac{w}{L} \right) \frac{1 + \frac{\Delta L}{L}}{1 - \left(\frac{\Delta L}{L} \right)^2} (V_{as} - V_t)^2$$

→ Negligible

Assuming $\frac{\Delta L}{L} \ll 1$ and $\Delta L \propto V_{DS}$

$$\approx \frac{1}{2} k_n' \left(\frac{w}{L} \right) \left(1 + \frac{\Delta L}{L} \right) (V_{as} - V_t)^2$$

$$\Delta L = \lambda' V_{DS}$$

\uparrow process technology parameter

$$i_D = \frac{1}{2} k_n' \left(\frac{w}{L} \right) \left(1 + \frac{\lambda' V_{DS}}{L} \right) (V_{as} - V_t)^2$$

$$\text{let } \lambda = \frac{\lambda'}{L}$$

$$i_D = \frac{1}{2} k_n' \left(\frac{w}{L} \right) \left(1 + \lambda V_{DS} \right) (V_{as} - V_t)^2$$

$$\text{For } i_D = 0, V_{DS} = -\frac{1}{\lambda} = -V_A$$

$$\Rightarrow V_A = \frac{1}{\lambda} \quad V_A \propto L \quad \boxed{V_A = V_A' L}$$

$$i_D = \frac{1}{2} k_n' \left(\frac{w}{L} \right) \left(1 + \frac{V_{DS}}{V_A} \right) (V_{as} - V_t)^2$$

Early voltage

$$r_o = \left. \frac{1}{\frac{\partial i_D}{\partial V_{DS}}} \right|_{V_{as}=\text{constant}}$$

$$r_o = \frac{1}{\frac{1}{2} k_n' \left(\frac{w}{L} \right) (V_{as} - V_t)^2 \frac{V_{DS}}{A}} = \frac{1}{\frac{I_D}{V_A}}$$

No early effect

$$\boxed{r_o = \frac{V_A}{I_D}}$$

D/P resistance is inversely proportional to drain current.

④ MOSET circuits at DC

MOSFET circuit operating in DC

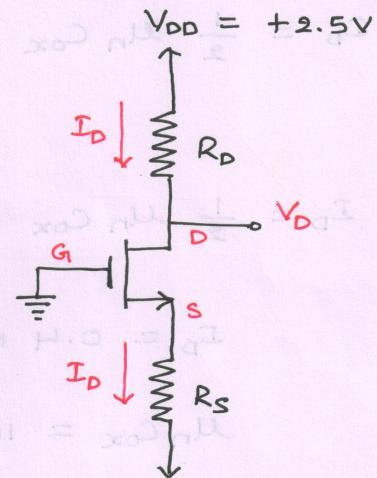
- ⑤ Design the circuit so that $I_D = 0.4 \text{ mA}$
and $V_D = +0.5 \text{ V}$

$$V_t = 0.7 \text{ V}$$

$$\mu_n C_{ox} = 100 \text{ } \mu\text{A/V}^2$$

$$L = 1 \text{ } \mu\text{m}$$

$$W = 32 \text{ } \mu\text{m}$$



Solution

Design ?

calc. R_D & R_S

Step ① Determine the mode of operation of MOSFET

Triode Saturation ✓ Cutoff

Compare V_{GD} and V_t

$$V_{GD} = V_G - V_D = -V_D < V_t \quad \text{Saturation Mode}$$

Step ② Write the appropriate equation for I_D

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)$$

$\uparrow \quad \uparrow \quad \uparrow \quad \uparrow$

Given Known process
Drain current parameter
(Design Aspect ratio
parameter) of MOSFET

$$V_{GS} = V_G - V_S$$

$\uparrow \quad \uparrow$

Known

$$V_S = 2 \text{ V}$$

Step ③ calculate the values of R_D and R_S

$$R_D = \frac{V_{DD} - V_D}{I_D} \quad R_S = \frac{V_S - V_{SS}}{I_D}$$

→ By applying KVL

From step ② $V_{D.S} = V_D$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_{ov}^2 \quad \text{--- ①}$$

$$I_D = 0.4 \text{ mA} = 400 \text{ } \mu\text{A}$$

$$\mu_n C_{ox} = 100 \text{ } \mu\text{A}/\text{V}^2$$

$$\frac{W}{L} = \frac{32 \text{ } \mu\text{m}}{1 \text{ } \mu\text{m}} = \frac{32}{1} ; \text{ Assume } \lambda = 0$$

(Neglecting channel length modulation effect)

$$400 = \frac{1}{2} \times 100 \times \frac{32}{1} \times V_{ov}^2$$

$$V_{ov} = 0.5 \text{ V}$$

$$V_{GS} = V_{ov} + V_t$$

$$V_{GS} = 0.5 + 0.7 = 1.2 \text{ V}$$

$$V_{AS} = 1.2 \text{ V}$$

$$V_{AS} = V_A - V_S$$

$$1.2 \text{ V}$$

$$V_S = -1.2 \text{ V}$$

From Step ③

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{2.5 - 0.5}{0.4} = 5 \text{ k}\Omega$$

(10)

$$R_D = 5 \text{ k}\Omega$$

$$R_S = \frac{V_S - V_{SS}}{I_D} = \frac{-1.2 - (-2.5)}{0.4} = 3.25 \text{ k}\Omega$$

$$R_S = 3.25 \text{ k}\Omega$$

$$V_{GSS} = -1.2 \text{ V}$$

$$V_S = -1.2 \text{ V}$$

$$R_S = 3.25 \text{ k}\Omega$$

$$R_D = 5 \text{ k}\Omega$$

Therefore, to establish a DC voltage of 0.5V at Drain

$$R_D = 5 \text{ k}\Omega, \text{ & } R_S = 3.25 \text{ k}\Omega$$

P Design the circuit so that $I_D = 80 \text{ mA}$
calculate R and V_D

$$V_t = 0.6 \text{ V}$$

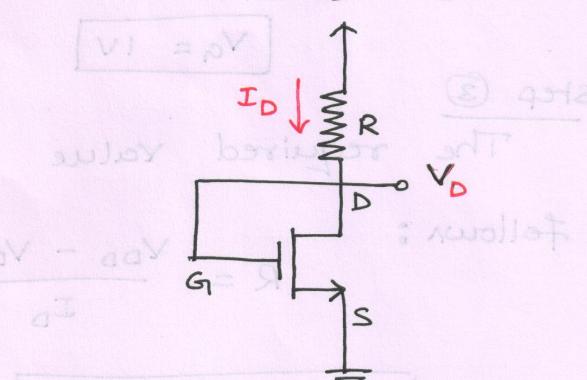
$$4nCox = 200 \text{ mA/V}^2$$

$$L = 0.8 \mu\text{m}$$

$$W = 4 \mu\text{m}$$

$$V_{DD} = +3 \text{ V}$$

$$V_I = 0 \text{ V}$$



Solution

1. Determine the mode of operation of MOSFET

Compare V_{GD} & V_t

$$V_{GD} = V_G - V_D = 0, \text{ since } V_G = V_D$$

$V_{GD} = 0 < V_t$ (0.6V) Saturation Region

2. Write the appropriate equation for I_D

$$I_D = \frac{1}{2} \ln C_{ox} \frac{W}{L} (V_{as} - V_t)^2$$

Known process
Transconductance parameter
 $(2.5 - 1) = 1.1$
H.O.

Given
as
Design parameter

Known
Aspect ratio of MOSFET

$V_{as} = V_G - V_S$
 $(V_G = V_D)$
 $= V_D - V_S$

$$80 = \frac{1}{2} \times 200 \times \frac{4}{0.8} \times V_{ov}^2$$

prior to V_{as} p

$$V_{ov} = 0.4V$$

$$V_{ov} = V_{as} - V_t \Rightarrow$$

$$V_{as} = 1V$$

$$\text{All } C_{ox} = 0.1 \text{ to } 0.6V$$

$$V_D = 1V$$

$$V_G = 1V$$

step ③

The required value of R can be found as follows:

$$R = \frac{V_{DD} - V_D}{I_D} = \frac{3 - 1}{0.080} = 25 k\Omega$$

$$V_D = V_g = +1V$$

$$R = 25 k\Omega$$

$$V_{as} = 3V$$

$$V_D = 1V$$

$$V_G = 1V$$

$$R = 25 k\Omega$$

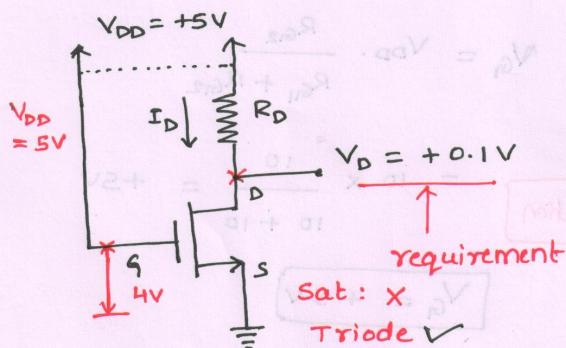
Solution

Dr. M. C. Hanumantharaju
Associate Professor
Dept. of ECE, BMSIT

ph: 9742290764

(P) Design the circuit in the figure below to establish a drain voltage of 0.1V . What is the effective resistance between drain and source at this operating point? Let $V_t = 1\text{V}$ and

$$k_n' \left(\frac{W}{L} \right) = 1\text{mA/V}^2$$



solution :

$$V_t = 1\text{V}, k_n' \left(\frac{W}{L} \right) = \frac{1\text{mA}}{\text{V}^2}$$

$$R_D = ?$$

$$\begin{aligned} V_G &= 5\text{V} \\ V_D &= 0.1\text{V} \end{aligned} \quad \left. \begin{aligned} V_{GD} &= 4.9 \\ V_{AD} &= 4.9 \end{aligned} \right\}$$

$V_{GD} > V_t \Rightarrow$ Triode Region

$$\begin{aligned} i_D &= k_n' \left(\frac{W}{L} \right) \left[(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \\ &= 1 \left[(5 - 1)(0.1) - \frac{1}{2}(0.1)^2 \right] \end{aligned}$$

$$i_D = 0.395 \text{ mA}$$

$$r_{ds} = \frac{V_{DS}}{i_D} = \frac{0.1}{0.395}$$

The required value of R_D is

$$R_D = \frac{V_{DD} - V_D}{i_D} = \frac{5 - 0.1}{0.395} = 12.4 \text{ k}\Omega$$

$$r_d = 253 \Omega$$

$$R_D = 12.4 \text{ k}\Omega$$

(P) Analyze the circuit shown to determine the voltages at all nodes and currents through all branches. Let $V_t = 1\text{V}$ and $k_n' \left(\frac{W}{L} \right) = 1\text{mA/V}^2$. Neglect the channel length modulation effect (i.e. assume $\lambda = 0$)

$$V_S = 5 - 2 = 3\text{V} - 0\text{V} = 3\text{V}$$

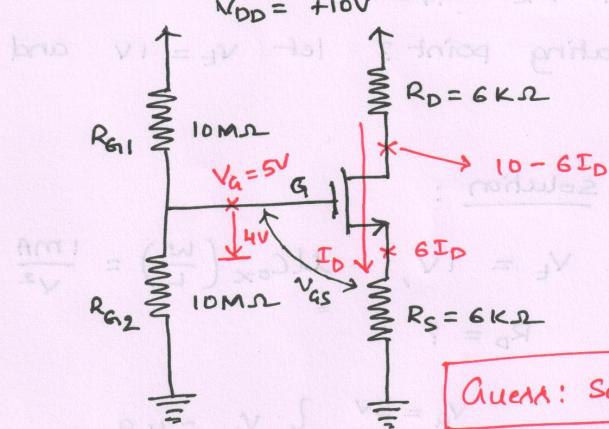
$$V_F = 2.0 \times 2.40 = 4.8 - 0 = 4\text{V}$$

Next page

No voltage regulation if $V_S > V_D \Leftarrow$

because voltage across source is zero

④ A drain of loaded output in the circuit set in fig. Draw the equivalent circuit for power supply.



Solution:

$$i_G = 0$$

by using voltage division rule,

$$V_G = V_{DD} \cdot \frac{R_{G2}}{R_{G1} + R_{G2}}$$

$$= 10 \times \frac{10}{10 + 10} = +5V$$

$$\boxed{V_G = +5V}$$

Since $V_G = +5V$, NMOS = ON

$$V_S = I_D (\text{mA}) \times 6 (\text{k}\Omega) = 6 I_D (\text{V})$$

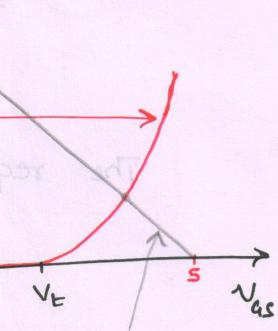
$$V_{GS} = 5 - 6 I_D$$

$$I_D = \frac{1}{2} \mu_C \alpha \left(\frac{W}{L} \right) (V_{GS} - V_t)^2$$

$$I_D = 0.5 (5 - 6 I_D - 1)^2$$

$$18 I_D^2 - 25 I_D + 8 = 0$$

This equation yields two values



$$5 = V_{GS} + 6 I_D$$

~~$$I_D = 0.89 \text{ mA}$$~~ and
$$\boxed{I_D = 0.5 \text{ mA}}$$

$$V_S = 6 I_D = 6 \times 0.89 \text{ mA} = 5.34 \text{ V} > V_G, \text{ NMOS OFF}$$

$$V_S = 6 I_D = 6 \times 0.5 \text{ mA} = 3 \text{ V} < V_G \checkmark$$

$$V_{GS} = V_G - V_S = 5 - 3 = 2 \text{ V}$$

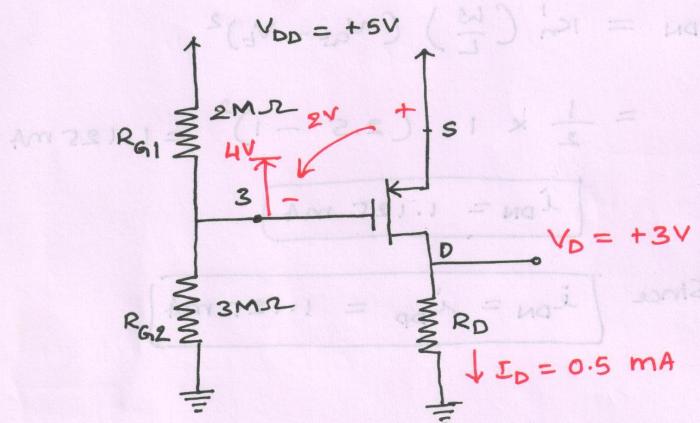
$$V_D = 10 - 6 I_D = 10 - 6 \times 0.5 \text{ mA} = +7 \text{ V}$$

$$\text{since } V_{GD} = -2 \text{ V}$$

$\Rightarrow V_{GD} < V_t$ Transistor operates in saturation region, as initially assumed

(P) Design the circuit so that $I_D = 0.5 \text{ mA}$
 4.6 and $V_D = +3V$

such that it operates in saturation. What is the largest value of R_D such that operation in the saturation mode is maintained.



$$V_t = -1V$$

$$K_p' \left(\frac{W}{L} \right) = 1 \text{ mA/V}^2$$

→ p. channel Transistor

$$I_D = \frac{1}{2} K_p' \left(\frac{W}{L} \right) (V_{GS} - V_t)^2$$

$$0.5 = \frac{1}{2} \times 1 \left(V_{GS} + 1 \right)^2$$

$$V_{GS} - V_t = \pm 1$$

$$V_{GS} = -2V$$

$$\boxed{V_{GS} = 0V} X$$

$$V_a = V_{GS} + V_s = -2 + 5 = 3V$$

choose $R_{G1} = 2 \text{ M}\Omega$ and $R_{G2} = 3 \text{ M}\Omega$ (Ratio is 2:3)

R_{G1} & R_{G2} : No matter

$$R_D = \frac{V_D}{I_D} = \frac{3V}{0.5 \text{ mA}} = 6 \text{ k}\Omega$$

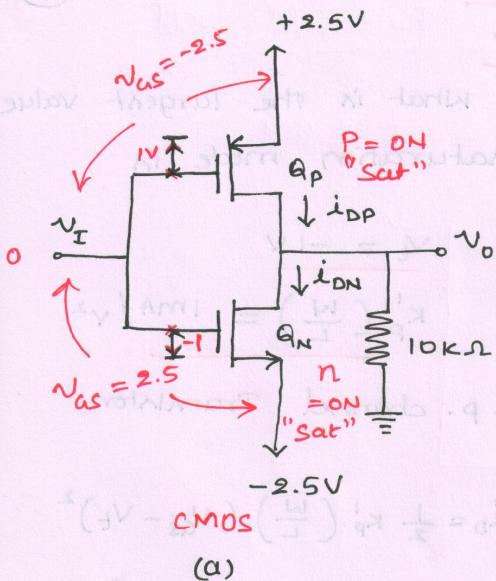
to find larger value of R_D for saturation

$$R_D = \frac{4}{0.5} = 8 \text{ k}\Omega = \frac{V_{Dmax}}{I_D} = \frac{V_{Dmax}}{0.5} = V_{Dmax} = V_a + |V_t| \\ = 3 + 1 = 4V$$

(P) Ex. 4.7 : The NMOS and PMOS transistors in the circuit of figure shown below are matched with $K_n' \left(\frac{W_n}{L_n} \right) = K_p' \left(\frac{W_p'}{L_p'} \right) = 1 \text{ mA/V}^2$ and $V_{tN} = -V_{tp} = 1V$. Assuming $\lambda = 0$ for both devices, find the drain currents I_{DN} and I_{DP} , as well as the voltage V_o , for $V_I = 0V, +2.5V$, and $-2.5V$.

$$AM H.R.O = mai$$

$$VN.H.S = mai$$



$$i_{DP} = i_{DN}$$

$$V_{as} - V_t = -2.5 - (-1) = -1.5 \rightarrow p$$

$$V_{as} - V_t = 2.5 - 1 = 1.5 \rightarrow n$$

$$i_{DP} = i_{DN}$$

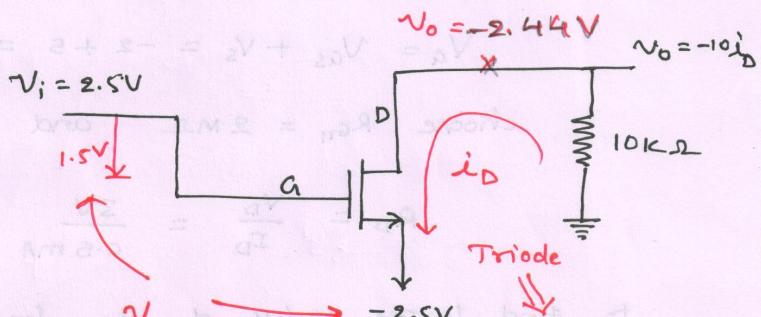
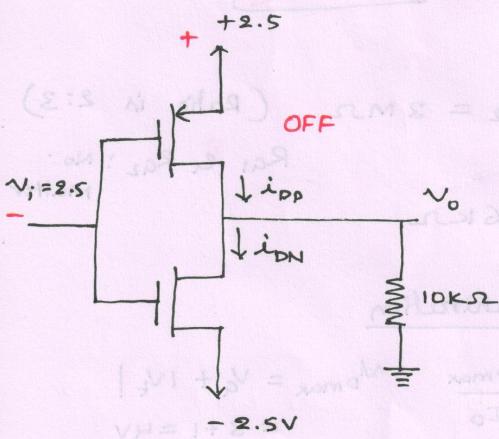
$$i_{DN} = k_n' \left(\frac{W}{L} \right) (V_{as} - V_t)^2$$

$$= \frac{1}{2} \times 1 \times (2.5 - 1)^2 = 1.125 \text{ mA}$$

$$i_{DN} = 1.125 \text{ mA}$$

Since $i_{DN} = i_{DP} = 1.125 \text{ mA}$

(iii) $V_i = 2.5 \text{ V}$



$$V_{DS} = V_o - (-2.5 \text{ V})$$

$$= 2.5 - 10i_{DN}$$

$$i_{DN} = k_n' \left(\frac{W}{L} \right) \left[(V_{as} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

Assume V_{DS} is very small

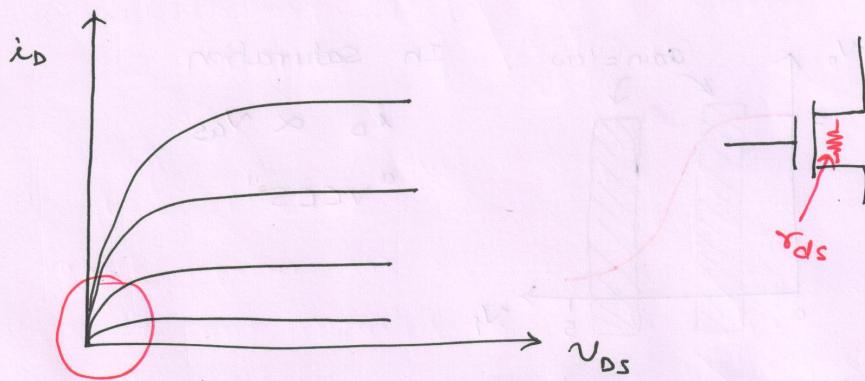
$$i_{DN} = \frac{1}{2} (5 - 1) (2.5 - 10i_{DN})$$

$$i_{DN} = 0.244 \text{ mA}$$

$$V_o = -2.44 \text{ V}$$

$$V_{DS} = 2.5 - 2.44$$

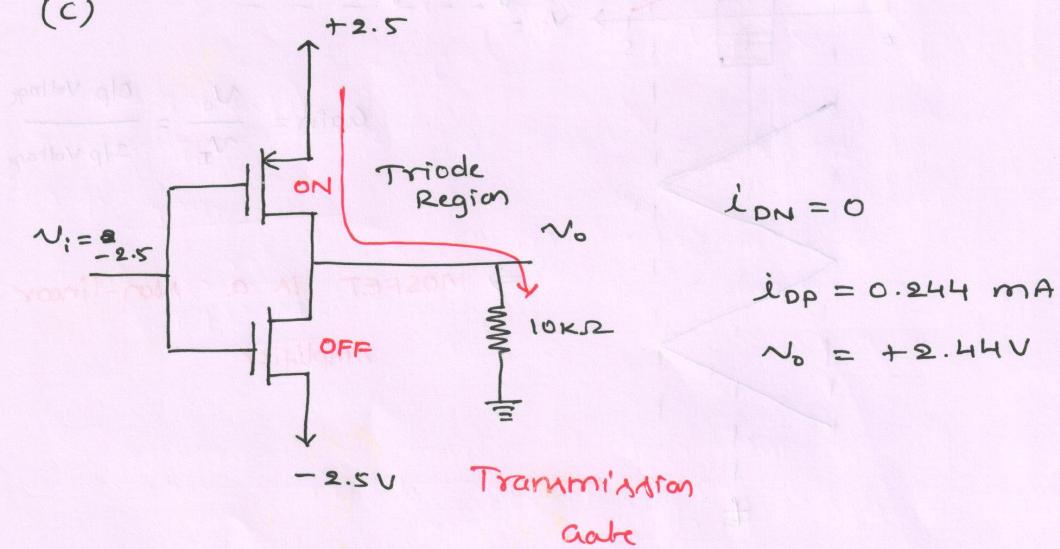
$$V_{DS} = 0.06 \text{ V}$$



$$r_{DS} = \frac{V_{DS}}{i_D} = \frac{1}{k' \left(\frac{W}{L}\right) (V_{GS} - V_T)} \Rightarrow r_{DS} \text{ very small}$$

Very large

(c)



Dr. M. C. Hanumanthareju
Associate Professor

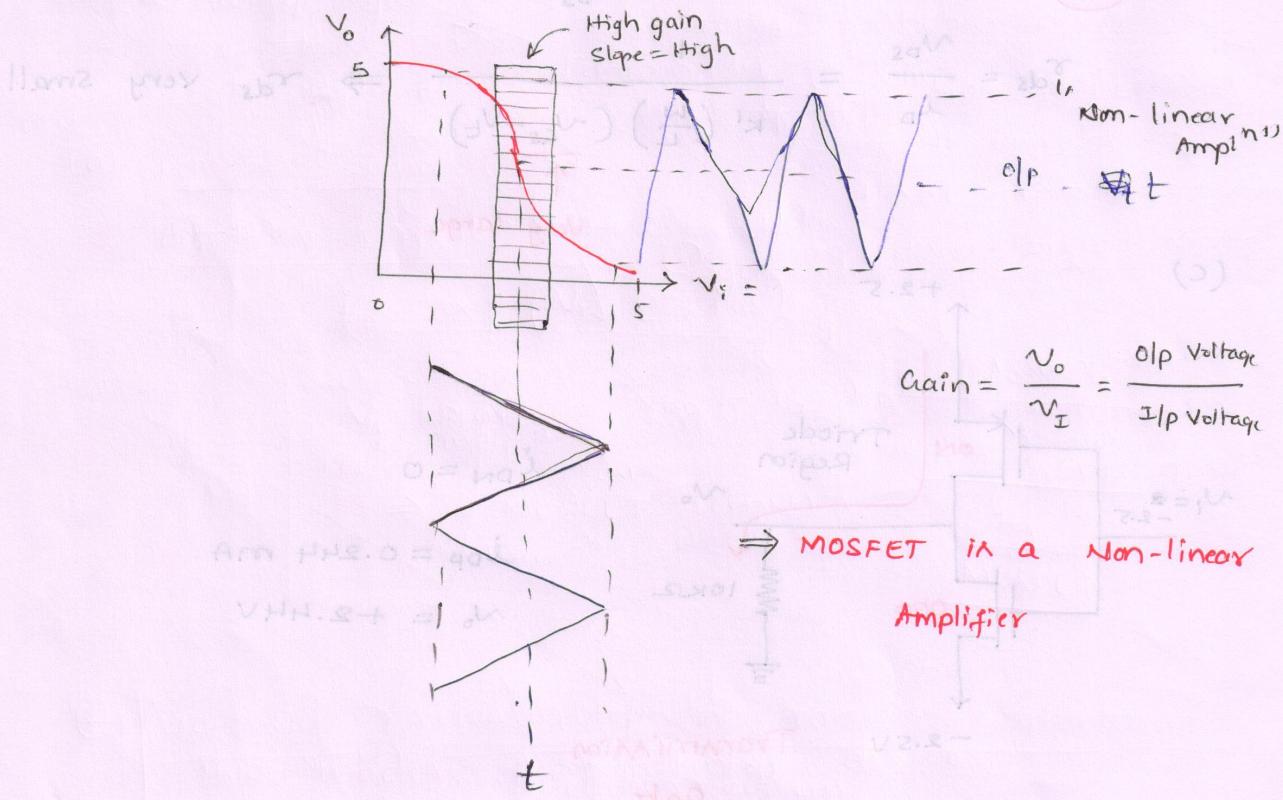
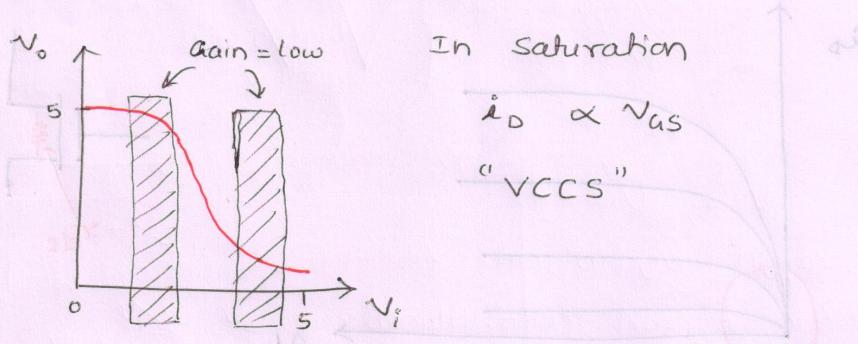
Dept. of ECE

BMSIT, Bangalore

ph: 9742290764

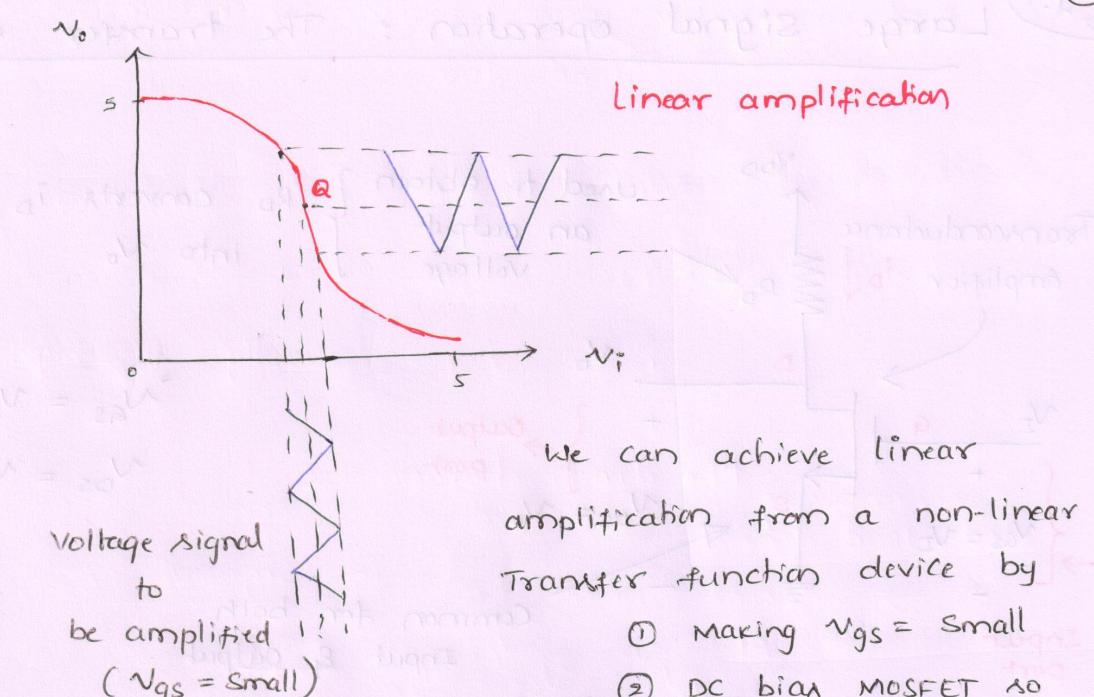
The MOSFET as an Amplifier and as a switch

MOSFET : Non linear Device



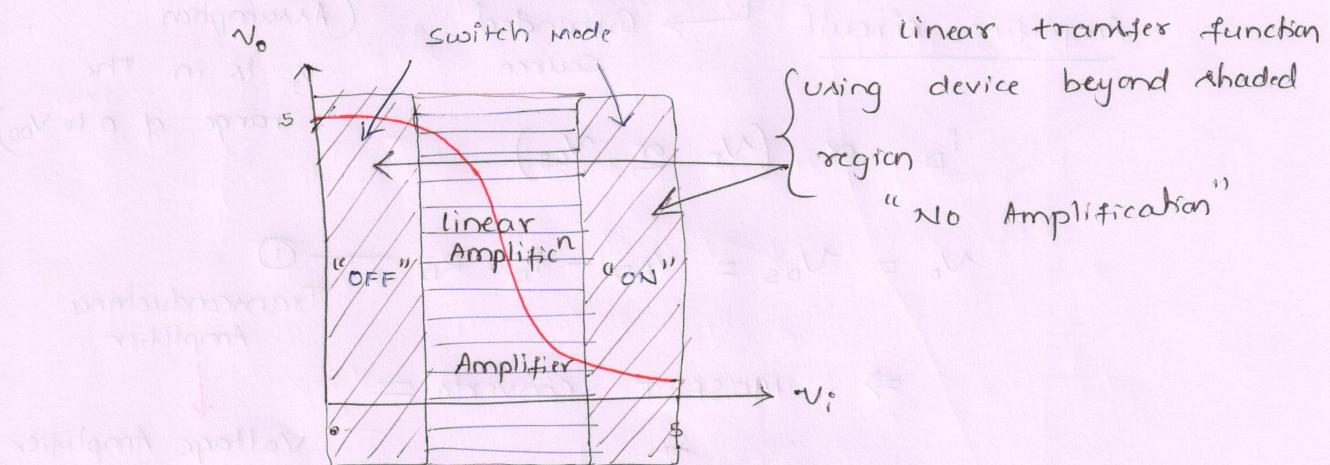
How do we get linear amplification from device that have highly non-linear transfer function?

Solution: DC biasing MOSFET to operate at appropriate v_{as}



We can achieve linear amplification from a non-linear Transfer function device by

- ① Making $V_{gs} = \text{small}$
- ② DC bias MOSFET so that it operates in



Two modes of Non-linear device

① linear amplifier mode

Achieved linear amplification by choosing appropriate bias bi-point

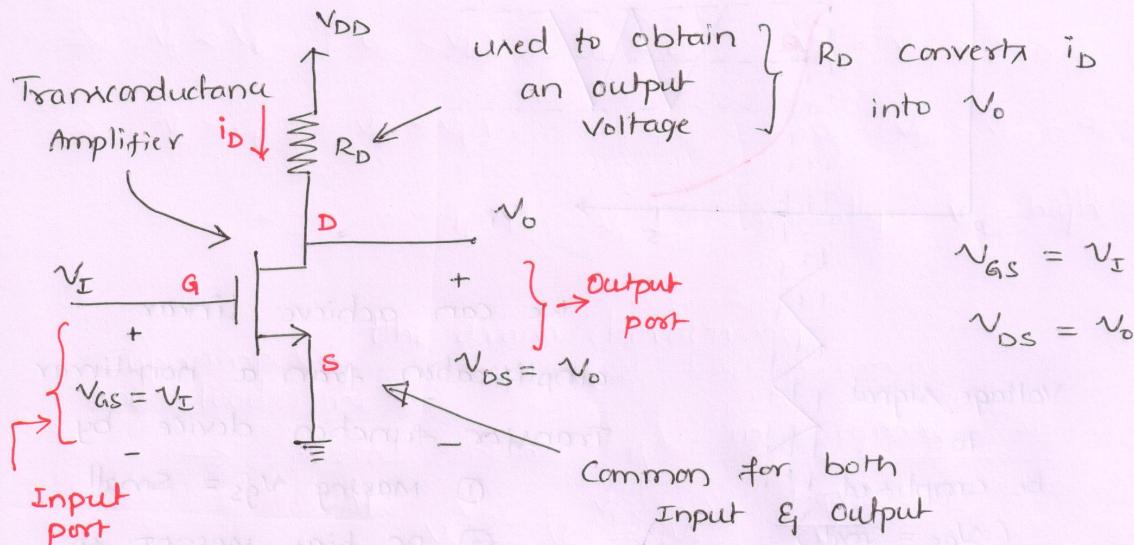
② switch mode

Output = constant for a range of input

④.1

Large signal operation : The transfer characteristic

Referencing notes



$$V_{GS} = V_I$$

$$V_{DS} = V_o$$

Common for both
Input & output

(a) Common Source (CS)

Amplifier circuit \rightarrow Grounded Source

(Assumption

V_I is in the
range of 0 to V_{DD})

$$i_D \propto (V_I \text{ or } V_{GS})$$

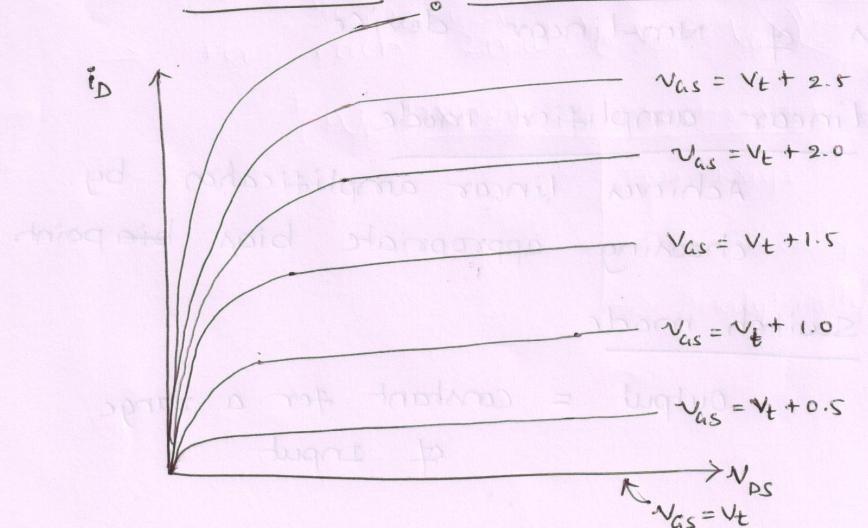
$$V_o = V_{DS} = V_{DD} - i_D \cdot R_D \quad \text{--- (1)}$$

\Rightarrow MOSFET converts =

Transconductance
Amplifier

\downarrow
Voltage Amplifier

Graphical Derivation of the Transfer characteristics



Relation between

V_{DS} & i_D

for

MOSFET

(15)

From Q1 we can draw drain current vs drain voltage

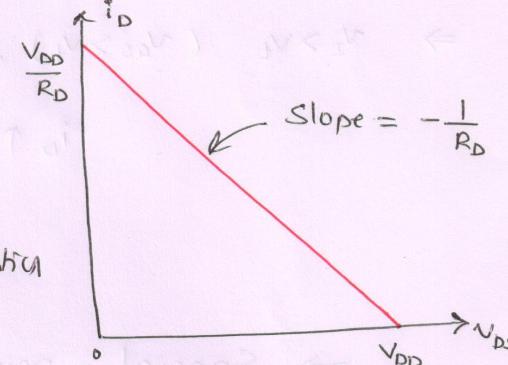
$$V_{DS} = V_{DD} - i_D \cdot R_D$$

or $i_D = \frac{V_{DD}}{R_D} + \left(-\frac{1}{R_D}\right)V_{DS} = \left(-\frac{1}{R_D}\right)V_{DS} + \frac{V_{DD}}{R_D} \Rightarrow$ straight line

Compare

$$y = mx + c$$

$$i_D = \left(-\frac{1}{R_D}\right)V_{DS} + \frac{V_{DD}}{R_D}$$



Superimposing the drain characteristic

and load line

Fig. (2) Graphical Representation

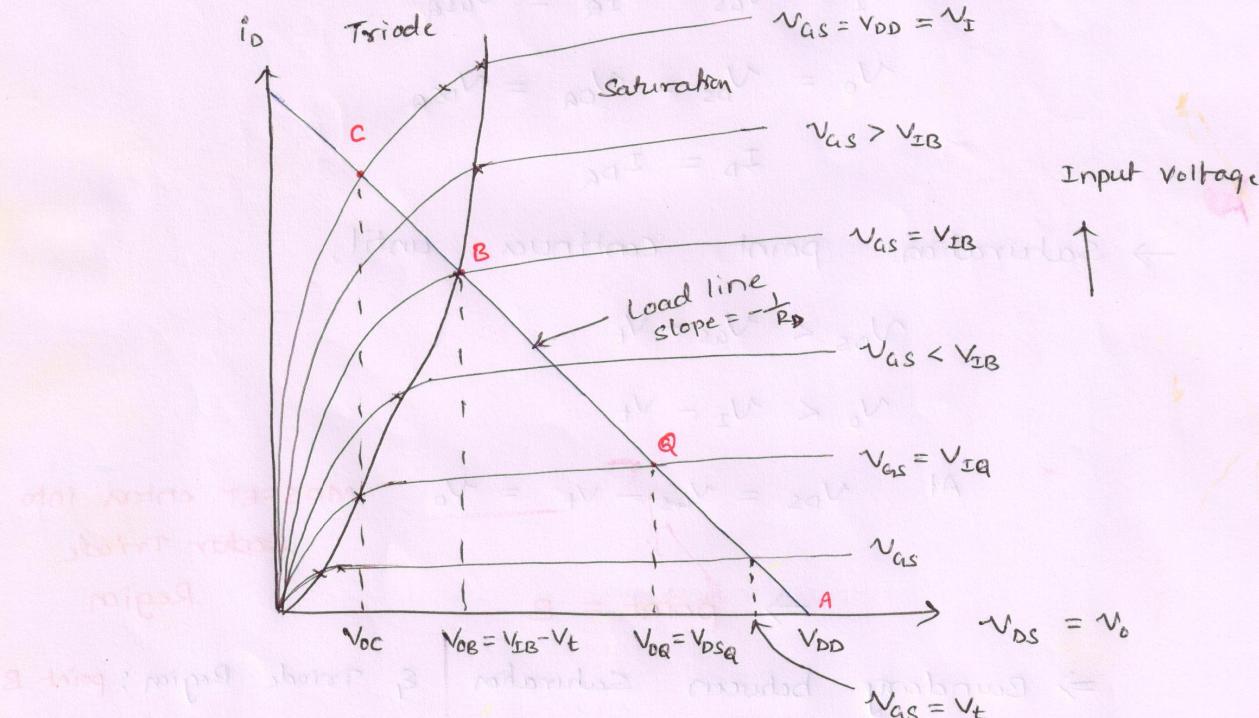


Fig. Transfer characteristics of the amplifier

- Two ways
 - Graphically ✓
 - Analytically

→ For each Input ($V_I = V_{GS}$), corresponding output ($V_0 = V_{DS}$)

21) Find intersection point of transfer characteristics & load line.

$$\Rightarrow V_I < V_t \quad (V_{AS} < V_t), \quad i_D = 0, \quad V_o = V_{DS} = V_{DD} \quad \text{point = A (cutoff)}$$

$$\Rightarrow V_I > V_t \quad (V_{AS} > V_t), \quad i_D \neq 0, \quad V_o = V_{DS} = V_{DD} - R_D \cdot i_D$$

$$i_D \uparrow, \quad V_o \downarrow, \quad \text{initially } V_o = \text{high}$$

"saturation"

load line segment: AB

→ Special point, Q in Segment AB

$$V_I = V_{AS} = V_{IQ} = V_{ASQ}$$

$$V_o = V_{DS} = V_{OQ} = V_{DSQ}$$

$$I_D = I_{DQ}$$

→ Saturation point continues until,

$$V_{DS} < V_{AS} - V_t$$

$$V_o < V_I - V_t$$

At $V_{DS} = V_{AS} - V_t = V_o$, MOSFET enters into
Triode Region

⇒ point = B

⇒ Boundary between Saturation & Triode Region: point B

At point B, $V_{OB} = V_{IB} - V_t$

$$V_{DS} = V_{AS} - V_t$$

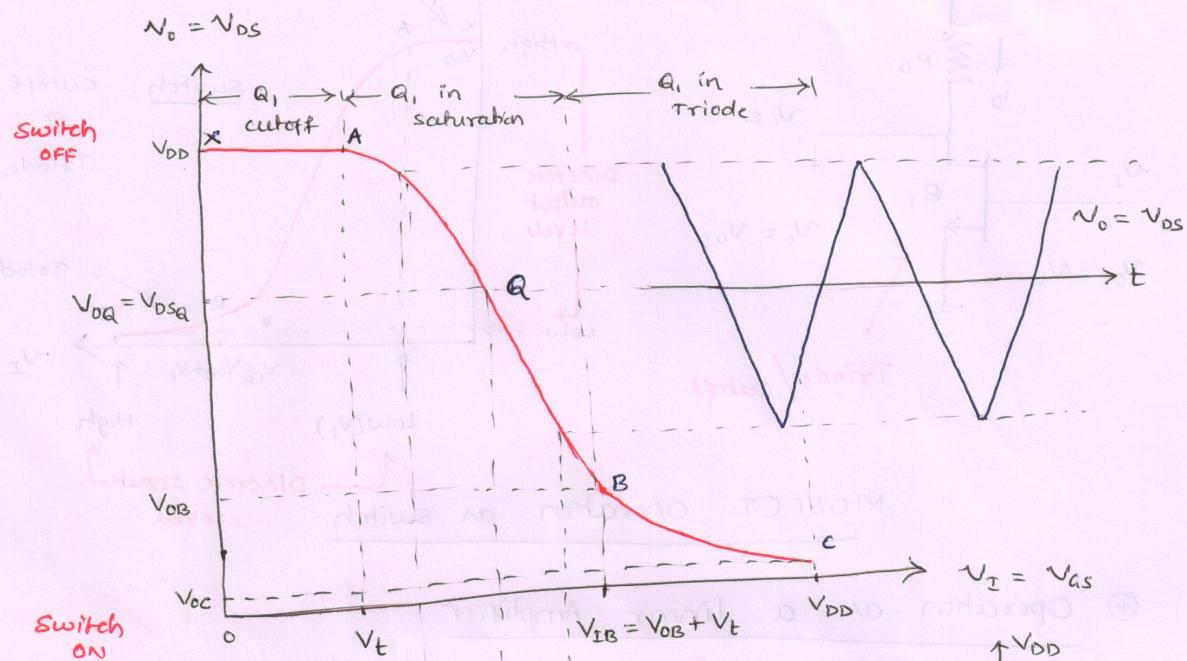
⇒ $V_I > V_{IB}$, MOSFET is Deep Triode Region

$V_o = V_{DS} \downarrow$ due to this \downarrow

⇒ $V_I = V_{DD}$, point C

④ Operation as a Linear Amplifier

(16)



Transfer characteristics:

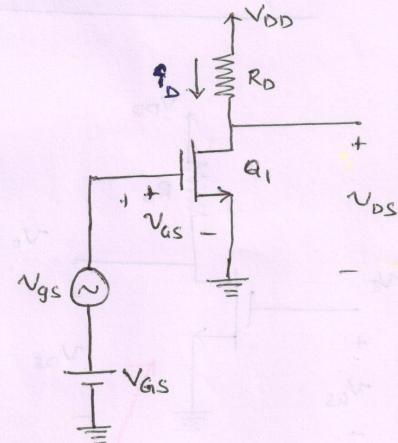
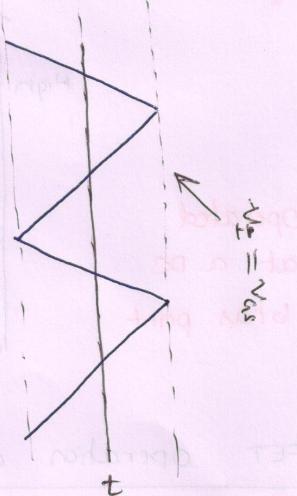
operation as an amplifier

$$V_{GS} = V_{GS} + V_{GS}$$

$$V_{DS} = V_{DS} + V_{DS}$$

$$i_D = i_D + i_d$$

constant bias
Signal &
Response



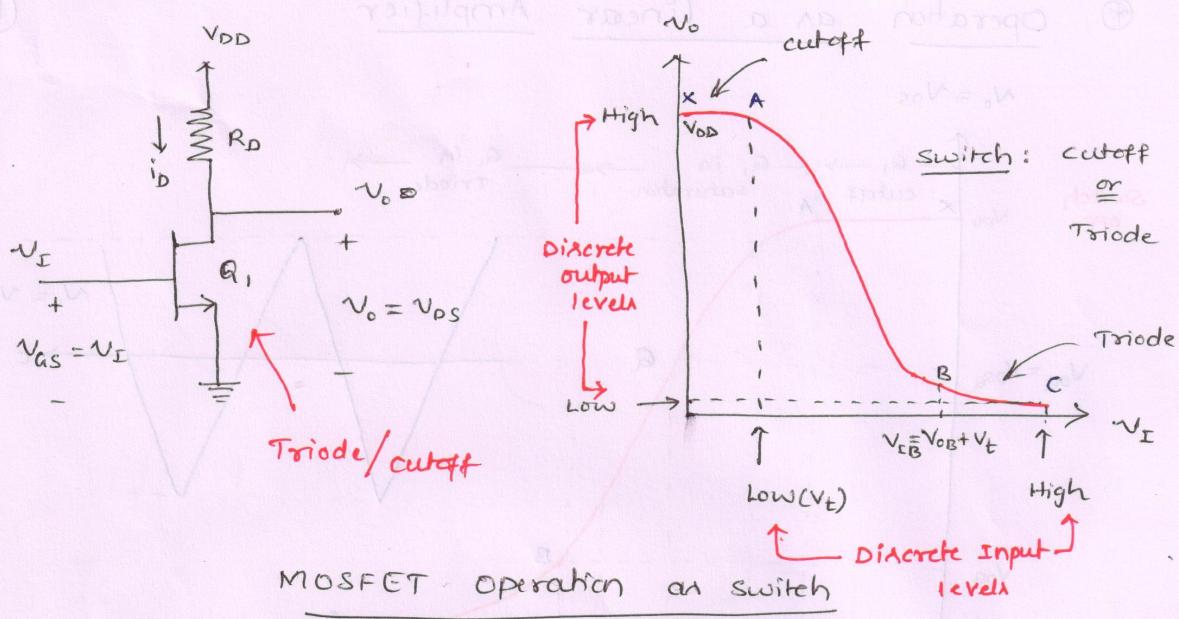
conceptual circuit of MOSFET amplifier

⑤ Operation as a Switch

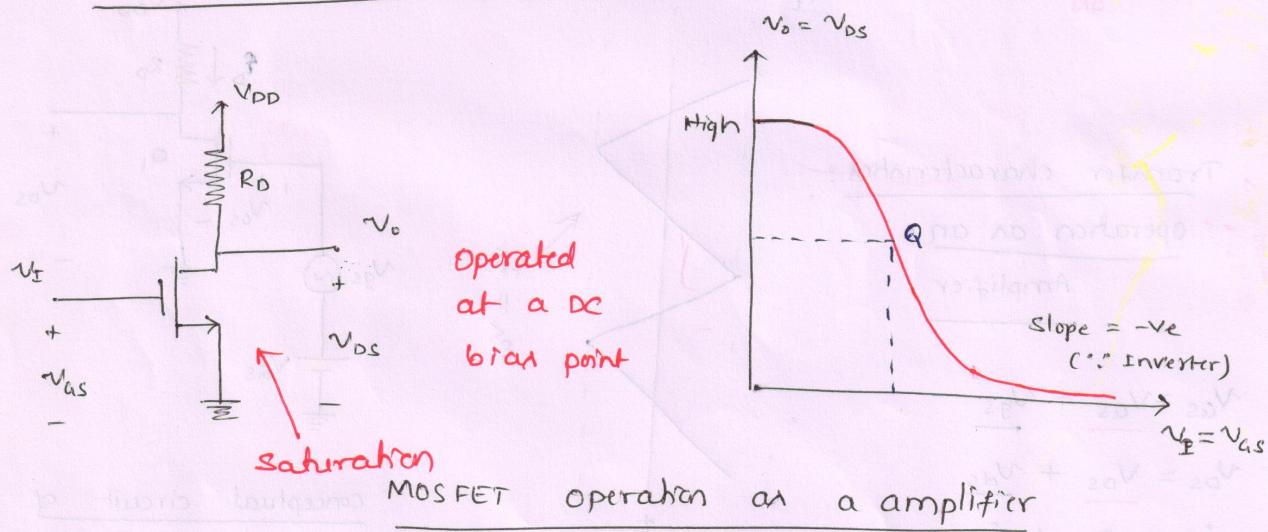
→ operated at extreme points of transfer curve

$$V_D = V_{DS} = V_{DD}, \text{ OFF}$$

$$V_D = V_{OC}, \text{ ON}$$

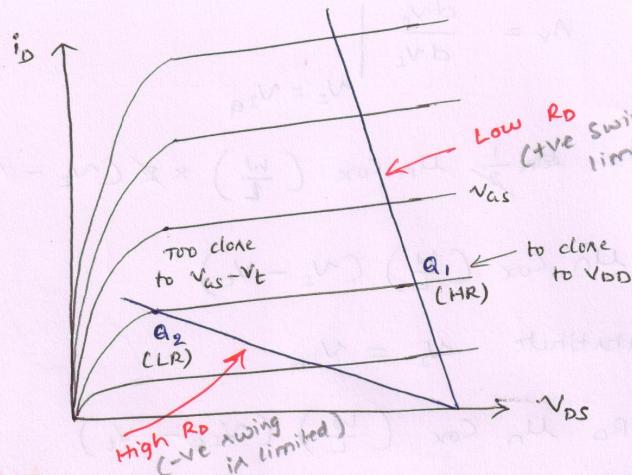


② Operation as a linear Amplifier



$$\text{Voltage gain} = A_v = \frac{dV_o}{dV_i} \left|_{V_i = V_{IQ}} \right. = \begin{cases} \text{slope of } x^{\text{for curve}} \\ @ \text{bias point Q} \end{cases}$$

Slope = -ve, \Rightarrow CS amplifier is Inverting



Head room : referred to VOD
Leg room : " " AND

Locating the bias point

Two load lines &
Corresponding bias points

Q₁ : - NO sufficient room for tve signal
- Swing at the drain (too close to V_{DD})

Φ_2 : - close to boundary of triode region
- do not allow for sufficient negative voltage swing

 Analytical Expression for the transfer characteristics

MOSFET operates in three regions, namely

- ① cutoff region ② saturation region ③ triode Region } From VTC

① cutoff region : Segment $\times A$

$$V_S \leq V_T \quad \text{and} \quad V_o = V_{DD}, \quad i_D = 0$$

cond'n

② The saturation region : Segment AGB

$$\frac{v_i \geq v_t}{\text{condn}} \quad \text{and} \quad \frac{v_o \geq v_i - v_t}{\text{condn}}$$

Neglecting channel length modulation

$$i_D = \frac{1}{2} M_n \cos(\frac{\omega}{L}) (v_e - v_t)^2 \quad \dots \quad (1)$$

$$V_o = V_{DD} - i_D \cdot R_D \quad \leftarrow (2)$$

substituting ① in ②

$$V_o = V_{DD} - R_D \cdot \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right) (V_i - V_t)^2 \quad \dots (3)$$

$$W \cdot K \cdot T \quad A_V = \left. \frac{dV_o}{dV_i} \right|_{V_i = V_{IQ}}$$

$$A_V = 0 - R_D \cdot \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right) \times (V_i - V_t)$$

$$A_V = -R_D \mu_n C_{ox} \left(\frac{W}{L} \right) (V_i - V_t)$$

Substitute $V_i = V_{IQ}$

$$A_V = -R_D \mu_n C_{ox} \left(\frac{W}{L} \right) (V_{IQ} - V_t)$$

using equation (3)

$$\left\{ \begin{array}{l} A_V \propto R_D \\ A_V \propto \mu_n C_{ox} \\ A_V \propto \frac{W}{L} \\ A_V \propto V_{ov} \end{array} \right.$$

$$V_o = V_{OA} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right) (V_{IQ} - V_t) (V_{IQ} - V_t)$$

$$V_{OA} = V_{DD} + \frac{A_V}{2} (V_{IQ} - V_t)$$

$$\text{but } V_{IQ} - V_t = V_{as} - V_t = V_{ov}$$

$$V_{OA} = V_{DD} + \frac{A_V}{2} V_{ov}$$

$$A_V = \frac{2(V_{OA} - V_{DD})}{V_{ov}} = -\frac{2(V_{DD} - V_{OA})}{V_{ov}}$$

$$A_V = \frac{-2V_{RD}}{V_{ov}} \quad \begin{matrix} \leftarrow \text{DC voltage across} \\ \text{drain resistance} \end{matrix}$$

$$V_{OB} = V_{IB} - V_t = V_{as} - V_t \Rightarrow \text{End point of saturation}$$

(3) The Triode Region : Segment BC

$V_i \geq V_t$ and $V_o \leq V_i - V_t$
condn condn

W.K.T $V_o = V_{DD} - R_D \cdot i_D \quad \text{--- (1)}$ $\quad \quad \quad \text{Equation for } i_D \text{ in Triode}$

$$i_D = \mu_n C_{ox} \left(\frac{W}{L} \right) \left[(V_i - V_t) V_o - \frac{1}{2} V_o^2 \right] \quad \text{--- (2)}$$

Substitute (2) in (1)

$$(V_i - V_o) \left(\frac{W}{L} \right) V_o - \frac{1}{2} V_o^2 - V_o V_t = i_D V_o$$

$$V_o = V_{DD} - \mu_n C_{ox} \left(\frac{W}{L} \right) \left[(V_i - V_t) V_o - \frac{1}{2} V_o^2 \right] R_D \quad (18)$$

Since V_o is small, V_o^2 becomes negligible

$$V_o = V_{DD} - \mu_n C_{ox} \left(\frac{W}{L} \right) [(V_i - V_t) V_o] R_D$$

$$V_o + \mu_n C_{ox} \left(\frac{W}{L} \right) [(V_i - V_t) V_o] R_D = V_{DD}$$

$$V_o = \frac{V_{DD}}{1 + \mu_n C_{ox} \left(\frac{W}{L} \right) (V_i - V_t) R_D} \quad (3)$$

W.K.T

Triode Region

$$\left\{ \begin{array}{l} r_{DS} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L} \right) (V_i - V_t)} \\ \text{negligible} \end{array} \right. \quad (4)$$

Substitute (4) in (3)

$$V_o = \frac{V_{DD}}{1 + \frac{R_D}{r_{DS}}} = \frac{V_{DD} \cdot r_{DS}}{R_D + r_{DS}}$$

It is possible to get
the appropriate T.F

both graphically &
Analytically

usually $r_{DS} \ll R_D$, r_{DS} is negligible

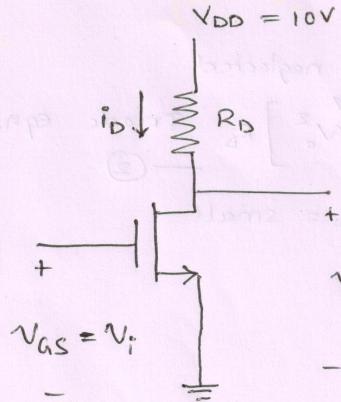
$$V_o = \frac{V_{DD} \cdot r_{DS}}{R_D}$$

MOSFET acts as a
Voltage controlled resistance

(P) (4.8) Consider a CS circuit

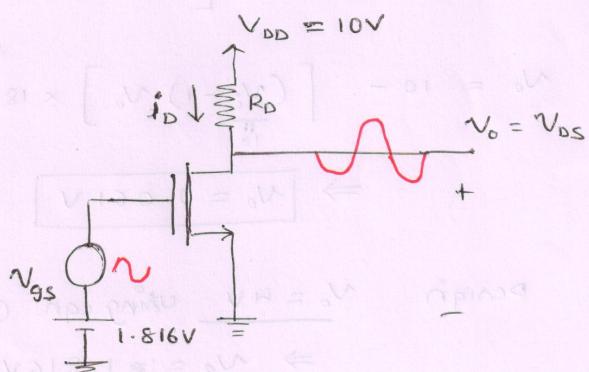
$$V_t = 1V, \mu C_{ox} \left(\frac{W}{L} \right) = 1mA/V^2, R_D = 18k\Omega \text{ and } V_{DD} = 10V$$

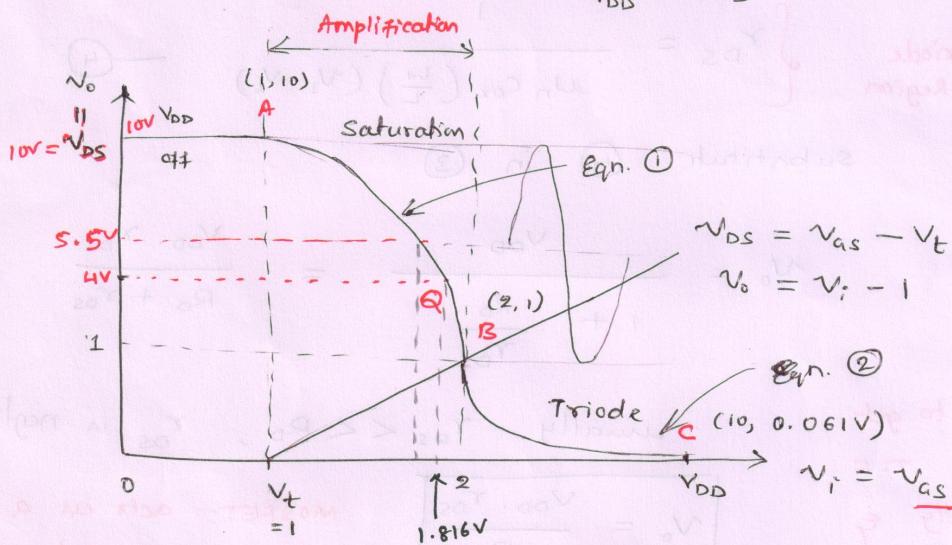
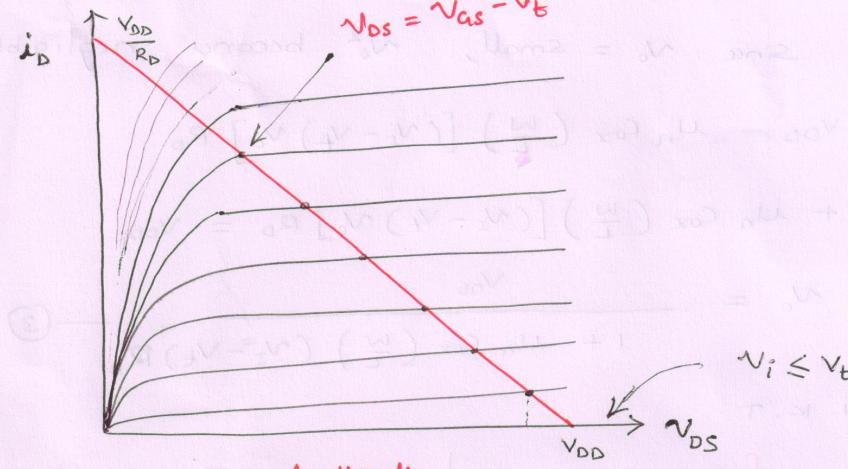
Analyze the circuit



$$V_{DS} = V_{DD} - i_D R_D$$

$$V_{DS} = V_o$$





$$V_o = V_{DD} - \frac{1}{2} \mu C_{ox} \left(\frac{W}{L} \right) (V_i - V_t)^2 R_D \quad \text{--- (1)}$$

$$\begin{cases} V_o = 10 - \frac{1}{2} (V_i - 1)^2 \times 18 \\ V_o = V_i - 1 \end{cases} \quad \xrightarrow{\text{neglected}} \text{Saturation equation}$$

$$V_o = 1, \quad V_i = 2 \Rightarrow \text{point B}$$

neglected

$$V_o = V_{DD} - \mu C_{ox} \left[(V_i - V_t) V_o - \frac{1}{2} \frac{V_o^2}{R_D} \right] \quad \text{Triode eqn. (2)}$$

$$V_o = 10 - \left[(V_i - 1) V_o \right] \times 18 \quad V_o = \text{small}$$

$$\Rightarrow V_o = 0.061 \text{ V}$$

$$\text{Design } V_o = 4 \text{ V using eqn. (1)}$$

$$\Rightarrow V_i = 1.816 \text{ V}$$

$$A_v = \frac{\partial V_o}{\partial V_i} = -\mu C_{ox} \left(\frac{w}{L} \right) (1.816 - 1) \frac{R_D}{18}$$

||
|

$$A_v = -14.7$$

Apply input signal = 150 mV (peak-to-peak amplitude)

Say triangular waveform

$$V_{asq} = 1.816 \text{ V}$$

V_{as} varies linearly between 1.741V and 1.891V around the bias value of 1.816V

$$\text{At } V_{as} = 1.741 \text{ V}, i_D = \frac{1}{2} \times 1 \times (1.741 - 1)^2 = 0.275 \text{ mA}$$

$$\text{At } V_{as} = 1.816 \text{ V}, i_D = \frac{1}{2} \times 1 \times (1.816 - 1)^2 = 0.333 \text{ mA}$$

$$\text{At } V_{as} = 1.891 \text{ V}, i_D = \frac{1}{2} \times 1 \times (1.891 - 1)^2 = 0.397 \text{ mA}$$

Negative increment in i_D is : $(0.333 - 0.275) = 0.058 \text{ mA}$
 positive increment in i_D is : $(0.397 - 0.333) = 0.064 \text{ mA}$

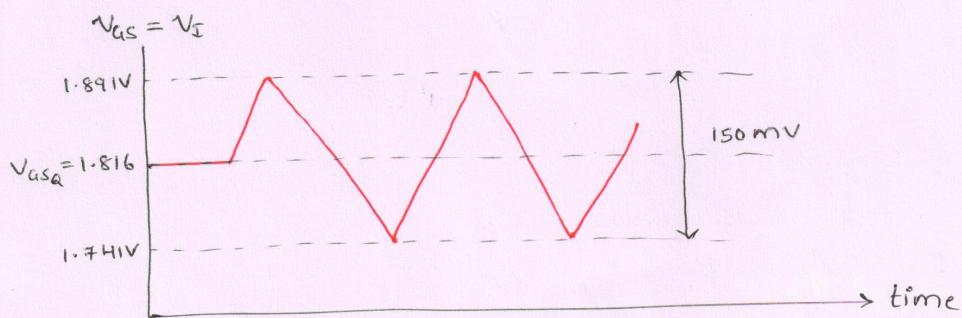
$\Rightarrow i_D - V_{DS}$ curve are not perfectly linear

$$\text{At } V_{as} = 1.741 \text{ V}, i_D = 0.275 \text{ mA, and } V_o = 10 - 0.275 \times 18 = 5.05 \text{ V}$$

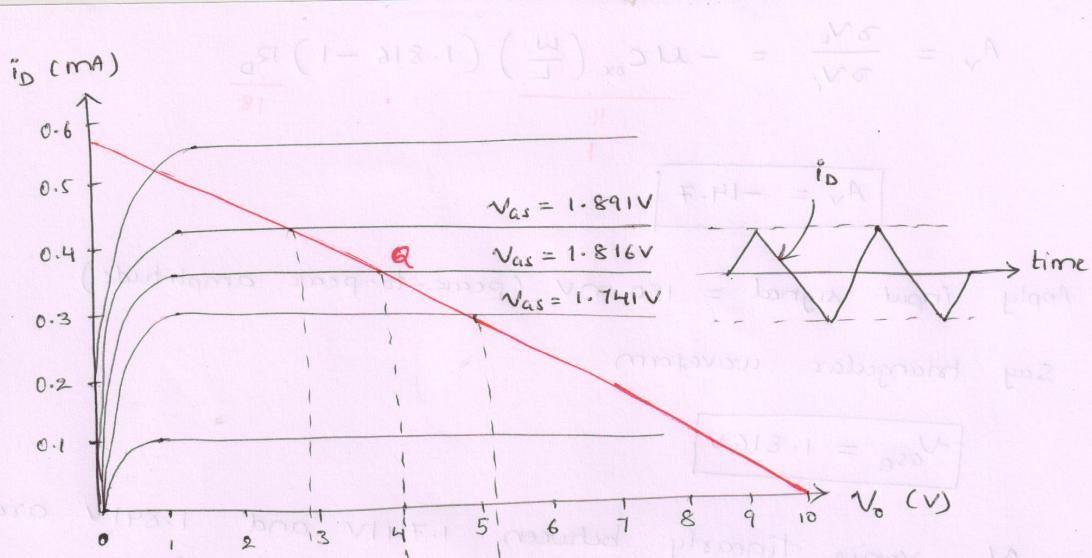
$$\text{At } V_{as} = 1.891 \text{ V}, i_D = 0.397 \text{ mA, and } V_o = 10 - 0.397 \times 18 = 2.85 \text{ V}$$

+ve excursion = 1.05V

-ve excursion = 1.15V



P1



$$Am_{2T8.0} = \frac{d}{dt} (1 - (M_{2T8.1}) \times \frac{V_D}{2}) = dI \quad V_{THF.1} = 20V - 4A$$

$$Am_{2S8.0} = \frac{d}{dt} (1 - (M_{2S8.1}) \times \frac{V_D}{2}) = dI \quad V_{2T8.1} = 20V - 4A$$

$$Am_{TP8.0} = \frac{d}{dt} (1 - (M_{TP8.1}) \times \frac{V_D}{2}) = dI \quad V_{TP8.1} = 20V - 4A$$

$$Am_{2S0.0} = (2T8.0 - 1.15V) - 1.05V \quad Am_{2S0.0} = 2T8.0 - 2.2V$$

$$Am_{H20.0} = (2S8.0 - TP8.0) : 2 \quad Am_{H20.0} = 2S8.0 - TP8.0$$

$$V20.2 = 21 \times 2T8.0 - 4I = 2V - b20 \quad Am_{2T8.0} = dI \quad V_{THF.1} = 20V - 4A$$

$$V20.3 = 21 \times 2S8.0 - 4I = 2V - b20 \quad Am_{2S8.0} = dI \quad V_{2T8.1} = 20V - 4A$$

$$V20.1 = \text{Invertor output} = 2V +$$

$$V20.0 = \text{Invertor output} = 2V -$$

