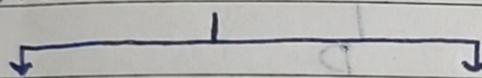


MOSFETS (Unit 2)

A transistor is called as transferred resistance because in a transistor there are three terminal that is emitter, base, ^{collector} conductor. The transistor to behave as an amplifier, EB must be forward biased and CB must be negative/reverse biased. As a result, when we move from input to output side, the resistance increases, i.e. there is a change in resistance, we call it as Transferred resistance / Transistor.

Transistors

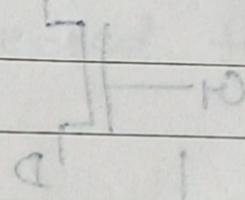


BJT (Bi-polar)

(Holes and e⁻ contribute to current)

FET (Uni-polar)

(Only one contributes to current)



* FET has 4 terminals: Source, gate, Drain, Body (or substrate or second gate or back gate). BJT has only 3 terminals: Emitter, Base, collector.

* BJT: Occupies more space on the circuit
MOSFET: Occupies less space.

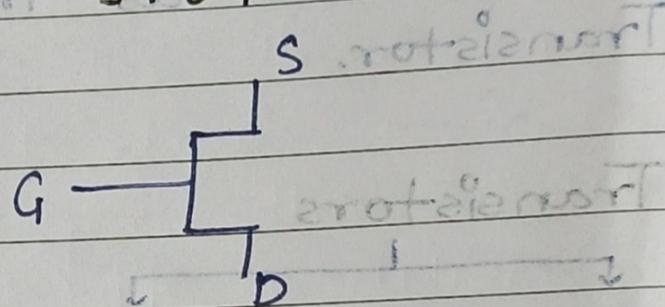
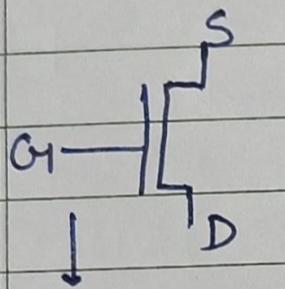
* BJT: Higher gain, lower input impedance
FET: Lesser gain, higher input impedance

MOSFET

Enhancement type n-channel / NMOS,
depletion type p-channel / PMOS,
CMOS.

Firstly FET is classified as JFET and mosfet (Junction)

In MOSFET



Here gate is isolated from the junction of source and drain.

In JFET, the gate is not isolated from source and drain.

MOSFET are preferred because, the isolation of gate from the region between source and drain act as a barrier allowing only necessary charge to travel.

Difference between Depletion and Enhancement type:

The channel in MosFET is always present in depletion type but in enhancement type, it is (channel)

n^+ → indicates highly doped n-type

p^+ → indicates highly doped p-type (highly/heavily)

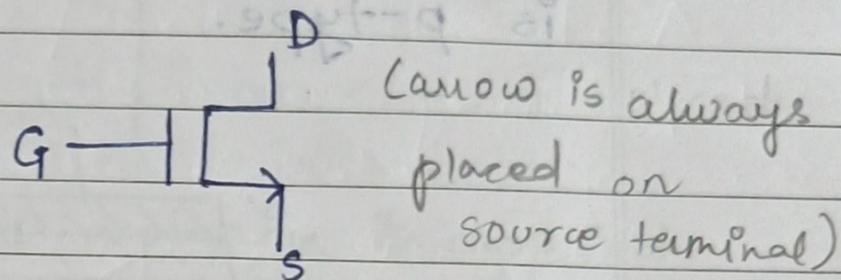
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is created only when there is a necessity, that is why enhancement type is preferred.

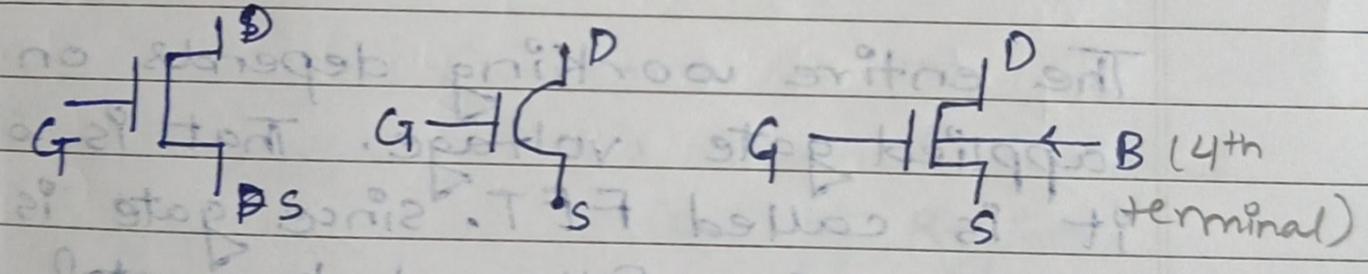
SYMBOL:

n-channel / NMOS:

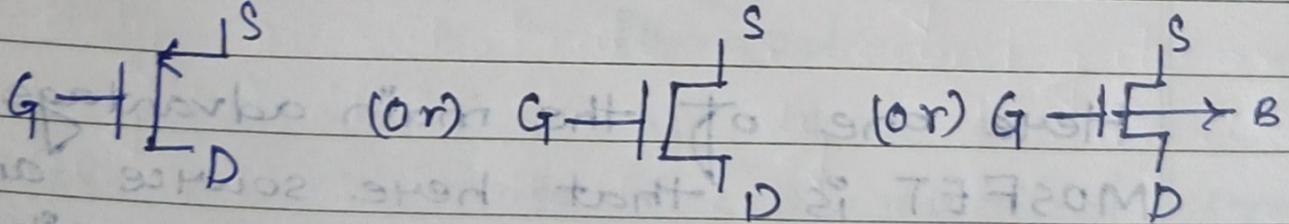


We have connected source below because n-channel is always connected to ground.

: n-channel



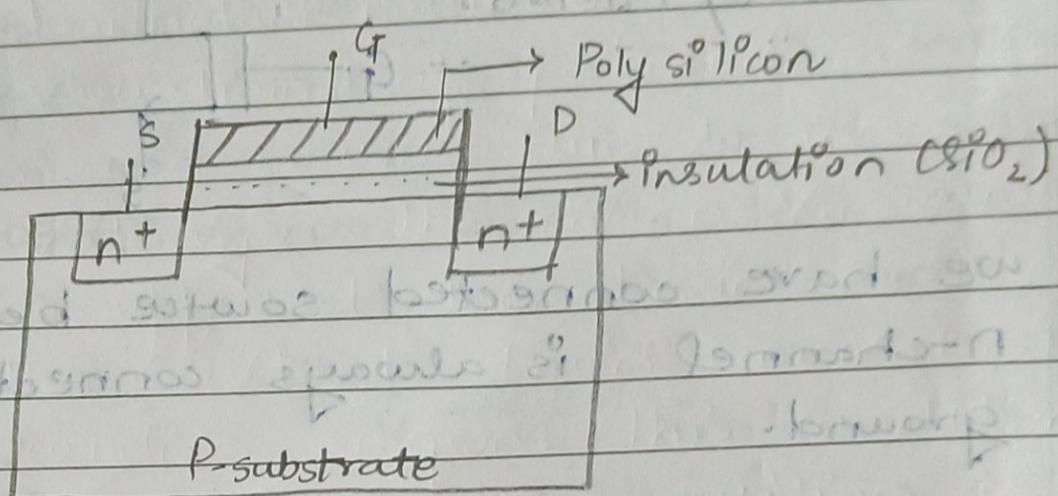
: p-channel



Construction of MOSFET:

n-channel (Enhancement type)

Since channel is n-type, source and drain must also be n-type. If they are p-type, then n and p type (i.e. e⁻ and holes) recombine and output is zero. Only substrate is p-type.

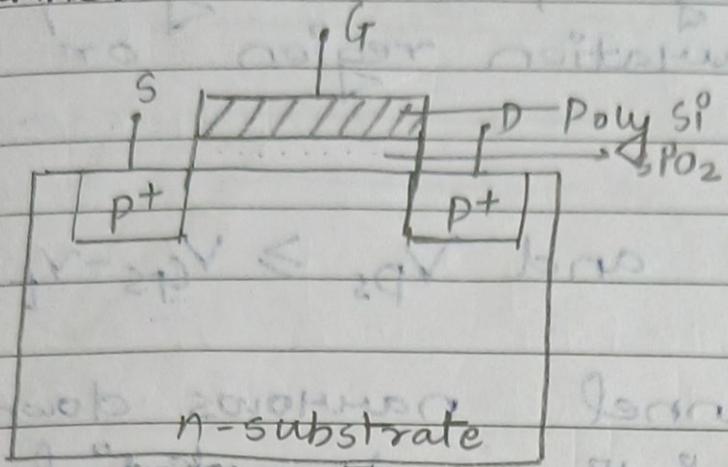


- * Here positive gate voltage is applied

The entire working depends on the applied gate voltage. That is why it is called FET. Since gate is placed on an oxide followed by metal, it is called metal oxide semiconductor FET.

Here one of the main advantages of MOSFET is that here source and drain are equally doped (unlike BJT where Emitter is heavily doped, Base is lightly doped and collector is moderately doped). Source and drain can be interchanged making it easy and flexible to use.

p-channel:



* Here negative gate voltage is applied.

: Working of N-chn1 and p-chn1 mosfets:

$$V_{GS} = V_G - V_S$$

$$V_{DS} = V_D - V_S$$

• n-chn1:

(i) When $V_{GS} < V_t$: No channel formed
(cutoff Region)

(ii) When $V_{GS} > V_t$: n-type channel is formed

(iii) When $V_{GS} > V_t$ and V_{DS} is applied, drain current starts flowing from drain to source (e⁻ from S to D)

a) $V_{GS} > V_t$ and $V_{DS} < V_{GS} - V_t$

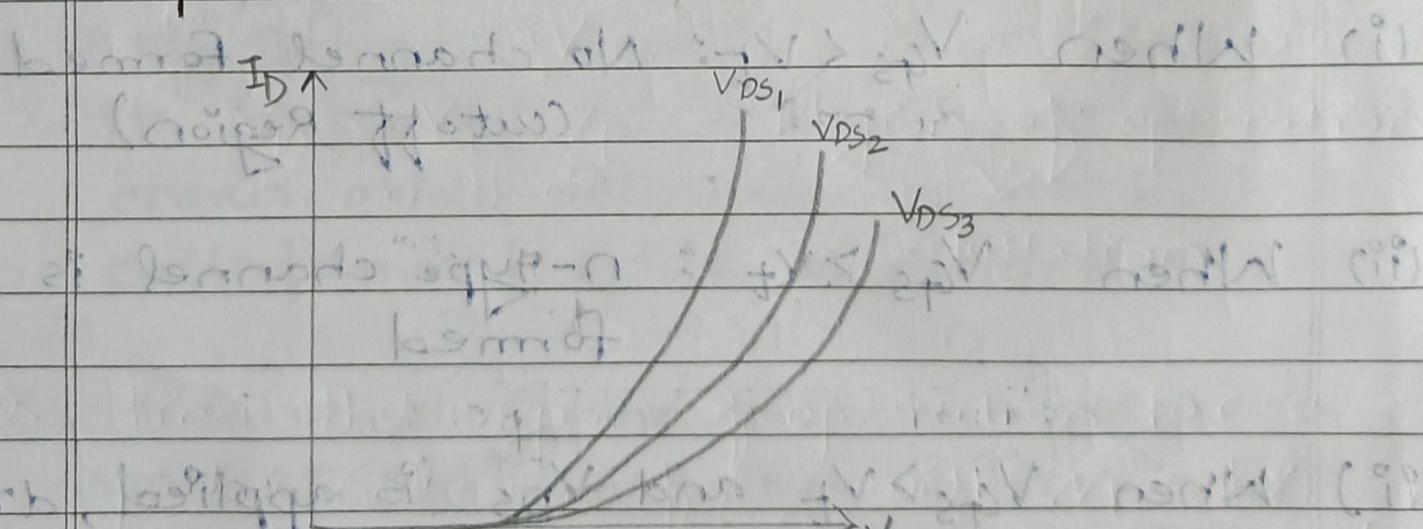
Here there is uniform formation of channel.
The region of operation is known to be

Ohmic region / Linear region / Triode region
 Non-saturation region or resistive region.

b) $V_{GS} - V_T$ and $V_{DS} \geq V_{GS} - V_T$

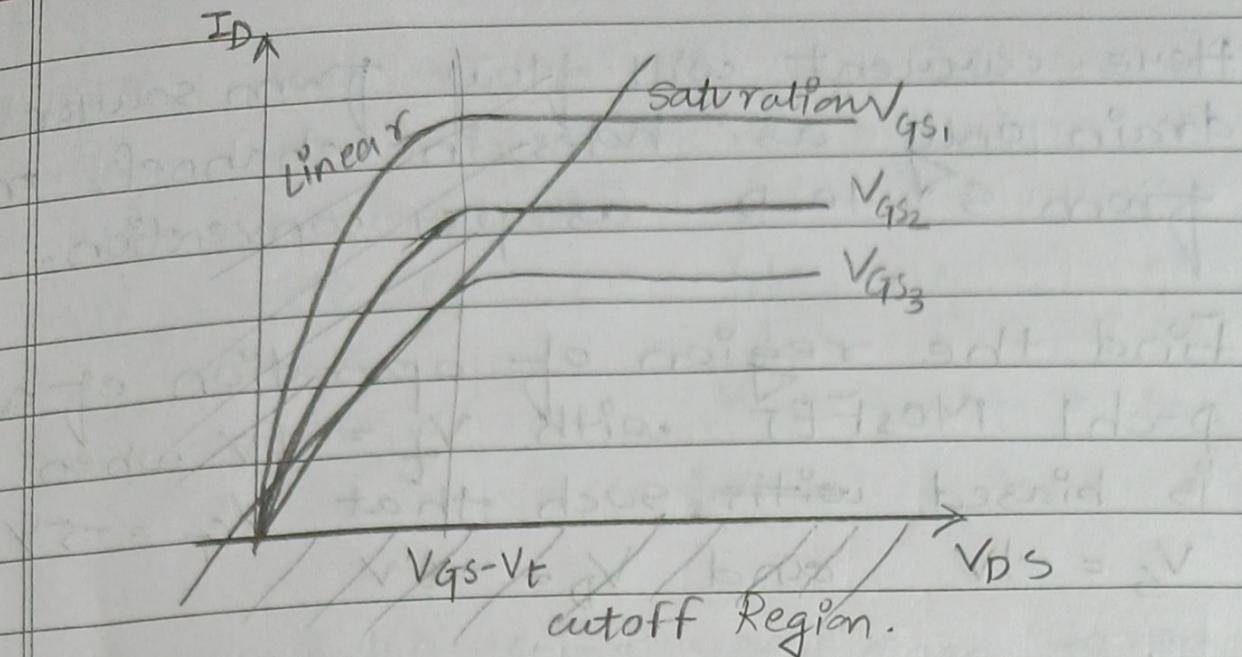
The channel narrows down due to the variation of potential at the drain and source due to increased V_{DS} voltage. The channel narrows/pinches off at the drain and results in the constant drain current. This is saturation region. This condition is called as Pinch off condition as the channel pinches off at the drain.

Input characteristics:

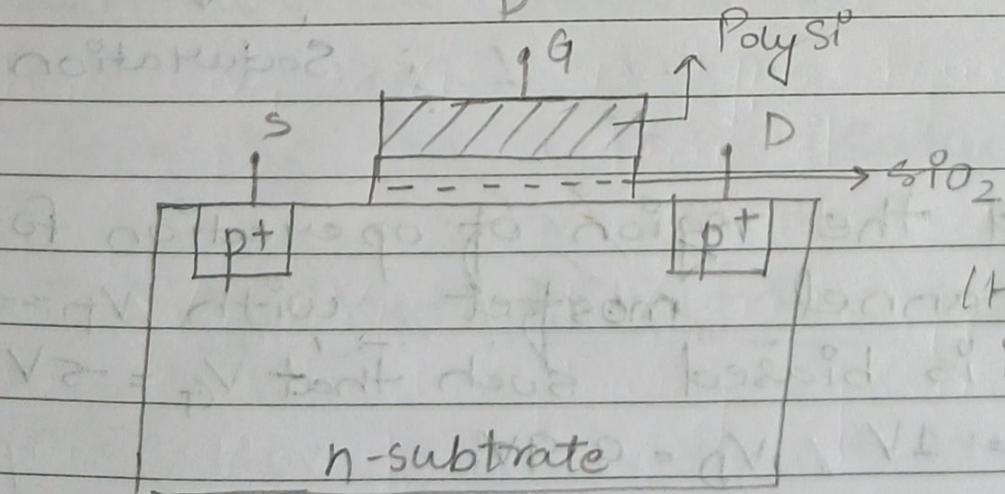
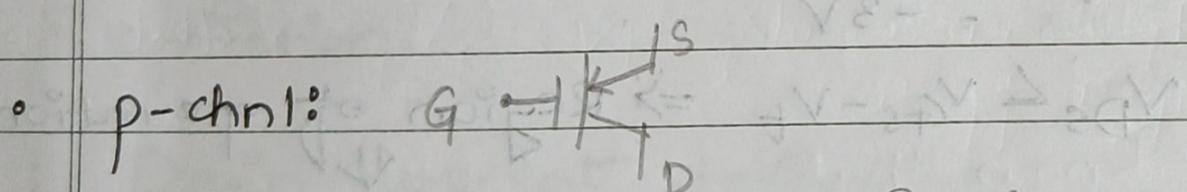
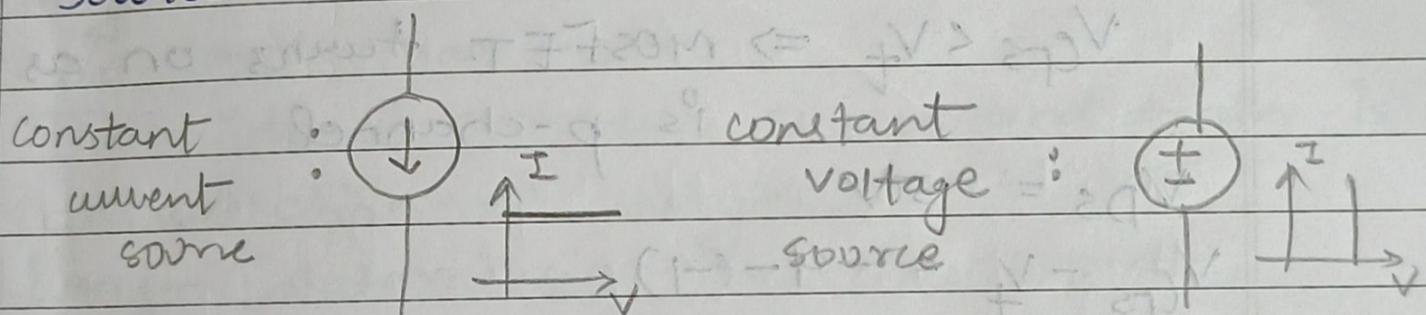


Output characteristics:

As long as V_{DS} is less than $V_{GS} - V_T$, I_D increases but as soon as $V_{DS} \geq V_{GS} - V_T$, I_D becomes constant.



MOSFET behaves as a resistor in linear region and in saturation region, MOSFET behaves as a constant current source.



- (i) $V_{GS} \geq V_t \rightarrow$ No channel formed
- (ii) $V_{GS} < V_t \rightarrow$ channel will be formed
 - a) $V_{DS} > V_{GS} - V_t \rightarrow$ Linear/Ohmic Region
 - b) $V_{DS} < V_{GS} - V_t \rightarrow$ Saturation Region

Here current will flow from source to drain only as holes in channel move from S \nwarrow to D as per convention.

- Q. Find the region of operation of a p-chl MosFET with $V_t = -1V$ when it is biased such that $V_G = -5V$, $V_S = -1V$ and $V_D = -6V$

$$V_{GS} = V_G - V_S = -5 - (-1) = -4V$$

$$V_{DS} = V_D - V_S = -6 - (-1) = -5V$$

$V_{GS} < V_t \Rightarrow$ MOSFET turns on as this is p-channel

$$V_{PS} = -5V$$

$$V_{GS} - V_t = -4 - (-1) = -3V$$

$V_{DS} < V_{GS} - V_t \Rightarrow$ Region of operation

Saturation

- Q. Find the region of operation for a p-channel mosfet with $V_t = -1V$ when it is biased such that $V_G = -5V$ and $V_S = 1V$, $V_D = 0.9V$

$$V_{GS} = -5V - 1V = -6V$$

$$V_{PS} = -0.1V$$

$$V_t = 0.4V$$

$V_{GS} < V_t$
(cutoff region)

V_t is +ve for NMOS.
 V_t is -ve for PMOS.

a. find the region of operation $\rightarrow V_t = 0.4V$

$$V_G = 1.5V \quad V_S = 0 \quad V_D = 0.5V$$

(n-channel)

$$V_{GS} = 1.5V$$

$$V_{DS} = 0.5V$$

$$V_t = 0.4V$$

$$V_{GS} > V_t$$

$$V_{GS} - V_t > V_{DS}$$

(Ohmic / Linear Region)

NOTE: • When S & D come very close to each other there are several second order effects.

• If given that transistors of 180 nm technology means that minimum channel length should be 180 nm and must not be less than that.

• The distance between source and drain is called channel length.

• Length determines the size of the operation.

: Drain current derivation:

$$I_D = K/2 (V_{GS} - V_t)^2 \quad (\text{Saturation Region})$$

$$I_D = \frac{K}{2} \left((V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right) \quad (\text{Linear Region})$$

$$\text{unit} = \mu\text{A}/\text{V}^2$$

$K = \mu_n C_{ox} \frac{(W)}{L} \rightarrow$ width of channel
 \downarrow \rightarrow Length of channel

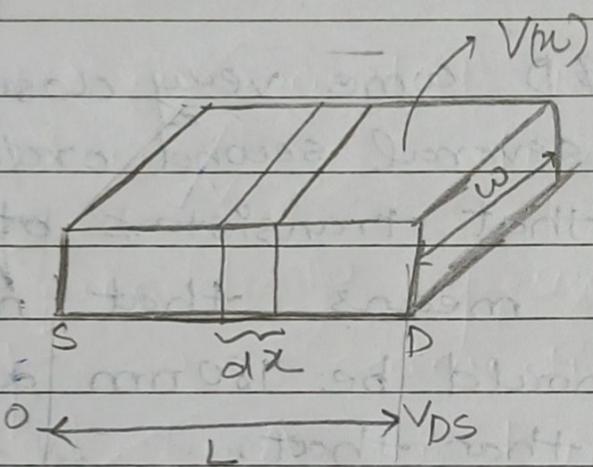
Mobility \downarrow aspect Ratio

oxide

capacitance

A mosfet in its construction looks like a capacitor as Poly Si and metal is separated by a dielectric SiO_2 . The capacitance offered by the entire MOSFET is C_{ox} .

$$C_{ox} = \frac{C_A}{\text{Area}} \quad (\text{Capacitance offered by gate})$$



Consider a small strip of length dx in the channel. Capacitance offered by the strip is equal to $C_{ox} \cdot w \cdot dx$

We know that

$$I = \frac{dQ}{dt} \quad \textcircled{A}$$

$$\text{but } Q = CV$$

$$dQ = C_{ox} \cdot w \cdot dx \cdot (V_{GS} - V_t - V(x)) \quad \textcircled{D}$$

where $V(x)$ is the voltage applied at the strip.

$$\frac{dQ}{dt} = \frac{dQ}{dx} \cdot \frac{dx}{dt}$$

$$= C_{ox} w (V_{GS} - V_t - V(x)) \cdot \left(\frac{dx}{dt} \right) \rightarrow \text{velocity}$$

$$C_{ox} = \frac{E_{ox}}{t_{ox}} = \frac{3 \cdot 9 E_0}{t_{ox}}$$

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oxide thickness

$$\frac{dx}{dt} = \mu_n \frac{dV(x)}{dx}$$

↳ mobility of e⁻

$$\frac{dQ}{dt} = C_{ox} \cdot w (V_{GS} - V_T - V_x) \mu_n \frac{dV(x)}{dx}$$

$$I = \mu_n C_{ox} w (V_{GS} - V_T - V_x) \frac{dV(x)}{dx}$$

$$\int_0^L I dx = \int_0^{V_{DS}} \mu_n C_{ox} w (V_{GS} - V_T - V_x) dV(x)$$

$$\int_0^L I dx = \mu_n C_{ox} w \int_0^{V_{DS}} (V_{GS} - V_T - V_x) dV(x)$$

$$I_L = \mu_n C_{ox} w \left((V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

~~for linear~~

$$I = \mu_n C_{ox} \left(\frac{w}{L} \right) \left((V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

(In Linear Region)

$$V_{DS} = V_{GS} - V_T$$

$$I = \mu_n C_{ox} \left(\frac{w}{L} \right) \left((V_{GS} - V_T)^2 - \frac{(V_{GS} - V_T)^2}{2} \right)$$

$$I = \frac{\mu_n C_{ox} (w/L)}{2} (V_{GS} - V_T)^2$$

(In saturation Region)

NOTE: • w/L = Aspect Ratio

• $\mu_n > \mu_p$ (mobility: NMOS > PMOS)

• $K_n' = \mu_n C_{ox}$ (K_p' for PMOS)

$$C_{ox} = \epsilon F / \mu m^2$$

$$K_n' = \mu n C_{ox} \left(\frac{W}{L} \right)$$

- $K_n = \mu_n C_{ox} \left(\frac{W}{L} \right)$
- $V_{ov} = V_{GS} - V_T \Rightarrow$ overdrive voltage
→ minimum voltages for drain current to flow
- Decides transistor is in linear / saturation Region

Q. For a 0.8 micrometer process $t_{ox} = 20 \text{ nm}$
 $\mu_n = 100 \text{ cm}^2/\text{V}\cdot\text{sec}$ find C_{ox} , K_n' ,

V_{ov} required to operate with aspect ratio of 20 in saturation region with a I_D of 1mA. Find minimum value of V_{DS} .

$$C_{ox} = \frac{3.9 \epsilon_0}{t_{ox}} = \frac{3.9 \times 8.85 \times 10^{-12}}{20 \times 10^{-9}}$$

$$= 1.753 \text{ fF}/\mu\text{m}^2$$

$$K_n' = \mu_n C_{ox}$$

$$= 100 \times 10^{-4} \times 1.753 \times 10^{-3}$$

$$= 17.53 \text{ } \mu\text{A}/\sqrt{\text{V}}$$

$$I_D = \frac{\mu_n C_{ox} \left(\frac{W}{L} \right)}{2} (V_{GS} - V_T)^2$$

$$10^{-3} = \frac{10^{-4} \times 100 \times 1.753 \times 10^{-3} \times 20}{2} (V_{ov})^2$$

$$V_{ov} = 2.3884 \text{ V}$$

conduct

Type 1

Type 2

$$V_{DS} = V_{GS} - V_T$$

$$V_{DS} = 2.3884 \text{ V}$$

↳ Minimum value

: Transconductance of an Amplifier (g_m)
 ↳ defined at saturation Region

$$V = IR$$

$$R = V/I$$

$$\text{conductance} \leftarrow G = I/V$$

$$g_m = \frac{I_D}{V_{GS}} \rightarrow \begin{array}{l} \text{output current} \\ \text{input voltage} \end{array}$$

Ratio of output current (I_D) to input voltage (V_{GS})

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

$$I_D = \frac{k_n' (w/L)}{2} (V_{GS} - V_T)^2$$

$$\frac{\partial I_D}{\partial V_{GS}} = \frac{k_n' (w/L)}{2} 2(V_{GS} - V_T)$$

Type 1:

$$g_m = k_n' (w/L) (V_{GS} - V_T)$$

Type 2: We have, $I_D = \frac{k_n' (w/L)}{2} (V_{GS} - V_T)^2$

$$k_n' (w/L) = \frac{2 I_D}{(V_{GS} - V_T)^2}$$

$$g_m = \frac{2 I_D}{V_{GS} - V_T}$$

k_n^l = process parameter constant

Type 3: $I_D = \frac{k_n^l}{2} \left(\frac{\omega}{L}\right) (V_{GS} - V_T)^2$

$$(V_{GS} - V_T)^2 = \frac{2 I_D}{k_n^l (\omega/L)}$$

$$V_{GS} - V_T = \sqrt{\frac{2 I_D}{k_n^l (\omega/L)}}$$

$$g_m = \sqrt{2 I_D k_n^l (\omega/L)}$$

Summary,

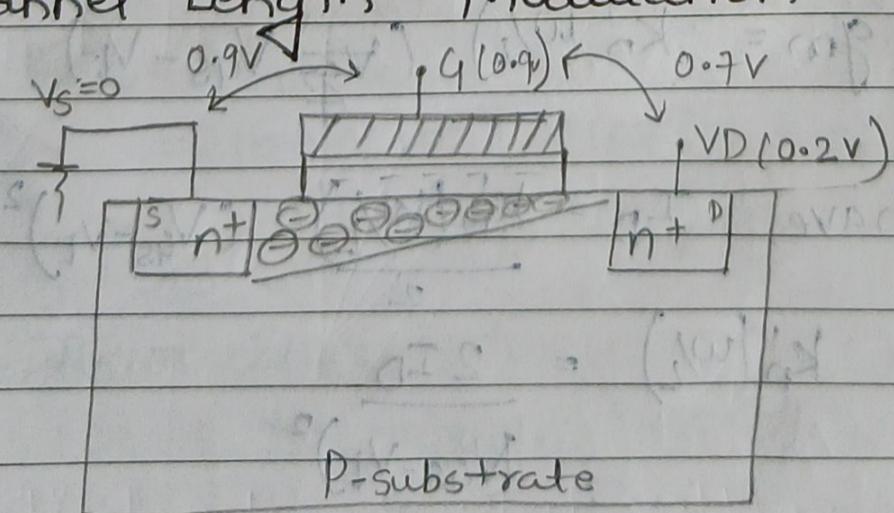
$$g_m = k_n^l (\omega/L) (V_{GS} - V_T)$$

$$g_m = \frac{2 I_D}{V_{GS} - V_T}$$

$$g_m = \sqrt{2 I_D k_n^l (\omega/L)}$$

: Second Order Effect

@ channel Length Modulation

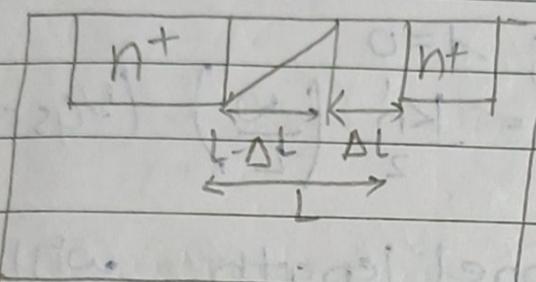


(Result in pinch off)

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Here because of high voltage of V_{GS} compared to V_{GD} the channel length increases near source and decreases towards drain. But when drain voltage is arbitrary increases, the channel length decreases to a certain length extent such that the channel pinches off completely.



In pinch off conductivity decreases and further increase will result in breaking of transistor.

$$I_D = \frac{K_n' (w/L)}{2} (V_{GS} - V_T)^2$$

$$= \frac{K_n'}{2} \left(\frac{w}{L - \Delta L} \right) (V_{GS} - V_T)^2$$

$$= \frac{K_n'}{2} \frac{w}{L} \frac{1}{\left(1 - \frac{\Delta L}{L} \right)} (V_{GS} - V_T)^2$$

$\frac{\Delta L}{L}$ = very small

$$\frac{1}{\left(1 - \frac{\Delta L}{L} \right)} = 1 + \frac{\Delta L}{L}$$

$$I_D = \frac{K_n'}{2} \left(\frac{w}{L} \right) \left(1 + \frac{\Delta L}{L} \right) (V_{GS} - V_T)^2$$

$$\Delta L \propto V_{DS}$$

$$\Delta L = k' V_{DS}$$

$$I_D = \frac{K_n}{2} \left(\frac{w}{L} \right) \left(1 + \frac{1'}{L} V_{DS} \right) (V_{GS} - V_T)^2$$

$$\frac{1'}{L} = 1$$

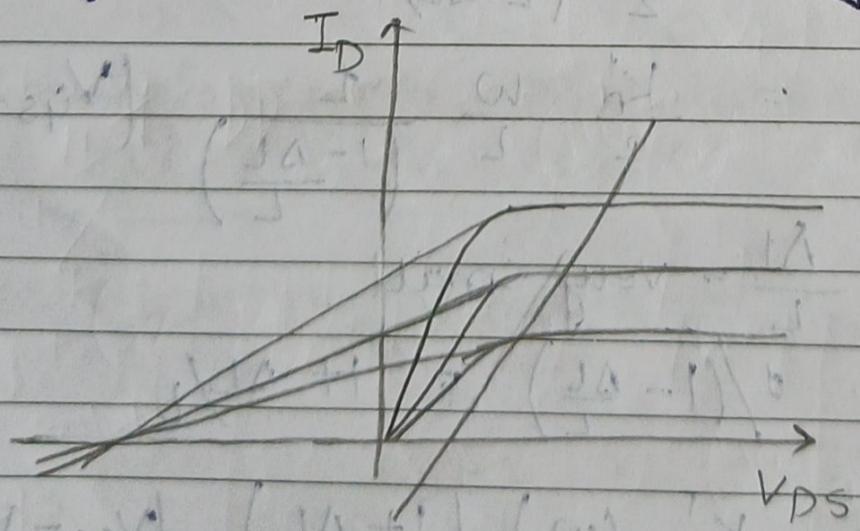
$$I_D = \frac{K_n}{2} \left(\frac{w}{L} \right) (V_{GS} - V_T)^2 (1 + 1' V_{DS})$$

NOTE: If $1=0$, it will be in normal saturation region. If $1=0$

$$I_D = \frac{K_n}{2} \left(\frac{w}{L} \right) (V_{GS} - V_T)^2$$

Hence, channel length will not come into picture.

Faulty voltage (V_A): It is the negative V_{DS} voltage that is applied to the transistor in order to make the drain current zero in saturation region is called as faulty voltage.



To find out at what voltage I_D becomes zero we have to follow following approach.

NOTE:

Resistance
Linear

$$V_{DS} = -I$$

only if the above condition is
there $I_D = 0$ in saturation region.

$$V_{DS} = -\frac{1}{I}$$

$$-V_{DS} = \frac{1}{I}$$

$$V_A = \frac{1}{I} \quad (\text{In saturation Region only})$$

: Resistance offered by the transistor

i) Resistance offered in ohmic region (r_{ds})

$$I_D = k_n \left(\frac{w}{L} \right) (V_{GS} - V_T) V_{DS}$$

Here there is $\frac{V_{DS}^2}{2}$ but we are neglecting

that term because in linear region, V_{DS} is very small. \therefore It's square = neglect.

$$\frac{\partial I_D}{\partial V_{DS}} = k_n \left(\frac{w}{L} \right) (V_{GS} - V_T)$$

Resistance in $\leftarrow r_{ds} = \frac{\partial V_{DS}}{\partial I_D}$
Linear region

$$r_{ds} = \frac{1}{k_n \left(\frac{w}{L} \right) (V_{GS} - V_T)} \quad (\text{in linear Region})$$

NOTE: We have $g_m = k_n \left(\frac{w}{L} \right) (V_{GS} - V_T)$ but we cannot

For a transistor to operate normally substrate voltage and source voltage must be same.

r_{ds} as $\frac{1}{g_m}$ because g_m is defined in saturation region and r_{ds} in linear.

ii) Resistance offered in saturation Region (r_o)

$$r_o = \frac{\partial V_{DS}}{\partial I_D}$$

$$I_D = \frac{k_n' (w/L)}{2} (V_{GS} - V_T)^2 (1 + \frac{1}{r_o})$$

$$\frac{\partial I_D}{\partial V_{DS}} = \frac{k_n' (w/L)}{2} (V_{GS} - V_T)^2$$

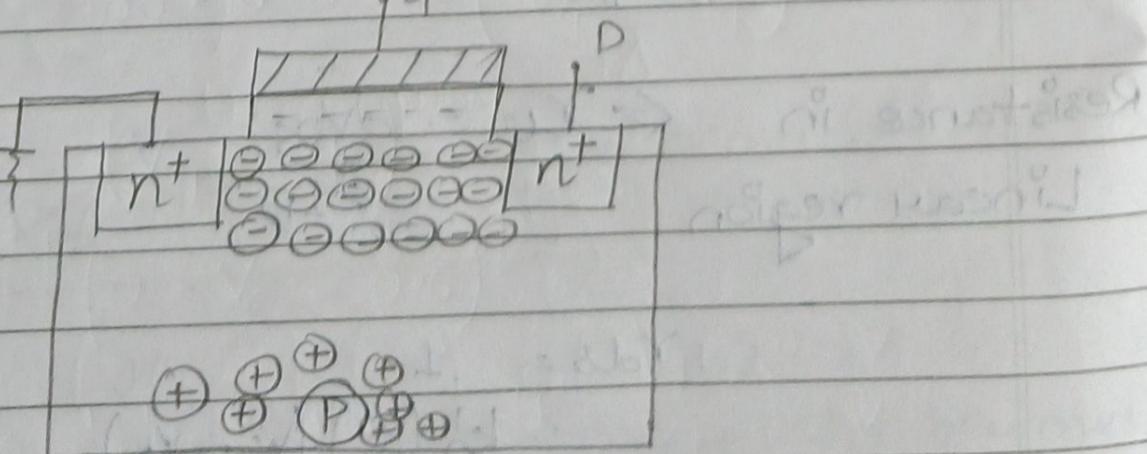
$$r_o = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{\frac{1}{r_o} + I_D} = \frac{V_A}{I_D}$$

NOTE:

If $\lambda = 0$, $r_o = \infty$ that is when there is no CLM, do not consider r_o .

(b) Body effect (Second order effect)

substrate/
Back gate
body also controls
gate voltage &
current flow



NOTE:

Here when substrate become more

negative, the body starts attracting more holes. As a result, the channel width widens with more e^- . As a result the applied voltage also increases and corresponding threshold voltage also increases.

It is the variation of threshold voltage with the increase in the substrate voltage.

$$V_t = V_{to} + Y \left[e^{\sqrt{2\phi_b + V_{SB}} - \sqrt{2\phi_s}} \right]$$

↓ ↓ ↓
 original Body $V_s - V_B$
 Threshold Body voltage
 voltage parameter

NOTE: If $V_{SB} = 0 \Rightarrow V_t = V_{to}$

: Transistor Application

1. Transistor as switch
2. Transistor as an amplifier.

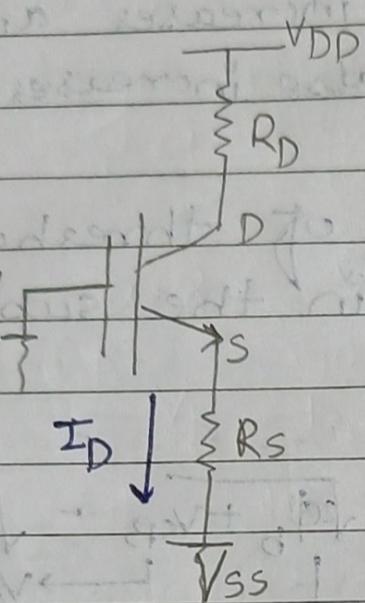
Transistor behaves as switch in linear & cutoff region for reducing complication we assume that it is at the verge of linear & saturation and consider current for saturation region.

NOTE:

- Current through gate is always zero.
- Only when AC signals is given, only then it

is amplifier, otherwise it is switch.

Q. For the circuit shown below



$$I_D = 1 \text{ mA}$$

$$V_T = 0.6 \text{ V}$$

$$k_n C_{ox} = 100 \text{ MA/V}^2$$

$$V_{DD} = 3 \text{ V}$$

$$V_{SS} = -3 \text{ V}$$

$$V_D = 0.8 \text{ V}$$

$$w/L = 20$$

Design circuit (finding resistance value)

$$V_{DD} - V_D = I_D R_D$$

$$3 - 0.8 = 1 \times R_D$$

$$R_D = 2.2 \text{ k}\Omega$$

$$I_D = \frac{k_n (w/L)}{2} (V_{GS} - V_T)^2$$

$$10^{-3} = \frac{100 \times 10^{-6} \times 20}{2} (V_{GS} - V_T)^2$$

$$1 = (V_{GS} - V_T)^2$$

$$1 = (0 - V_S - 0.6)^2$$

$$V_S^2 + 1.2 V_S + 0.36 = 1$$

$$V_S^2 + 1.2 V_S + 0.36 = 0$$

$$V_S = -1.6 \text{ V} \text{ or } 0.4 \text{ V}$$

Q. Design circuit

NOTE: Diode

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also
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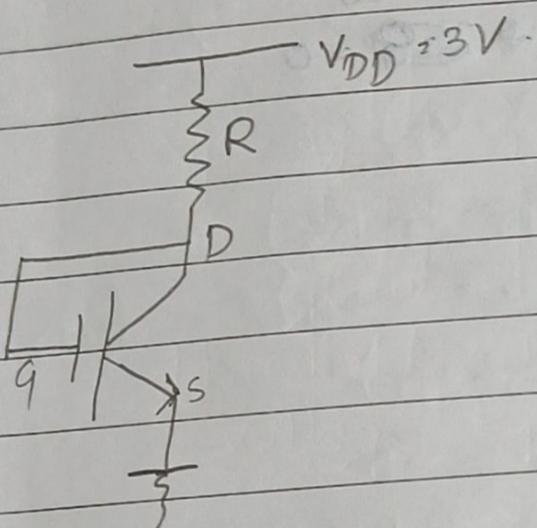
consider $-V_S$ as V_{SS} is negative

$$V_S - V_{SS} = I_D R_S$$

$$-1.6 + 3 = 10^{-3} \cdot R_S$$

$$R_S = 1.3 \text{ k}\Omega.$$

a. Design the resistance value for the circuit shown in the figure.



$$I_D = 200 \mu\text{A}$$

$$V_t = 0.6 \text{ V}$$

$$\mu n(\alpha) = 100 \mu\text{A}/\text{V}^2$$

$$W/L = 5$$

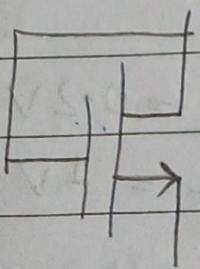
For saturation region.

$$V_{DS} > V_{GS} - V_t$$

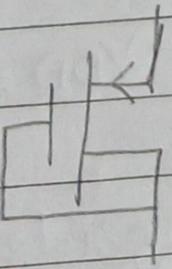
$$V_D > V_G - V_t$$

NOTE: Diode connected Load

When gate and drain terminals are connected together, the transistor is always in saturated region.
It will now be considered as load.



(NMOS)



(PMOS)

$$I_D = \frac{K_n'(\omega)}{2} [V_{GS} - V_T]^2$$

$$200 \times 10^{-6} = \frac{100 \times 10^{-6} \times 5}{2} (V_D - 0 - 0.6)^2$$

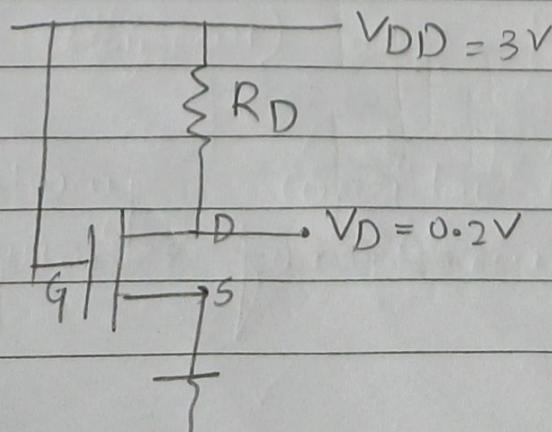
$$\frac{4}{5} = (V_D - 0.6)^2$$

$$0.8 = V_D^2 + 0.36 - 1.2 V_D$$

$$V_D^2 - 1.2 V_D - 0.28 = 0$$

Ans

Q. Find R_D and y_{DS} for the circuit



$$V_D = 0.2V$$

$$V_T = 1V$$

$$K_n' \left(\frac{\omega}{L} \right) = 1mA/V^2$$

→ Input R_1 and R_2 to MOSFET must be in M_N because FET should have very high input impedance.

$$V_G = 3V$$

$$V_{DS} = 0.2V$$

$$V_{GS} = 3V$$

$$V_{GS} - V_t = 2V$$

$(V_{DS} < V_{GS} - V_t)$ ⇒ Linear Region

$$\begin{aligned} I_D &= \frac{k_n' (w/L)}{2} \left((V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right) \\ &= \frac{10^{-3}}{2} \left(2 \times 0.2 - \frac{0.04}{2} \right) \\ &\Rightarrow \frac{10^{-3}}{2} \left(0.4 - 0.02 \right) \\ &= 0.38 \text{ mA} \end{aligned}$$

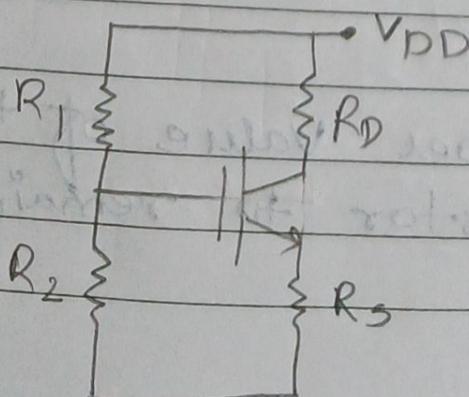
$$V_{DD} - V_D = I_D R_D$$

$$R_D = 7.368 \text{ k}\Omega$$

$$r_{ds} = \frac{1}{k_n' (V_{GS} - V_t)} = 500\Omega$$

NOTE: In linear region, the transistor must offer some finite resistance whereas in saturation region it offers ∞ resistance (it behaves like a constant current source which has by default ∞ resistance)

Q For the circuit shown, find V_G , V_D & I_S :



$$V_t = 1V$$

$$k_n' (w/L) = 2 \text{ mA/V}^2$$

$$V_{DD} = 12V$$

$$R_1 = 8M\Omega$$

$$R_2 = 4M\Omega$$

$$R_D = 5k\Omega, R_S = 2k\Omega$$

Using Thevenin's Theorem,

$$V_G = \frac{V_{DD} R_2}{R_1 + R_2} = \frac{12(9)}{12} = 4V$$

Assuming that transistor is in saturation.

$$I_D = \frac{K_n'(\omega)}{2} (V_{GS} - V_T)^2$$

$$I_D = \frac{2 \times 10^{-3}}{2} (4 - V_G - 1)^2$$

$$I_D = 10^{-3} (3 - V_S)^2$$

$$I_D = 10^{-3} (3 - I_D R_S)^2$$

$$I_D = 10^{-3} (3 - 2I_D)^2 \quad (I_D \text{ in mA})$$

$$I_D = (3 - 2I_D)^2$$

$$9 + 4I_D^2 - 12I_D = I_D$$

$$4I_D^2 - 13I_D + 9 = 0$$

$$4I_D^2 - 9I_D - 4I_D + 9 = 0$$

$$4I_D(I_D - 1) - 9(I_D - 1) = 0$$

$$I_D = 9/4 \text{ mA} \quad I_D = 1 \text{ mA}$$

$$I_D = 2.25 \text{ mA}$$

$$I_D = 1 \text{ mA}$$

$$V_D = 12 - I_D R_D$$

$$V_D = 7V$$

$$= 12 - (2.25) \times 5$$

$$= 0.75V$$

$$V_D < V_G - V_T$$

$$V_D > V_G - V_T \\ (\text{saturation})$$

$$V_D < (4 - 1) \\ (\text{Linear})$$

NOTE: Always consider lower value of the current for transistor to remain in

saturation region. Higher value of current will drive the transistor to linear region.

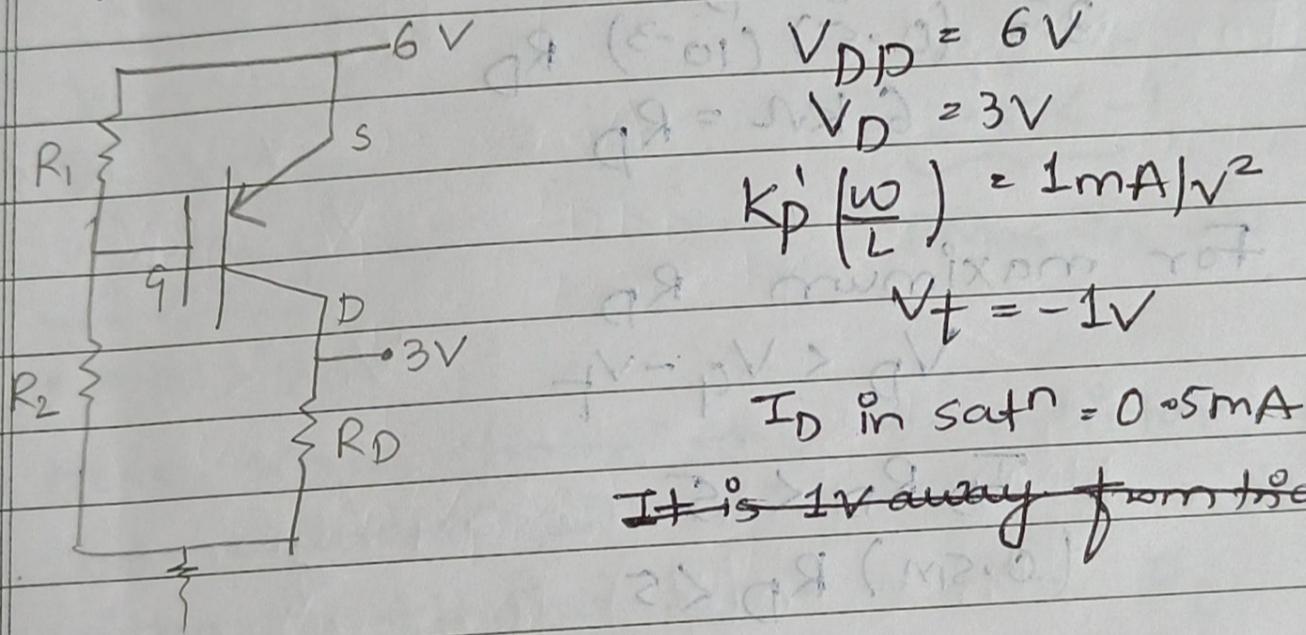
Here, $I_d = 1\text{mA}$

$$V_D = 7\text{V}$$

$$V_S = I_D R_S$$

$$V_S = 2\text{V}$$

Q. Design the circuit and find max R_D to operate the device \neq in saturation.



PMOS

$$V_{DS} < V_{GS} - V_T \quad (\text{for saturation})$$

V_T and V_{OV}

$$\text{must be -ve. } I_D = K_P' \left(\frac{W}{L}\right) (V_{GS} - V_T)^2$$

$$0.5 \times 10^{-3} = \frac{10^{-3}}{2} (V_G - V_S - V_T)^2$$

$$1 = (V_G - 6 + 1)^2$$

$$1 = (V_G - 5)^2 \quad (V_{OV} = \text{negative})$$

$$V_G - 5 = -1$$

$$V_G = 4\text{V}$$

$$V_G = \frac{6 R_2}{R_1 + R_2}$$

$$\frac{4}{6} = \frac{R_2}{R_1 + R_2}$$

$$R_2 = 4 \text{ M}\Omega$$

$$R_1 = 2 \text{ M}\Omega$$

$$V_{GS} = V_G - V_S$$

$$= 4 - 6 = -2 \text{ V}$$

$$V_D = I_D R_D$$

$$3 = (0.5) (10^{-3}) R_D$$

$$6 \text{ k}\Omega = R_D$$

For maximum R_D .

$$V_D < V_G - V_T$$

$$I_D R_D < 5$$

$$(0.5m) R_D < 5$$

$$R_D < 10 \text{ k}\Omega$$

(R_D must be less than $10 \text{ k}\Omega$)

$$\text{max. } R_D = 10 \text{ k}\Omega$$

Observation: R_D of $6 \text{ k}\Omega$ to $10 \text{ k}\Omega$ will retain the transistor in saturation region.

- Q. For the circuit shown below $k_n'(\frac{\mu_0}{L}) = k_p'(\frac{\mu_0}{L}) = 1 \text{ mA/V}^2$ $V_{tn} = |V_{tp}| = 1 \text{ V}$. Find I_{DP} , I_{Dn} and V_{out} for

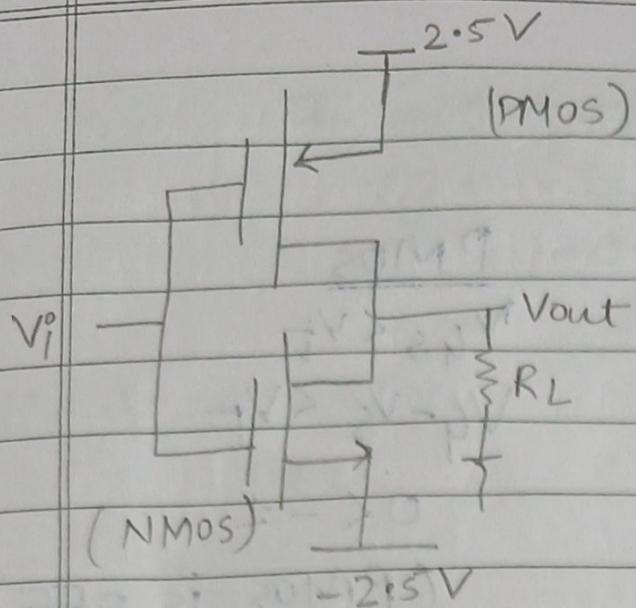
i)
ii)
iii)

$$V_J^o = 0 \text{ V}$$

$$V_J^d = 2.5 \text{ V}$$

$$V_J^i = -2.5 \text{ V}$$

$$R_L = 10 \text{ k}\Omega$$



$$(i) \quad V_i = 0V$$

NMOS

$$V_{GS} > V_t$$

$$V_g - V_s > V_t$$

$$\underbrace{2.5}_{>1} > 1$$

NMOS in ON

PMOS

$$V_{GS} < V_t$$

$$-2.5 < -1$$

PMOS in ON

Here, since both the transistors are ON, the current will directly flow down without flowing across the R_L .
 $\therefore V_{out} = 0$

$$\left. \begin{array}{l} V_{DS} = 0 - (-2.5) \\ = 2.5V \end{array} \right\}$$

$$\left. \begin{array}{l} V_{DS} > V_{GS} - V_t \\ (\text{Saturation}) \end{array} \right\}$$

$$\left. \begin{array}{l} V_{DS} = 0 - 2.5V \\ V_{DS} = -2.5V \end{array} \right\}$$

$$\left. \begin{array}{l} V_{DS} < V_{GS} - V_t \\ (\text{saturation}) \end{array} \right\}$$

Same current is flowing through PMOS and NMOS.

$$I_{Dp} = I_{DN} = \frac{k_n}{2} \left(\frac{W}{L} \right) (V_{GS})^2$$

$$= \frac{1}{2} (V_{GS} - V_t)^2$$

$$I_{Dp} = I_{DN} = 1.125 \text{ mA}$$

$$V_D = 2.5V$$

NMOS

$$V_{GS} > V_t$$

$$2.5 - (-2.5) > 1$$

$$5 > 1$$

(NMOS is ON)

PMOS

$$V_{GS} < V_t$$

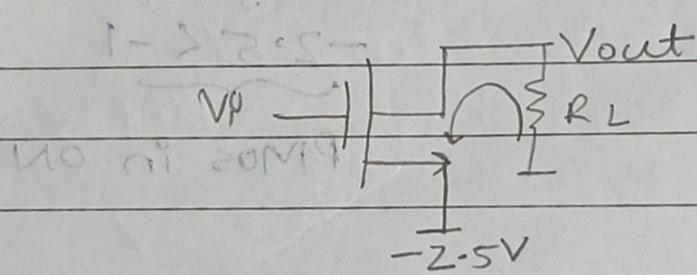
$$V_g - V_s < V_t$$

$$0 < -1$$

(PMOS is OFF)

$$I_{Dp} = 0 \quad (\text{PMOS} = \text{OFF})$$

For NMOS:



$$V_D = -2.5V$$

V_D only b/w 0 & -2.5V

$$V_{DS} < V_{GS} - V_t$$

NMOS is in Linear region

$$I_{Dn} = k_n \left(\frac{W}{L} \right) \left[(V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$\left(\frac{V_{DS}^2}{2} = \text{negligible} \right)$$

$$I_{Dn} = k_n \left(\frac{W}{L} \right) (V_{GS} - V_t) V_{DS}$$

$$V_{DS} = V_D - V_S$$

$$V_D = -(I_D R_L)$$

(negative sign is used to show that current is flowing from ground to V_S)

$$I_D = 1 \left((5-1) (-10 I_D + 2.5) \right)$$

$$I_D = 0.2439 \text{ mA}$$

$$V_D = -I_D R_L$$

$$= -2.44 \text{ V}$$

(iii) $V_i = -2.5 \text{ V}$

NMOS

$$V_{GS} > V_t$$

$$V_G - V_S > V_t$$

 $0 > 1 \neq \text{True}$

$$\text{NMOS} = 0$$

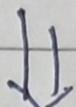
$$I_{DN} = 0$$

PMOS

$$V_{GS} < V_t$$

$$-5 < -1$$

True

 $\} \text{PMOS} = \text{on}$ Here max V_{out}

is possible b/w 0-2.5V

PMOS:

$$V_{DS} = V_D - V_S \quad (V_D = 1 \Rightarrow \text{for evaluation of region})$$

$$V_{GS} - V_t = -4$$

$$V_{DS} > V_{GS} - V_t \quad (\text{Linear/Ohmic Region})$$

$$I_D = K_p \left(\frac{W}{L} \right) \left(V_{GS} - V_t \right) V_{DS} \quad (V_{GS} = -4)$$

$$= (V_{GS} - V_t) V_{DS}$$

$$V_D = I_D R_L \quad (\text{Here the dirn is +ve})$$

$$I_D = -4 (10 I_D - 2.5)$$

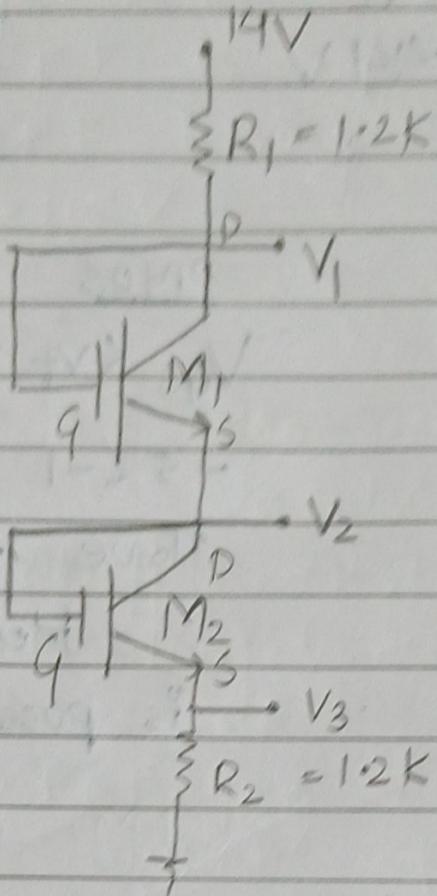
$$I_D = 0.244 \text{ mA}$$

$$V_{out} = I_D R_L$$

$$= 2.44 \text{ V}$$

Q. Find V_1, V_2 and V_3 if the two transistors are identical with $V_t = 1 \text{ V}$,

$$K_n^I(\omega_L) = 0.25 \text{ mA/V}^2$$



for M_1 : $I_D = \frac{K_n^I(\omega_L)}{2} (V_{GS} - V_T)^2$

We also have:

$$14 - I_D R_1 = V_1 \quad \textcircled{1}$$

$$I_D = \frac{0.25}{2} (V_1 - V_2 - 1)^2 \quad \textcircled{A}$$

$$V_3 = I_D R_2 \quad \textcircled{2}$$

for M_2 : $I_D = \frac{0.25}{2} (V_2 - V_3 - V_T)^2$

$$I_D = 0.125 (V_2 - V_3 - 1)^2 \quad \textcircled{B}$$

Equating \textcircled{A} and \textcircled{B}

$$0.125 (V_1 - V_2 - 1)^2 = 0.125 (V_2 - V_3 - 1)^2$$

$$V_1 - V_2 = V_2 - V_3$$

$$V_2 = \frac{V_1 + V_3}{2} - \textcircled{E}$$

for M_1 :

$$I_D = \frac{14 - V_1}{1.2} \leftarrow \textcircled{C}$$

for M_2 :

$$I_D = \frac{V_3}{1.2} - \textcircled{D}$$

Equate \textcircled{C} and \textcircled{D}

$$\frac{14 - V_1}{1.2} = \frac{V_3}{1.2}$$

$$V_1 + V_3 = 14$$

$$\text{Put in } \textcircled{E} \quad V_2 = 7V$$

Put V_2 in \textcircled{B}

$$I_D = 0.125 (7 - I_D(1.2) - 1)^2$$

$$I_D = 0.125 (6 - 1.2 I_D)^2$$

$$I_D = 4.5 - 1.8 I_D + 0.18 I_D^2$$

$$I_D = 13.73 \text{ mA or } 1.82 \text{ mA}$$

Consider the lower value:

$$I_D = 1.82 \text{ mA}$$

$$V_3 = I_D(1.2)$$

$$V_S = 2.184V$$

From C

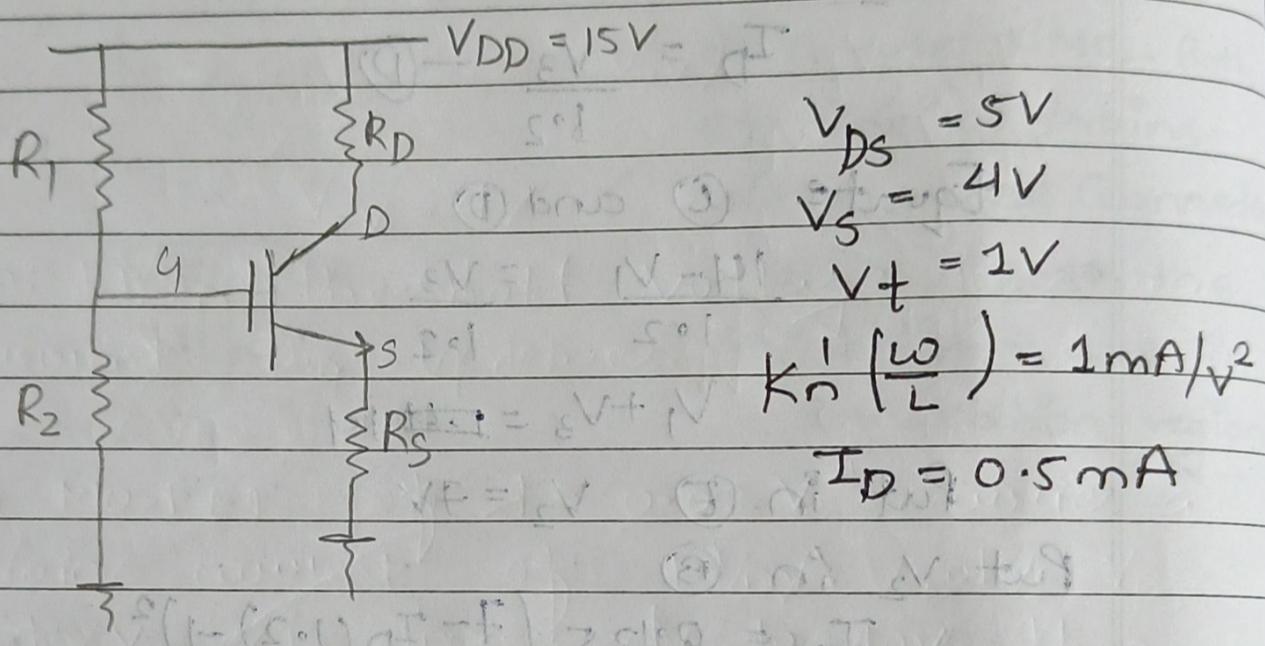
$$I_D = 2.184$$

$$14 - V_1 = 2.184$$

$$V_1 = 11.8V$$

- Q. Design the circuit to obtain $I_D = 0.5 \text{ mA}$,
 $V_S = 8V$, $V_{DS} = 5V$ and $V_T = 1V$, $k_n(\frac{\omega}{L}) = 1 \text{ mA/V}^2$

$V_{DD} = 15V$. Also, calculate the percentage change in I_D obtained when the MOSFET is replaced with another MOSFET having the same $k_n'(\frac{w}{L})$ but $V_t = 1.5V$



Assuming the transistor in saturation region

$$I_D = A k_n' (\frac{w}{L}) \cdot (V_{ov})^2$$

$$0.5 = \frac{1}{2} (V_{ov})^2$$

$$V_{ov} = 1V$$

$$V_{GS} - V_t = V_{ov}$$

$$V_{GS} = V_{ov} + V_t$$

$$V_{GS} = 1 + 1$$

$$V_{GS} = 2V$$

$$V_G = 6V$$

$$V_{DD} - V_G = I_D R_1$$

$$R_1 = \frac{V_{DD} - V_G}{I_D} = \frac{15 - 6}{0.5} \times 10^3$$

$$R_1 = 18 \text{ k}\Omega$$

$$\left\{ \begin{array}{l} V_G = I_D R_2 \\ R_2 = \frac{6}{0.5} \times 10^3 \\ R_2 = 12 \text{ k}\Omega \end{array} \right\}$$

$$V_{DS} = 5V$$

$$V_D - V_S = 5$$

$$V_D = 9V$$

$$R_D = \frac{V_{DD} - V_D}{I_D} = 12 \text{ k}\Omega$$

$$R_S = \frac{V_S}{I_D} = 8 \text{ k}\Omega$$

By voltage divider,

$$V_G = \frac{V_{DD} R_2}{R_1 + R_2}$$

$$\frac{6}{15} = \frac{R_2}{R_1 + R_2}$$

$$R_1 = 9 \text{ M}\Omega$$

$$R_2 = 6 \text{ M}\Omega$$

for replacement:

$$k_n'(\omega/L) = 1 \text{ mA/V}^2$$

$$V_t = 1.5V$$

$$I_D = \frac{k_n'(\omega/L)}{2} (V_G - V_S - V_t)^2$$

$$I_D = 0.5 (6 - I_D R_S - 1.5)^2$$

$$32 I_D^2 - 37 I_D + 10.125 = 0$$

$$I_D = 0.7116 \text{ mA or } 0.4446 \text{ mA}$$

Considering the lower value of I_D

$$I_D = 0.4446 \text{ mA}$$

Observation: When threshold voltage increases current I_D decreases.

Q. A MOSFET of $\alpha = 0.02 \text{ V}^{-1}$ carries a drain current of 1.1 mA when $V_{DS} = 5\text{V}$. If V_{DS} is increased to 10V , then drain current of the device will be _____?

$$I_D = 1.1 \text{ mA} \quad \text{when } V_{DS} = 5\text{V} ; \alpha = 0.02 \text{ V}^{-1}$$

$$I_D = \frac{K_n(\omega/L)}{2} (V_{GS}) (1 + \alpha V_{DS})$$

$$I_{D1} \propto 1 + \alpha V_{DS}$$

$$I_{D1} = \beta (1 + \alpha V_{DS})$$

$$= \beta (1 + 0.02(5))$$

$$= \beta (1 + 0.1)$$

$$I_{D1} = \beta (1.1)$$

$$1.1 \text{ mA} = \beta (1.1) \quad \text{--- (1)}$$

$$I_{D2} = \beta (1 + 0.02(10))$$

$$I_{D2} = \beta (1.2)$$

$$I_{D2} = 1.2 \beta \quad \text{--- (2)}$$

Ratio of ① and ②

- Q. for a mass transition if w/L is increased by 16 times while maintaining its I_D constant, its g_m will be increased by a factor of _____?

$$g_m \propto \sqrt{w/L}$$

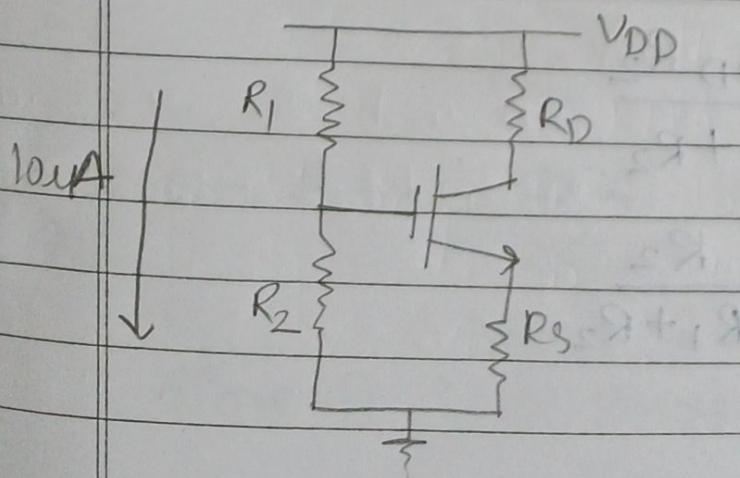
$$\frac{g_{m_1}}{g_{m_2}} = \sqrt{\frac{w_1}{L_1} \times \frac{L_2}{w_2}}$$

$$\frac{g_{m_2}}{g_{m_1}} = \sqrt{\frac{A R_2}{A R_1}}$$

$$g_{m_2} = 4 g_{m_1}$$

(Four times increase in g_m)

- Q. Design the circuit so that it operates in the saturation with $I_D = 2\text{mA}$, $V_D = 6\text{V}$, $V_{DP} = 10\text{V}$, $k_n'(w/L) = 0.25 \text{ mA/V}^2$, $V_t = 1\text{V}$ and it is 1V away from triode region.



$$I_D = 2\text{mA}$$

$$V_D = 6\text{V}$$

$$V_{DD} = 10\text{V}$$

$$k_n'(w/L) = 0.25 \text{ mA/V}^2$$

$$V_t = 1\text{V}$$

Since, they are telling that V_T is 1V away from linear region.

$$V_{DS} = V_{GS} - V_T + 1$$

$$I_D = \frac{k_n(w/L)}{2} (V_{OV})^2$$

$$2 = \frac{0.25}{2} (V_{OV})^2$$

$$V_{OV} = 4V$$

$$V_{DS} = V_{OV} + 1$$

$$V_{DS} = V_{GS} - V_T + 1$$

$$V_{DS} = 4 + 1$$

$$V_{DS} = 5V$$

$$V_D - V_S = 5$$

$$V_S = 1V$$

$$V_{OV} = V_{GS} - V_T$$

$$V_{OV} = V_G - V_S - V_T$$

$$4 = V_G - 1 - 1$$

$$V_G = 6V$$

$$R_D = \frac{V_{DD} - V_D}{I_D}$$

$$R_S = \frac{V_S}{I_D}$$

$$= \frac{10 - 6}{2 \times 10^{-3}}$$

$$= 1/2 \times 10^3$$

$$= 2k\Omega$$

$$R_S = 500\Omega$$

Using voltage divider rule,

$$V_G = \frac{V_{DD} R_2}{R_1 + R_2}$$

$$\frac{6}{10} = \frac{R_2}{R_1 + R_2}$$

In PMOS, V_{ov} and V_t must be negative

PAGE EDGE

Date :

We have an additional 10mA current there

$$(10\text{mA}) (R_1 + R_2) = V_{DD}$$

$$R_1 + R_2 = \frac{10}{10 \cdot 10^{-6}}$$

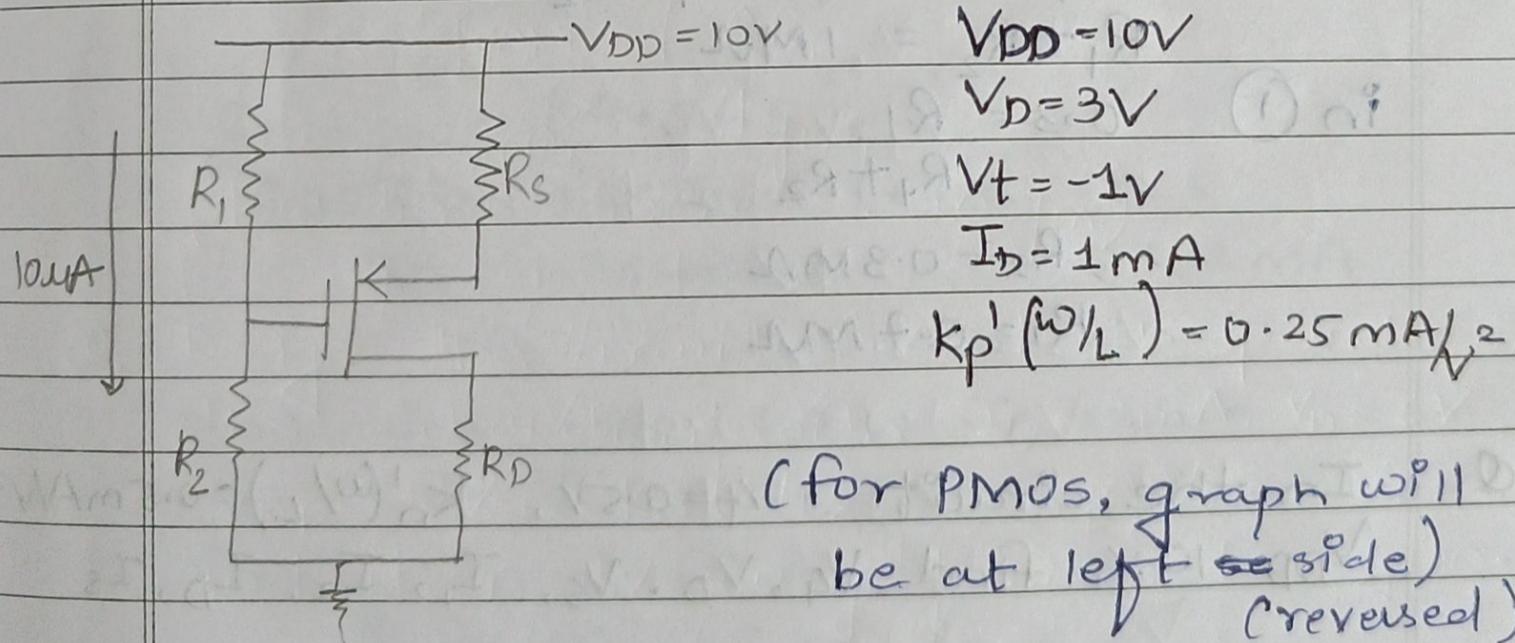
$$R_1 + R_2 = 10^6 \Omega$$

$$\frac{6}{10} = \frac{R_2}{R_1 + R_2}$$

$$\frac{6 \times 10^6}{10} = R_2$$

$$R_2 = 0.6 \text{ M}\Omega, R_1 = 0.4 \text{ M}\Omega$$

Q. Design the circuit such that the transistor is biased one volt from the edge of triode region.



(for PMOS, graph will
be at left side)
(reversed)

$$I_D = k_p' \frac{(\omega/L)}{2} (V_{ov})^2$$

$$I = 0.25 \frac{(V_{ov})^2}{2}$$

$$V_{ov} = \pm 2.84V$$

Since it is a PMOS $V_{ov} = -ve$

$$V_{ov} = -2.84V$$

$$V_{DS} = V_{GS} - V_t - 1$$

$$V_D - V_s + V_{DS} = V_{OV} - 1$$

$$V_s = 6.82V$$

$$V_{OV} = V_{GS} - V_t$$

$$V_{OV} = V_G - V_s - V_t$$

$$-2.82 = V_G - 6.28 + 1$$

$$V_G = 3V$$

$$R_S = \frac{V_{DD} - V_s}{I_D}$$

$$= 3.18 k\Omega$$

$$R_D = \frac{V_D}{I_D} = 3k\Omega$$

$$V_G = \frac{V_{DD} R_2}{R_1 + R_2}$$

$$\frac{3}{10} = \frac{R_2}{R_1 + R_2} \quad \text{--- (1)}$$

$$\text{But, } V_{DD} = 10mA(R_1 + R_2)$$

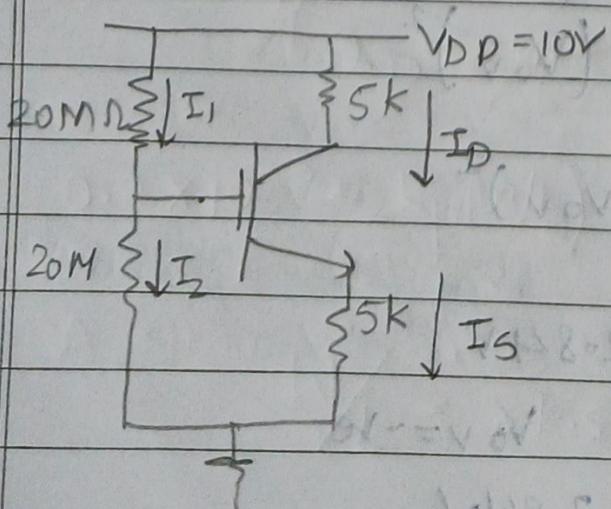
$$R_1 + R_2 = 1M\Omega$$

$$\text{in (1)} \quad 0.3 = \frac{R_1}{R_1 + R_2}$$

$$R_2 = 0.3M\Omega$$

$$R_1 = 0.7M\Omega$$

- Q. In the circuit $V_t = 0.5V$, $K_n'(w/L) = 0.5mA/V^2$
 $V_{DD} = 10V$, find V_G , V_D , V_s , I_1 , I_2 , I_D , I_S



I_D and I_S are same.

I_1 and I_2 are same

$$\frac{V_{DD} - V_D}{5K} = I_D \quad I_S = \frac{V_S}{5K}$$

$$\frac{10 - V_D}{5K} = I_D \quad \text{--- (1)}$$

Assuming to be in saturation

$$V_G = \frac{V_{DD} R_2}{R_1 + R_2}$$

$$V_G = \frac{10 \times 20M}{(20+20)M} = 5V$$

$$I_D = \frac{k_n'}{2} \left(\frac{w}{L}\right) (V_{GS} - V_T)^2$$

$$= \frac{k_n'}{2} \left(\frac{w}{L}\right) (V_G - V_S - V_T)^2$$

$$I_D = \frac{k_n'}{2} \left(\frac{w}{L}\right) (V_G - 5I_D - 0.5)^2$$

$$I_D = \frac{0.5}{2} (5 - 0.5 - 5I_D)^2$$

$$I_D = 0.25 (4.5 - 5I_D)^2$$

$$6.25I_D^2 - 12.25I_D + 5.0625 = 0$$

$$I_D = 1.3678 \text{ mA or } 0.5922 \text{ mA}$$

Considering the lower I_D value

$$I_D = 0.59 \text{ mA}$$

Putting I_D in (1)

$$\frac{10 - V_D}{5K} = 0.59 \text{ mA}$$

$$V_D = 7.05V$$

$$I_D = I_S$$

$$I_S = \frac{V_S}{5K}$$

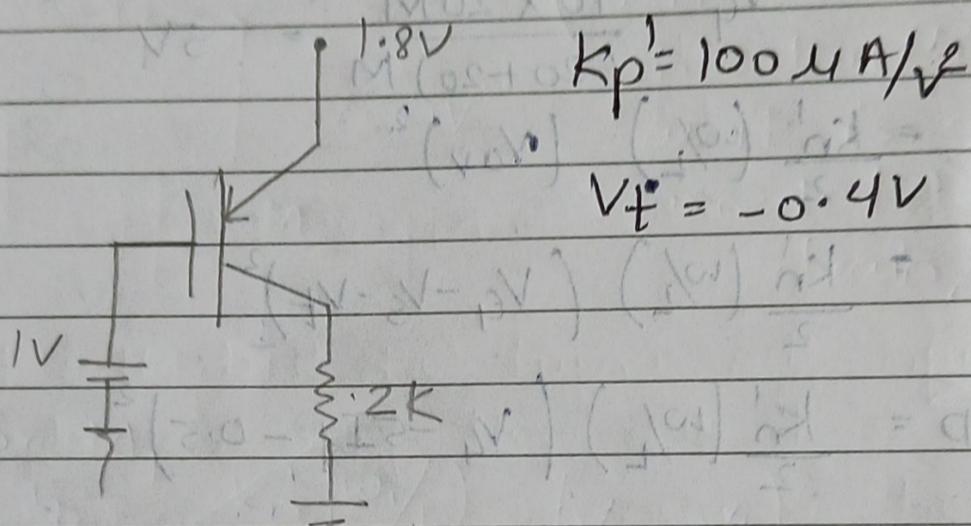
$$V_S = 2.95V$$

$$V_{DD} = I_1 (40 \times 10^6)$$

$$I_1 = \frac{10}{40} \times 10^{-6}$$

$$I_1 = 0.25 \text{ mA} = I_2$$

Q. What value of (W/L) places the device in saturation.



At the verge,

$$V_{DS} = V_{GS} - V_F$$

$$V_{DS} = V_G - V_S - V_F$$

$$= 1 - 1.8 + 0.4$$

$$V_{DS} = -0.4V$$

$$V_{DS} = -0.4V$$

$$V_D - 1.8 = -0.4$$

$$V_D = 1.4$$

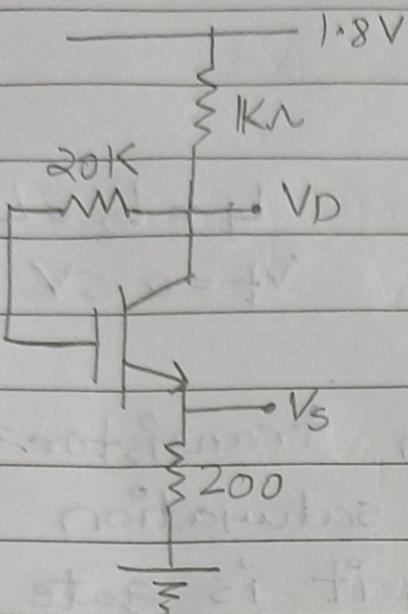
$$V_D = 2 \times I_D$$

$$I_D = 0.7 \text{ mA}$$

$$0.7 \times 10^{-3} = \frac{k_p (W/L)}{2} \frac{(1 - 1.8 + 0.4)^2}{V_{DS}}$$

$$W/L = 87.5$$

Q If $k_n = 100 \mu A/V^2$, $V_T = 0.5V$, $w/L = 5/0.18$



Find drain current.

Gate and drain is shorted.

(No current will flow through the resistor as $I_g = 0$)

$$V_g = V_D$$

$$I_D \text{ in } \mu A$$

$$I_D = \frac{k_n' (w/L)}{2} (V_{GS} - V_T)^2$$

$$\left\{ \begin{array}{l} V_{DD} - V_D = I_D \times 1K \\ 1.8 - V_D = 1.8 - I_D \end{array} \right. \quad \left\{ \begin{array}{l} V_S = 0.2 I_D \\ \end{array} \right.$$

$$I_D = \frac{k_n' (w/L)}{2} (V_{GS} - V_T)^2$$

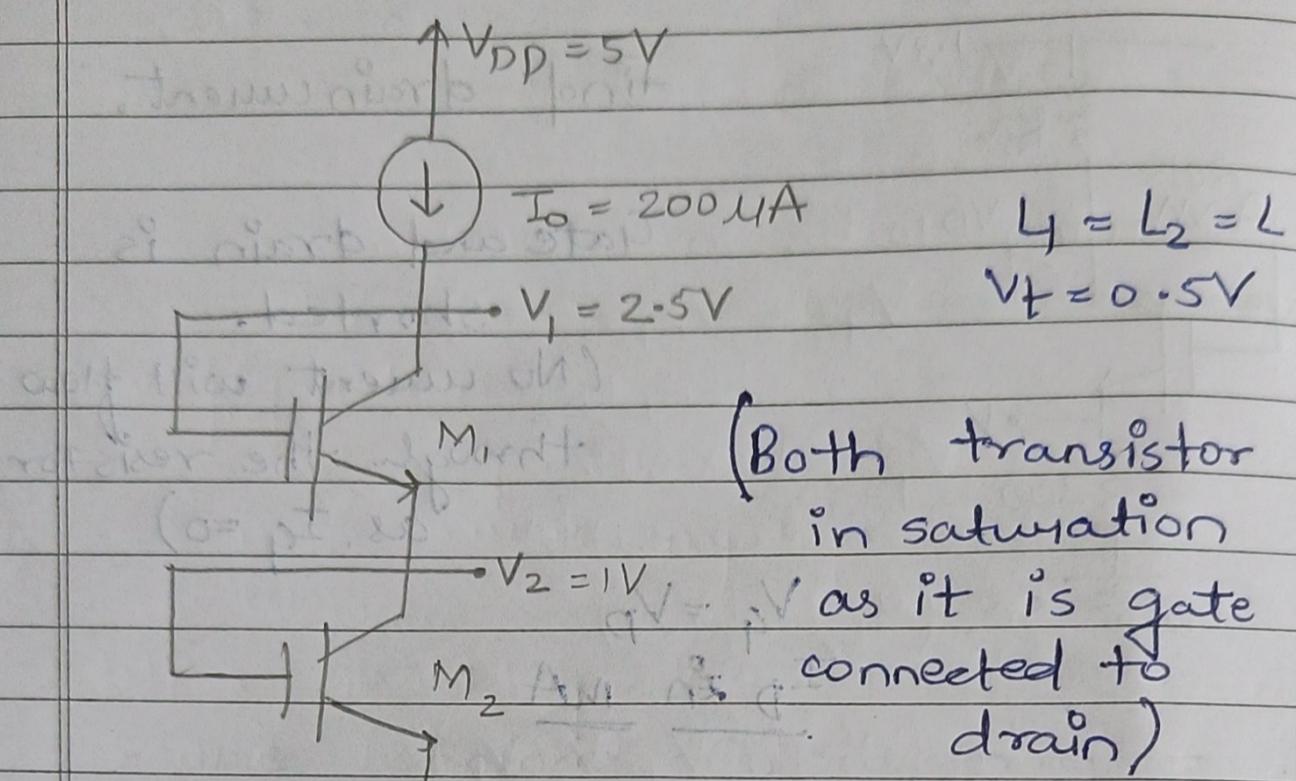
$$I_D = \frac{k_n' (w/L)}{2} (V_B - V_S - V_T)^2$$

$$I_D = \frac{k_n' (w/L)}{2} (1.8 - I_D - 0.2 I_D - 0.5)^2$$

$$I_D = 2.122 \mu A \text{ or } 0.55 \mu A$$

Q The NMOS transistor in the circuit are identical in all respects except their gate width find the gate width of transistor (w_1 and w_2) if $I_D = 200 \mu A$ of the transistor $V_{DD} = 5V$, $V_B = 2.5V$,

$$V_2 = 1V, V_t = 0.5V, K_n = 100 \mu A/V^2$$



For M_1 :

$$I_D = \frac{K_n}{2} \left(\frac{W_1}{L} \right) (V_{GS} - V_T)^2$$

$$200 = \frac{100 k_1}{2L} (V_1 - V_S - V_T)^2$$

$$2 = \frac{w_1}{2L} (2.5 - 1 - 0.5)^2$$

$$w_1 = 4L$$

For M_2 :

$$I_D = \frac{K_n}{2} \left(\frac{W_2}{L} \right) (V_{GS} - V_T)^2$$

$$4 = \left(\frac{w_2}{L} \right) (0.25)$$

$$w_2 = 16L$$

Q. A NMOS transistor has $C_{ox} = 10 fF/\mu m^2$

$w = 100 \mu m$, $L = 0.8 \mu m$, $V_t = 0.5 V$ if
 $V_{GS} = 1.5 V$. The total charge stored in
the channel when V_{DS} is 0 is _____.

$$Q = \frac{1}{2} C_{ox} \cdot w \cdot L (V_{GS} - V_t) (V_{GS} - V_t)$$

$$= \frac{10 \times 10^{-15}}{(10^{-6})^2} (100 \cdot (0.8)) (10^{-12}) (1.5 - 0.5)$$

$$= 10^{-12} (10 \cdot 8)$$

$$Q = 800 fC.$$

- Q For the circuit shown, calculate the incremental impedance between A and B. Assume NMOS is operating with $I_D = 1 \text{ mA}$, $\lambda = 0$, and $k_n' [f_0/L] = 0.5 \text{ mA/V}^2$

