RV College of Engineering, Bengaluru-560059

(Autonomous Institution affiliated to VTU, Belgaum)

Department of Electronics and Communication Engineering

Analysis and Design of Digital Circuits with HDL EC234AI

Laboratory Manual and Observation Book

Academic Year

2025-2026

(Autonomous Scheme 2022)

RV College of Engineering, Bengaluru-560059

(Autonomous Institution affiliated to VTU, Belgaum)

Department of Electronics and Communication Engineering

Laboratory Certificate

This is to certify that the following student has satisfactorily completed the course of Experiments in Practical **Analysis and Design of Digital Circuits with HDL (EC234AI)** prescribed by the Department during the year 2025-26

Name of the Candidate:_____

USN No.: _____

Semester: III

Marks	
Maximum	**Obtained**
50	

Marks in words	

Signatures:

Staff in-charge: **Head of the Department**

Date:

RV College of Engineering, Bengaluru-560059

(Autonomous Institution affiliated to VTU, Belgaum)

Department of Electronics and Communication Engineering

Analysis and Design of Digital Circuits with HDL (EC234AI)

SCHEME OF CONDUCTION AND EVALUATION

CLASS: III SEMESTER CIE MARKS: (Max.): 50

Expt. No.	TITLE	Page No.	Duration in Hrs	Max. Marks
1	Truth Table verification of all Gates and Half adder/subtractor, Full adder/subtractor with NAND gates using IC trainer kit.	7-13	2.00	10
2	Realization of Binary adder/ subtractor using IC-7483.	14-16	2.00	10
3	Realization of the given Boolean expressions using MUX/DEMUX using IC-74153,IC- 74139.	17-20	2.00	10
4	Realization of Binary Adder and Subtractor using Verilog HDL and verification by simulation	21-24	2.00	10
5	Realization of Multiplexer/Decoders/Encoder using Verilog HDL and verification by simulation.	25-20	2.00	10
6	Realization of D, T, JK flip flop in Verilog HDL and verification by simulation and Implementation on FPGA	31-32	2.00	10
7	Design of synchronous 3-bit up/down counter using IC-7476/IC-74112 on IC trainer kit. Verifcation of function table of presettable counter using IC 74192	33-39	2.00	10
8	Design of synchronous up/down/BCD counter using Verilog HDL and verification by simulation. Implementation on FPGA	40-42	2.00	10
9	Design of Shift register, ring counter, Johnson counter using Verilog HDL and verification by simulation. Implementation on FPGA	43-45	2.00	10
10	Design of Sequence generator and detector using Verilog HDL and verification by simulation.	46-47	2.00	10
11	Innovative Experiments (Multiplier and Processor Design)	48	2.00	10
Experiment Conduction 30 Marks				
Conduction of Innovative experiments 10 Marks				
Lab Test Evaluation 10 Marks				
Final Lab CIE 50 Marks				

Particulars of the Experiments Performed

CONTENTS

Evaluation Rubrics:

Sl.No	Criteria	Excellent	Good	Average	Max Score
Data sheet					
A	Problem statement	9-10	6-8	1-5	**10**
B	Design & specifications	9-10	6-8	1-5	**10**
C	Expected output	9-10	6-8	1-5	**10**
Record					
D	Simulation/ Conduction of the experiment	14-15	11-13	1-10	**15**
E	Analysis of the result.	14-15	11-13	1-10	**15**
Viva					**40**
Total					**100**
Scale down to 10 marks					

VISION

Imparting quality technical education through interdisciplinary research, innovation and teamwork for developing inclusive & sustainable technology in the area of Electronics and Communication Engineering.

MISSION

M1: To impart quality technical education to produce industry-ready engineers with a research outlook.

M2: To train the Electronics & Communication Engineering graduates to meet future global challenges by inculcating a quest for modern technologies in the emerging areas.

M3: To create centers of excellence in the field of Electronics & Communication Engineering with industrial and university collaborations.

M4: To develop entrepreneurial skills among the graduates to create new employment opportunities.

Truth Table verification of all Gates and Half adder/subtractor, Full adder/subtractor with NAND gates using IC trainer kit.

Experiment 01

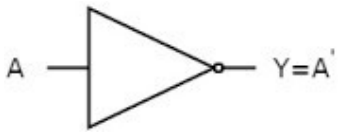
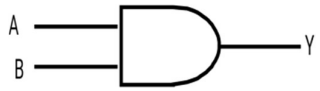
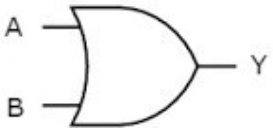
Aim: To verify the truthtable of all basic gates and To design and implement half/full adder and half/full subtractor using NAND gates .

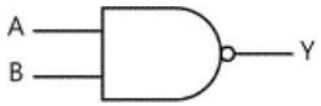
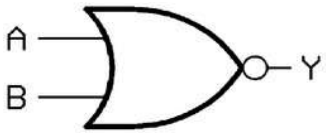
Components Required: ICs -74LS00,74LS86, 74LS83 ,Digital trainer kit, patch chords.

Note: Data Sheet should be referred for pin details.

PART-1

1) Truth Table verification of basic, universal and XOR gate.

Gate	Symbol	Input A	Input B	Output Y
BASIC GATES				
NOT Gate (IC-7404) Y=A'		0	NA	1
		1	NA	0
AND Gate (IC-7408) Y=A.B		0	0	0
		0	1	0
		1	0	0
		1	1	1
OR Gate (IC-7432) Y=A+B		0	0	0
		0	1	1
		1	0	1
		1	1	1

Gate	Symbol	Input A	Input B	Output Y
UNIVERSAL GATES				
NAND Gate **(IC-7400)** **Y=(A.B)'**		0	0	1
		0	1	1
		1	0	1
		1	1	0
NOR Gate **(IC-7402)** **Y=(A+B)'**		0	0	1
		0	1	0
		1	0	0
		1	1	0
DERIVED GATES				
XOR Gate **(IC-7486)** **Y=A⊕B**		0	0	0
		0	1	1
		1	0	1
		1	1	0
XOR Gate **(IC-74266)** **Y=(A⊕B)'** Note: Use XOR gate followed by NOT gate		0	0	1
		0	1	0
		1	0	0
		1	1	1

(a) Half adder (HA):

(i) Design:

B1	B0	S	C
0 +	0 =	0	0
0 +	1 =	1	0
1 +	0 =	1	0
1 +	1 =	0	1

(a) 1-bit addition

Inputs		Outputs	
A	B	S_O	C_O
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

(b) HA Function Table (TT)

Fig. 1.1: Design of Half Adder

Simplified (K-map) design equations for the outputs Sum(S_O) and Carry(C_O) are in Eq. 1.1

$$S_O = \Sigma_m(1,2) = \overline{A}\,B + A\,\overline{B} = A \oplus B \text{ and } C_O = \Sigma_m(3) = A\,B \qquad \textbf{Eq. 1.1}$$

(ii) Implementation using NAND gates:

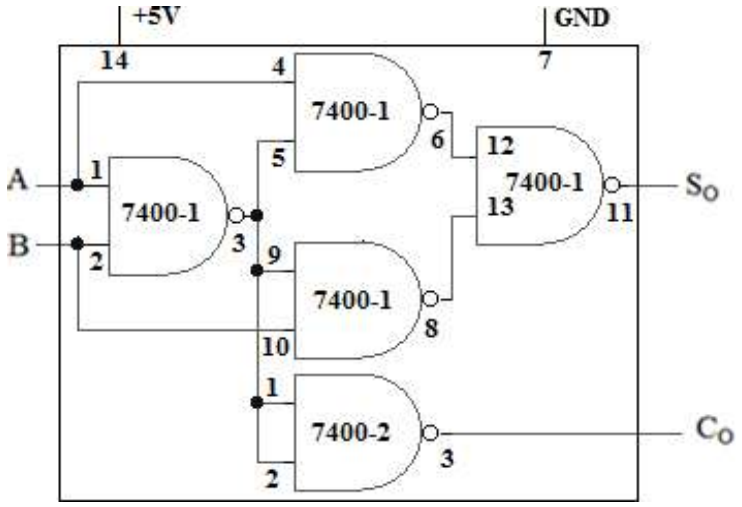


Fig. 1.2: Logic diagram of Half Adder using NAND gates

(iii) Observations:

Inputs		Outputs	
A	B	S_O	C_O
0	0		
1	0		
0	1		
1	1		

(b) Full Adder (FA):

(i) Design:

Ci	B1	B0	S	Co
0 +	0 +	0 =	0	0
0 +	0 +	1 =	1	0
0 +	1 +	0 =	1	0
0 +	1 +	1 =	0	1
1 +	0 +	0 =	1	0
1 +	0 +	1 =	0	1
1 +	1 +	0 =	0	1
1 +	1 +	1 =	1	1

1-bit addition with carry input

Inputs			Outputs	
A	B	C_{in}	S_O	C_O
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(b) FA Function Table (TT)

Fig. 1.3: Design of Full Adder

Simplified (K-map) design equations for the outputs Sum(S_O) and Carry(C_O) are in Eq. 1.2

$$S_O = \Sigma_m(1,2,4,7) = A \oplus B \oplus C_{in}$$

$$C_O = \Sigma_m(3,5,6,7) = A\,B + BC_{in} + AC_{in} \qquad \textbf{Eq. 1.2}$$

(ii) Implementation using NAND gates :

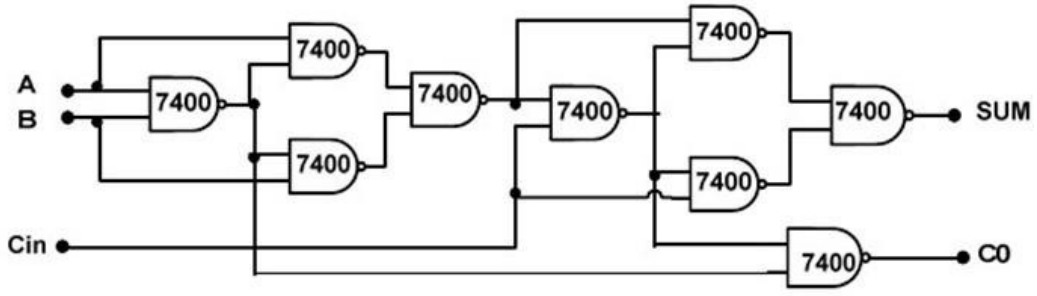


Fig. 1.4: Design of Full Adder using NAND gates

(iii) Observations:

Inputs			Outputs	
A	B	C_{in}	S_0	C_0
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

(c) Half Subtractor (HS):

(i) Design:

0 - 0 = 0

0 - 1 = 1 1

1 - 0 = 1

1 - 1 = 0 0

(a) 1-bit subtraction

Inputs		Outputs	
A	**B**	**S_O**	**C_O**
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

(b) HS Function Table (TT)

Fig. 1.5: Design of Half Subtractor

Simplified (K-map) design equations for the outputs Difference (D_O) and Borrow(B_O) are given in Eq. 1.3

$$D_O = \Sigma_m(1,2) = \overline{A}\,B + A\,\overline{B} = A \oplus B \text{ and } B_O = \Sigma_m(3) = \overline{A}\,B \qquad \textbf{Eq. 1.3}$$

(ii) Implementation using NAND gates:

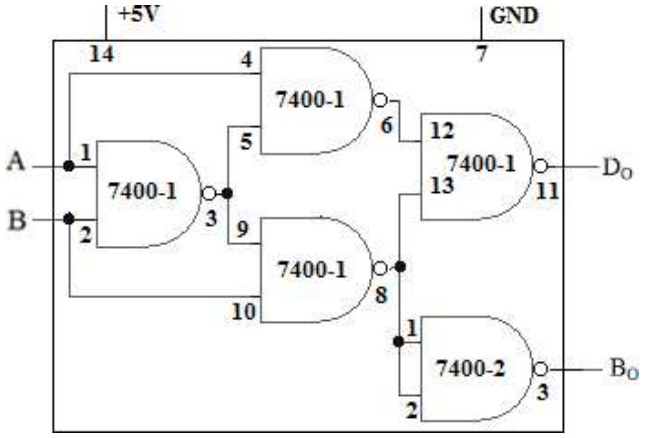


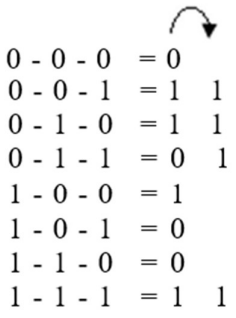
Fig. 1.6: Logic diagram of Half Subtractor using NAND gates

(iii) Observations:

Inputs		Outputs	
A	B	D_O	B_O
0	0		
1	0		
0	1		
1	1		

(d) Full Subtractor:

Design:



(a) 1-bit subtraction with borrow input

Inputs			Outputs	
A	B	B_{in}	D_O	B_O
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

(b) FS Function Table (TT)

Fig. 1.7: Design of Full Subtractor

Simplified (K-map) design equations for the outputs Difference (D_O) and Borrow(B_O) are given in Eq. 1.4

$$D_O = \Sigma_m(1,2,4,7) = A \oplus B \oplus B_{in} \text{ and}$$

$$B_O = \Sigma_m(1,2,3,7) = \bar{A}\,\bar{B}B_{in} + A\,\bar{B}\,\bar{B}_{in} + \bar{A}\,B\,B_{in} + A\,B\,B_{in} \quad \textbf{Eq. 1.4}$$

(iv)Implementation using NAND gates:

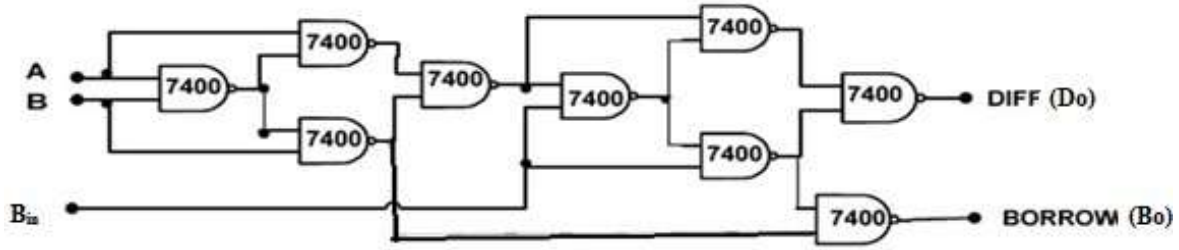


Fig. 1.8: Design of Full Subtractor using NAND gates

(v) Observations:

Inputs			Outputs	
A	B	B_{in}	D_0	B_0
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Procedure:

1. The circuit connections are made as shown in the diagrams (as per the designs).
2. V_{dd} and Gnd are connected to all the ICs used in the design.
3. The inputs are connected to logic switches and the corresponding outputs are connected to LEDs
4. Input values are varied as per the Truth table (TT) and verified output as per the TTs.
5. The above procedure is repeated for all the four circuits and the TTs are verified.
6. Conclusions/Inferences are derived from the conducted experiments.

Inferences/Conclusions:

Sl.No	Criteria	Max Marks	Marks obtained
Data sheet			
A	Problem statement	10	
B	Design & specifications	10	
C	Expected output	10	
Record			
D	Simulation/ Conduction of the experiment	15	
E	Analysis of the result.	15	
F	Viva	40	
	Total	100	
Scale down to 10 marks			

Staff Signature:

Realization of Binary Adder and Subtractor using IC 74LS83

Experiment 02

Aim: To design and implement Binary adder and substractor using IC-7483.

Components Required: ICs -74LS00,74LS86, 74LS83 ,Digital trainer kit, patch chords.

Note: Data Sheet should be referred for pin details.

Parallel Adder/Subtractor:

Logic diagram of IC-74LS83:

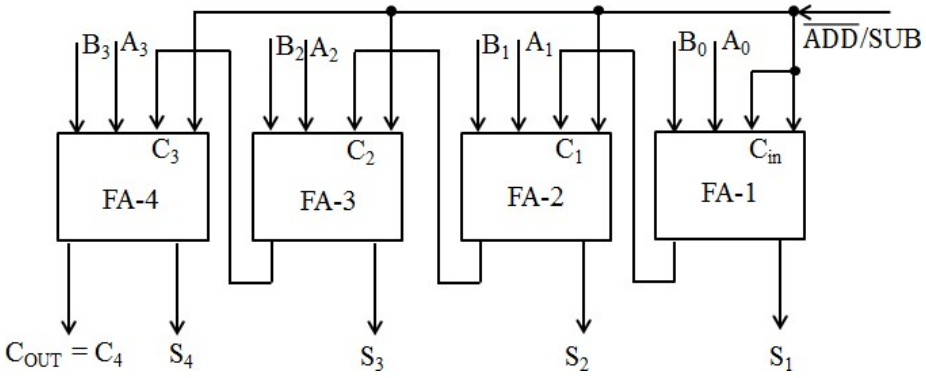
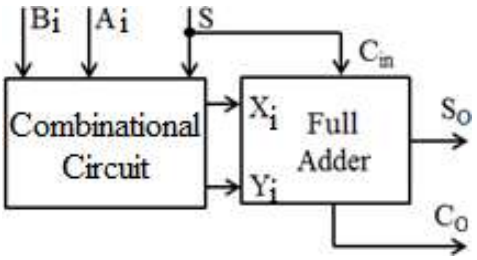


Fig. 2.1: Logic diagram of Parallel Adder

(i) Design:



S	X	Y	Cin
0	X	Y	0
1	X	Y′	1

S	A	B	X	Y
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	1	1
1	0	0	0	1
1	0	1	0	0
1	1	0	1	1
1	1	1	1	0

Fig. 2.2 : Algorithm for Adder/Subtractor design

Simplification using K-map results in the expressions of Eq. 1.5;

$X_i = A_i$, $Y_i = B_i$ xor S, and $C_{in} = S$. **Eq. 1.5**

The resulting combinational circuit is called the 'Controlled Inverter' as it produces 1s complement to realize 2s complement addition. Implementing the expressions in Eq. 1.5 along with a parallel adder results in a parallel adder/subtractor circuit shown in Fig. 1.11.

(ii) Implementation:

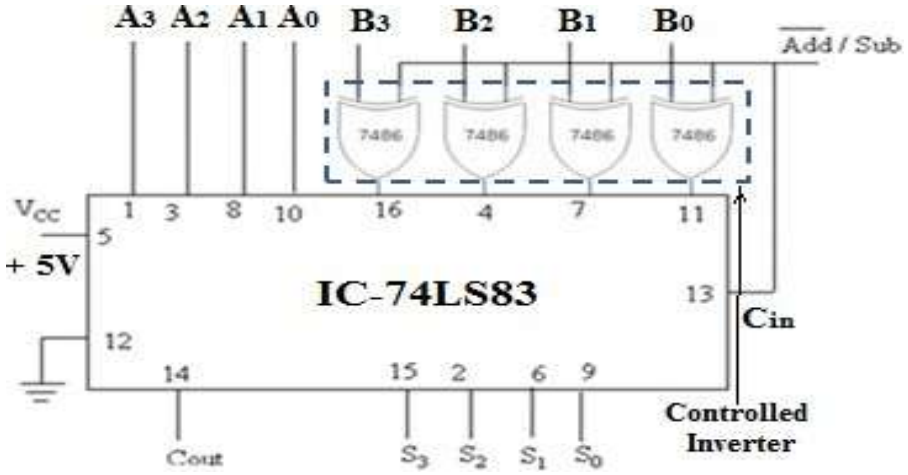


Fig. 2.3 : Logic diagram of Parallel Adder

(iii) Observations and sample calculations :

Procedure:

Four bit Parallel Adder:

1. Connections are made as shown in the circuit diagram of Fig. 2.1.
2. The control input $\overline{\text{Add}}/\text{Sub} = 0$, the inputs are applied through logic switches and the adder outputs are noted (LEDs) for different values of inputs.
3. The procedure is repeated for different set of inputs and verified the respective outputs

Four bit Parallel Subtractor:

1. Connections are made as shown in the circuit diagram of Fig. 2.1
2. The control input $\overline{\text{Add}}/\text{Sub} = 1$,the inputs are applied through logic switches and the adder outputs are noted (LEDS) for different values of inputs.
3. The procedure is repeated for different set of inputs and verified the respective outputs.

Note:

The adder IC-74LS83 performs addition of the minuend and 2's complement of subtrahend which is subtraction of the 2-binary numbers (C_{in} = '1')

Practice Questions:

a) **Design a parallel binary subtractor to get actual difference based on the value of Cout using IC 7483.**

Conclusion /Inference:

Evaluation:

Sl.No	Criteria	Max Marks	Marks obtained
Data sheet			
A	Problem statement	10	
B	Design & specifications	10	
C	Expected output	10	
Record			
D	Simulation/ Conduction of the experiment	15	
E	Analysis of the result.	15	
F	Viva	40	
	Total	100	
Scale down to 10 marks			

Staff Signature:

Arithmetic circuits- Realize the given Boolean expressions using MUX/DEMUX using IC-74153,IC- 74139.

Experiment 03

Aim: To realize the given Boolean expressions using multiplexer and de-multiplexer.

Components Required: ICs - 7404, 74153, 74139, 7420,Digital trainer kit, patch cords.

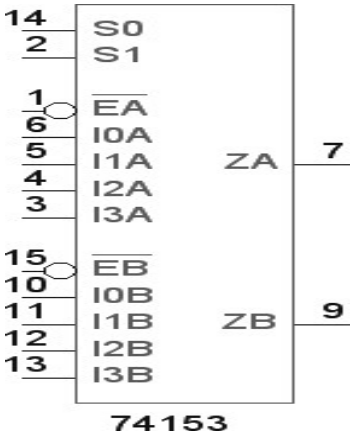
(a) Implementation of Boolean expression using MUX- IC 74153

(i) Design

The given Boolean expression for the implementation are,

F1(A,B,C)=∑m(1,2,4,7) and F2(A,B,C)=∑m(0,4,5,6)

Pin diagram of 74153



Implementation Table

	I_0	I_1	I_2	I_3
F1 (MUXA)	A	A’	A’	A
F2(MUX B)	1	A	A	0

(ii) Implementation

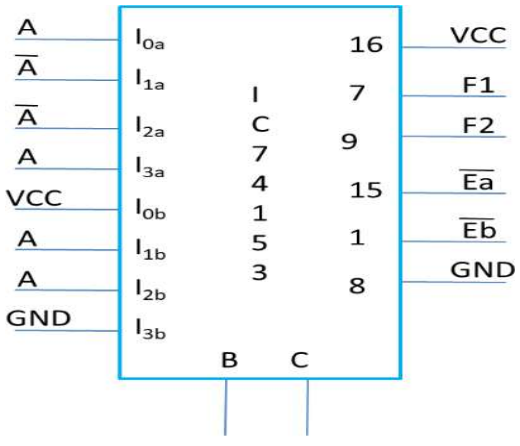


Fig.3.1 Implementation using IC-74153

(iii) Procedure:

1) Rig up the circuit using IC-74153 and NAND gates as shown in the design(Refer Fig.3.1)

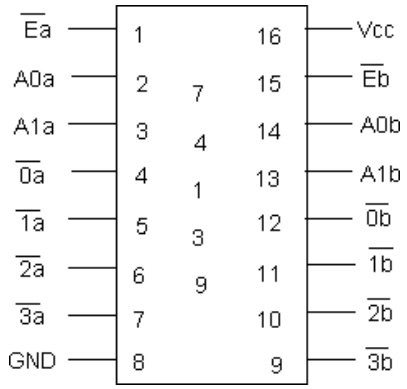
2) Verify the output with the truth table Values.

(iv)Observations:

Inputs			Outputs	
A	B	C	F1	F2
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

(b) Implementation of Boolean expression using DEMUX- IC 74139

Pin Diagram of 74139



Function Table of IC-74139:

Decoder A

$\overline{Ea}$	A1a	A0a	$\overline{0a}$	$\overline{1a}$	$\overline{2a}$	$\overline{3a}$
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

Decoder B

$\overline{Eb}$	A1b	A0b	$\overline{0b}$	$\overline{1b}$	$\overline{2b}$	$\overline{3b}$
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

Note: Where E, A1 and A0 are Enable and Input lines respectively.

(i) Design:

The given Boolean expressions for the implementation are,

F1(A,B,C)=∑m(1,2,4,7) and F2(A,B,C)=∑m(0,4,5,6)

(ii) Implementation:

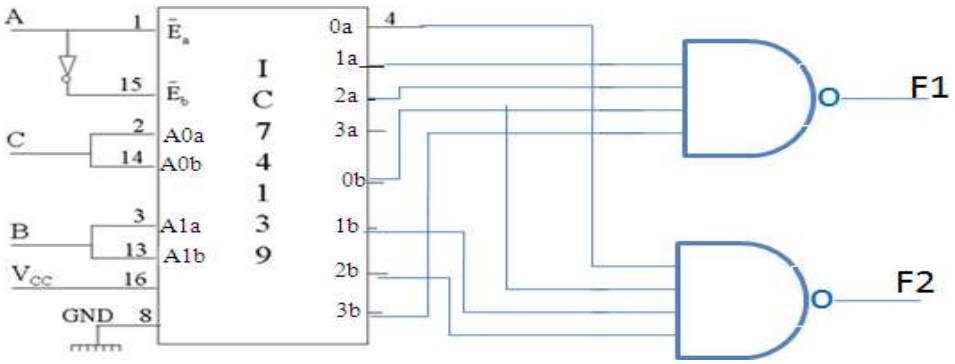


Fig.3.2 Implementation using IC-74139

(iii)Procedure:

1)Rig up the circuit using IC-74139 and NAND gates as shown in the design(Refer Fig.3.2)

2)Verify the output with the truth table Values.

(iv)Observation:

Inputs			Outputs	
A	B	C	F1	F2
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Practice Questions:

a) Realize FA/FS using MUX/DEMUX using IC 74153 and IC 74139

Inferences/Conclusions:

Evaluation:

Sl.No	Criteria	Max Marks	Marks obtained
	Data sheet		
A	Problem statement	10	
B	Design & specifications	10	
C	Expected output	10	
	Record		
D	Simulation/ Conduction of the experiment	15	
E	Analysis of the result.	15	
F	Viva	40	
	Total	100	
Scale down to 10 marks			

Staff Signature: