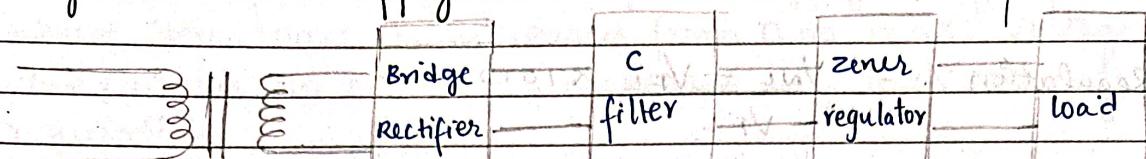


Regulated Power Supply  $\Rightarrow$



transformer  
step down AC (for home appliances)

pulsating DC (constant DC waveform)

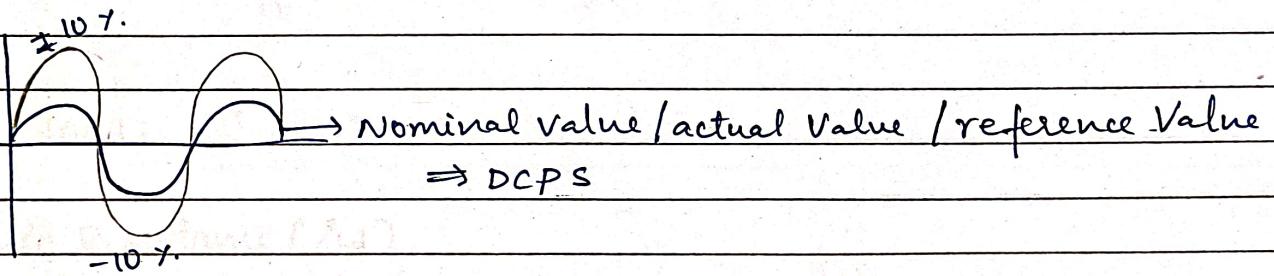
en: 9V charge  
7V discharge

constant

$$\text{output} \Rightarrow \frac{9+7}{2} = 8V$$

performance analysis of DC power supply  $\Rightarrow$

1) line Regulation



Step down Voltage

line Regulation  $\gamma_L = \frac{\Delta V_o}{V_o} \text{ for } \pm 10\% V_s \times 100$

Calways w.r.t input  $\rightarrow$  What if there  
are fluctuations  
in the input)

Nominal Voltage /  
Reference Voltage

2) load regulation  $\Rightarrow$  ← wiggel. gegen belastung

$$\text{load Regulation \%} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

$V_{NL}$  = No load (open circuit)  $\Rightarrow I_L = 0, R_L = \infty$  (max)

$V_{FL}$  = Full load  $\Rightarrow I_L = \uparrow, R_L = \downarrow$

(closed switch condition)

← wiggel. gegen da die ankerlast ändert sich

anker generat. und lasten (aber dann nicht)

Ex1: The output voltage of a DC power supply changes from 20V to 19.7V when the load is increased from 0 to max. Voltage increases to 20.2V when the AC supply increases by 10%. calculate line & load regulation.

$$\text{Load regulation} = \frac{20 - 19.7}{19.7} \times 100 = \frac{0.3}{19.7} \times 100 = 1.52\%$$

$$\text{Line regulation} = \frac{20.2 - 20}{20} \times 100 = \frac{0.2}{20} \times 100 = 1\%$$

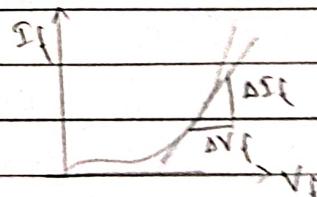
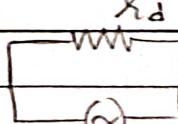
Ex2: A dc power supply output drops from 15V to 14.95V when the AC source voltage falls by 10%. the output also falls from 15V to 14.9V when the load current is increased from 0 to max. find line & load regulation.

$$\text{line : } \frac{15 - 14.95}{15} \times 100 = \frac{1}{3}\%$$

$$\text{load : } \frac{15 - 14.9}{15} \times 100 = 2\%$$

Dynamic Resistance ( $r_d$ )

$$r_d = 26mV$$



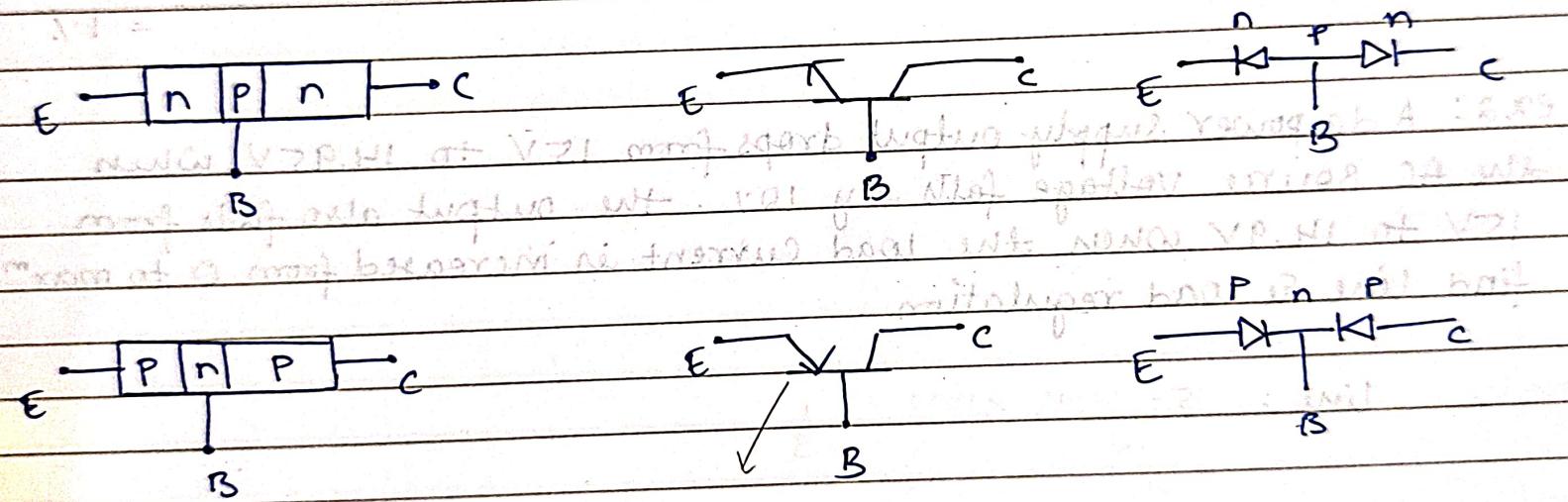
$$\frac{\Delta I_f}{\Delta V_f} = \text{slope} = \frac{1}{r_d}$$

Transistors (BJT)  $\Rightarrow$  more popular because it is a small device with low cost and easy to manufacture. It has three terminals: base, collector, and emitter.

$E = V_{BE} + V_{CE}$   $\Rightarrow$   $V_{BE} = V_{BE} - 0.6$  = collector bias

$E = V_{BE} + V_{CE}$   $\Rightarrow$   $V_{BE} = 0.6 - 0.6 =$  collector bias

Types of BJT transistors (pnp & npn)

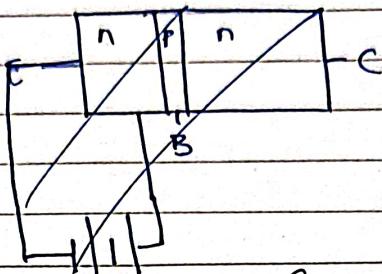
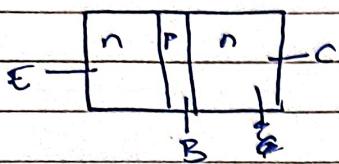


arrow indicates  
direction of current  
(always  $P \rightarrow N$ )

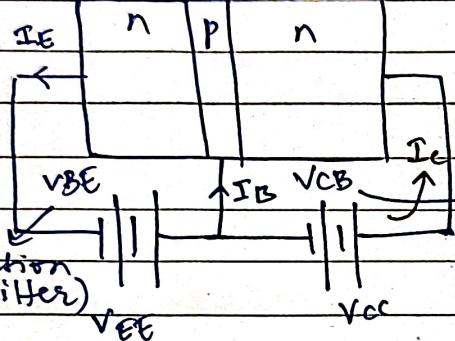
application  
 1. amplifier  
 2. switch.

### Transistor Operations

n - p - n



for amplifier (C)



Junction  $V_{BQ}$   $\rightarrow$  B collector to base

$$I_E = I_B + I_C$$

Common emitter voltage      common collector voltage

total current.



common base configuration

## Regions of transistor

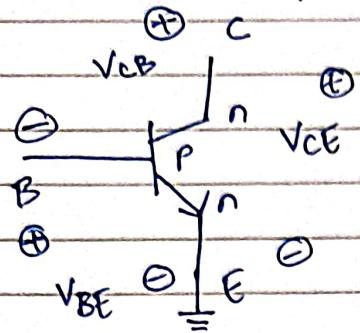
Region	E-B-J <sup>n</sup>	C-B-J <sup>n</sup>	Application
1. Active	FB	RB	Amplifier
2. Saturation	FB	FB	closed switch
3. Cutoff	RB	RB	open switch
4. Reverse / inverse Active	RB	FB	Attenuator

Anti-parallel NPN diode A<sub>1</sub> is connected in series with R<sub>2</sub> and E<sub>2</sub>. It is also connected in parallel with R<sub>1</sub> and R<sub>3</sub>.

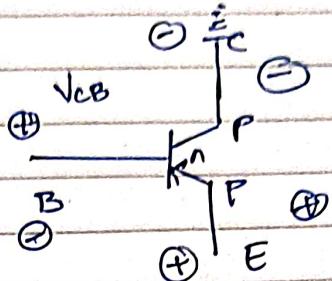
$$E_{12} = 0.1 \times 0.6 + 0.1 \times 0.2 + 0.1 = 0.14V$$

$$E_{12} = (20.0 + 2.0) \times 0.05$$

## Transistor Voltages



{NPN}



{PNP}

$$V_{BE} = -V_{EB}$$

$$V_{CE} = -V_{EC}$$

Current gain

1)  $\alpha$  - It is the ratio of collector current ( $I_C$ ) over emitter current ( $I_E$ ). Generally applied for common collector configuration

$$\alpha = \frac{I_C}{I_E} < 1, 0.99$$

2)  $\beta$  - Ratio of  $I_C$  over  $I_B$ . generally applied for common emitter configuration

$$\beta = I_C / I_B, 25 \text{ to } 500$$

$$I_E = I_C + I_B$$

$$I_E = \beta I_B + I_B = I_B(1 + \beta)$$

$$\alpha = \frac{\beta}{1 + \beta}; \beta = \frac{\alpha}{1 - \alpha}$$

relation b/w  $\alpha$  &  $\beta$

(a)

If the  $I_B$  in a transistor is  $20 \mu\text{A}$  when  $I_E$  is  $6.4 \text{ mA}$ . find the values of  $\alpha$  &  $\beta$  also calculate  $I_C$

$$I_C = I_E - I_B = 6.4 \times 10^{-3} - 20 \times 10^{-6}$$

$$10^{-3} (6.4 - 0.02) = 6.38 \times 10^{-3}$$

$$\frac{20 \times 10^{-3}}{0.02 \times 10^{-3}} = \frac{6.4 \times 10^{-3}}{0.02} = 38$$

$$\alpha = \frac{6.38 \times 10^{-3}}{6.4 \times 10^{-3}} = 0.996$$

$$\beta = \frac{6.38 \times 10^{-3} \times 10^3}{20 \times 10^{-6}} = 319$$

Q) calculate  $I_C$ ,  $I_E$  and  $\beta$  for a transistor having  $\alpha = 0.98$ ,  $I_B = 120 \mu A$

$$\frac{0.98}{I_E} = I_C$$

$$\beta = \frac{I_C}{120 \times 10^{-6}}$$

$$\beta = \frac{0.98}{1 - 0.98} = \frac{0.98}{0.02} = 49$$

$$49 \times 120 \times 10^{-6} = I_C$$

$$= 5.88 \times 10^{-3}$$

Q)  $I_C = 12.4 \text{ mA}$ ,  $I_B = 200 \mu A$  find  $I_E$ ,  $\alpha$ ,  $\beta$ .

ii) find  $I_C$  when  $I_B = 150 \mu A$

$$i) I_E = 0.0126$$

$$\alpha = \frac{I_C}{I_E} = \frac{12.4 \times 10^{-3}}{0.0126} = 0.984$$

$$\beta = \frac{I_C}{I_B} = 62$$

$$ii) \frac{62}{0.984} = \frac{I_C}{150 \times 10^{-6}} = \cancel{62} \times 10^{-3} \times 150 \times 10^{-6} = 9.3 \times 10^{-3}$$

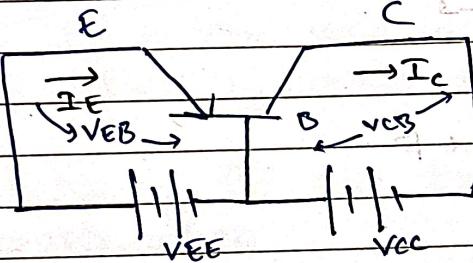
$\therefore$

Q)  $I_C = 16 \text{ mA}$ ,  $I_E = 16.04 \text{ mA}$  find the new values of  $I_C$  &  $I_E$  for the same value of  $I_C$  if the transistor is replaced with a transistor of  $\beta = 25$

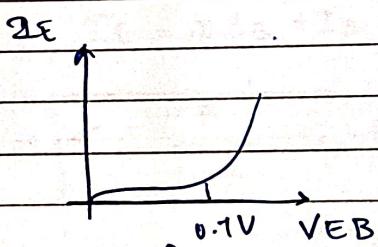
$$\beta = \frac{I_E}{I_B} = \frac{16.04 \text{ mA}}{16 \text{ mA}} \Rightarrow I_B = 6.4 \times 10^{-4} \text{ A}$$

$$I_E = I_B(1 + \beta) = 6.4 \times 10^{-4} \times 26$$

Common Base configuration



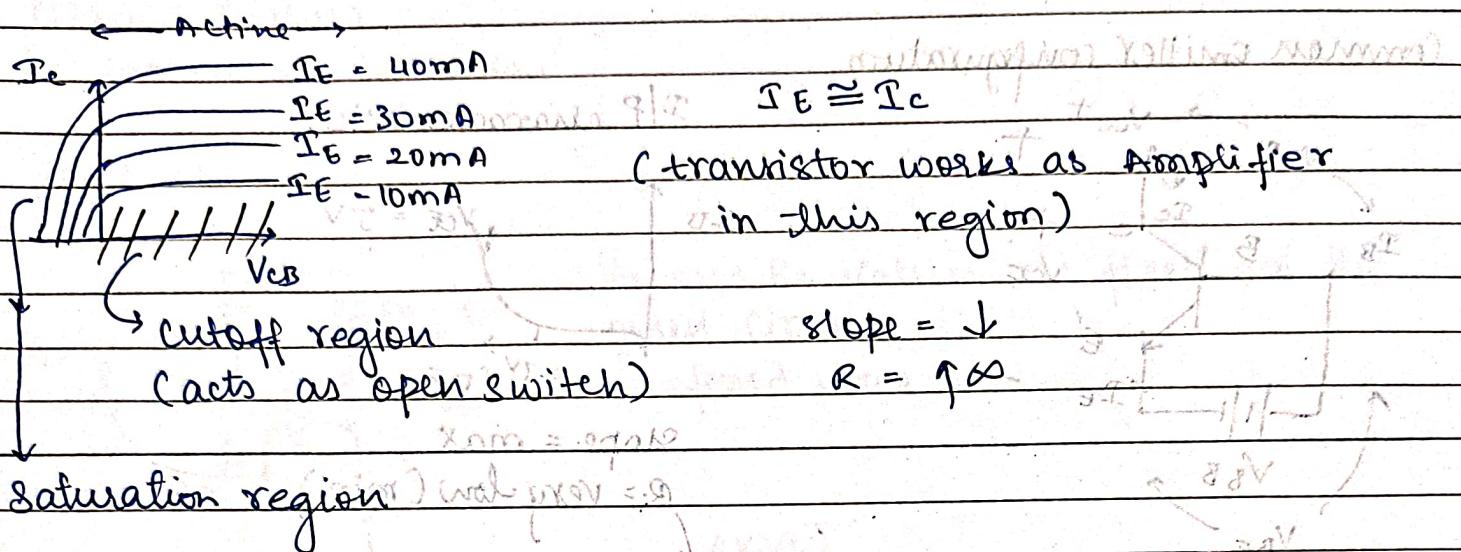
input characteristics: input current  $I_E$  vs input voltage  $V_{EB}$  keeping output voltage constant



if silicon

input resistance = min  
 $V_{EB} = \text{max.}$

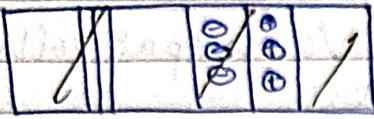
Output characteristics : output current vs. Output Voltage  
keeping input current constant.



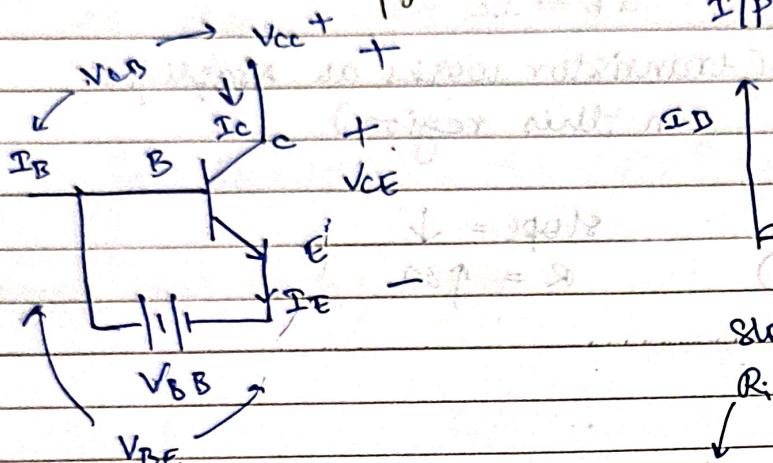
### Common Emitter Configuration

- punch through effect / Early effect / Base width modulation

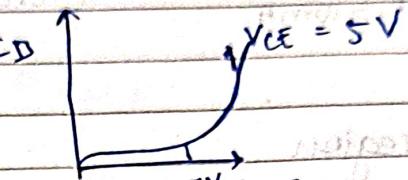
- when the RB voltage  $V_{CB}$  increases, the width of the depletion region increases which reduces base width.
- due to reduction in base width the concentration of charge carriers increases in the base region and this effect is called Early effect.
- when the reverse bias voltage  $V_{CB}$  in the common base region exceeds the value specified by the manufacturer, the CB depletion region penetrates deep into the base until it comes in contact with EB depletion region. this region is called Punch through. This leads to Break down & very large current flows through the device.



## Common emitter configuration



## I/P characteristics



slope = max

$R_s$  = very low (min)

$$I_{C(sat)} = f(V_{BE}) \quad | \text{saturation region}$$

$I_B = \text{constant}$

## O/P characteristics

active region

$$I_C = \beta I_B \quad | \text{active region} (\beta < 1, 50 \leq \beta \leq 500)$$

$\beta = 25 \text{ to } 500$

$$I_B = \text{constant} \quad | \text{saturation region}$$

$$I_C = \text{constant} \quad | \text{saturation region}$$

## Saturation

region (gradually increases then becomes constant)

(gradually increases then becomes constant)

slope  $\rightarrow$  small value

$$R_o = \frac{\Delta V_{CE}}{\Delta I_C} \quad | \text{middle about saturation region with small slope with respect to } I_C$$

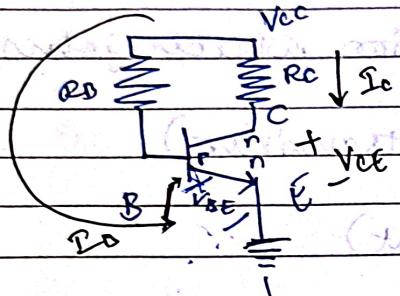
$I_B = \text{constant}$

## Transistor Biasing $\Rightarrow$

(1) Fixed Biasing

(2) Voltage divider Bias

(1) Fixed Bias



V<sub>cc</sub> and R<sub>b</sub> values are fixed for the given circuit.  $\therefore$  fixed bias

using Kirchoff's voltage law for input voltage (KVL)

$$V_{cc} - I_B R_B - V_{BE} = 0$$

$$I_B = V_{cc} - V_{BE} \quad \text{--- (1)}$$

$$I_C = \beta I_B \quad \text{--- (2)}$$

using KVL to output

$$V_{cc} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{cc} - I_C R_C \quad \text{--- (3)}$$

(have to use the eqns to plot the graph)

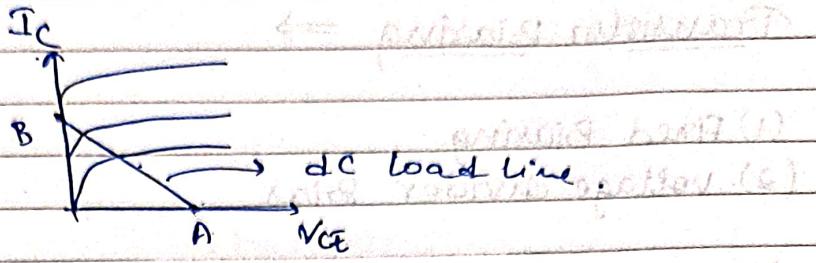
### DC load line

$$I_C = 0 \text{ in eqn } ③$$

$$V_{CE} = V_{CC} \rightarrow A$$

$$V_{CE} = 0 \text{ in eqn } ③$$

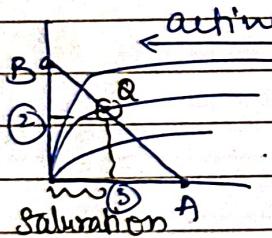
$$I_C = \frac{V_{CC}}{R_C} \rightarrow B$$



It is the straight line approximation which joins saturation point & cut off point.  
(in order to find the operating pt. of a transistor)

Operating point of a transistor ( $Q'$ - point)

the intersection of O/P characteristics of the transistor and DC load line.



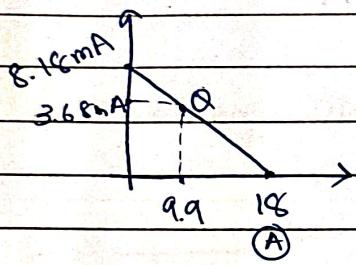
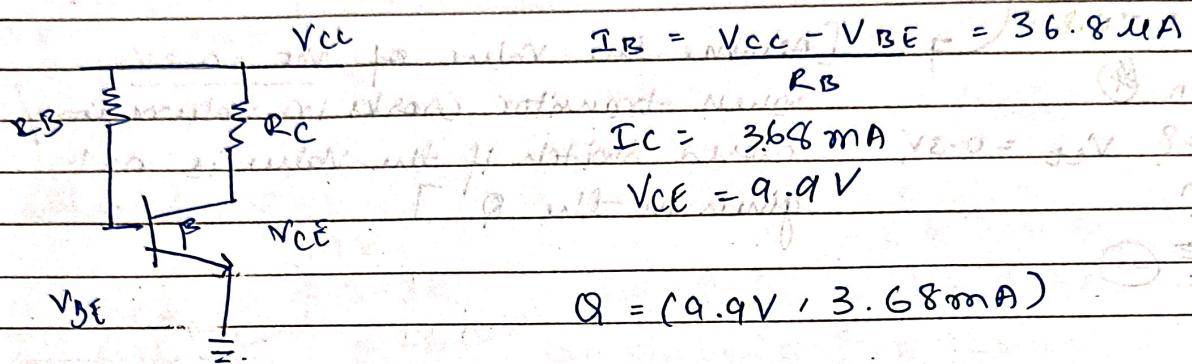
usually almost always at the center  
of DC load line  
(active region)

for faithful amplification

x coordinate  $\rightarrow$  eqn ③  $V_{CE} = V_{CC} - I_C R_C$

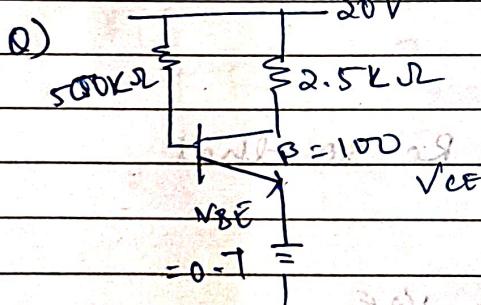
y coordinate  $\rightarrow$  eqn ②  $P_C = P_I B_A X$

- Q) for a fixed bias circuit find  $I_B$ ,  $I_C$ ,  $V_{CE}$  if  $R_C = 2.2k\Omega$   
 $R_B = 470k\Omega$ ,  $V_{CC} = 18V$ ,  $\beta = 100$ , silicon transistor is taken.  
 Draw the DC load line and find the operating point. ( $V_{BE} = 0.7V$ )



$$I_B = 20V - 0.7V = 38.6 \mu A$$

$$I_C = \beta I_B = 100 \cdot 38.6 \mu A = 3.86 mA$$

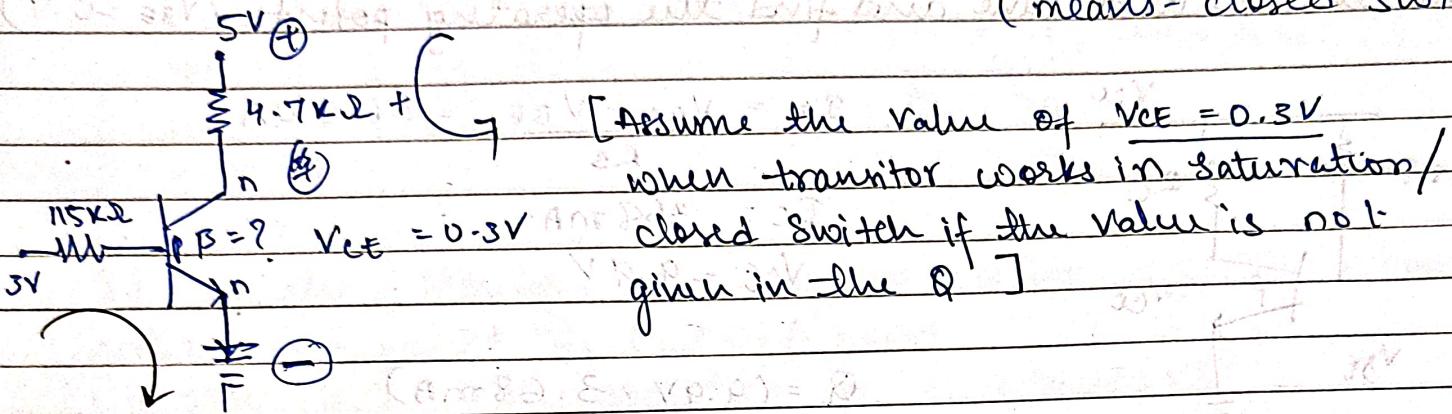


$$V_{CE} = 20V - 10.35V = 9.65V$$

$$\Rightarrow Q = (10.35V, 3.86mA)$$

$$V_{DE} = 0.7$$

Q) determine the min value of  $\beta$ . req. for a silicon transistor so that it works in saturation. (means - closed switch)



$$3V - I_B(115k\Omega) - V_{BE} = 0$$

$$I_B = \frac{3V - 0.7}{115k} = 20 \mu A$$

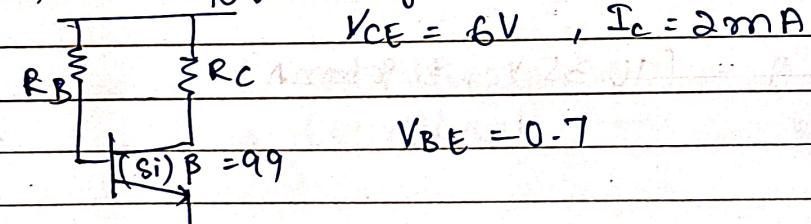
$$5V - I_C(4.7k) - V_{CE} = 0$$

$$I_C = 1mA$$

$$I_C = \beta I_B$$

$$\beta = \frac{I_C}{I_B} = 50$$

a) 10V design the values of  $R_B$  &  $R_C$  so that



$$V_{BE} = 0.7$$

$$I_B = \frac{V_{CC} - V_{CE}}{R_B}$$

$$I_C = \beta I_B$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$I_C = \beta I_B$$

$$\frac{2 \times 10^{-3}}{99} = I_B = 20 \mu A \times 10^{-3}$$

G

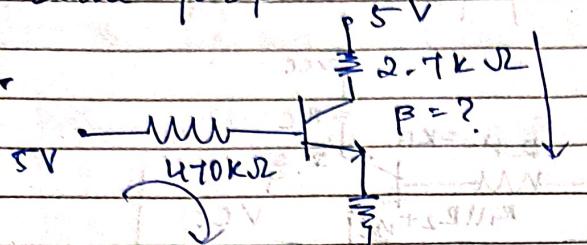
$$I_C R_C = V_{CC} - V_{CE}$$

$$R_B = 465 \times 10^3 \Omega$$

$$R_C = \frac{10 - 6}{2 \times 10^{-3}} = \frac{4}{2 \times 10^{-3}} = 2k\Omega$$

HW

a) solve for  $\beta$



$$\text{closed switch} \rightarrow V_{BE} = 0.7 \text{ V}$$

$$5 - I_D \cdot (470 \text{ k}) - 0.7 = 0$$

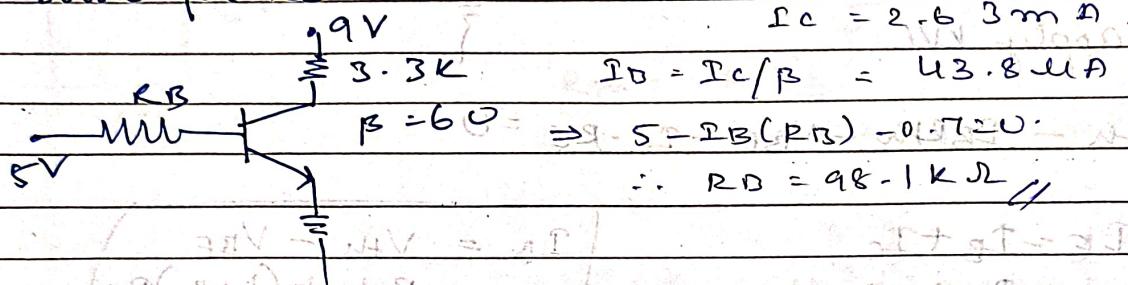
$$I_D = 7.1 \text{ mA}$$

$$5 - I_C \cdot (2.7 \text{ k}) - 0.3 = 0$$

$$I_C = 1.7 \text{ mA}$$

$$\beta = 1.7 \text{ mA} / 7.1 \text{ mA} = \underline{\underline{186}}$$

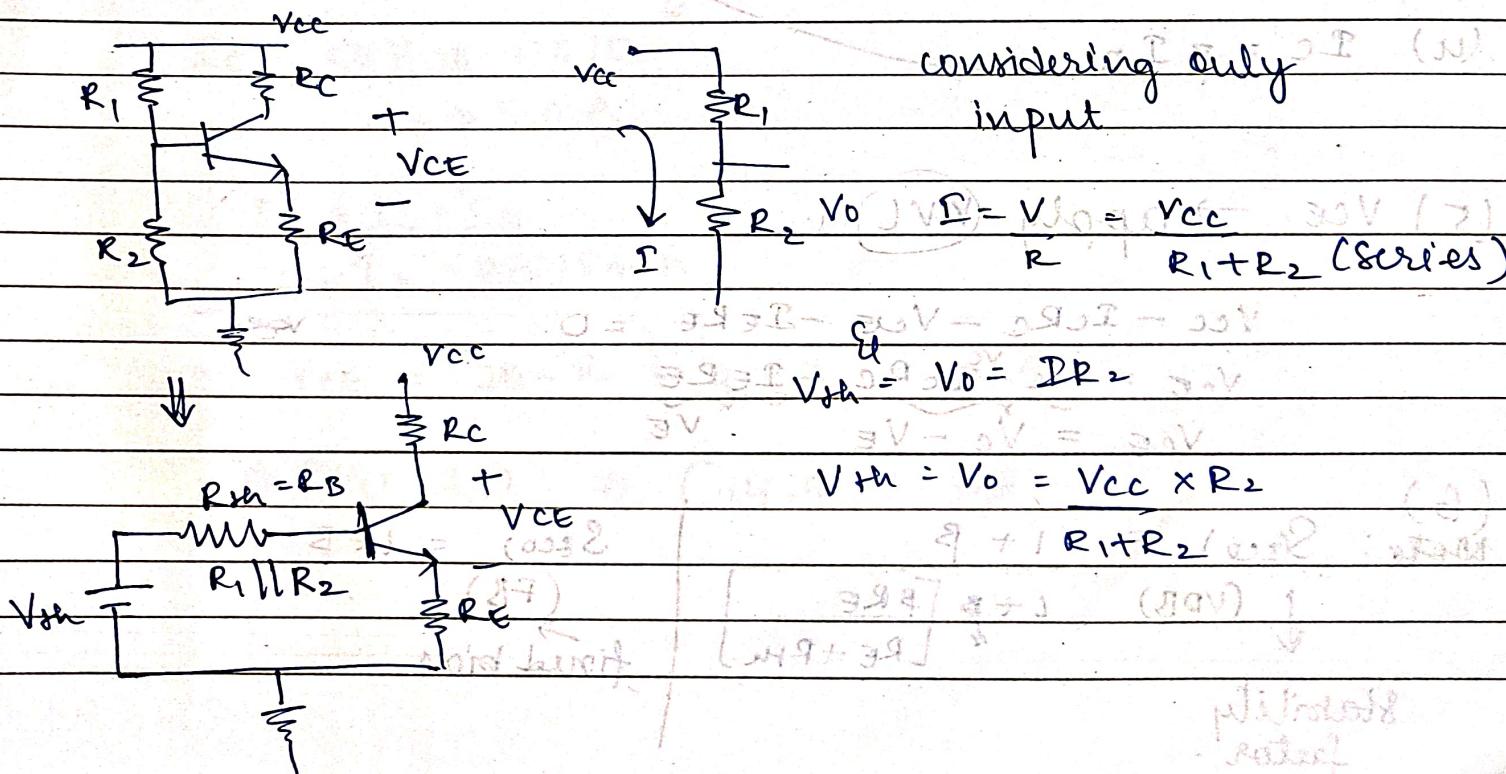
a) solve for  $R_B$



$$I_D = I_C / \beta = 43.8 \text{ mA}$$

$$\therefore R_B = 98.1 \text{ k}\Omega$$

(2) Voltage Divider Bias / Thevenin's theorem.



→ Design equations to find operating point (Q) of a transistor using Voltage divider Bias.

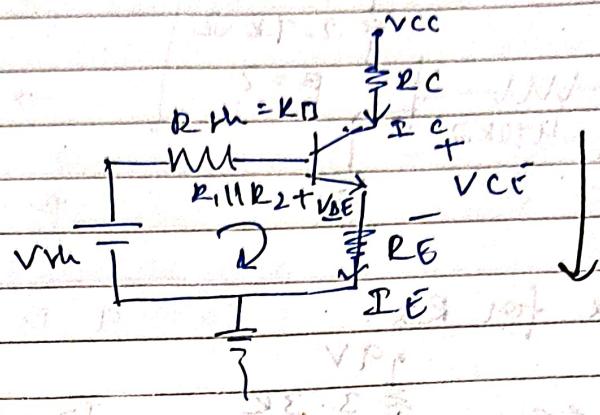
(steps)

$$(1) V_{Th} = \frac{V_{CC} \cdot R_2}{R_1 + R_2}$$

$$(2) R_{Th} = R_1 \| R_2$$

$$(3) I_B \rightarrow \text{apply KVL}$$

$$V_{Th} - I_B R_{Th} - V_{BE} - I_E \cdot R_E = 0$$



wkt,  
 $I_E = I_B + I_C$   
 $= I_B + \beta I_B$

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (1 + \beta) R_E}$$

$$I_E = (1 + \beta) I_B$$

$$(4) I_C = \beta I_B$$

$$(5) V_{CE} \rightarrow \text{apply KVL}$$

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - \underbrace{I_C R_C}_{V_C} - \underbrace{I_E R_E}_{V_E}$$

$$V_{CE} = V_C - V_E$$

$$(6)$$

$$\text{note: } S_{(IC0)} = \frac{1}{1 + \beta}$$

$$\downarrow (V_{DB}) \quad \frac{1 + \beta}{[R_E + R_{Th}]} [R_E]$$

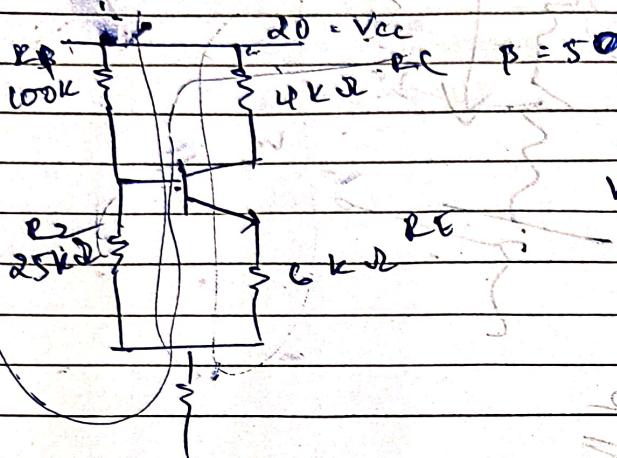
$$S_{(CO)} = 1 + \beta$$

$$(FB)$$

fixed bias

stability factor:

Q) find the operating point for voltage divider Bias. Assume the BJT to be silicon ( $V_{BE} = 0.7V$ )



$$V_{RE} = \frac{20 \times 25 \times 10^3}{100 \times 10^3 + 25 \times 10^3} = 4V$$

$$R_{RE} = \frac{R_1 R_2}{R_1 + R_2} = \frac{100 \times 25 \times 10^3}{100 \times 10^3 + 25 \times 10^3} = 20k\Omega$$

$$I_B = \frac{4 - 0.7}{20k\Omega + (1 + 50)6k\Omega} = \frac{3.3}{10^3(20 + 36)} = 10.1 \mu A$$

$$I_E = 0.0589 \times 10^{-3} A$$

$$I_C = 50 \times 10.1 \times 10^{-3} = 0.5mA$$

$$I_E = I_C + I_D$$

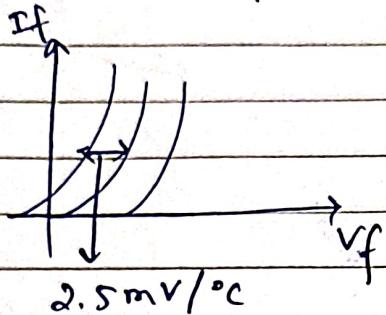
$$I_E = 0.515mA$$

$$V_{CE} = 20 - 2 - 3.09 = 14.9V$$

$$\text{Q: } (V_{CE}, I_C) \Rightarrow (14.9, 0.5mA)$$

## Thermal Stability

When temperature is increased the forward voltage shifts towards the left in  $2.5 \text{ mV}/^\circ\text{C}$ .



$$T \uparrow V_f \downarrow$$

$I_{CO}$  = Reverse saturation current  
(leakage current)

It measures how stable the  $\beta$ ,  $I_C$  and  $V_C$  remain when circuit temperature changes - Temp dependent / sensitive.

there are three temperature sensitive parameter.

- 1)  $I_{CO}$
- 2)  $V_{BE}$
- 3)  $\beta$

i) Affect of  $I_{CO}$  (Leakage Current)

The flow of current in the circuit produces heat at the junction. This heat increases the temperature. We know, minority carriers are temp. dependent and they increase with temperature.

The reverse saturation current doubles for every  $10^\circ\text{C}$  rise in temperature

$$I_C = \underbrace{\beta I_B}_{\text{majority carrier}} + \underbrace{(1+\beta) I_{CO}}_{\text{minority}}$$

## (2) Effects of $V_B$

•  $I_B$  depends on  $V_{BE}$

•  $I_C$  depends on  $I_B$

In turn  $I_C$  depends on  $V_{BE}$  (as  $I_C \propto (1 + \beta I_B)$ )

as  $I_C$  changes w.r.t temperature due to change in  
 $V_{BE}$   $I_C \uparrow T \uparrow V_{BE} \downarrow$

$$P_D = \frac{V_{BE}}{R_E} \cdot I_B = \frac{V_{BE}}{R_E} \cdot \frac{I_C}{\beta + 1} = \frac{V_{BE} I_C}{\beta + 1}$$

$$P_D = I_C \cdot V_{BE}$$

## (3) Effect of $\beta$ .

•  $\beta$  is temperature dependent.

• we know  $I_C = \beta I_B$ .

∴ as temp  $\uparrow$ ,  $T \uparrow \rightarrow \beta \uparrow$

## Bias Stabilisation (stability factor) ( $S_{I_C}$ )

• Stability factor indicates the degree of change in the operating point ( $Q$ ) due to variations in the temperature

① Stability factor is the ratio of  $S = \frac{\Delta I_C}{\Delta I_{C0}}$   $| \beta, V_{BE} \rightarrow \text{constant}$

②  $S = \frac{\Delta I_C}{\beta} | \Delta I_{C0}, V_{BE} \rightarrow \text{constant}$ .

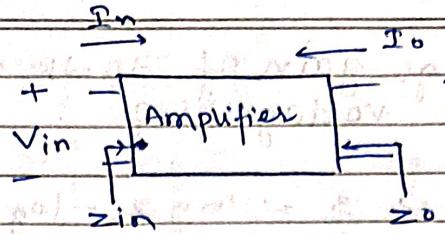
③  $S = \frac{\Delta I_C}{V_{BE}} | I_{C0}, \beta \rightarrow \text{constant}$ .

Fixed bias  $\Rightarrow$

$$S = 1 + \beta$$

$$\text{Voltage Divider Bias} \Rightarrow S = \frac{1 + \beta}{1 + \left[ \frac{\beta R_E}{R_E + R_m} \right]}$$

## Amplifiers



DECIBELS [dB]

For a small amount of input voltage we get a large amt.

$$[A_p]_{dB} = 10 \log \left[ \frac{P_o}{P_i} \right] = 10 \log \left[ \frac{V_o^2 / R}{V_i^2 / R} \right]$$

Gain = output quantity / I/P

$$[A_v]_{dB} = 20 \log \left[ \frac{V_o}{V_i} \right] = 20 \log \left[ \frac{V_o}{V_i} \right]$$

$$[A_i]_{dB}$$

$$A_p = \frac{P_o}{P_i} \quad A_v = \frac{V_o}{V_i}$$

$$[A_{VA}]_{dB} = 20 \log \left[ \frac{I_o}{I_i} \right] = 20 \log \left[ \frac{I_o}{I_i} \right]$$

Q) If the power gain of an amplifier is 20 dB. the input power required to obtain the output power of 100W is?

$$20 = 10 \log \left[ \frac{100}{P_i} \right] \quad 20 = 20 \log \left[ \frac{10}{P_i} \right]$$

$$10 = 10 - \log P_i = 1$$

$$\log P_i = 0$$

Ans: Power required is  $P_i = 1 \text{ W}$

Ans: Power required is  $V_{in} = 10V$  and current  $I_i = 10A$

Ans: The power required is  $A_{VA} = 100$

Q) An amplifier has voltage gain of 30 dB to obtain an output of 2V. the input voltage is?

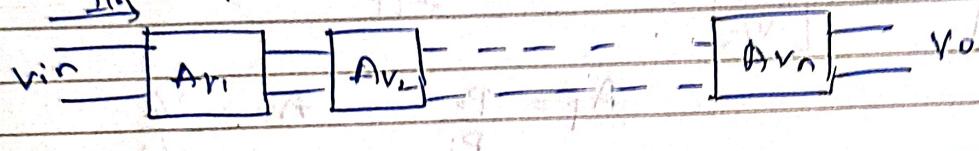
$$30 = 20 \log \left[ \frac{V_o}{V_i} \right] \Rightarrow \frac{V_o}{V_i} = 10^{\frac{30}{20}} = 10^{1.5}$$

$$10^{1.5} = 3.16$$

$$\log V_i = 0.8010 - 1.5$$

$$\log V_i = -1.1990$$

### Cascading of Amplifier



$$[Av] = Av_1 \times Av_2 \times \dots \times Av_n$$

$$[Av]_{dB} = [Av_1]_{dB} + [Av_2]_{dB} + \dots + [Av_n]_{dB}$$

Q) three voltage amplifiers are cascaded to provide an overall gain of 66 dB. if the first two amplifiers have gains of 40 dB & 20 dB respectively. The gain of 3rd stage amplifier is?

$$40 + 20 = 60 \text{ dB}$$

$$66 - 60 = 6 \text{ dB}$$

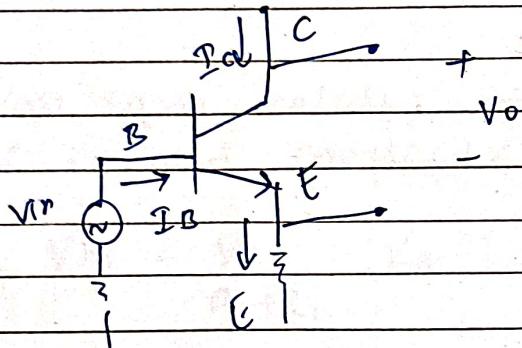
Q) the output of a cascaded chain of 3 voltage amplifier is 5V when the Vin is 1mV. if the voltage gains of 1st & 3rd stage amplifiers are 16 dB & 32 dB the voltage gain of 2nd stage amplifier is?

$$[Av] = 10 \log \left[ \frac{5}{10^{-3}} \right]^2$$

$$\Rightarrow 20 \left[ \log 5 - \log 10^{-3} \right]$$

$$\Rightarrow 20 [0.6990 + 3]$$

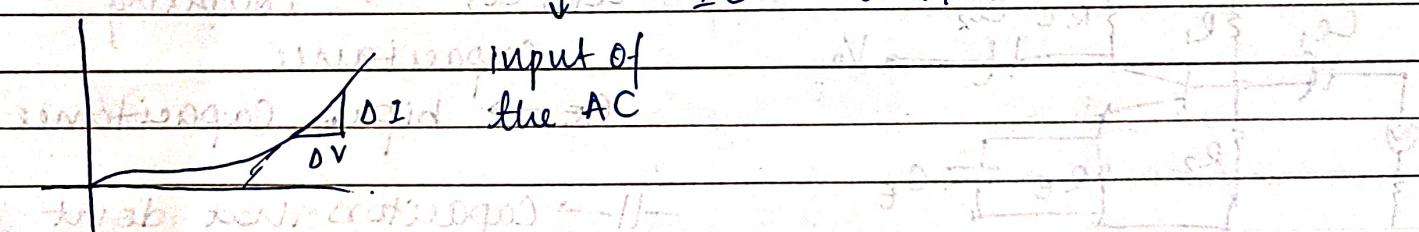
### Small Signal Equivalent



$r_e$  model - conversion of physical circuit  $\rightarrow$  electrical model.

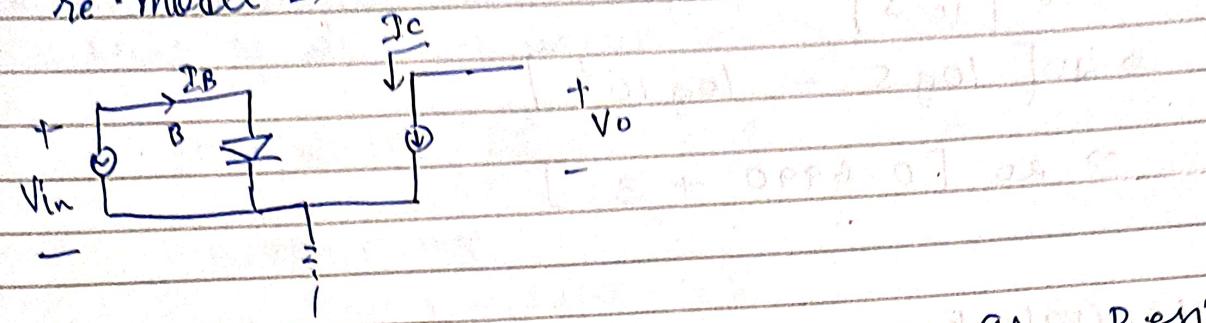
small letter for b, e, c due to AC Source  
capital letter for B, E, C due to DC Source

Dynamic resistance  $r_e = 26mV$  measured between base and emitter  
 $I_e \rightarrow$  emitter current.



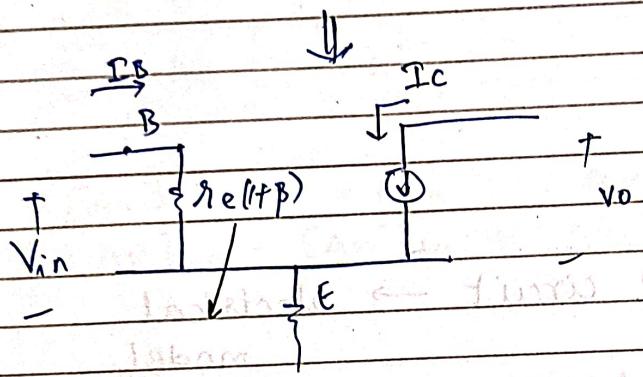
slope.

Re-model  $\Rightarrow$



when AC source  $\rightarrow$  Diode as a resistor

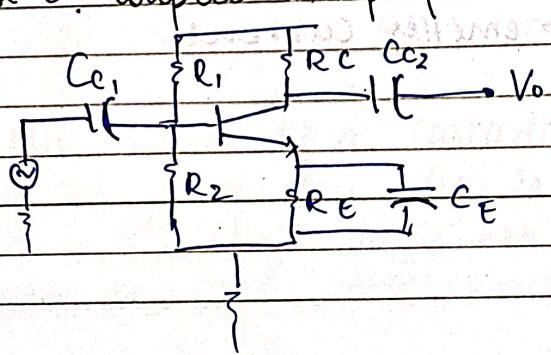
then the equivalent circuit



through the resistor both  $I_B$  &  $I_E$  flows through

$$I_E = (1+\beta)I_B$$

R.C. coupled Amplifier



$C_{c1}, C_{c2} \rightarrow$  coupling

Capacitance.

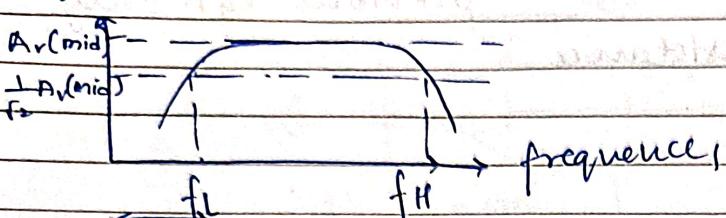
$C_E \rightarrow$  bypass Capacitance

-|| → Capacitors that don't have polarity

+| - passes polarity.

## Frequency response.

$G_{AV}(Av)$



$C_A, C_C, C_E$

Design eqns. related to  
RC coupled amplifier.

$$1. V_{TH} = \frac{V_{CC} \cdot R_2}{R_1 + R_2}$$

$$2. R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

$$3. I_D = \frac{V_{TH} - V_{BE}}{R_m + (1+\beta)R_E}$$

$$4. P_C = \beta I_D^2$$

$$5. I_E$$

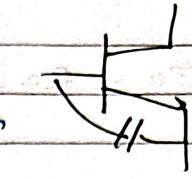
$$6. V_{CE} = V_C - V_E$$

$$7. Q\text{-point } (V_{CE}, I_C)$$

$$a. Z_{in} = R_m \parallel (1+\beta)R_E r_e$$

$$b. Z_{out} = R_C \parallel (1+\beta)R_E r_e$$

$$11. Av = -\frac{R_C}{r_e}$$



internal capacitor,

Junction capacitor.

at higher frequencies due to capacitive reactance decreases so the internal/junction capacitors come into play which are parallel to Junction (PN). This reduces  $V_o$  as a result  $[Av]$  drops.

frequency gain deviates at higher frequency side.

lower freq. side

Considering load Resistance.

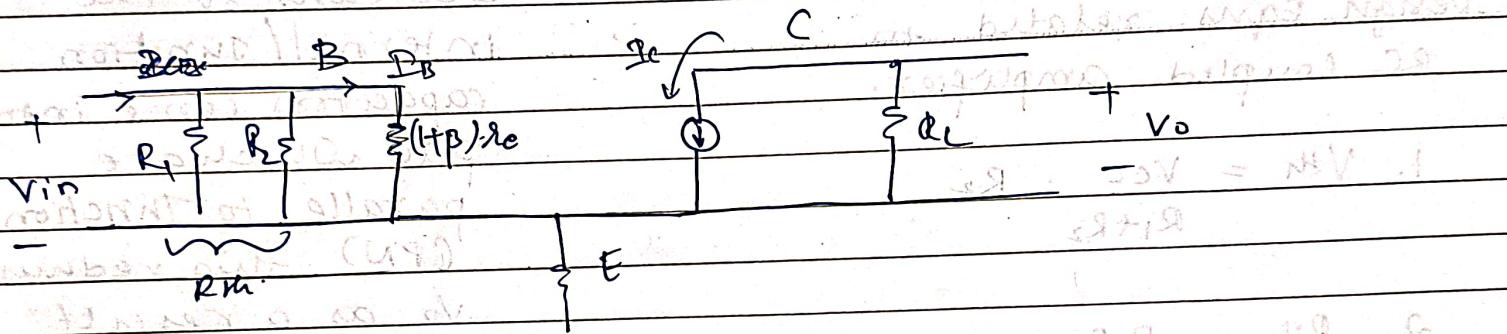
$$Z_0 = R_C \parallel R_L$$

↳ load resistance

$$\Delta V = -R_C \parallel R_L$$

$R_E$

Small signal Equivalent for RC coupled amplifier.



$$\text{Bandwidth} = BW = f_H - f_L$$

$$\text{Gain at cut-off} \Rightarrow Av = \frac{1}{\sqrt{2}} Av_{\text{mid}}$$

- Q) an amplifier has a bandwidth of 500 kHz. if the lower cut-off freq. is 25 Hz what is the upper cut-off freq? Also find the voltage gain at lower cut off freq. if the mid band gain is 120.

$$1. 500 \text{ kHz} = f_H - 25$$

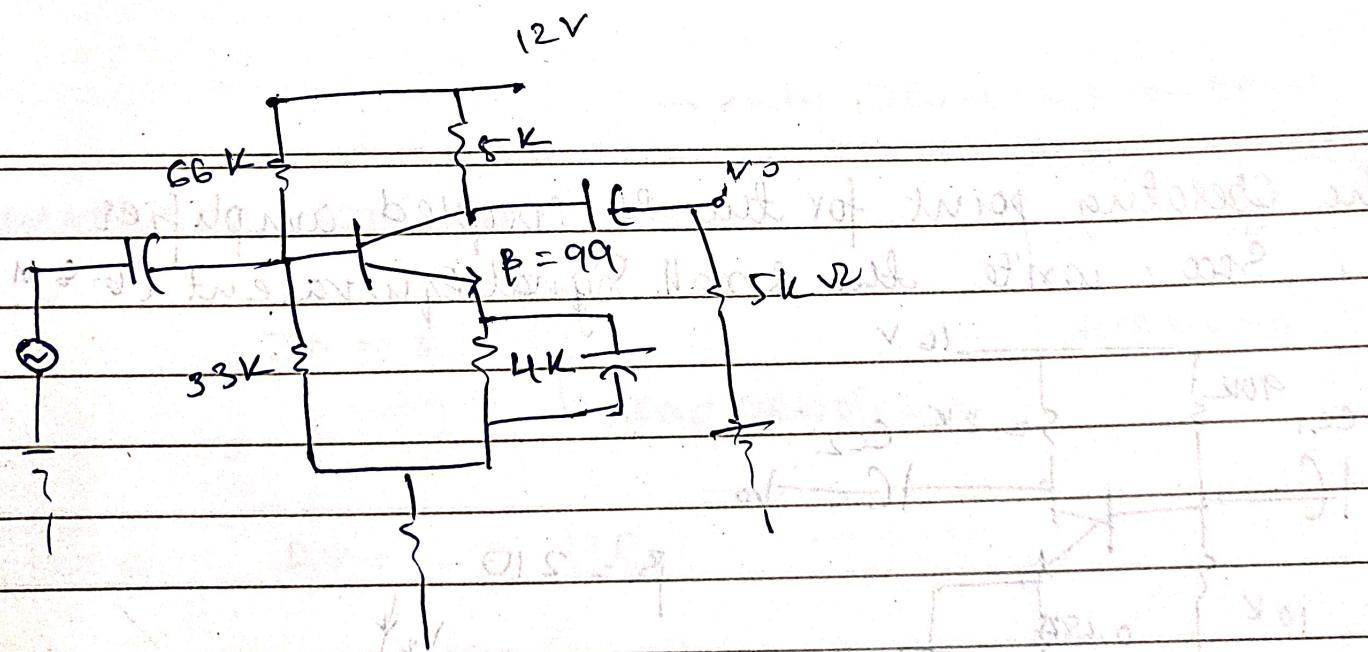
$$500 \times 10^3 + 25 = f_H$$

$$500025 = f_H$$

$$Av = \frac{1}{\sqrt{2}} \times 60 \times r_2 / \sqrt{2}$$

$$Av = 60\sqrt{2}$$

$$= 84.85$$



$$V_{TH} = \frac{12}{10^3(66+33)} \times 33K = UV$$

$$R_{TH} = \frac{66K \times 33K}{99} = \frac{2178 \times 10^3}{99} = 22K$$

$$V_m = 4$$

$$R_m = 22k$$

$$I_D = \frac{V_m - V_{BE}}{R_m + (1+\beta)R_E} = \frac{4 - 0.7}{22k + 400k} = 7.8mA$$

$$I_C = 99 \times 7.8mA = 0.77mA$$

$$I_E = 100 \times 7.8mA = 0.78mA$$

$$\begin{aligned} V_{CE} &= V_{CC} - I_C R_C - I_E R_E \\ &= 12 - 3.85 - 3.12 = \underline{\underline{5V}} = V_{CE} \end{aligned}$$

$$\begin{aligned} S_{IO} &= \frac{1+\beta}{1+\left[\frac{BRE}{R_m+R_E}\right]} = \frac{100}{1+\left[\frac{99 \times 4 \times 10^3}{10^3(22+4)}\right]} = \frac{100}{1+15.2} \\ &= \frac{100}{16.2} = 6.17 // \end{aligned}$$

$$r_e = \frac{26 \times 10^{-3}}{0.78mA} = 33.3 \Omega$$

$$z_{in} = R_m \parallel (1+\beta) r_e$$

$\frac{1}{22k} \quad \frac{100 \times 33.3}{100 \times 33.3} = 3.33k$

$$\cancel{\frac{22k \times 3.33k}{22+3.33}} = 2.9k\Omega$$

$$Z_o = R_C \parallel R_L = \frac{5k \times 8k}{5k+8k} = 2.5k\Omega$$

$$\Delta V = -\frac{2.5k}{33.3} = -75.1//$$

Small signal equi.

