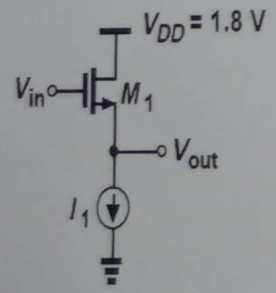
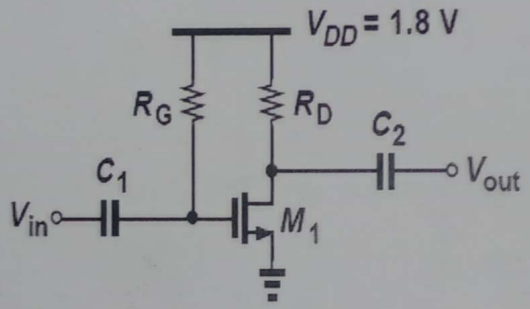
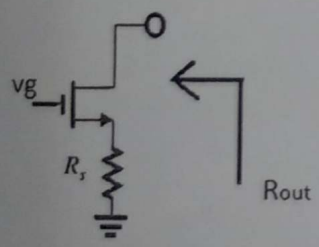
RV College of Engineering®
Mysore Road, RV Vidyaniketan Post,
Bengaluru - 560059, Karnataka, India

NBA Accredited (UG - 6 Years)

Department of Electronics & Communication Engineering

Date: 21-10-2024	Quiz - 1	Max. Marks: 10
Semester: 03	UG	Duration: 20 Mins
Course: Analog Microelectronic circuits		Code: EC233AI

No	Part A	M	BT	CO
	The power budget of the circuit shown in fig 1.1 should be 2mW and the output impedance should be 50Ω. The transistor has $Kn' = 200\mu A/V^2$ with no CLM. Find the aspect ratio of the transistor to achieve the required output impedance.  Fig 1.1  Fig 1.2	2	2	1
	Determine the current for the circuit shown in fig 1.2. The requirements are as below: Maximum voltage gain is to be achieved but with an aspect ratio less than 277.78. The maximum output impedance should only be 500Ω. Assume Vt=0.4V and no CLM.	2	2	1
	For the circuit given in Fig.1.3, if Vov =2V, I_D=2mA, V_A =100V, R_s=20kΩ, the exact output impedance of the circuit is = _____.  Fig.1.3	2	2	2
	Calculate the gain of a CS amplifier with current source load. Assume NMOS M1 behaves as the amplifier device and PMOS M_2 behaves as a current source load. r_{o1} = 10kΩ, r_{o2} = 10kΩ, g_{m1} = 2mA/V g_{m2} = 2mA/V.	2	3	2
	In enhancement type NMOS operating in saturation mode, drain current is found to be 2 mA when V_{DS}=4V is applied. Considering channel length modulation, find the modulation factor λ if drain current is found to be 2.05 mA for V_{DS}=5V while keeping V_{GS} as constant.	2	2	1

RV College of Engineering®
Mysore Road, RV Vidyaniketan Post,
Bengaluru - 560059, Karnataka, India

NBA Accredited (UG - 6 Years)

Department of Electronics & Communication Engineering

ate: 21-10-2024	**Test - 1**	**Max. Marks: 50**
emester: 03	**UG**	**Duration: 90 Mins**
ourse: Analog Microelectronic circuits		**Code: EC233AI**

No		Part B	M	BT	CO
.	a	A circuit as shown in the Fig. 1a is connected and the transistor parameters are as given below: $\frac{w}{l} = \frac{20}{0.18}$, $\lambda = 0.1\,v^{-1}, Kn' = 200\mu A/V^2$, $V_t = 0.4V$. Find the voltage gain of the circuit.	5	2	1
	b	For the amplifier shown in Fig. 1b, find aspect ratio to achieve a voltage gain of 5 and output impedance of 1KΩ. The transistor is biased such that it operates 100mV away from the triode region. The capacitors used are very large and Gate resistance used is 1MΩ. Let $Kn' = 200\mu A/V^2$ and λ=0.	5	2	1
2.		For the circuit shown in Fig 2 draw a small signal model and derive equations for voltage gain and output impedance by considering Channel length modulation.	10	3	2
3.		For the circuit of CS amplifier with source degeneration given in Fig.3, determine I_D, g_m,r_o, mid frequency gain vo/vi, vo/vs, R_{in} and R_{out}. Given that, K_n' W/L =2 mA/V², Vt=1V, V_{DD}=15V and V_A=24V.	10	1	2

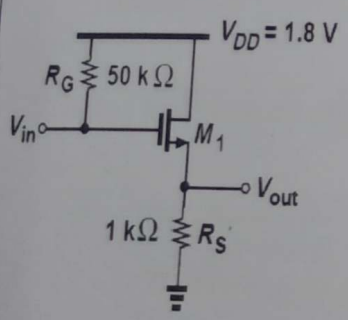


Fig. 1 a

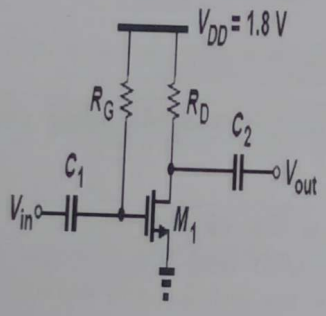


Fig. 1b

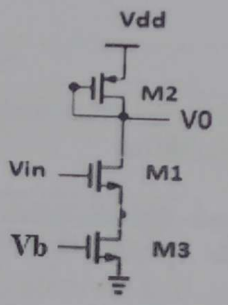


Fig. 2

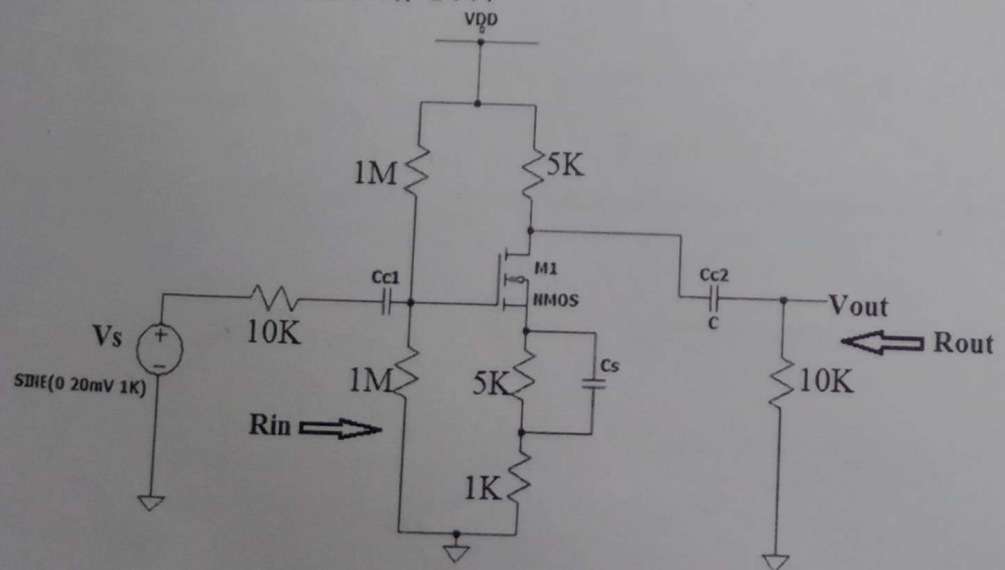


Fig. 3

4.	a	Design the circuit given in Fig. 4a to obtain a current I_D of 80 μA. Find the value for R and the dc voltage V_D. Let the nMOS transistor have Vt= 0.6 V, K_n'=200μA/V², L=0.8 μm, and W = 4 μm. Neglect the channel length modulation effect.	5	

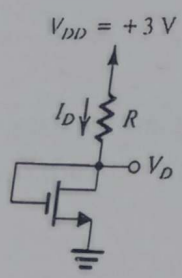


Fig. 4 a

	b	Explain with a neat sketch and equations how a MOSFET exhibits finite output resistance in Saturation.	5	2
5		The NMOS and PMOS transistors in the circuit of Fig. 5 are matched with $Kn'(Wn/Ln) = Kp'(Wp/Lp) = 200\mu A/V^2$ and Vtn = -Vtp= 1V. Assuming λ=0 for both devices, find the drain currents i_{DN} and i_{DP} and the voltage Vo for V_I = 0V, 2.5 V and -2.5 V	10	3

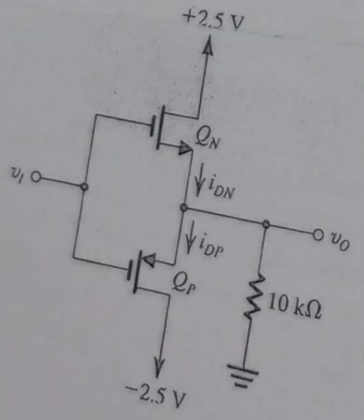


Fig. 5

Date:	Quiz - 1	Max. Marks: 10
Semester: 03	UG	Duration: 20Mins
Course: Analog Microelectronic circuits		Code:EC233AI

SCHEME & SOLUTIONS

S No	Solutions with Scheme	Marks
1.	Aspect ratio = 900	02
2.	Id max = 0.8mA	02
3.	Output impedance = ro+Rs+gmroRs= 2.07MOhm	
4.	Av= -10	
5.	λ=0.0277 V^{-1}	

S No	Solutions with Scheme	Marks
1. a	Id= 1.08mA --- (02) gm = 0.66mS, --- (01) r0=9.2K --- (01) Av = 0.372 -- (01)	05
b	gm=5mS –(01) Vd=1.5V – (02) Id=0.3mA --(01) aspect ratio= 208 --(01)	05
2.	Small signal model — (02) Deriving equation for voltage gain — (05) $Av = \frac{-gm1 * ro1 * (\frac{1}{gm2} \| ro2)}{ro3 + gm1(ro3)(ro1) + ro1 + (\frac{1}{gm2} \| ro2)}$ Deriving equation for output impedance — (03) $Rout = (ro3) + gm1(ro3)(ro1) + ro1$	10
3.	ID=0.923mA —--2M small signal model —--1M gm= 1.92m, r0= 26k —---2M Av= vo=/vi= -gmRDro/(r0+RS+RD+gmroRS) = -3 —---2M Avs= vi/vs=500k/510k = 0.98 —---1M Rout = 76.92K –1M Rin = 500K --- 1M	
4. a	Vov=0.4 V, VD=1V, R=25 KΩ	
4. b	Derivation of ID equation for CLM —--- 3M Sketch of CLM —---- 1M Output impedance —--- 1M	
5	vI=0V: idn= 0 mA, idp = 0 mA, v0 = 0V; ..... 3 M vI=2.5V: idn= 0.104 mA, idp = 0 mA, v0 = 1.04 V; ..... 3 M vI=-2.5V: idn= 0 mA, idp = 0.104 mA, v0 = -1.04 V; ..... 3 M Circuit diagram and analysis for three different cases ..... 1 M	

	Test - 1	Max. Marks: 5
Date:	UG	Duration: 90 M
Semester: 03		Code: EC233A
Course: Analog Microelectronic circuits		

Part B

S No		M	
1. a	A circuit as shown in the Fig. 1a is connected and the transistor parameters are as given below: $\frac{w}{l} = \frac{20}{0.18}$, $\lambda = 0.1\,v^{-1}, Kn' = 200\mu A/V^2$, $V_t = 0.4V$. Find the voltage gain of the circuit.	5	
b	For the amplifier shown in Fig. 1b, find aspect ratio to achieve a voltage gain of 5 and output impedance of 1KΩ. The transistor is biased such that it operates 100mV away from the triode region. The capacitors used are very large and Gate resistance used is 1MΩ. Let $Kn' = 200\mu A/V^2$ and λ=0.	5	
2.	For the circuit shown in Fig 2 draw a small signal model and derive equations for voltage gain and output impedance by considering Channel length modulation.	10	
3.	For the circuit of CS amplifier with source degeneration given in Fig.3, determine I_D, g_m, r_o, mid frequency gain Vo/Vi, Vo/Vs, Rin and Rout. Given that, K_n' W/L =2 mA/V², Vt=1V, V_{DD}=15V and V_A=24V.	10	

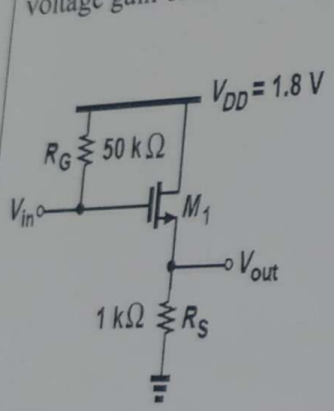


Fig. 1 a

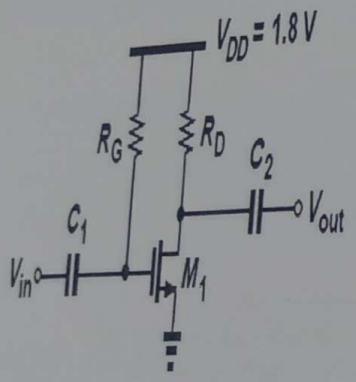


Fig. 1b

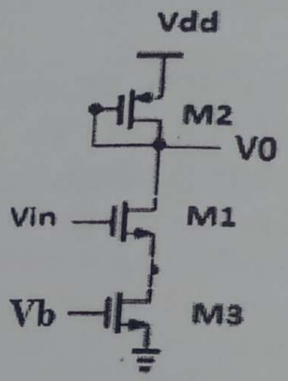


Fig. 2

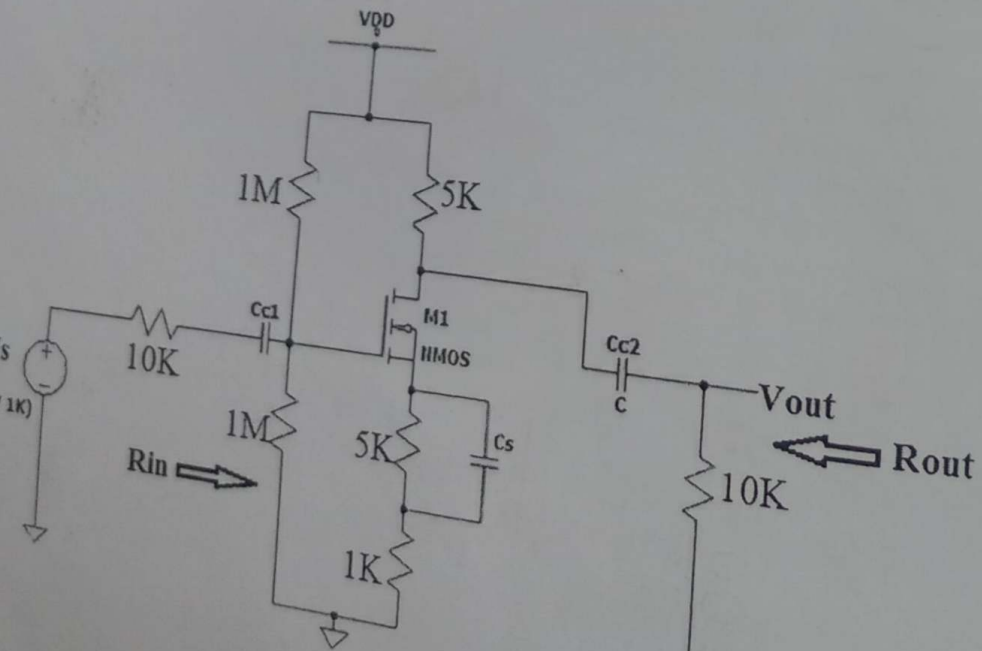
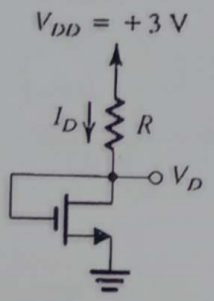
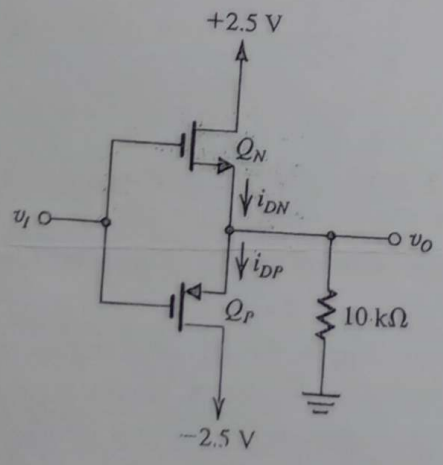


Fig. 3

a	Design the circuit in Fig. 4a to obtain a current I_D of 80 μA. Find the value of R and the dc voltage V_D. Let the nMOS transistor have Vt= 0.6 V, K_n'=200μA/V², L=0.8 μm, and W = 4 μm. Neglect the channel length modulation effect.  Fig. 4 a	5	2	1
b	Explain with a neat sketch and equations how a MOSFET exhibits finite output resistance in Saturation.	5	2	2
	The NMOS and PMOS transistors in the circuit of Fig. 5 are matched with $Kn'(Wn/Ln) = Kp'(Wp/Lp) = 200\mu A/V^2$ and Vtn = -Vtp= 1V. Assuming λ=0 for both devices, find the drain currents i_{DN} and i_{DP} and the voltage Vo for V_I= 0V, 2.5 V and -2.5 V  Fig. 5	10	3	1