CS152B: Digital Design Project Laboratory MW 12:00PM-1:50PM @ BH 3436	TA: Babak Moatamed babakm@cs.ucla.edu

Course Objectives

1. Develop expertise using the Verilog hardware description language.
2. Familiarize yourself with the Xilinx software and simulation environment.
3. Develop an understanding of FPGA architecture and applications.
4. Use the Xilinx system builder to design embedded systems using the MicroBlaze platform.

Assignments & Schedule (Tentative)

Assignment	**Percent**	**Due Date (soft deadline)**
Lab 0: ISE Introduction	10%	Week 1 (F)
Lab 1: ALU Design	10%	Week 3 (F)
Lab 2: State Machine Design	10%	Week 5 (F)
Lab 3: EDK Introduction + Serial Communication	10%	Week 6 (F)
Exam: FPGA Applications + Verilog HDL	20%	Week 8
Lab 4: Final Project + Presentation	30%	Week 10
Participation + Attendance	10%	

Project Submission

When you have completed your lab assignment, please inform your TA and your work will be checked off. The four labs, as well as the final project, must be accompanied by a written report (one per group). Please submit your report CCLE by the date the project is due. It is suggested to keep your reports brief. Your lab assignments will be graded on the following criteria:

Item	**Points**
Implementation: Project functions correctly, as verified by the demo. Project accurately meets specifications.	50%
Report: Your report answers all the questions in the lab handout, and includes relevant schematics, waveforms, and Verilog code. Your report should also include a description of the major components of the system and any challenges you faced.	25%
Test: If applicable, your project is verified with a testbench or test plan which considers different use cases. The report includes the test description and output waveforms (if necessary).	15%
Participation: Both group members participated equally in the design and were present for the project demo. Each partner's contribution is listed in the lab report.	10%

Lab Guidelines

Lab equipment must be kept in the locker when not in use. Make sure you use the power supplies provided (and not your laptop power supply). Professional and courteous behavior is expected during the lab at all times.

Academic Integrity

Please be mindful of University policies with respect to cheating and plagiarism. Please do not use course materials from previous quarters. These include previous exams, project solutions, or code fragments.

Room Access + Resources

Every team should have one access card to the laboratory (one per group), which will allow you to enter the lab during non-class hours. Please see the Access-Card document on CCLE for more specific instructions. Since lab resources are shared, it is important to backup all of your work on USB drives or DropBox. Otherwise, your files could be deleted by other students.