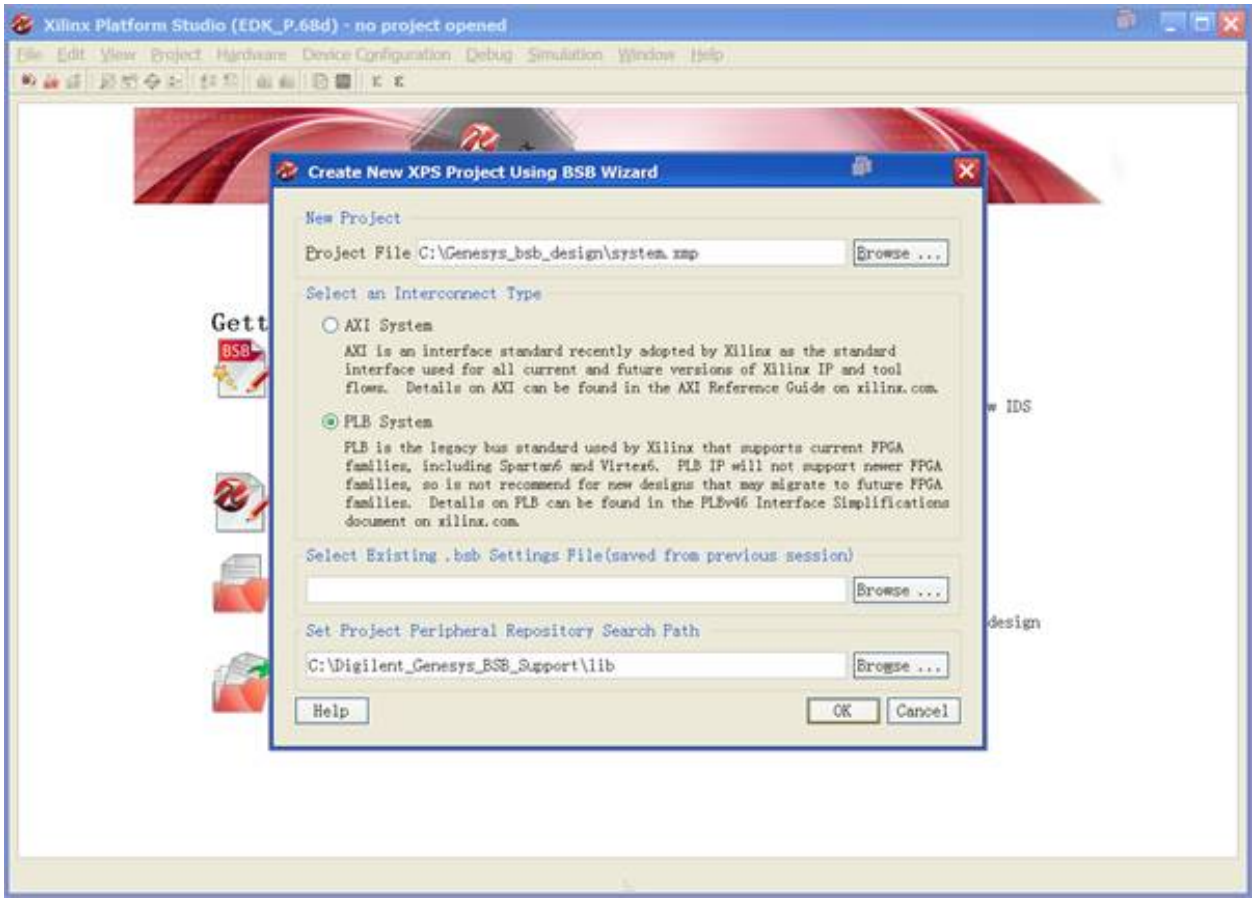
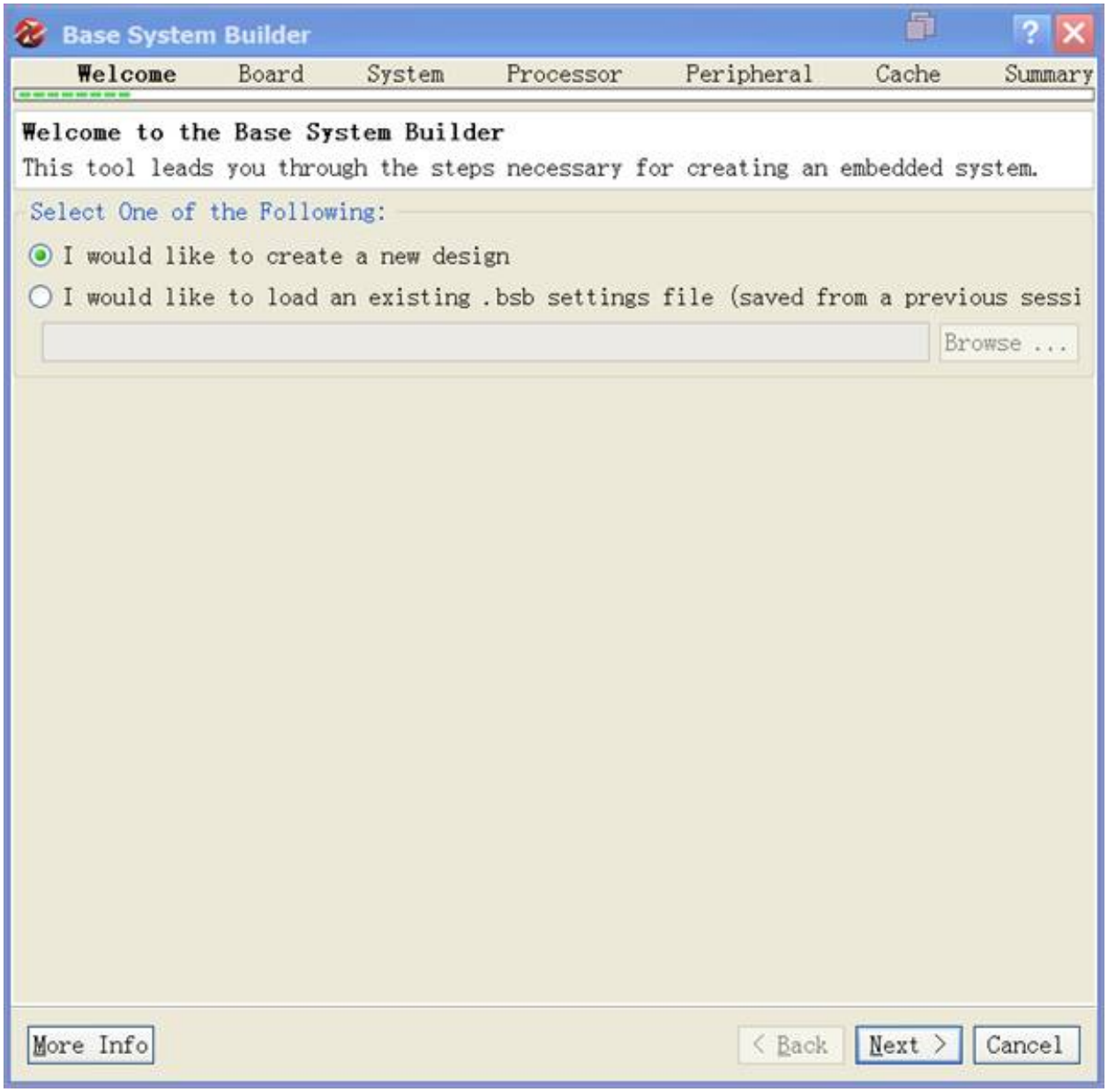
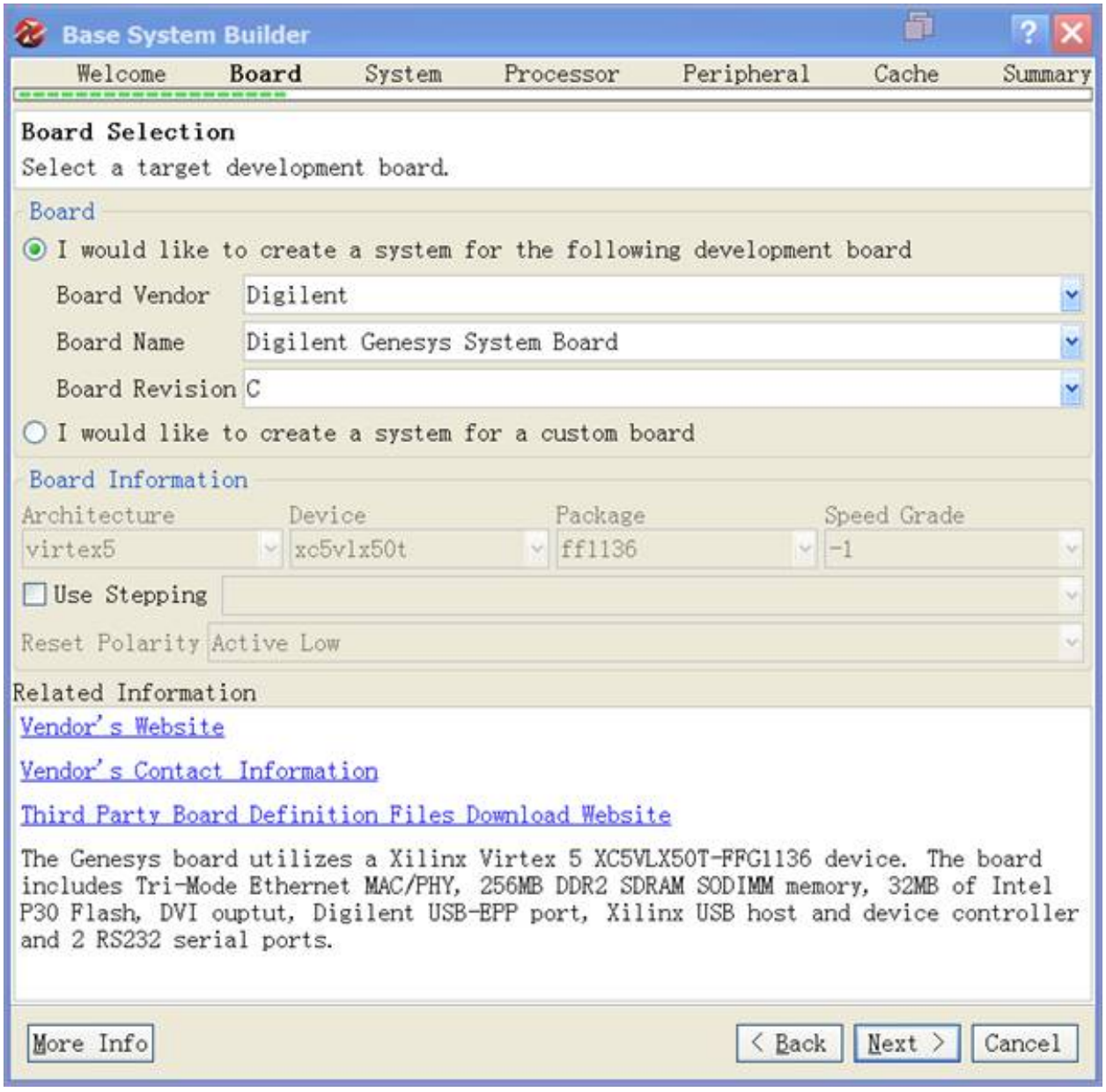
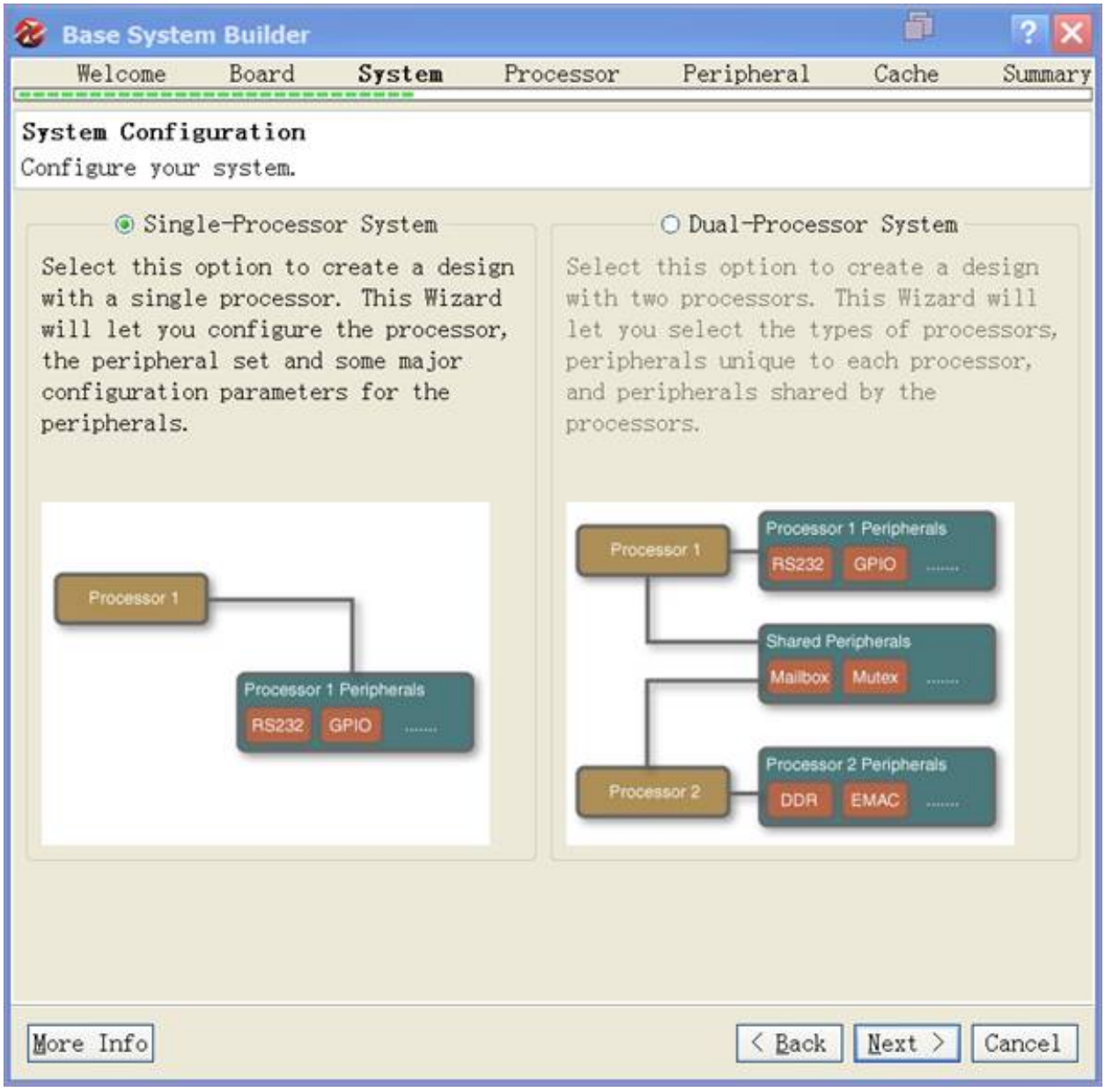
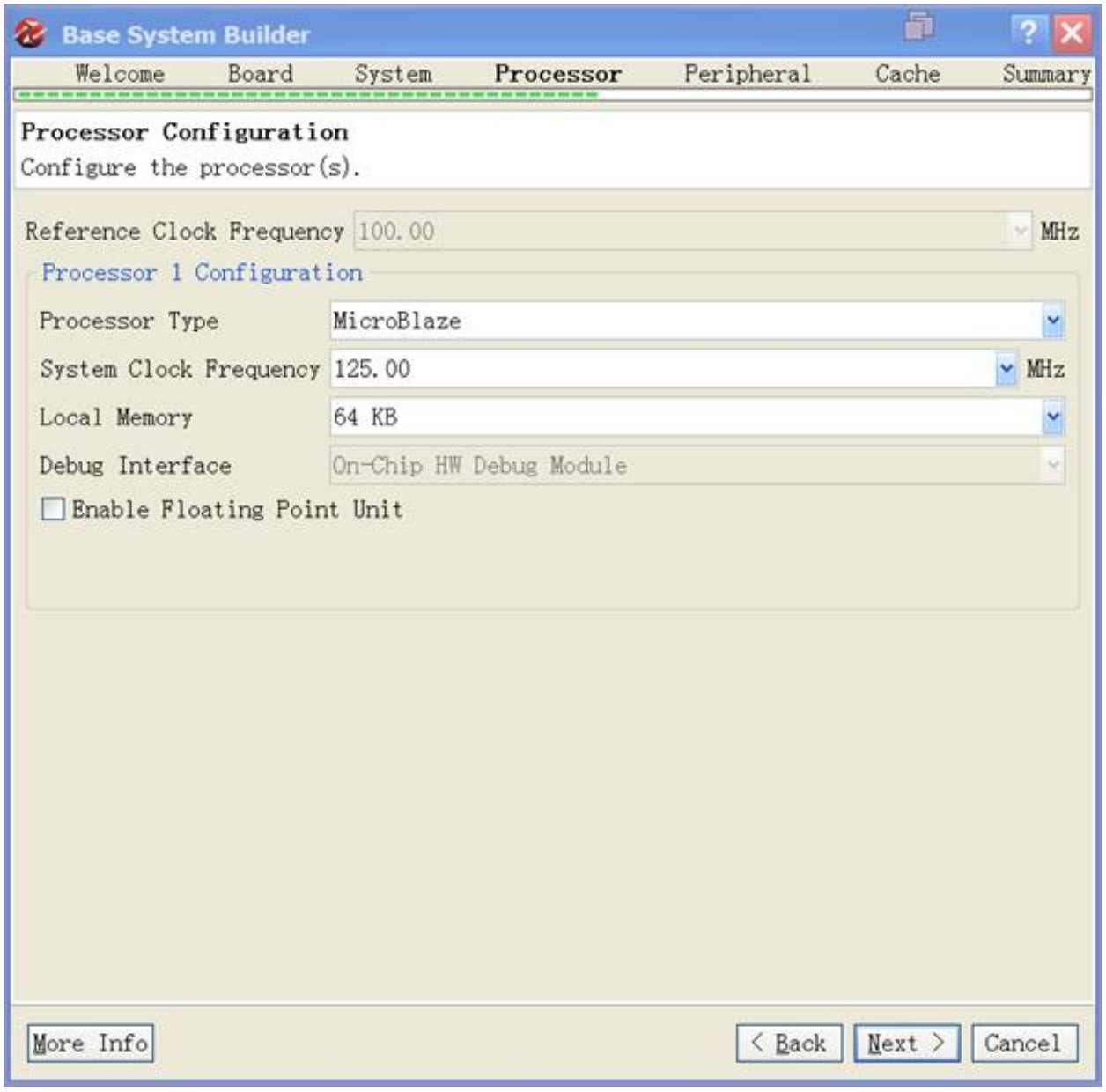
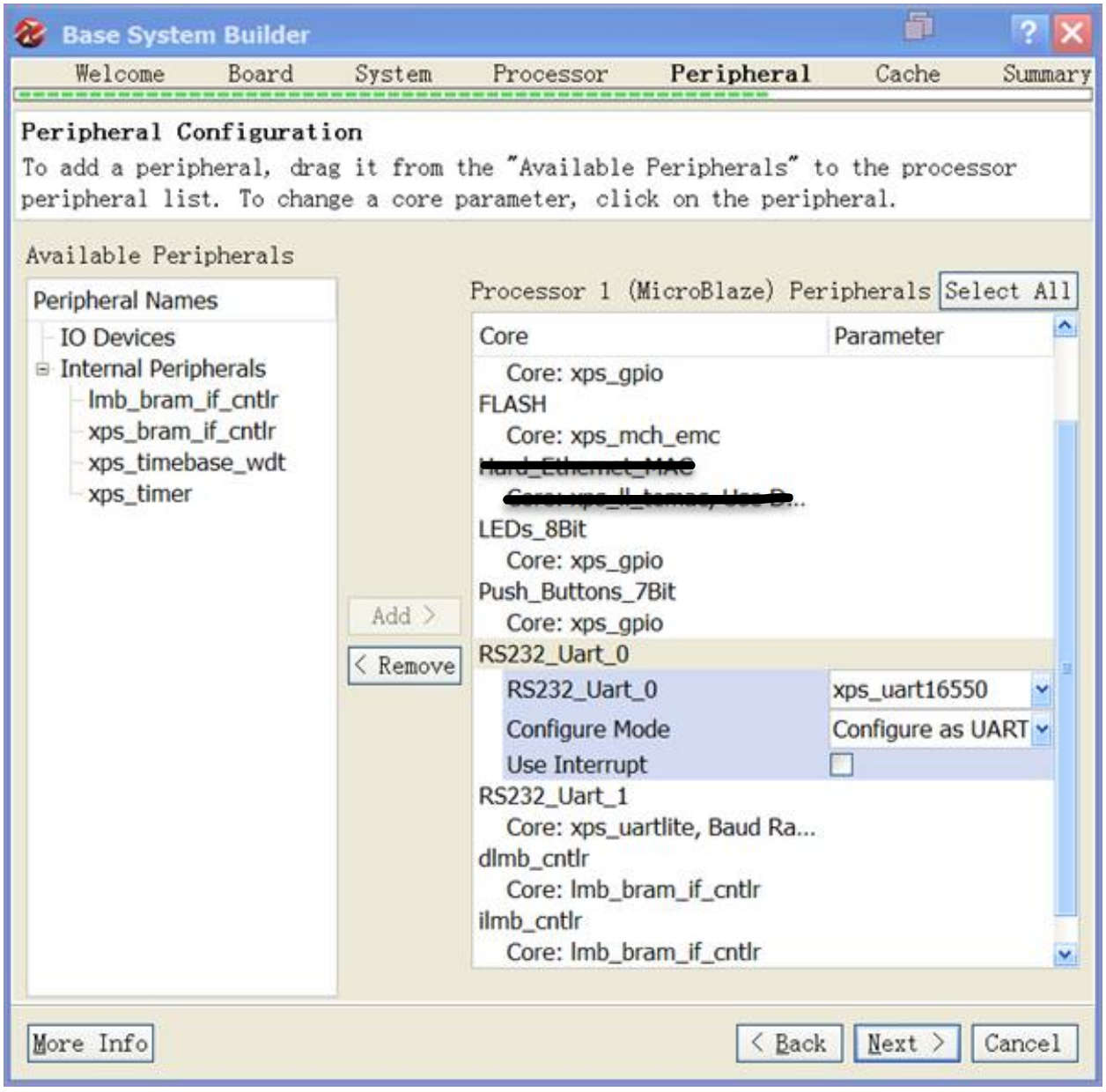

Xilinx Platform Studio (EDK_P.68d) - no project opened
File Edit View Project Hardware Device Configuration Debug Simulation Window Help
Create New XPS Project Using BSB Wizard
New Project
Project File C:\Genesys_bsb_design\system.xmp
Browse ...
Select an Interconnect Type
AXI System
AXI is an interface standard recently adopted by Xilinx as the standard interface used for all current and future versions of Xilinx IP and tool flows. Details on AXI can be found in the AXI Reference Guide on xilinx.com.
PLB System
PLB is the legacy bus standard used by Xilinx that supports current FPGA families, including Spartan6 and Virtex6. PLB IP will not support newer FPGA families, so is not recommend for new designs that may migrate to future FPGA families. Details on PLB can be found in the PLBv46 Interface Simplifications document on xilinx.com.
Select Existing .bsb Settings File(saved from previous session)
Browse ...
Set Project Peripheral Repository Search Path
C:\Digilent_Genesys_BSB_Support\lib
Browse ...
Help
OK
Cancel
Gett
BSB
w IDS
design

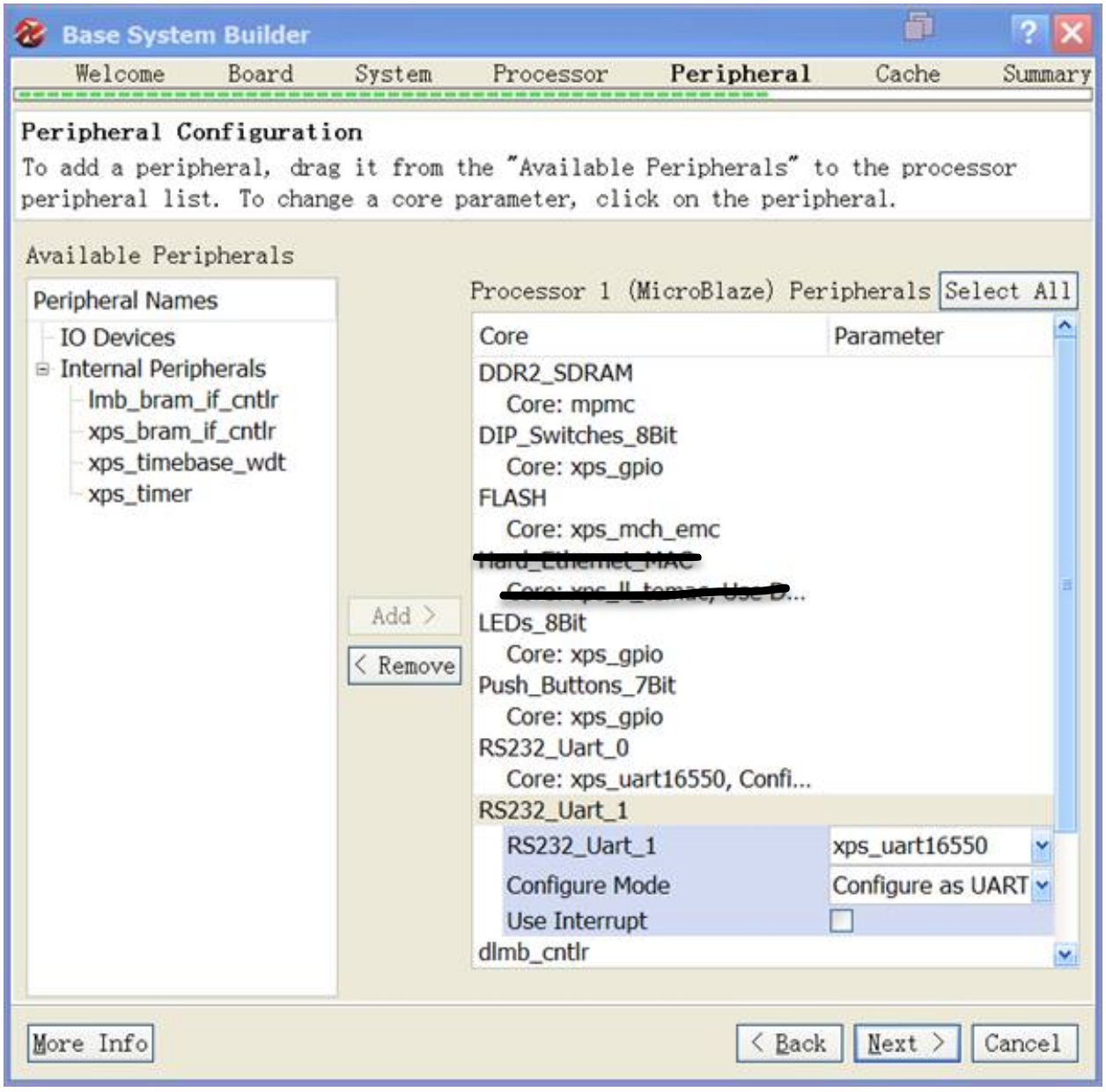

Base System Builder
Welcome
Board
System
Processor
Peripheral
Cache
Summary
Welcome to the Base System Builder
This tool leads you through the steps necessary for creating an embedded system.
Select One of the Following:
I would like to create a new design
I would like to load an existing .bsb settings file (saved from a previous sessi
Browse ...
More Info
< Back
Next >
Cancel

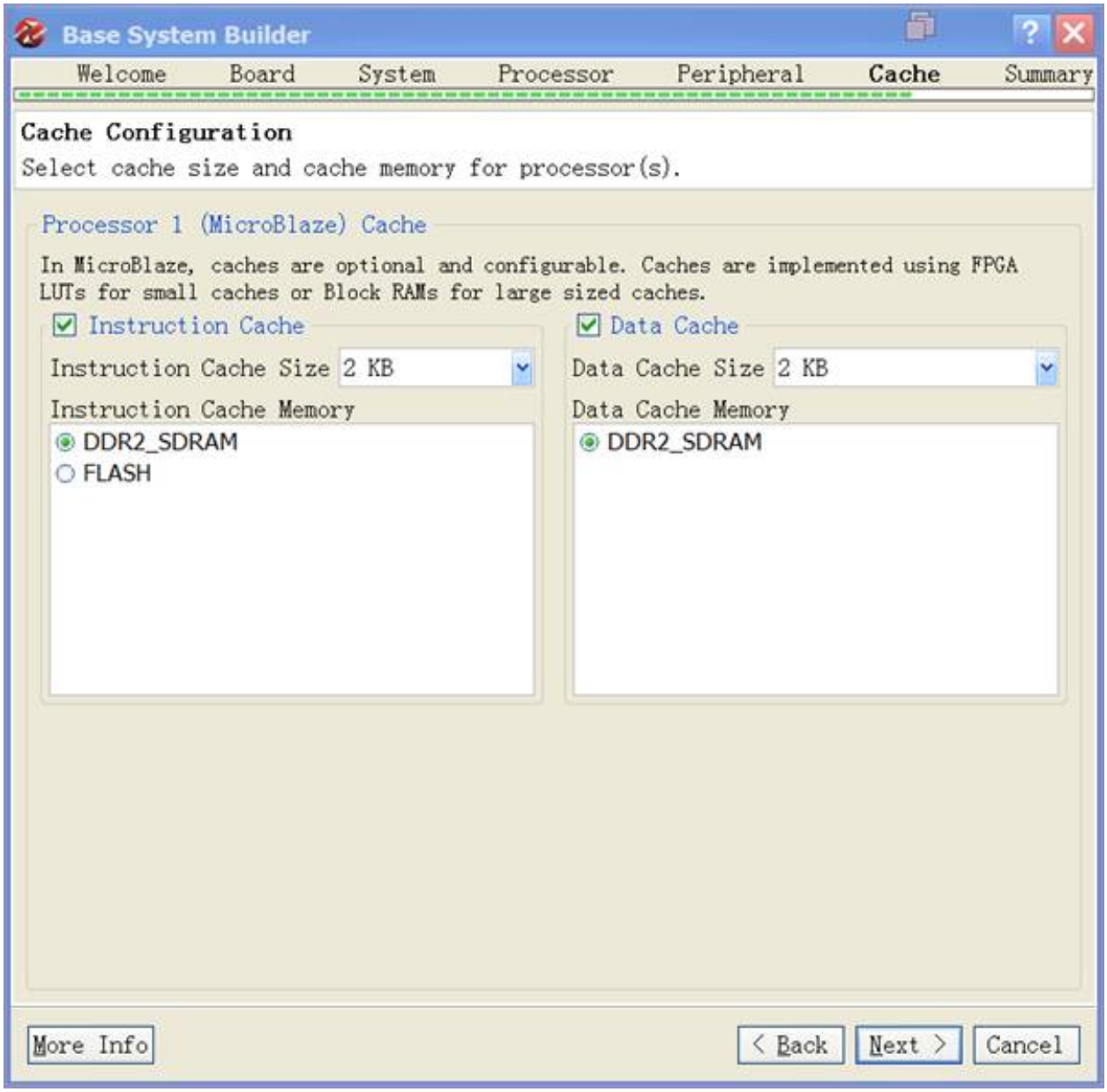

Base System Builder
Welcome
Board
System
Processor
Peripheral
Cache
Summary
Board Selection
Select a target development board.
Board
I would like to create a system for the following development board
Board Vendor
Digilent
Board Name
Digilent Genesys System Board
Board Revision
C
I would like to create a system for a custom board
Board Information
Architecture
Device
Package
Speed Grade
virtex5
xc5vlx50t
ff1136
-1
Use Stepping
Reset Polarity
Active Low
Related Information
Vendor's Website
Vendor's Contact Information
Third Party Board Definition Files Download Website
The Genesys board utilizes a Xilinx Virtex 5 XC5VLX50T-FFG1136 device. The board includes Tri-Mode Ethernet MAC/PHY, 256MB DDR2 SDRAM SODIMM memory, 32MB of Intel P30 Flash, DVI ouptut, Digilent USB-EPP port, Xilinx USB host and device controller and 2 RS232 serial ports.
More Info
< Back
Next >
Cancel


Base System Builder
Welcome
Board
System
Processor
Peripheral
Cache
Summary
System Configuration
Configure your system.
Single-Processor System
Select this option to create a design with a single processor. This Wizard will let you configure the processor, the peripheral set and some major configuration parameters for the peripherals.
Processor 1
Processor 1 Peripherals
RS232
GPIO
.....
Dual-Processor System
Select this option to create a design with two processors. This Wizard will let you select the types of processors, peripherals unique to each processor, and peripherals shared by the processors.
Processor 1
Processor 1 Peripherals
RS232
GPIO
.....
Shared Peripherals
Mailbox
Mutex
.....
Processor 2
Processor 2 Peripherals
DDR
EMAC
.....
More Info
< Back
Next >
Cancel


Base System Builder
Welcome
Board
System
Processor
Peripheral
Cache
Summary
Processor Configuration
Configure the processor(s).
Reference Clock Frequency
100.00
MHz
Processor 1 Configuration
Processor Type
MicroBlaze
System Clock Frequency
125.00
MHz
Local Memory
64 KB
Debug Interface
On-Chip HW Debug Module
Enable Floating Point Unit
More Info
< Back
Next >
Cancel


Base System Builder
Welcome
Board
System
Processor
Peripheral
Cache
Summary
Peripheral Configuration
To add a peripheral, drag it from the "Available Peripherals" to the processor peripheral list. To change a core parameter, click on the peripheral.
Available Peripherals
Peripheral Names
IO Devices
Internal Peripherals
lmb_bram_if_cntlr
xps_bram_if_cntlr
xps_timebase_wdt
xps_timer
Add >
< Remove
Processor 1 (MicroBlaze) Peripherals
Select All
Core
Parameter
Core: xps_gpio
FLASH
Core: xps_mch_emc
LEDs_8Bit
Core: xps_gpio
Push_Buttons_7Bit
Core: xps_gpio
RS232_Uart_0
RS232_Uart_0
xps_uart16550
Configure Mode
Configure as UART
Use Interrupt
RS232_Uart_1
Core: xps_uartlite, Baud Ra...
dlmb_cntlr
Core: lmb_bram_if_cntlr
ilmb_cntlr
Core: lmb_bram_if_cntlr
More Info
< Back
Next >
Cancel


Base System Builder
Welcome
Board
System
Processor
Peripheral
Cache
Summary
Peripheral Configuration
To add a peripheral, drag it from the "Available Peripherals" to the processor peripheral list. To change a core parameter, click on the peripheral.
Available Peripherals
Peripheral Names
IO Devices
Internal Peripherals
lmb_bram_if_cntlr
xps_bram_if_cntlr
xps_timebase_wdt
xps_timer
Add >
< Remove
Processor 1 (MicroBlaze) Peripherals
Select All
Core
Parameter
DDR2_SDRAM
Core: mpmc
DIP_Switches_8Bit
Core: xps_gpio
FLASH
Core: xps_mch_emc
LEDs_8Bit
Core: xps_gpio
Push_Buttons_7Bit
Core: xps_gpio
RS232_Uart_0
Core: xps_uart16550, Confi...
RS232_Uart_1
RS232_Uart_1
xps_uart16550
Configure Mode
Configure as UART
Use Interrupt
dlmb_cntlr
More Info
< Back
Next >
Cancel


Base System Builder
Welcome
Board
System
Processor
Peripheral
Cache
Summary
Cache Configuration
Select cache size and cache memory for processor(s).
Processor 1 (MicroBlaze) Cache
In MicroBlaze, caches are optional and configurable. Caches are implemented using FPGA LUTs for small caches or Block RAMs for large sized caches.
Instruction Cache
Instruction Cache Size 2 KB
Instruction Cache Memory
DDR2_SDRAM
FLASH
Data Cache
Data Cache Size 2 KB
Data Cache Memory
DDR2_SDRAM
More Info
< Back
Next >
Cancel