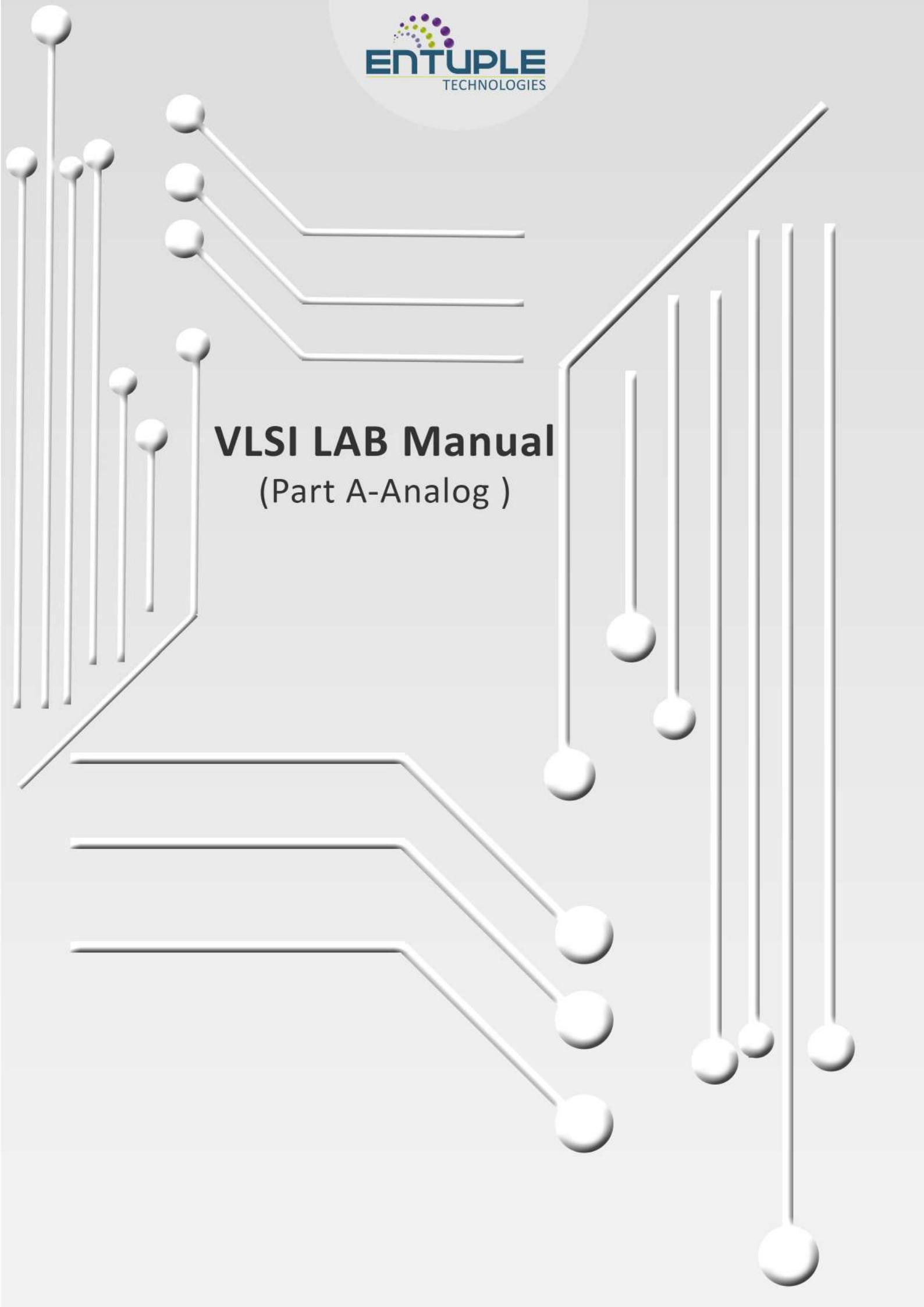


VLSI LAB Manual

(VTU curriculum - 2018)

Developed by
Application Engineering Team
Entuple Technologies Pvt Ltd.



VLSI LAB Manual

(Part A-Analog)

Custom IC Design Flow

Cadence design tools

(Analog Design)

PART - A

**IC 6.1.8
Spectre
Assura**

**Developed By
Application Engineering Team
Entuple Technologies Pvt Ltd, Bengaluru**

Objective

The main objective of this lab is to learn the Full Custom IC Design Flow along with the usage of tools such as the Virtuoso Schematic Editor, Spectre, Virtuoso Layout Editor and Assura. In this process, you will create components like an Inverter, a NAND Gate, Common Source Amplifier and a 2-Stage Operational Amplifier.

You will start the lab by creating a Library and attach it to a Technology Node gdk 180 / 90 / 45. By attaching it to a Technology Node, you ensure that you go through the entire Front-end and Back-end process.

You will also create a new cell with the Schematic View, build the Schematic by instantiating various components, create a Symbol, build a test Schematic by instantiating the Symbol and verify the circuit using Spectre. In the process, one will learn to use Spectre, Viva (Virtuoso Visualization and Analysis) tool and its Calculator option.

You will learn about the basics of Virtuoso Layout Editor by concentrating on the Automatic Layout Generation and followed by that, run the DRC and LVS checks, extract the Parasitics, Back Annotate them and complete the flow by generating the GDSII file.

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PHYSICAL VERIFICATION WITH ASSURA
TECHNOLOGY LIBRARY (assura_tech.lib) MAPPING
DRC (DESIGN RULE CHECK)
LVS (LAYOUT VERSUS SCHEMATIC)
QRC (RC / PARASITIC EXTRACTION)
BACKANNOTATION (POST LAYOUT SIMULATION)

Lab – 02: 2 – INPUT CMOS NAND GATE

Solution – (a):

SCHEMATIC CAPTURE - 106
FUNCTIONAL SIMULATION

Solution – (b):

SCHEMATIC CAPTURE
FUNCTIONAL SIMULATION
LAYOUT
DRC
LVS
QRC
BACKANNOTATION

Lab – 03: COMMON SOURCE AMPLIFIER WITH PMOS CURRENT MIRROR LOAD

Solution – (a):

SCHEMATIC CAPTURE - 119
FUNCTIONAL SIMULATION

Solution – (b):

LAYOUT
DRC
LVS
QRC
BACKANNOTATION

Lab – 04: 2 STAGE OPERATIONAL AMPLIFIER

Solution – (a):

SCHEMATIC CAPTURE - 127
FUNCTIONAL SIMULATION USING ADE EXPLORER
AND ADE ASSEMBLER
GENERATING THE EXPRESSIONS
GAIN MARGIN AND PHASE MARGIN

Solution – (b):

LAYOUT
DRC
LVS
QRC
BACKANNOTATION

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GENERAL NOTES

Before starting to work on a design, create a Workspace (Folder) for the project individually.

WORK SPACE CREATION:

Make a right click on the **Desktop** and select the option “**New Folder**” as shown in Figure - 1.

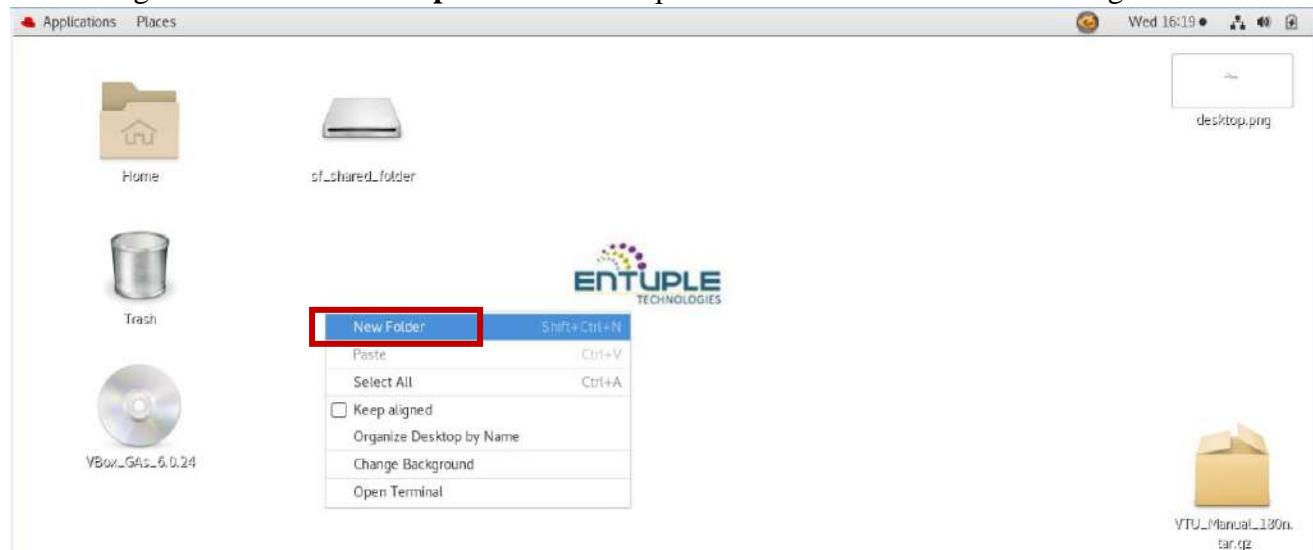


Figure – 1: Workspace Creation

Name the folder (for example: **VTU_LAB_EXP**) and click on “**Create**” as shown in Figure - 2.

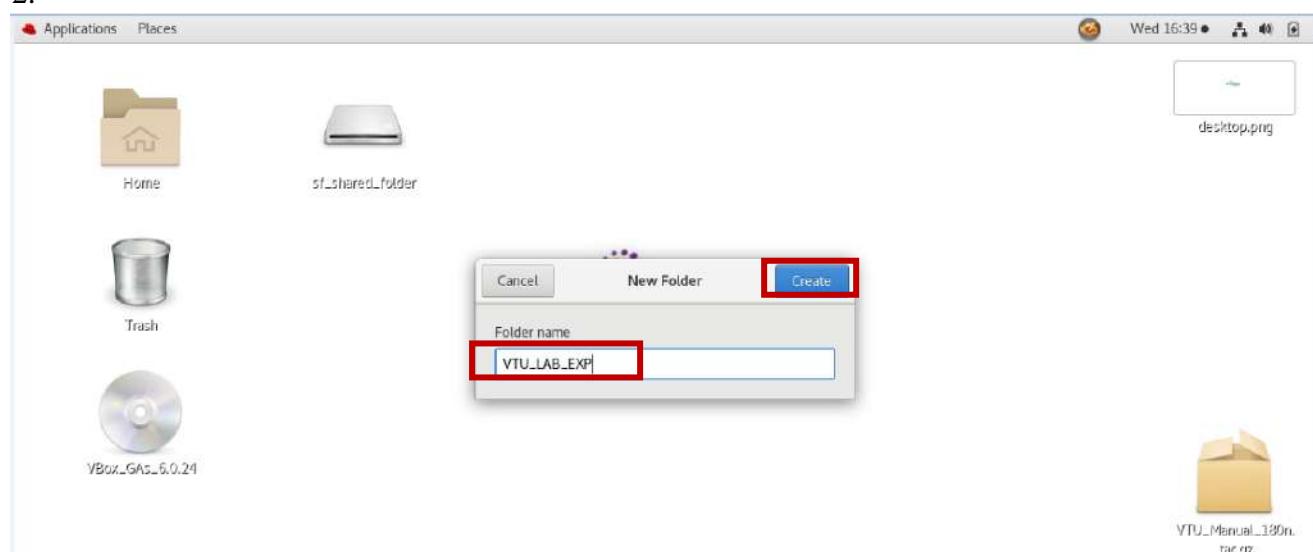


Figure – 2: Name the Folder

Open the folder by a double click and the window can be seen as shown in Figure - 3.

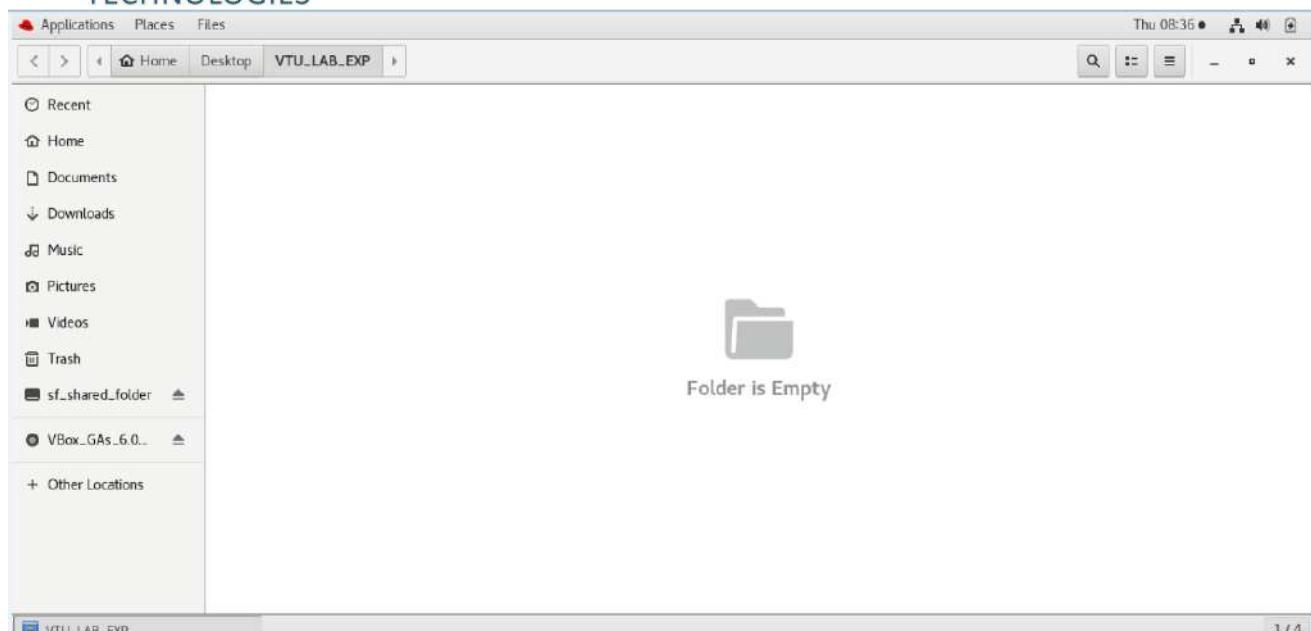


Figure – 3: Open the folder

INITIALISING csh & SOURCING cshrc:

Make a right click and select “Open in Terminal” as shown in Figure - 4.

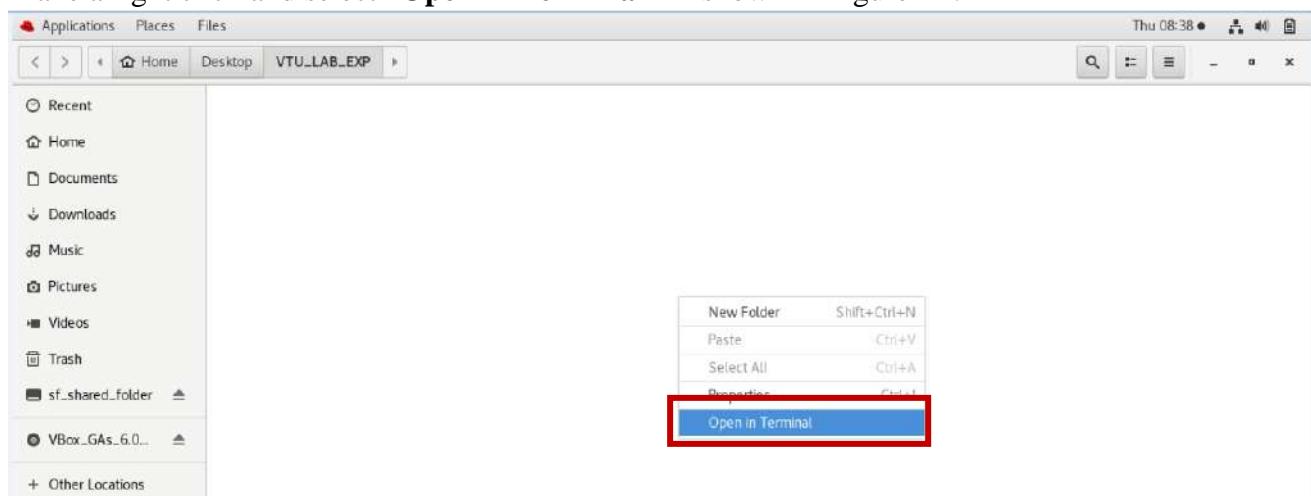
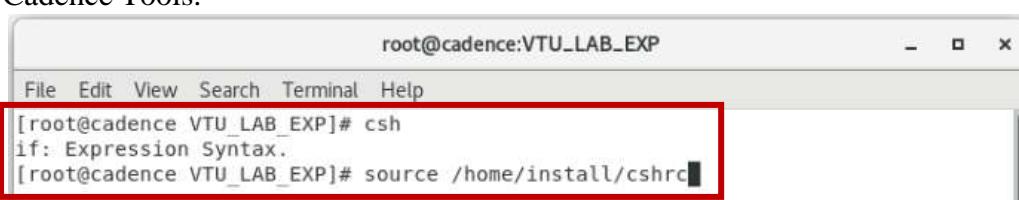


Figure – 4: Open in Terminal

Type the command “csh” to initialize shell and source the “cshrc” file with the command “source /home/install/cshrc”. “cshrc” file will provide the details of the installation directory of the Cadence Tools.



```
root@cadence:VTU_LAB_EXP
File Edit View Search Terminal Help
[root@cadence VTU_LAB_EXP]# csh
if: Expression Syntax.
[root@cadence VTU_LAB_EXP]# source /home/install/cshrc
```

Figure – 5: “csh” and “source /home/install/cshrc ” commands

INVOKING VIRTUOSO:

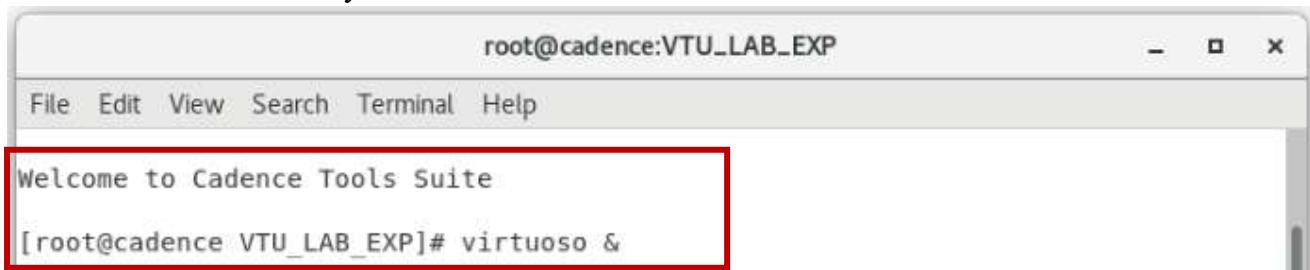
After sourcing the “`cshrc`” file, click on “Enter” on the keyboard. The welcome screen with the text “Welcome to Cadence Tools Suite” can be seen as shown in Figure - 5.



```
root@cadence:VTU_LAB_EXP
File Edit View Search Terminal Help
Welcome to Cadence Tools Suite
[root@cadence VTU_LAB_EXP]#
```

Figure - 6: Welcome screen

Invoke virtuoso using the command “`virtuoso &`” or “`virtuoso`” as shown in Figure – 7 and click on “Enter” in the keyboard.



```
root@cadence:VTU_LAB_EXP
File Edit View Search Terminal Help
>Welcome to Cadence Tools Suite
[root@cadence VTU_LAB_EXP]# virtuoso &
```

Figure - 7: Command to invoke “virtuoso”

The Virtuoso “Command Interpreter Window (CIW)” can be seen as shown in Figure - 8.

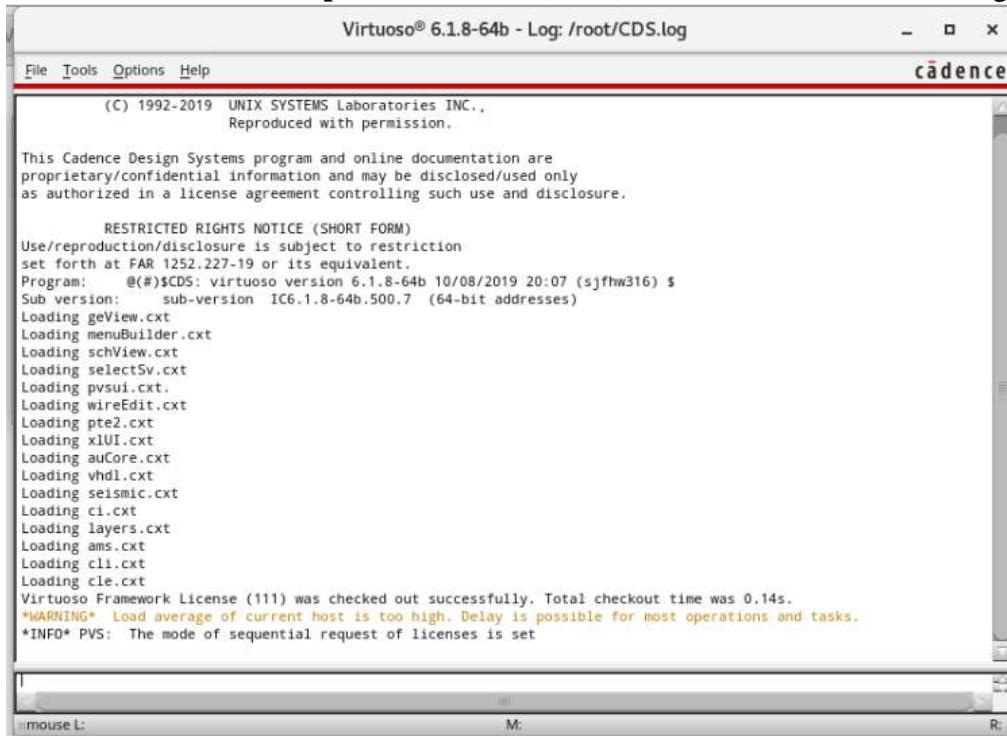


Figure – 8: Command Interpreter Window (CIW)

LAB – 01: CMOS INVERTER

Objective:

- (a) Capture the Schematic of a CMOS Inverter with Load Capacitance of 0.1 pF and set the Widths of Inverter with
- $W_N = W_P$
 - $W_N = 2 W_P$
 - $W_N = W_P / 2$

and Length at selected Technology. Carry out the following:

- Set the Input Signal to a pulse with Rise Time, Fall Time of 1 ps and Pulse Width of 10 ns, Time Period of 20 ns and plot the input voltage and output voltage of the designed Inverter
- From the Simulation Results, compute t_{PHL} , t_{PLH} and t_{PD} for all the three geometrical settings of Width
- Tabulate the results of delay and find the best geometry for minimum delay for CMOS Inverter

Solution:

- (a) Schematic Capture of CMOS Inverter

CREATE A LIBRARY:

To create a New Library, select “Tools → Library Manager” from the top menu as shown in Figure – 1.1.

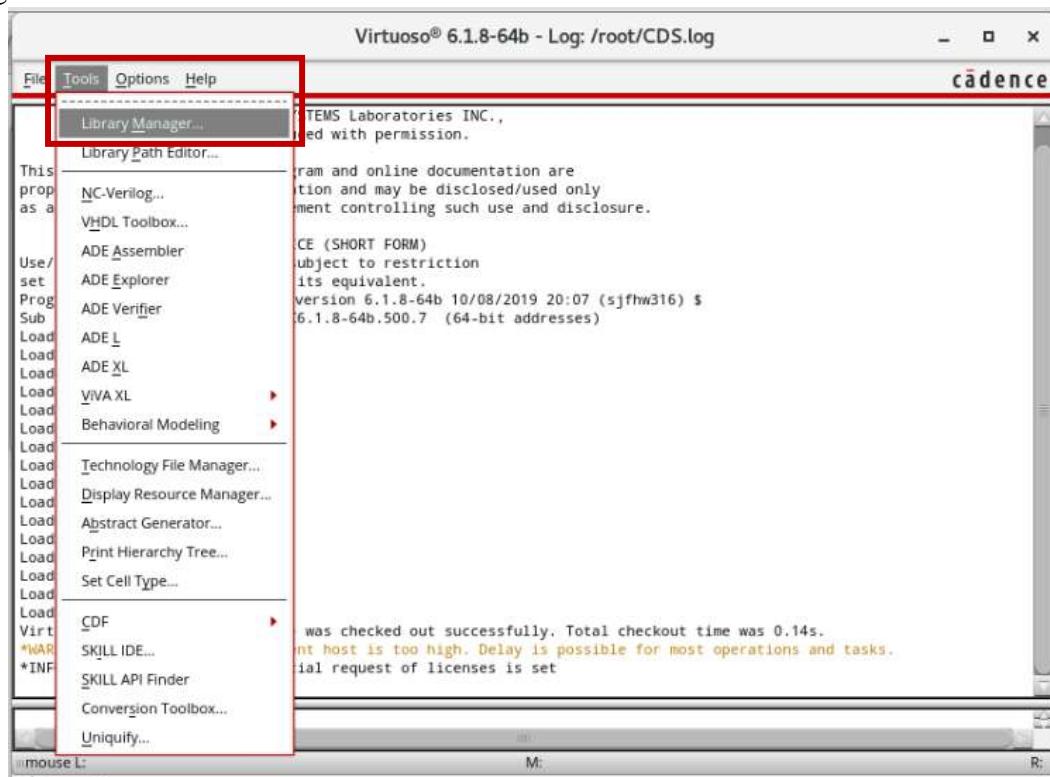


Figure – 1.1: Tools → Library Manager

The Cadence Library Manager shows up as in Figure – 1.2.

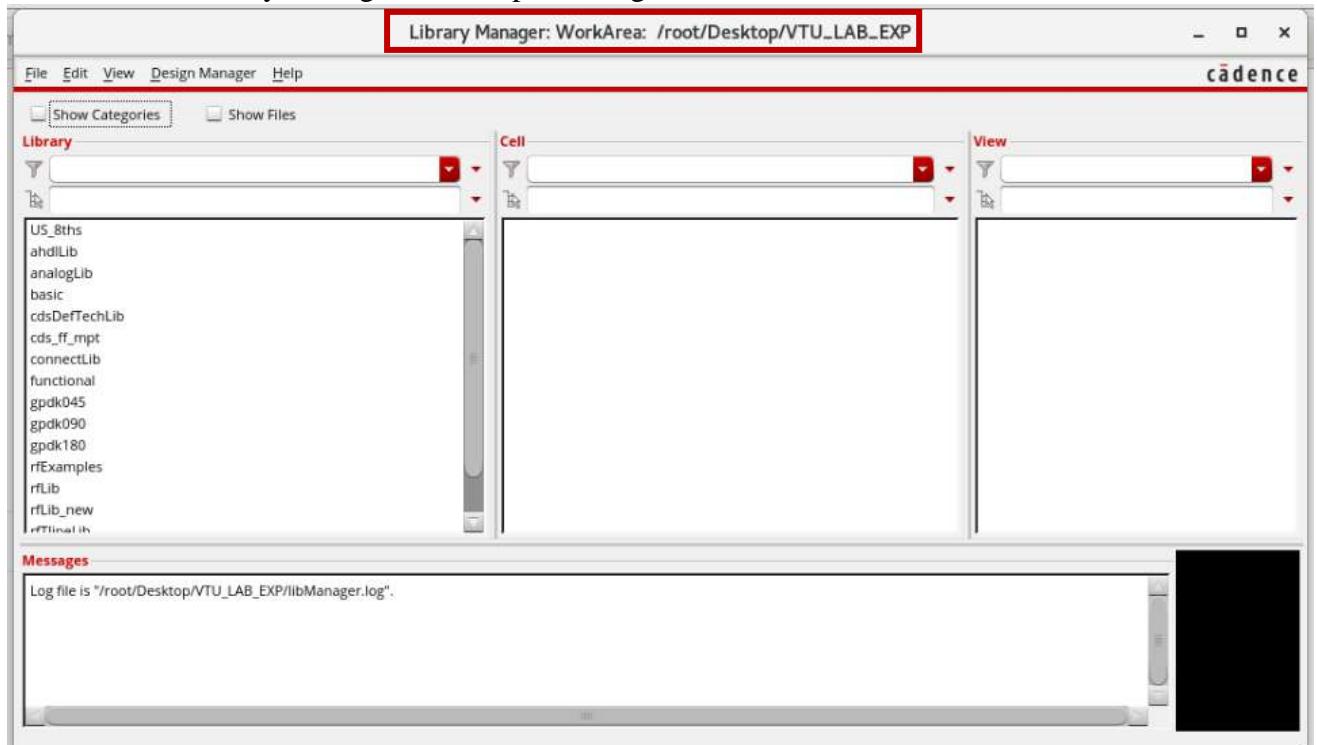


Figure – 1.2: Library Manager

Select “File → New → Library” from the top menu as shown in Figure – 1.3.

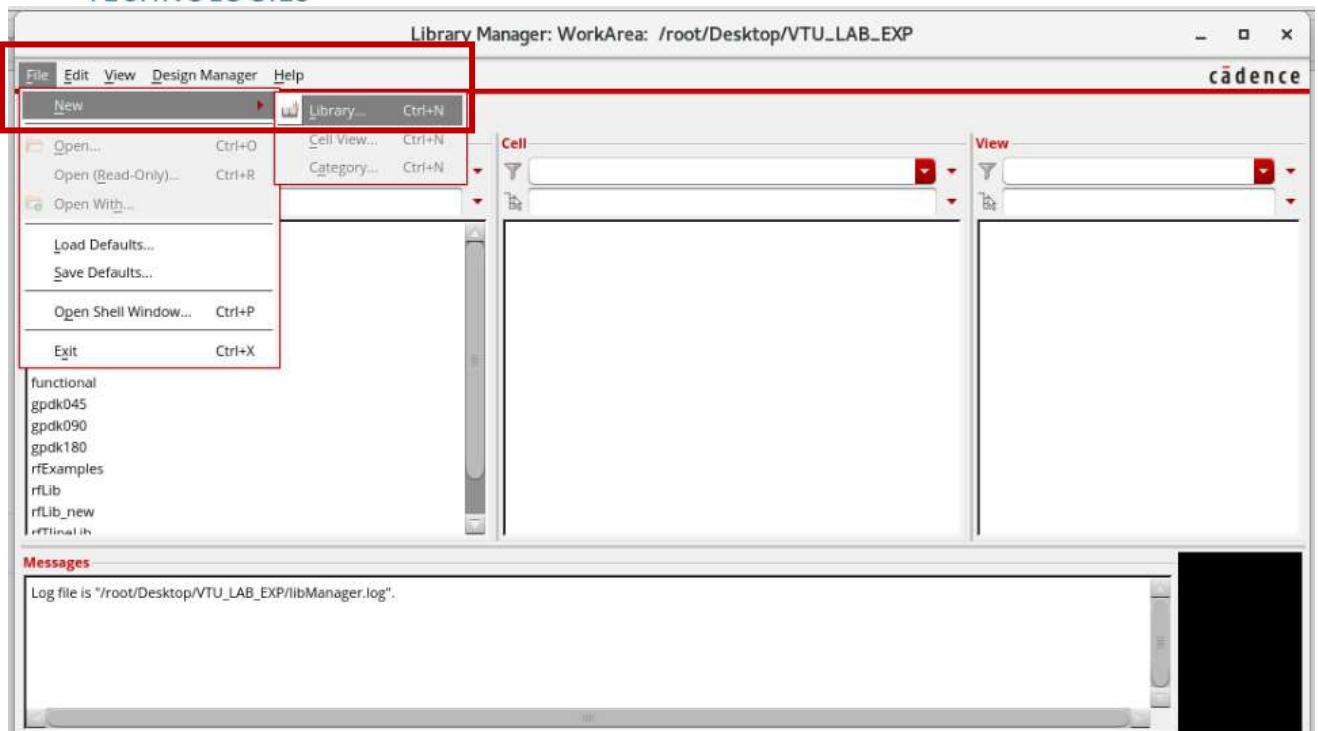


Figure – 1.3: File → New → Library

A “**New Library**” window will show up as in Figure – 1.4. Name the Library (for eg: VTU_LAB_MANUAL_180nm) and click on “**OK**”.

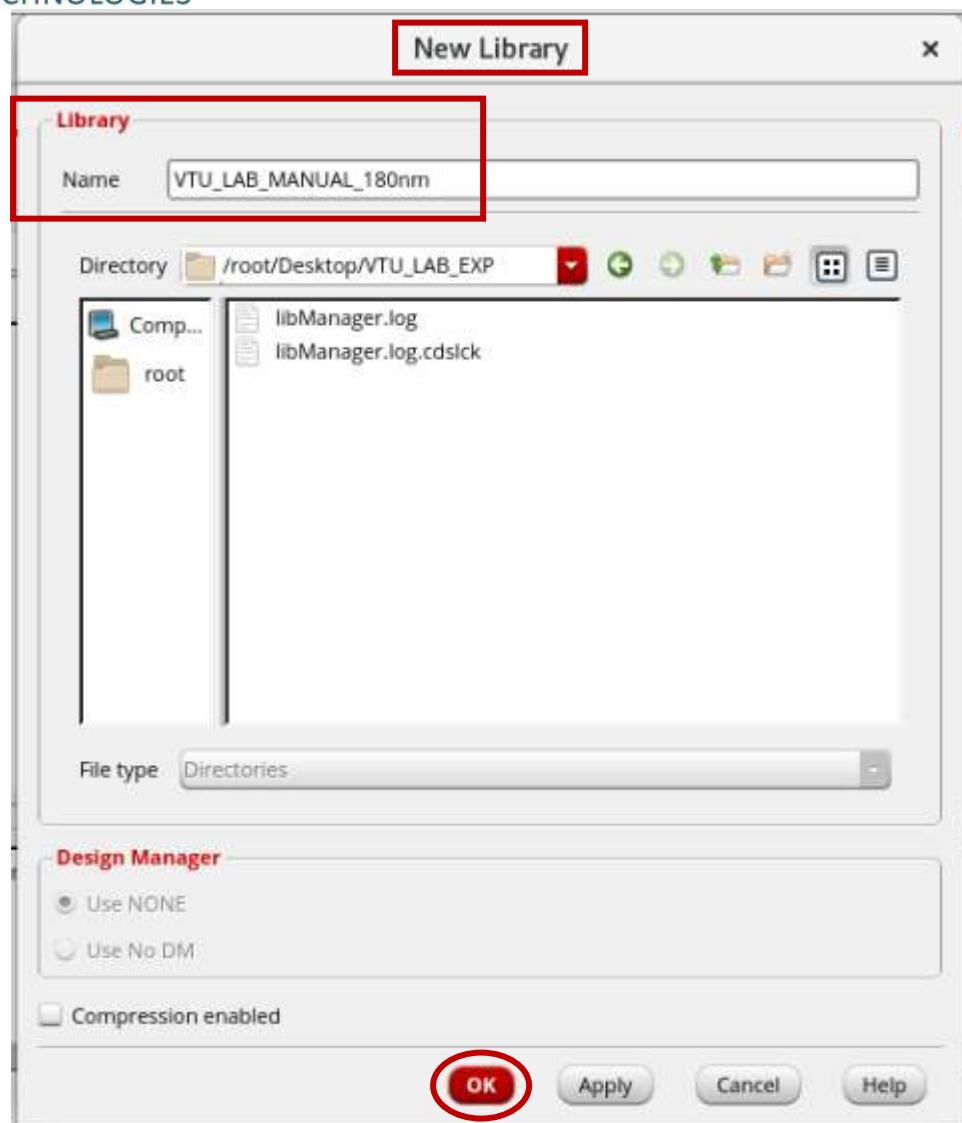


Figure – 1.4: Name the Library

Select “Technology File..” tab that keeps blinking at the bottom of the screen as shown in Figure – 1.5 to map the New Library to a technology node based on the specification.

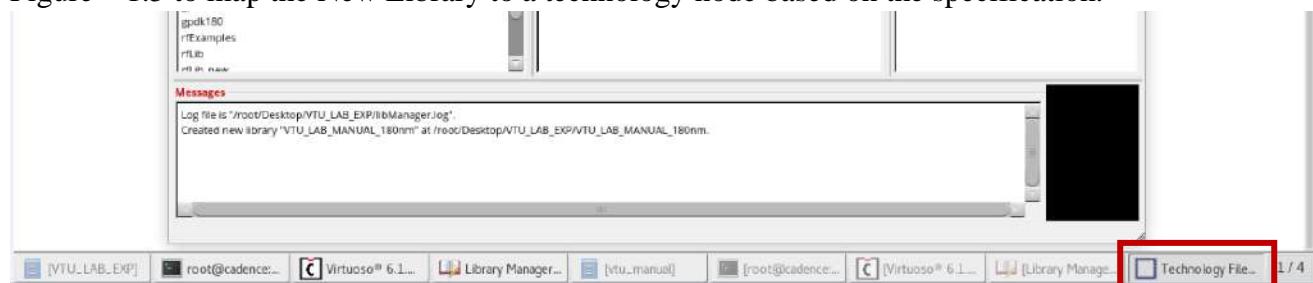


Figure – 1.5: “Technology File..” Tab

Click on the tab and “Technology File for New Library” window can be seen as in Figure – 1.6. Select “Attach to an existing technology library” and click on “OK”.

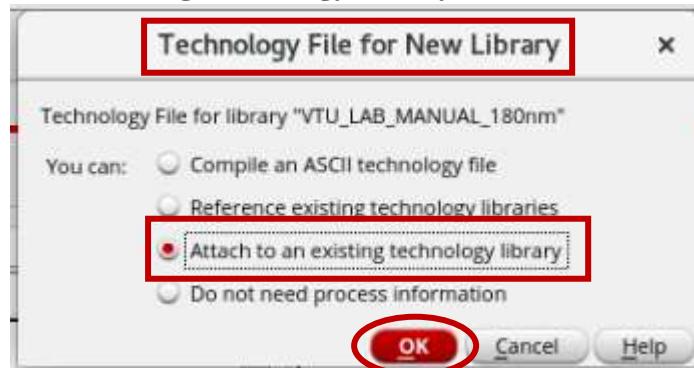


Figure – 1.6: Technology File for New Library form

From the list of available Technology Libraries, select the respective Technology Node as shown in Figure – 1.7 (for example: **gdk180**) and click on “OK”.

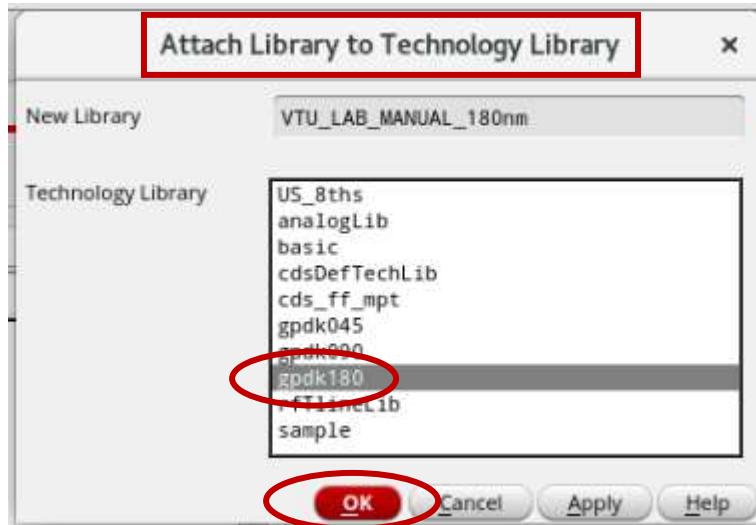


Figure – 1.7: Technology Node Selection

The New Library can be verified from the Library Manager under “Library” column as shown in Figure – 1.8.

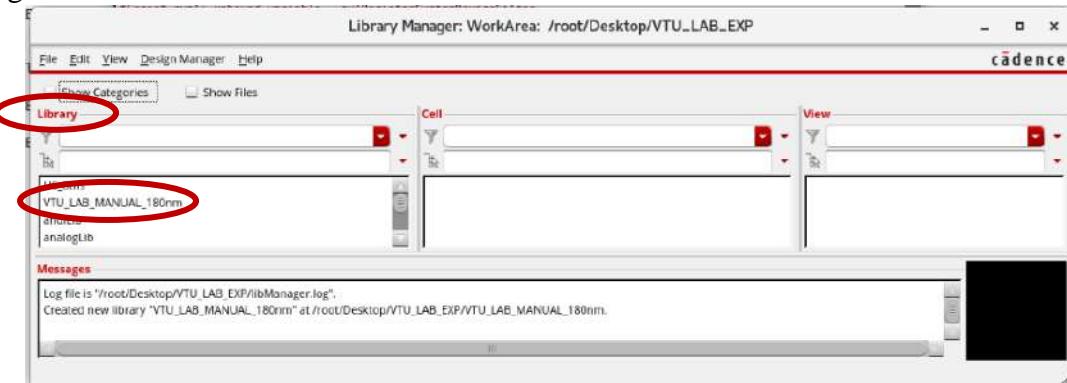


Figure – 1.8: New Library included to Library Manager

CREATE A CELLVIEW:

To create a Cellview within a Library, select the respective library as shown in Figure – 1.9.

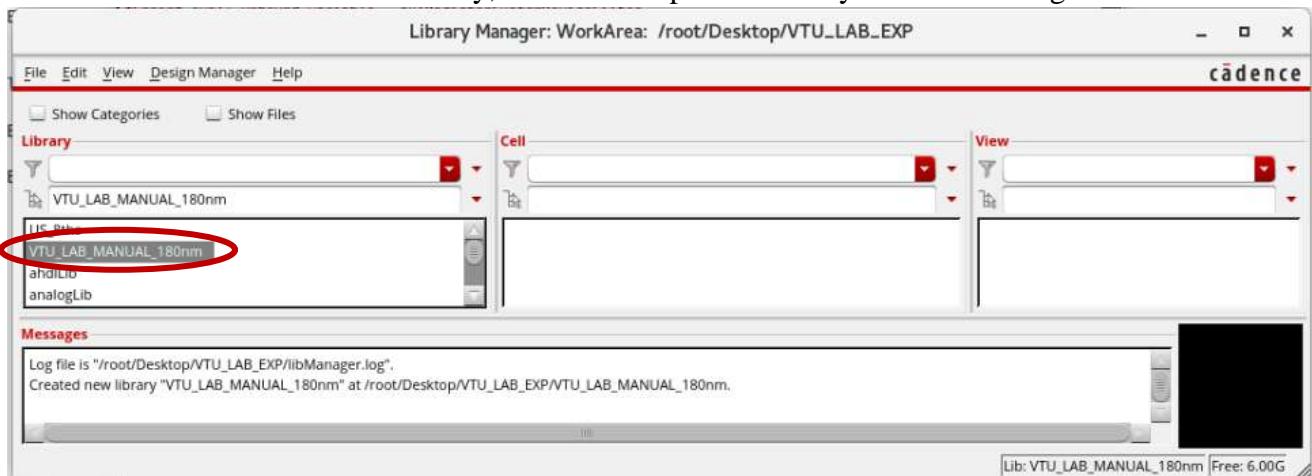


Figure – 1.9: Select the Library

Select **File → New → Cell View** as shown in Figure – 1.10.

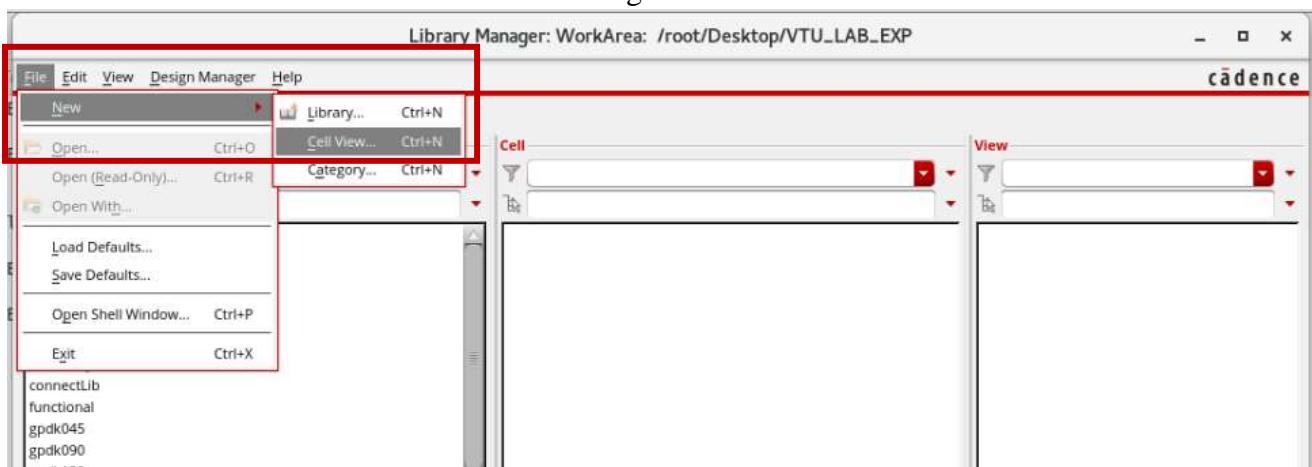


Figure – 1.10: File → New → Cell View

A “New File” window can be seen as shown in Figure – 1.11.

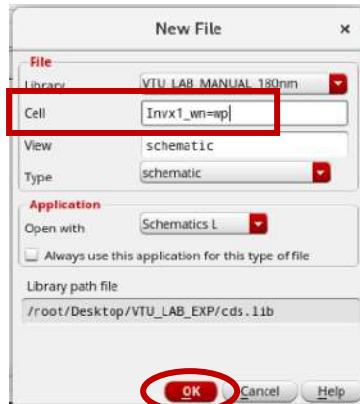


Figure – 1.11: “New File” Window

Name the Cell and click on “OK”. A blank “**Virtuoso Schematic Editor L Editing**” window can be seen as shown in Figure – 1.12.

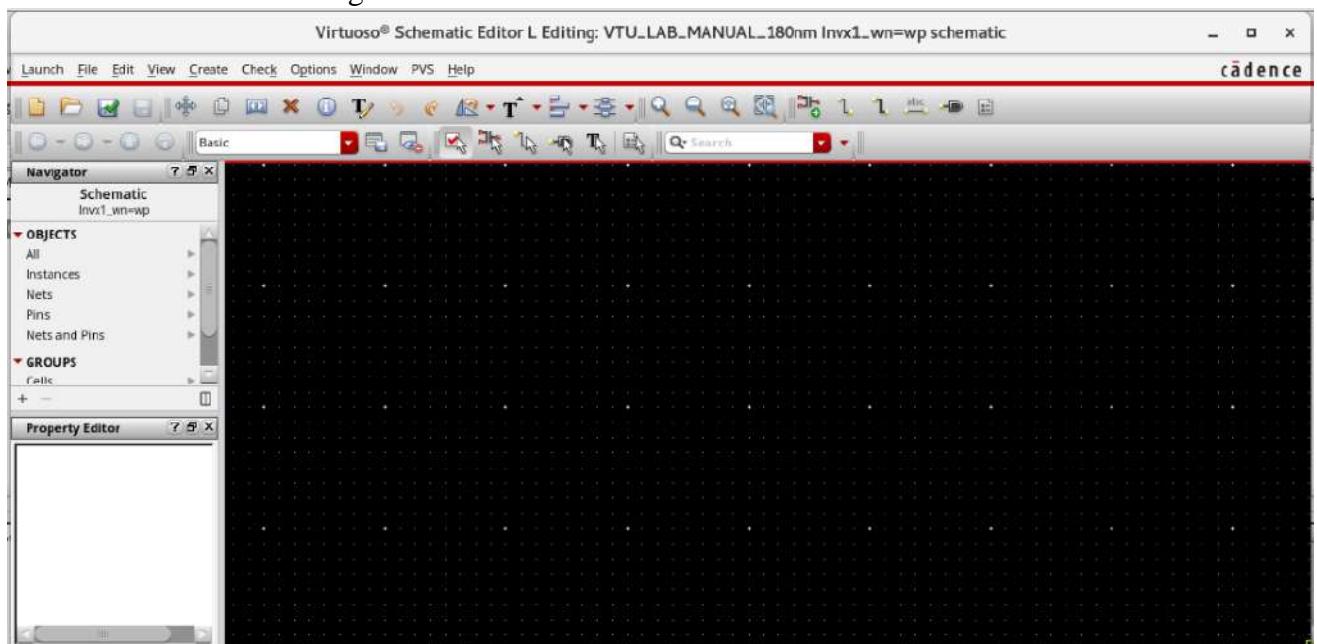


Figure – 1.12: Virtuoso Schematic Editor

(i) SCHEMATIC CAPTURE FOR THE CMOS INVERTER

To complete the Schematic for a CMOS Inverter with $W_N = W_P$, components have to be included to the blank Virtuoso Schematic Editor window. These components are called Instances. The procedure to include the components to the Schematic are given below.

ADD AN INSTANCE:

Select “Create → Instance” as in Figure – 1.13 (or) use the bind key ‘I’ (or) the icon as in Figure – 1.13.

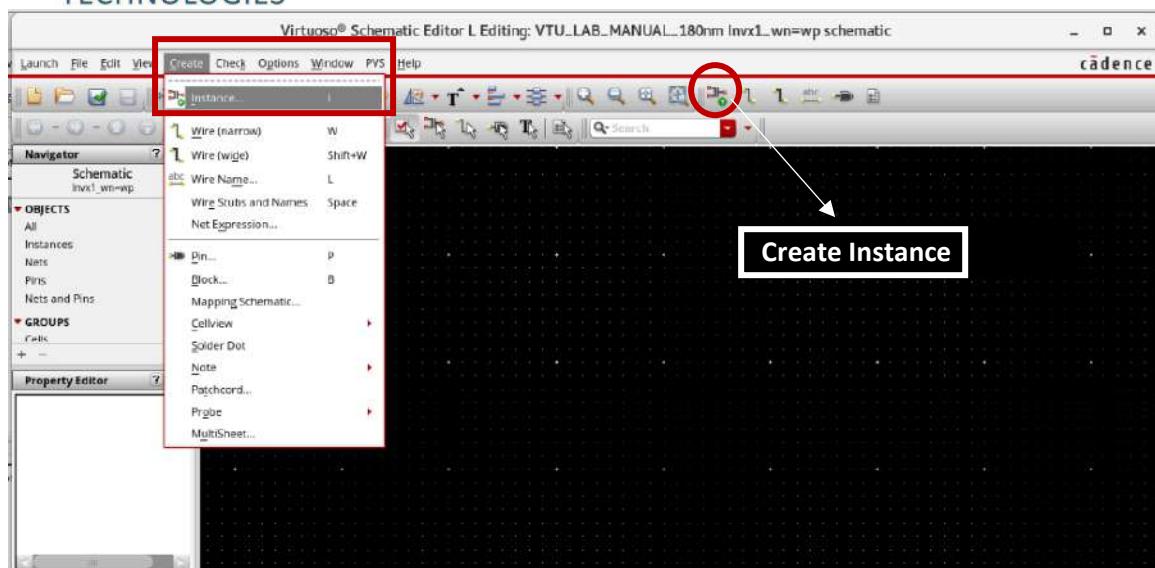


Figure – 1.13: Create → Instance

The “**Add Instance**” form can be seen as shown in Figure – 1.14.

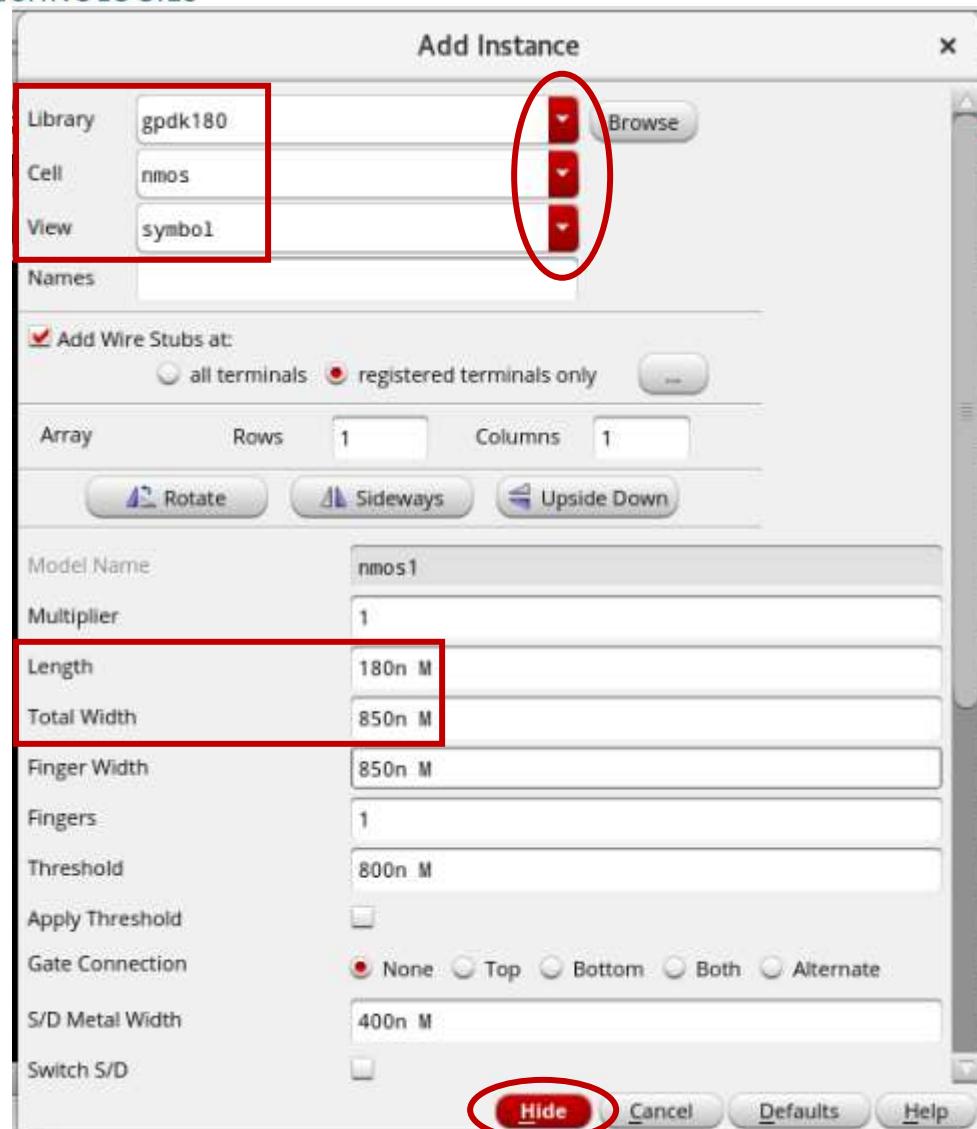


Figure – 1.14: “Add Instance” Window

Click on the drop down close to the **Browse** option as shown in Figure – 1.14. Select the Technology Node from the list of libraries. Similarly, click on the drop down next to **Cell** and select the required device from the list. For the CMOS Inverter circuit, PMOS and NMOS transistors are required. The parameters for the devices as given in the requirement are considered as in Table – 1, Table – 2 and Table – 3.

Table – 1: Length and Width of NMOS and PMOS Transistors for the condition $W_N = W_P$

| Library Name | Cell Name | Comments / Properties |
|--------------|-----------|---|
| gdk180 | Nmos | Width, $W_N = 850 \text{ n}$ Length, $L = 180 \text{ n}$ |
| gdk180 | Pmos | Width, $W_P = 850 \text{ n}$ Length, $L = 180 \text{ n}$ |

**Table – 2: Length and Width of NMOS and PMOS Transistors for the condition
 $W_N = 2 * W_P$**

| Library Name | Cell Name | Comments / Properties |
|--------------|-----------|---|
| gdk180 | Nmos | Width, $W_N = 850$ n Length, $L = 180$ n |
| gdk180 | Pmos | Width, $W_P = 1.7$ u Length, $L = 180$ n |

**Table – 3: Length and Width of NMOS and PMOS Transistors for the condition
 $W_N = W_P / 2$**

| Library Name | Cell Name | Comments / Properties |
|--------------|-----------|---|
| gdk180 | Nmos | Width, $W_N = 850$ n Length, $L = 180$ n |
| gdk180 | Pmos | Width, $W_P = 425$ n Length, $L = 180$ n |

Type the parameters and click on “**Hide**”. The device can be seen as shown in Figure – 1.15.

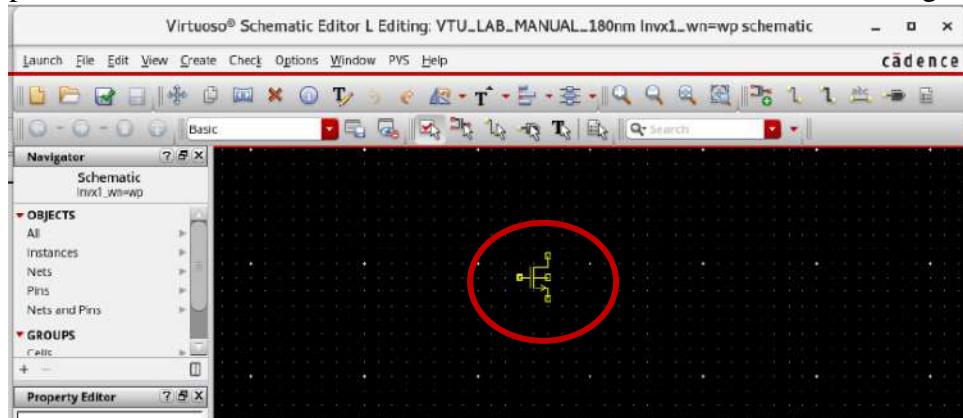


Figure – 1.15: Instance after Selection

Make a left mouse click to place it on the Schematic Editor. The device after placement on the Schematic Editor can be seen as shown in Figure – 1.16. Similarly, other components can be instantiated.

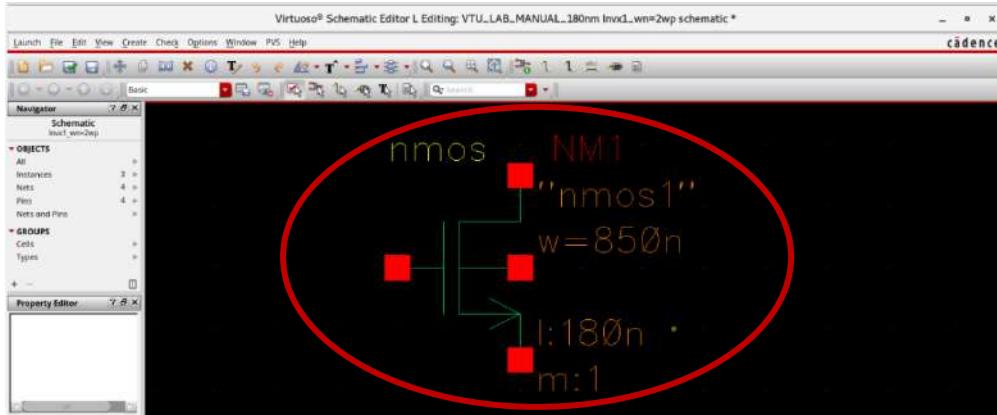


Figure – 1.16: Instance after left mouse click

ADD PIN:

To include pins to the schematic, select “**Create → Pin**” from the top menu (or) use the bind key ‘**P**’ (or) use the icon from the top menu as shown in Figure – 1.17.

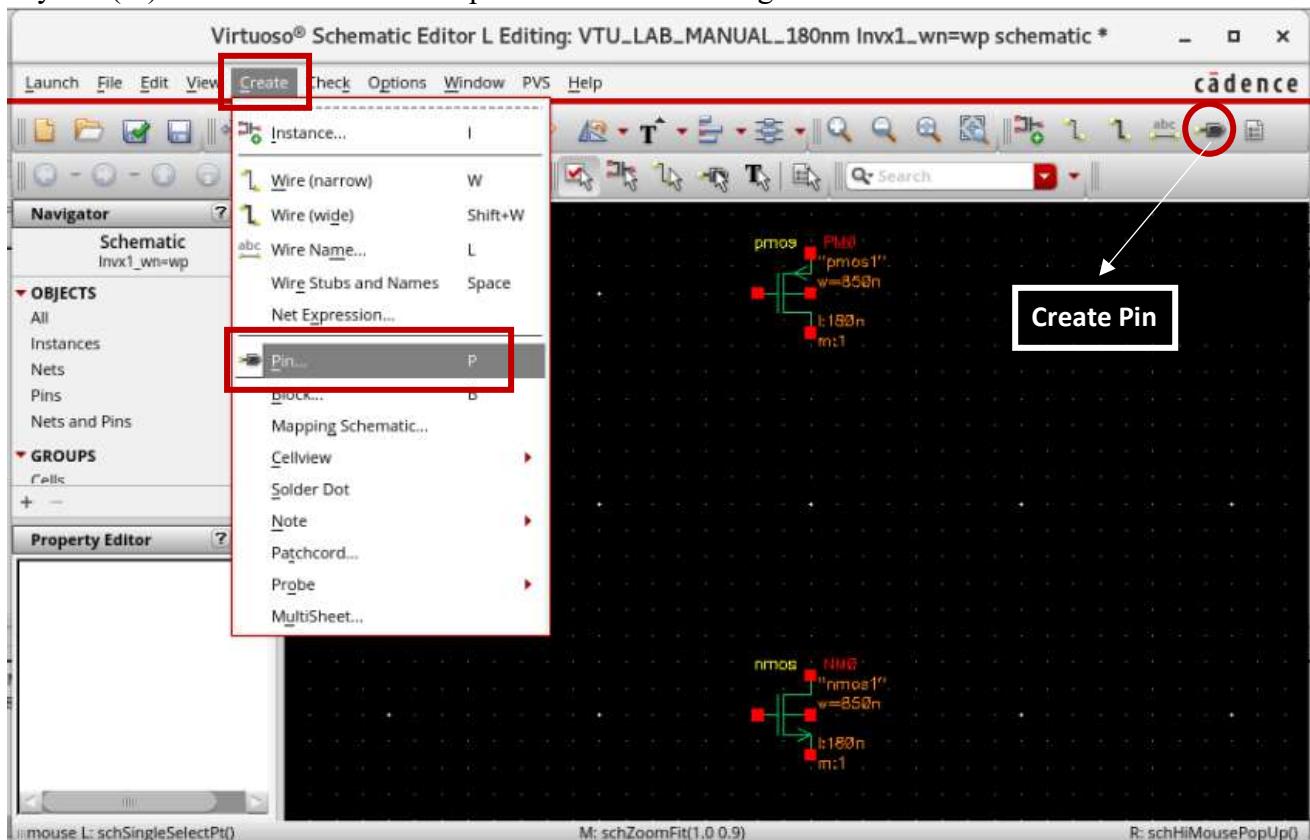


Figure – 1.17: Create → Pin

The “**Create Pin**” window pops up as shown in Figure – 1.18.



Figure – 1.18: Create Pin window

Name the pins by separating them with “space”, choose its direction and click on “Hide” as shown in Figure – 1.19(a) and Figure – 1.19(b).



Figure – 1.19(a): Naming the Input Pins

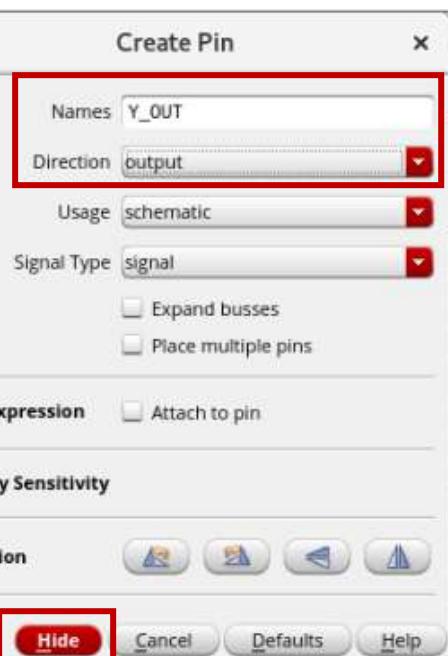


Figure – 1.19(b): Naming the Output Pins

The pins are visualized on the Schematic Editor as shown in Figure – 1.20.

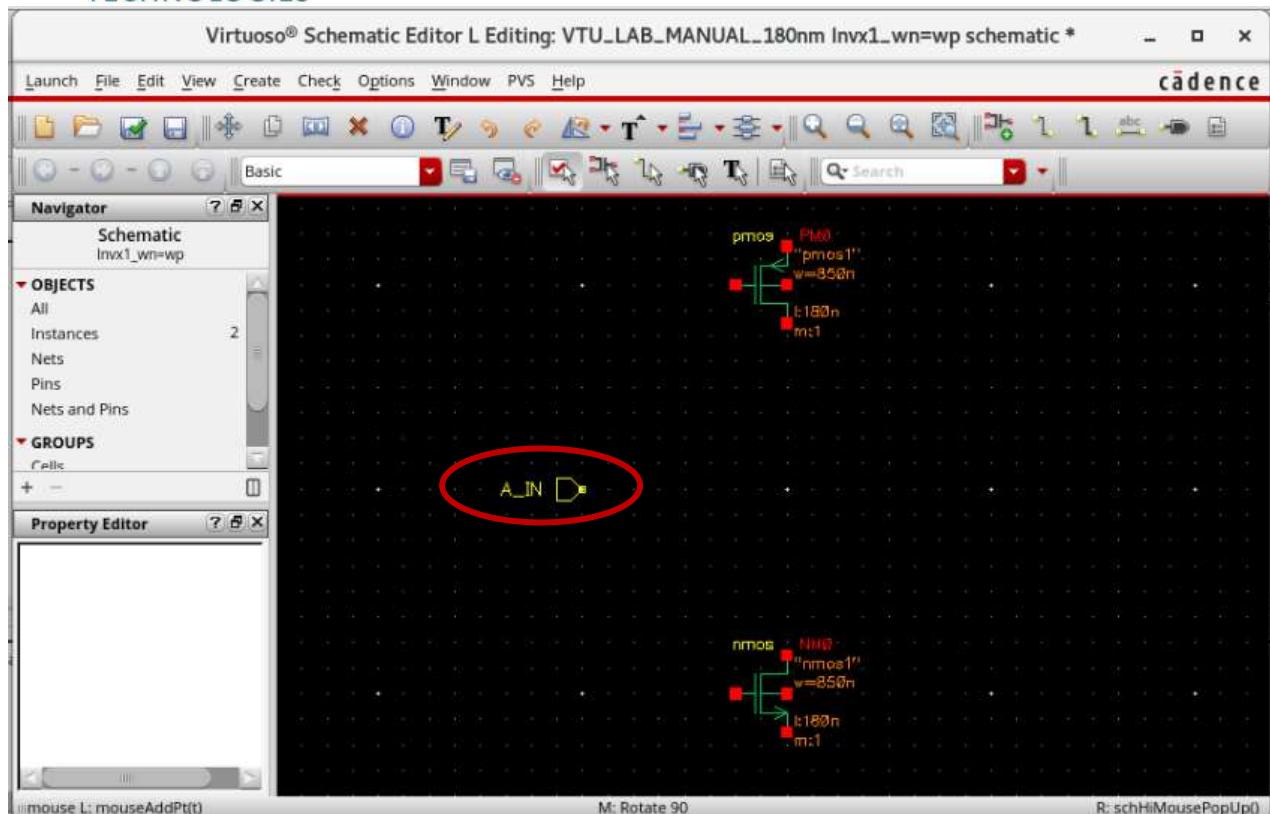


Figure – 1.20: Pins after left mouse click on “Hide”

Place the pins on the Schematic Editor using a left mouse click and the pins after placement can be visualized as shown in Figure – 1.21.

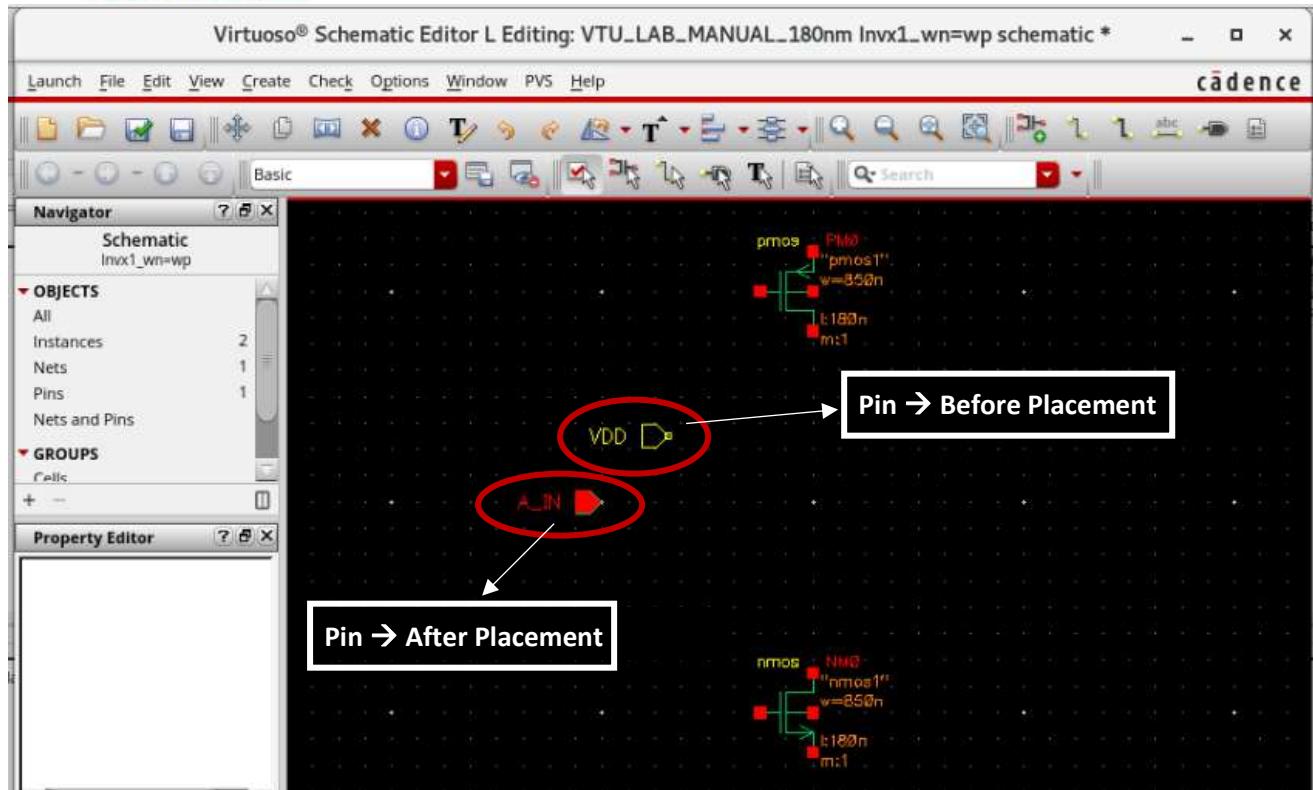


Figure – 1.21: Pins Before and After Placement

Use the bind key “R” to rotate the pins and it can be done either before or after Pin Placement. The direction of the pins before and after rotation are shown in Figure – 1.22.

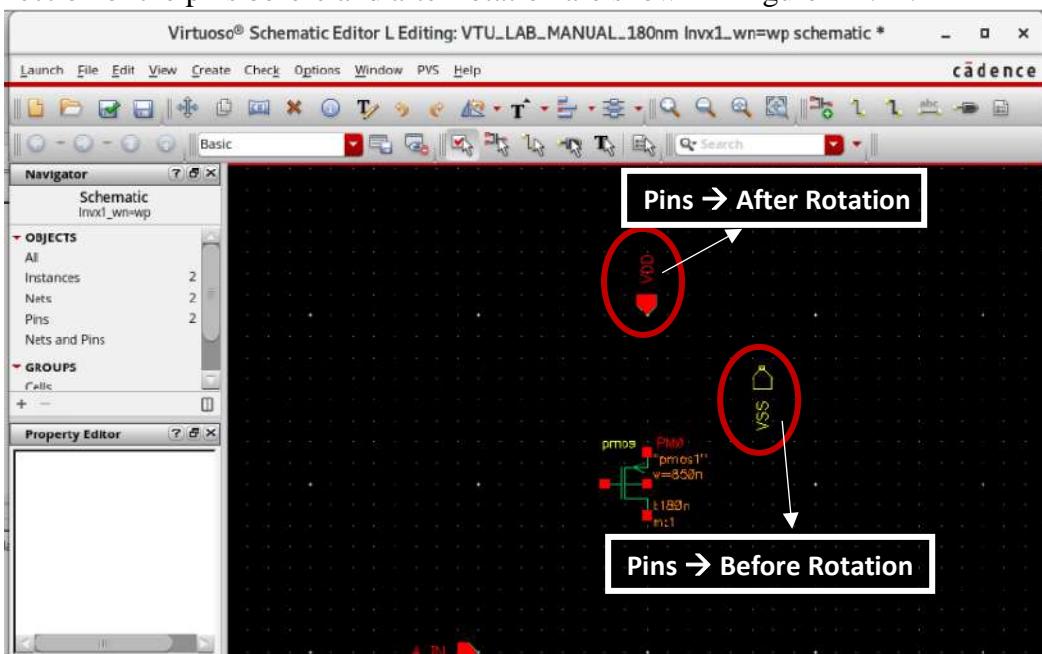


Figure – 1.22: Pins Before and After Rotation

The Schematic Editor window after pin placement is shown in Figure – 1.23.

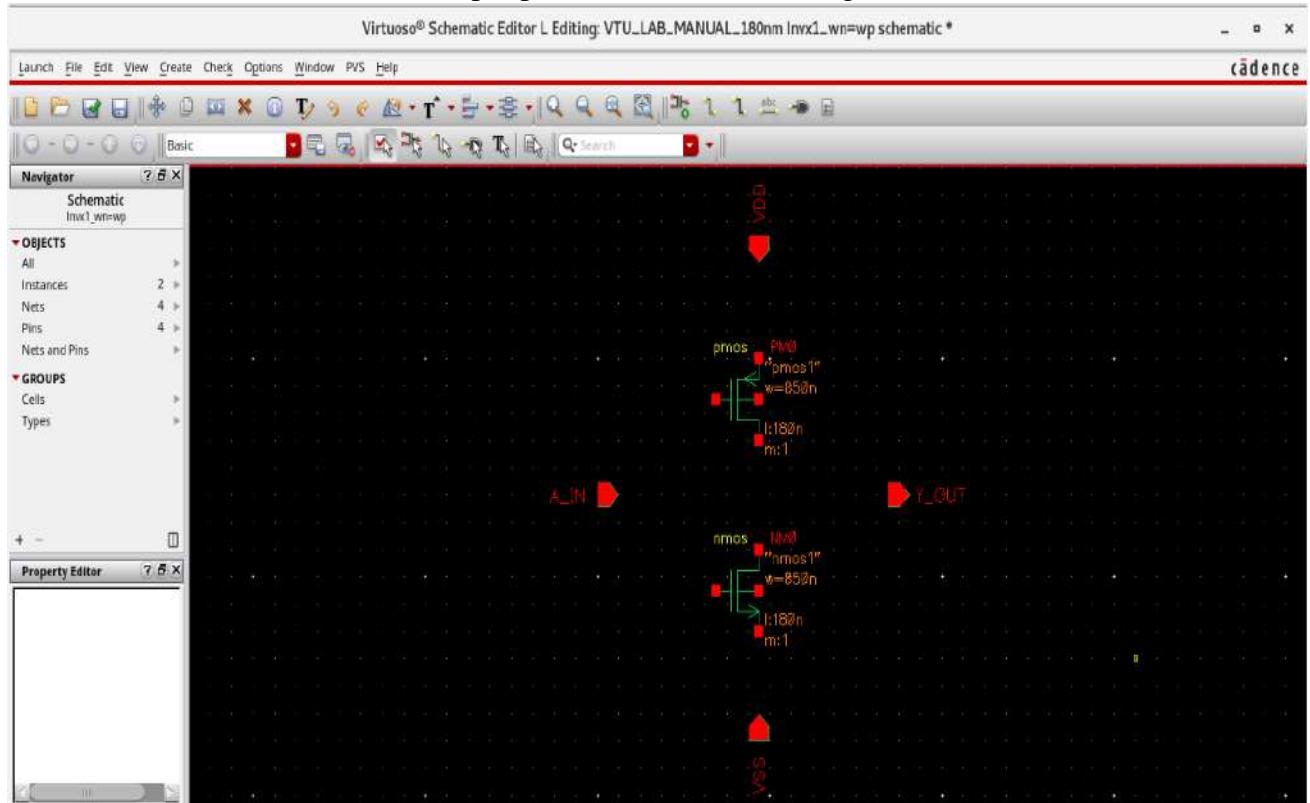


Figure – 1.23: Schematic Editor after pin placement

ADD WIRE:

For connecting the pins and the terminals, click on “Create → Wire” from the top menu (or) use the bind key ‘W’ (or) the icon from the top menu as shown in Figure – 1.24.

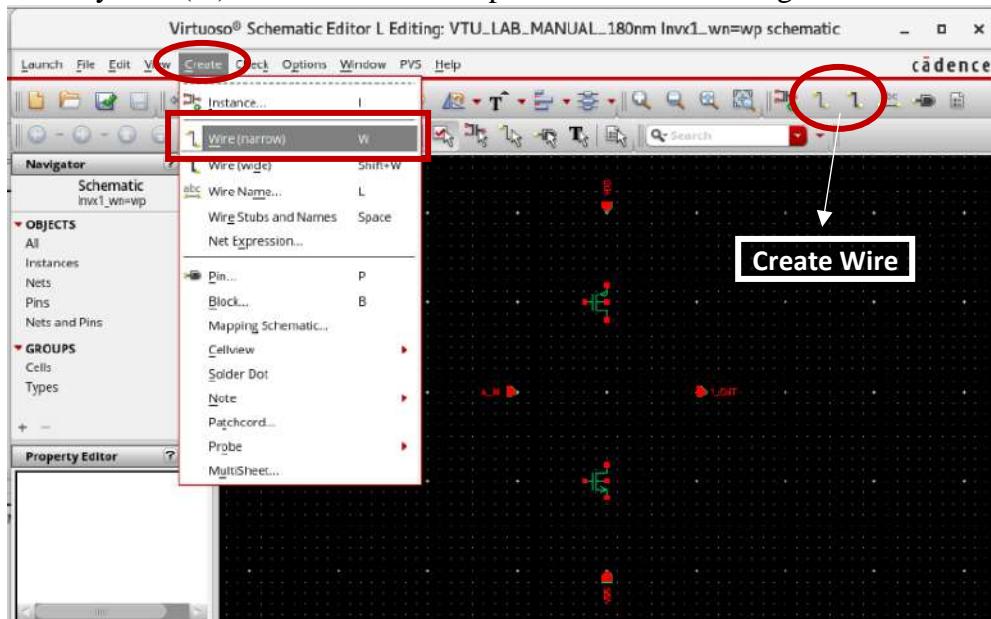


Figure – 1.24: Create → Wire

Use the left mouse click to start / complete the wire from one terminal / pin to another. The complete Schematic after connecting the pins and terminals for all the three conditions $W_N = W_P$, $W_N = 2 * W_P$, $W_N = W_P / 2$ is shown in Figure – 1.25(a), 1.25(b) and 1.25(c) respectively.

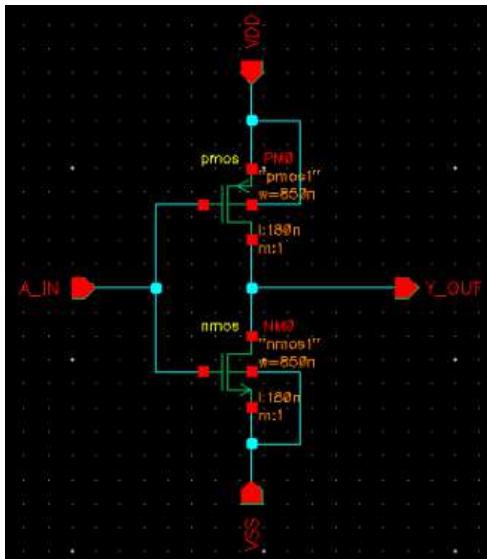


Figure – 1.25(a): $W_N = W_P$

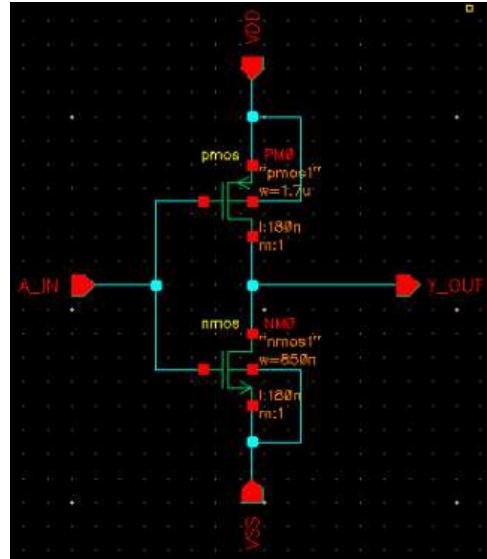


Figure – 1.25(b): $W_N = 2 * W_P$

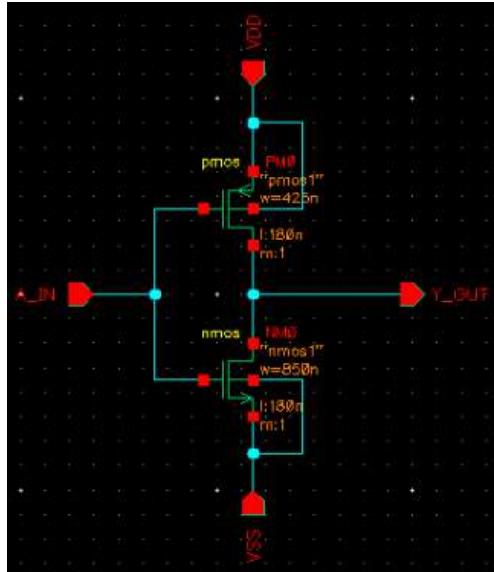


Figure – 1.25(c): $W_N = W_P / 2$

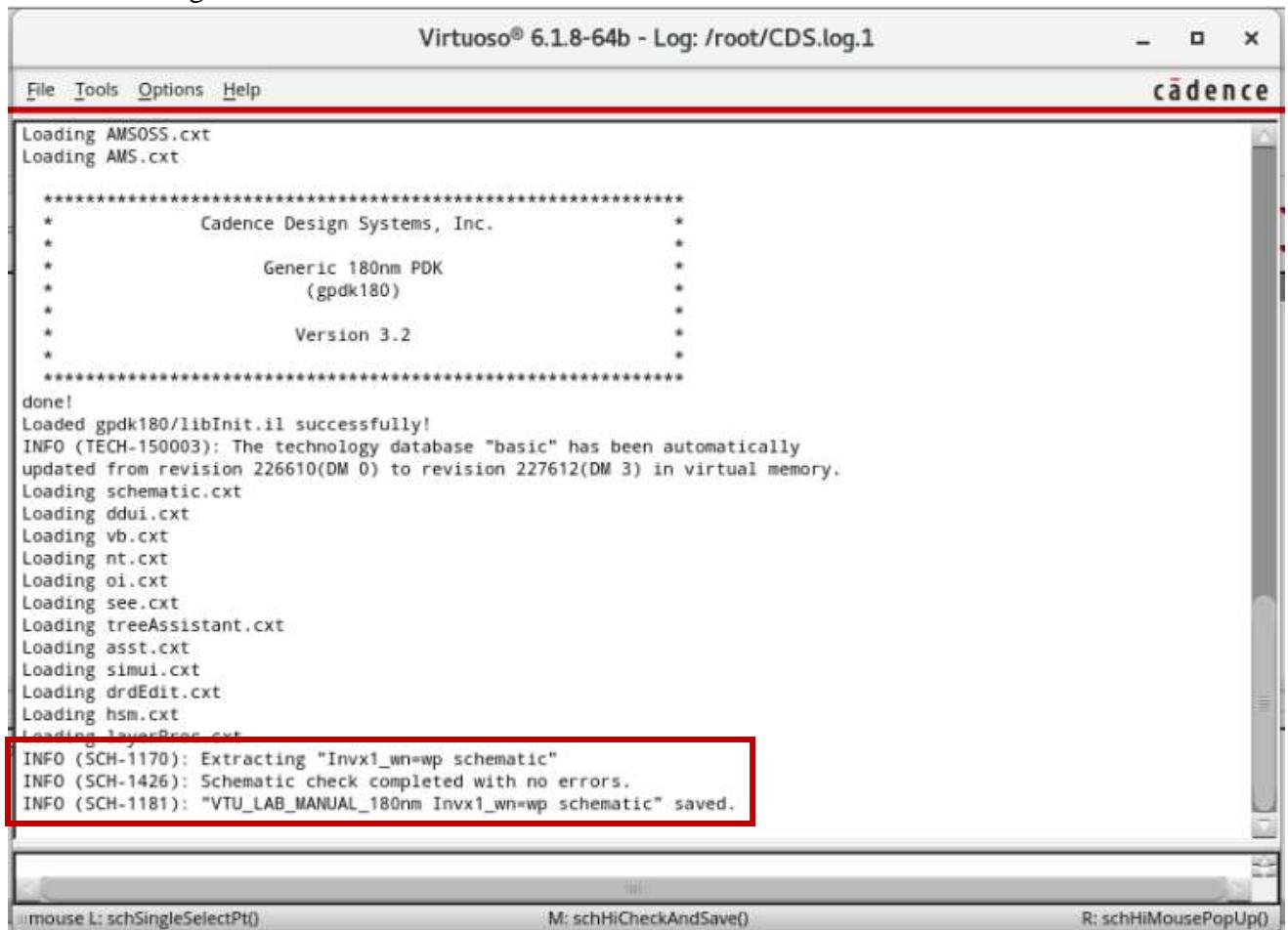
CHECK AND SAVE THE DESIGN:

It is mandatory to save the design before we move ahead to the Simulation and there are two options, “Save” and “Check and Save” as in Figure – 1.26.



Figure – 1.26: “Check and Save” and “Save” option

“Save” option saves the design as it is and “Check and Save” option checks for discontinuities like floating net or terminal and provides the “error” or “warning” messages accordingly and then saves the design. Sample message can be seen in the “Command Interpreter Window” as shown in Figure – 1.27.



```

Virtuoso® 6.1.8-64b - Log: /root/CDS.log.1

File Tools Options Help cadence

Loading AMSOSS.cxt
Loading AMS.cxt

*****
*          Cadence Design Systems, Inc.      *
*                                              *
*          Generic 180nm PDK                 *
*          (gdk180)                         *
*                                              *
*          Version 3.2                      *
*                                              *
*****done!
Loaded gdk180/libInit.il successfully!
INFO (TECH-150003): The technology database "basic" has been automatically
updated from revision 226610(DM 0) to revision 227612(DM 3) in virtual memory.
Loading schematic.cxt
Loading ddui.cxt
Loading vb.cxt
Loading nt.cxt
Loading oi.cxt
Loading see.cxt
Loading treeAssistant.cxt
Loading asst.cxt
Loading simui.cxt
Loading drdEdit.cxt
Loading hsm.cxt
Loading layerProc.cxt
INFO (SCH-1170): Extracting "Invx1_wn=wp schematic"
INFO (SCH-1426): Schematic check completed with no errors.
INFO (SCH-1181): "VTU_LAB_MANUAL_180nm Invx1_wn=wp schematic" saved.

```

Figure – 1.27: Message after selecting “Check and Save”

SYMBOL CREATION:

A Symbol view is very important in a design process to make use of a Schematic in a hierarchy. To create a symbol, select “**Create → Cellview → From Cellview**” from the top menu as shown in Figure – 1.28.

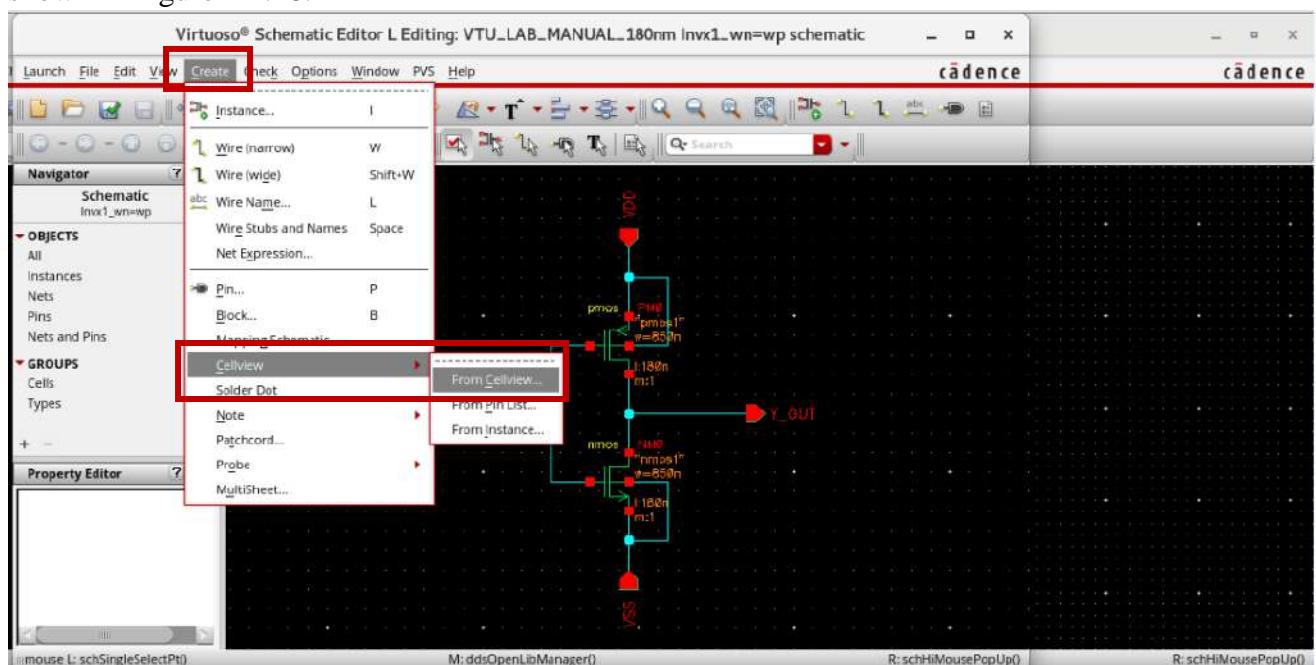


Figure – 1.28: **Create → Cellview → From Cellview**

Verify the Library Name, Cell Name, From View Name, To View Name, etc., as shown in Figure – 1.29 and Click on “OK”.

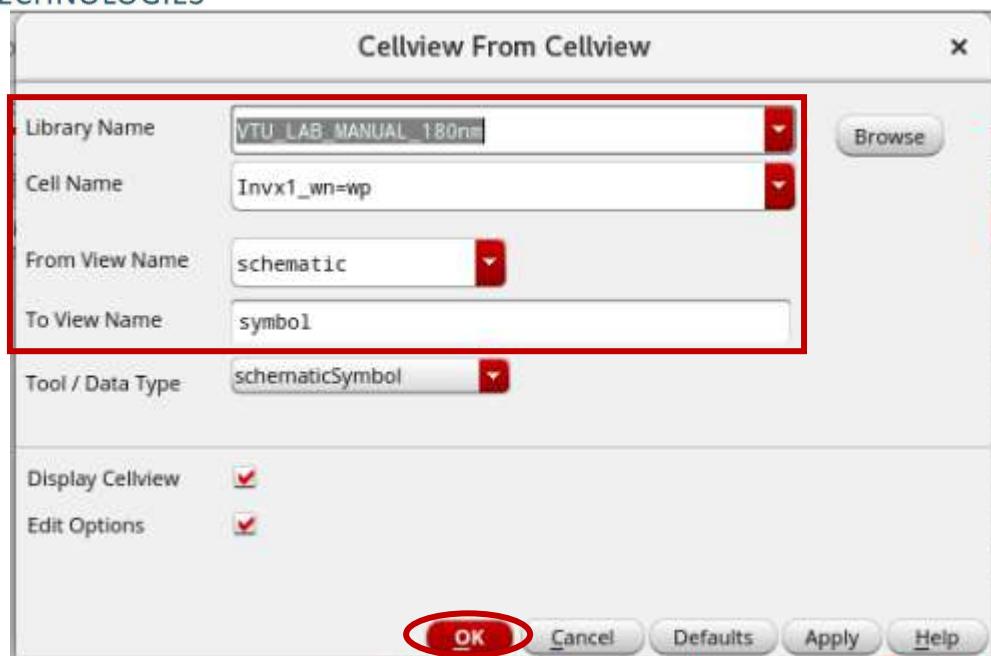


Figure – 1.29: “Cellview From Cellview” window

The “Symbol Generation Options” window can be seen as shown in Figure – 1.30.

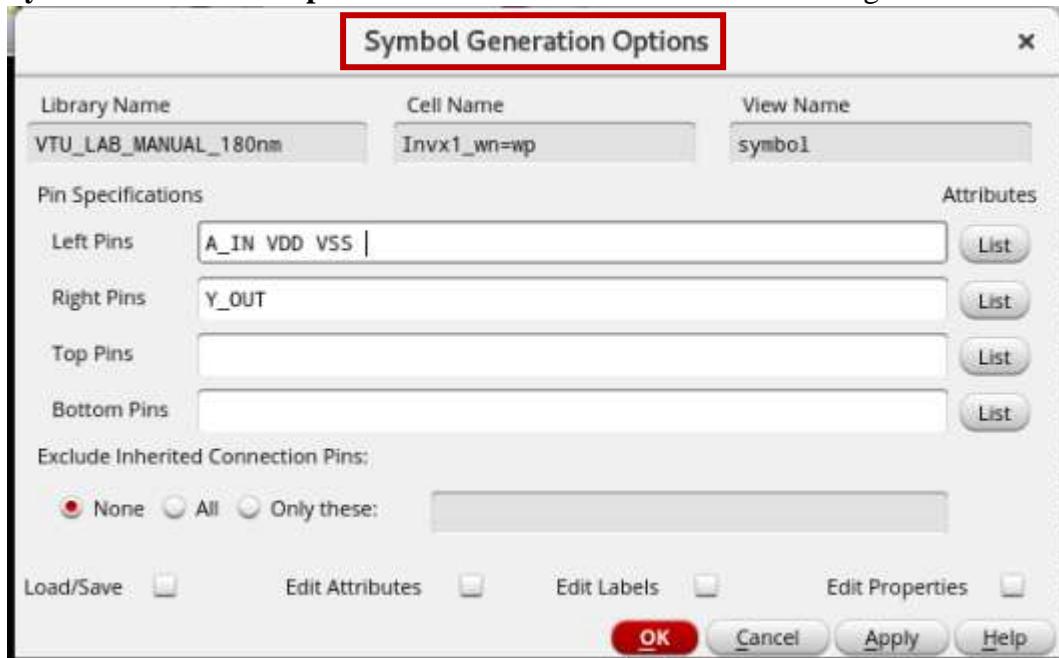


Figure – 1.30: “Symbol Generation Options” window

The pin location on the symbol can be fixed using the options **Left Pins**, **Right Pins**, **Top Pins** and **Bottom Pins**. Assign the pins and click on ‘OK’ as shown in Figure – 1.31.

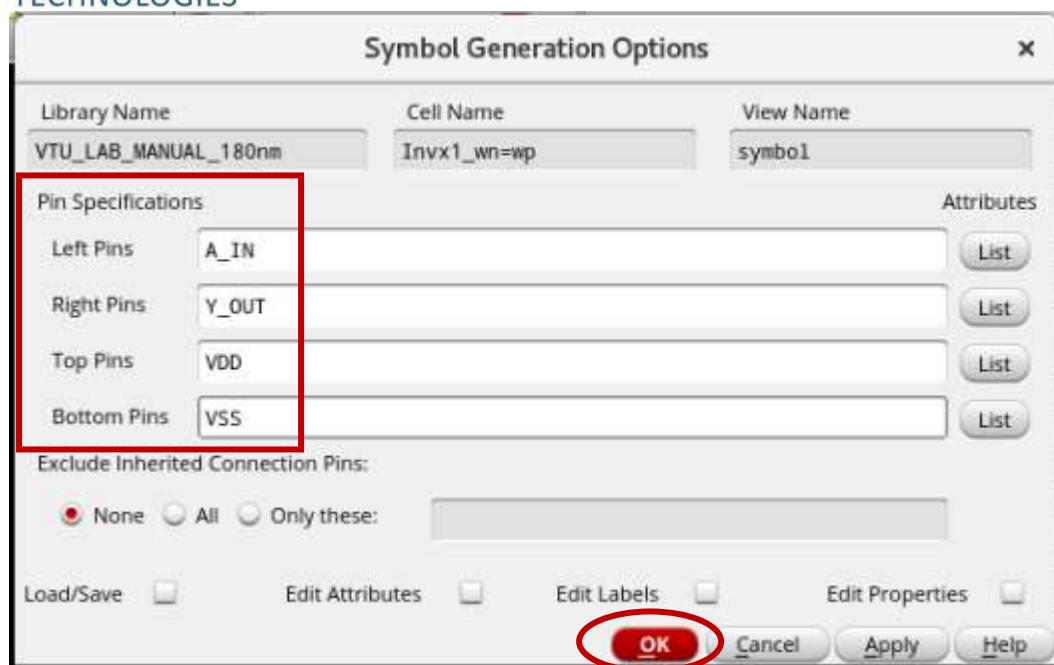


Figure – 1.31: “Symbol Generation Options” window

The “**Virtuoso Symbol Editor**” window pops up with a default symbol based on the Pin Assignment as shown in Figure – 1.32.

Create Circle **Create Polygon** **Create Ellipse** **Create Line** **Create Arc**

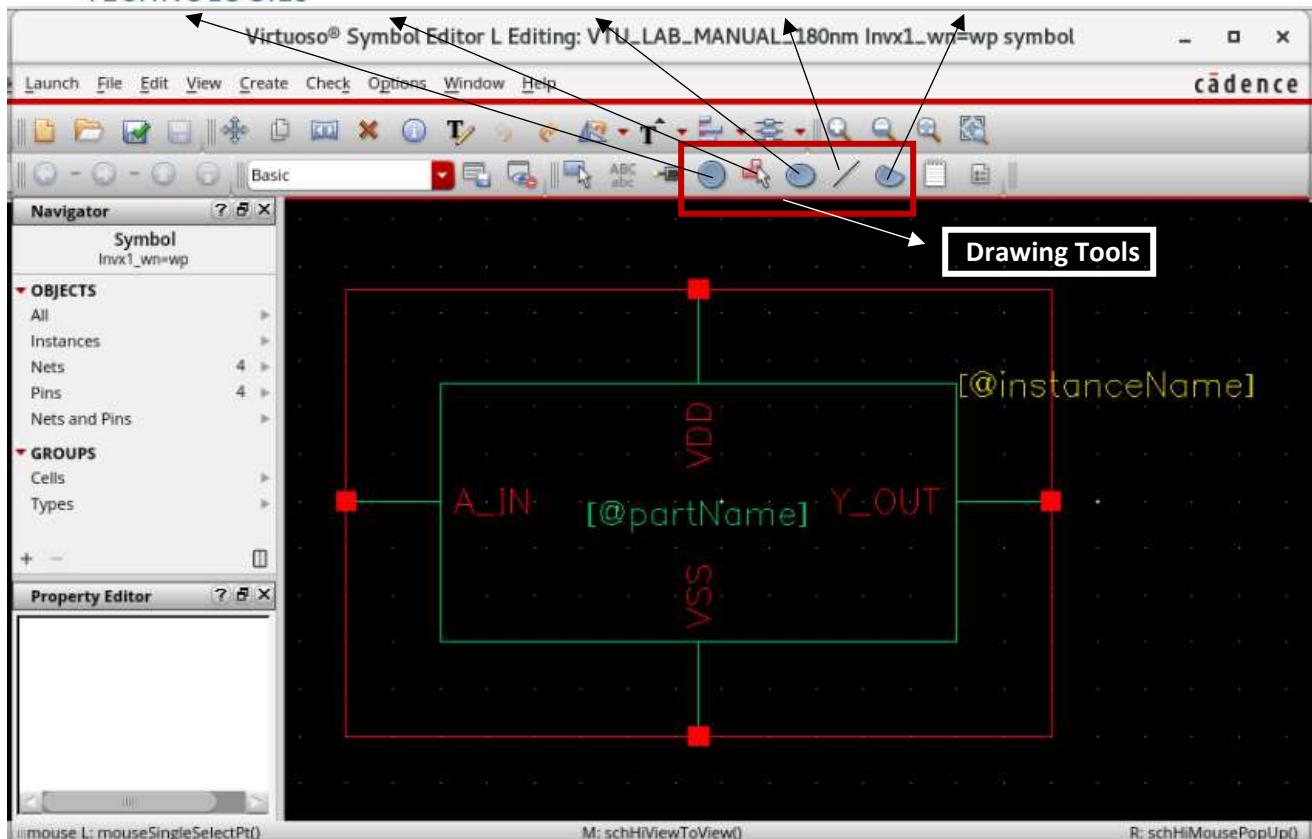


Figure – 1.32: “Virtuoso Symbol Editor” window with default symbol

SYMBOL MODIFICATION:

The symbol can be modified using the drawing tools from the top menu as shown in Figure – 1.32.

To modify the symbol, remove the inner rectangle (green), highlighted in Figure – 1.33(a). To remove the inner rectangle (green), place the mouse pointer within and make a left mouse click to select the entire rectangle as shown in Figure – 1.33(b). Click on ‘Delete’ in the keyboard to remove the rectangle as shown in Figure – 1.33(c).

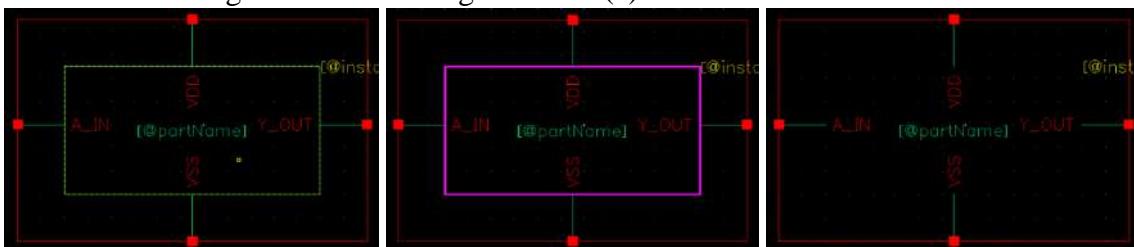


Figure – 1.33(a)

Figure – 1.33(b)

Figure – 1.33(c)

Figure – 1.33(a): Inner Rectangle Highlighted, Figure – 1.33(b): Inner Rectangle Selected, Figure – 1.33(c): Inner Rectangle Deleted

Since the focus is to design an Inverter, to create a triangle, use the “Create Line” option as shown in Figure – 1.32. Use the same procedure as “wiring the schematic” to create the triangle.

The symbol, after creating the triangle can be seen as shown in the Figure – 1.34.

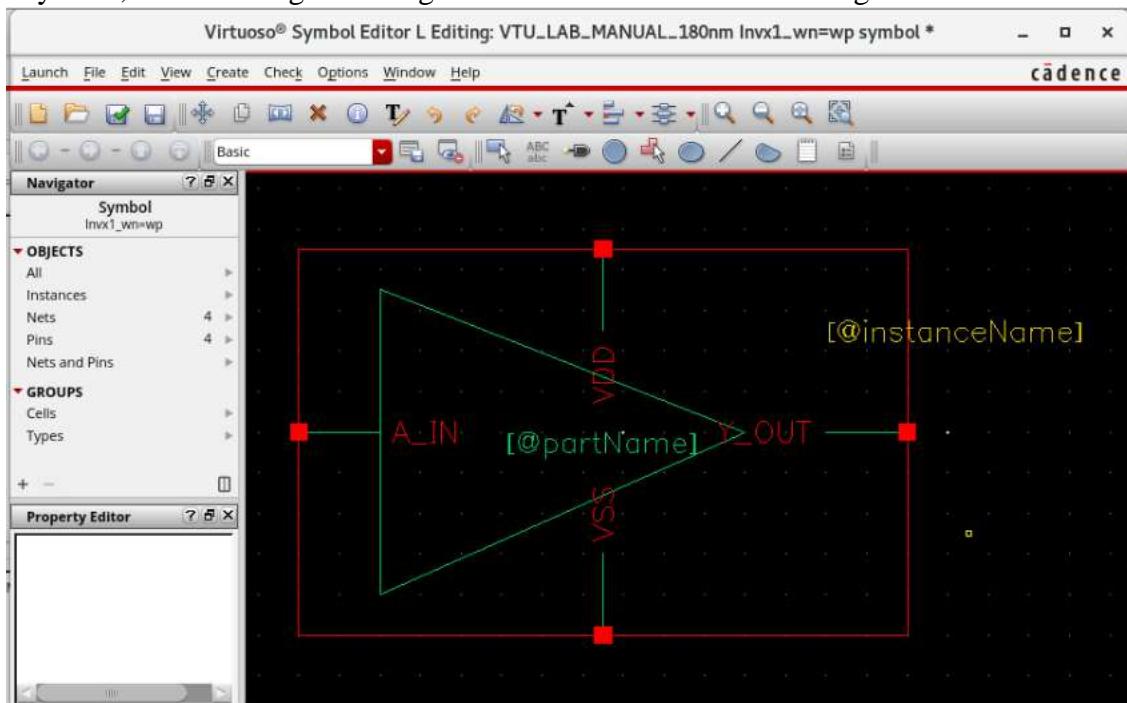


Figure – 1.34: Symbol after creating the Triangle

To create a bubble, use “Create Circle” option as shown in Figure – 1.32, place the mouse pointer at the center between the ‘Triangle’ and the ‘Output Pin’, make a left mouse click and expand the circle and make a left mouse click to fix its size as shown in Figure – 1.35. Click on “Check and Save” option to ‘Save’ the symbol.

at the center between the ‘Triangle’ and the ‘Output Pin’, make a left mouse click and expand the circle and make a left mouse click to fix its size as shown in Figure – 1.35. Click on “Check and Save” option to ‘Save’ the symbol.

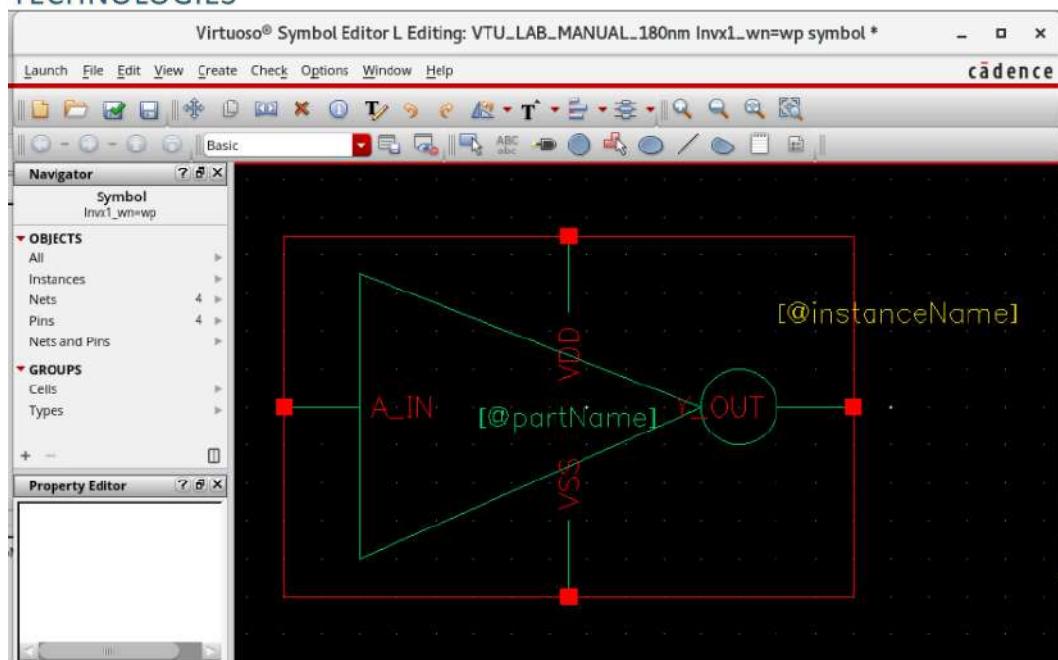


Figure – 1.35: Customized Symbol of an Inverter

(1) TEST CIRCUIT FOR SIMULATION:

The Test Circuit can be created using the symbol created in the previous section. To create a test circuit, create a “New Cellview” with a different “Cell Name” as shown in Figure – 1.36.

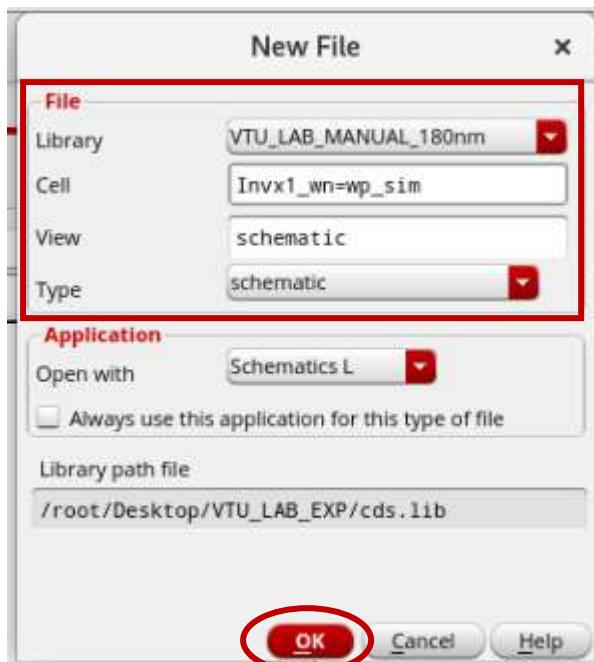


Figure – 1.36: New Cellview for Test Circuit

Use the “Add Instance” option, select the respective Library, Cell and View as in Figure – 1.37 to instantiate the symbol.

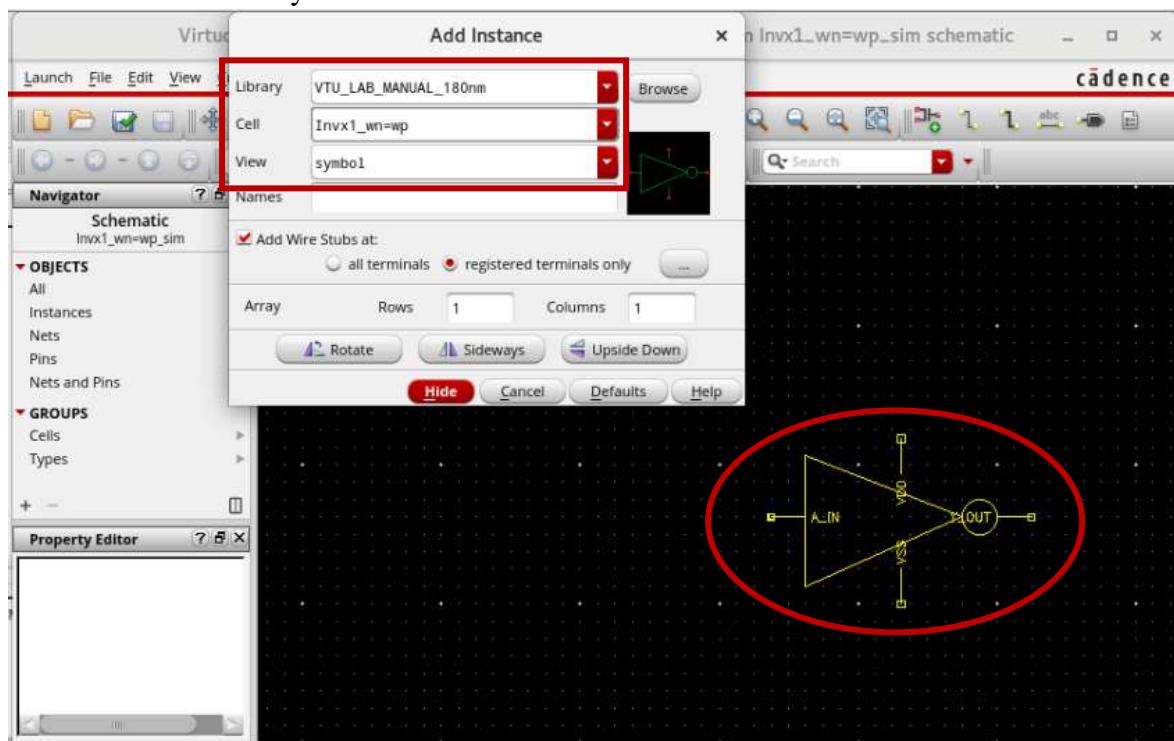


Figure – 1.37: Symbol Instantiation for the Test Circuit

The remaining devices to be included on the Schematic and its properties are given below in Table - 4.

Table – 4: Properties of vdc, vpulse, cap and gnd

| Library Name | Cell Name | Comments / Properties |
|--------------|-----------|---|
| analogLib | Vdc | DC voltage = 1.8 V |
| analogLib | Vpulse | Voltage 1 = 0 V, Voltage 2 = 1.8 V, Period = 20n s, Delay time = 10n s, Rise time = 1p s, Fall time = 1p s, Pulse width = 10n s |
| analogLib | Cap | Capacitance = 100f F |
| analogLib | Gnd | |

The screenshot of the device properties for the instances vdc, vpulse, cap and gnd are shown in Figure – 1.38, Figure – 1.39, Figure – 1.40 and Figure – 1.41. The complete Test Schematic after wiring is shown in Figure – 1.42.

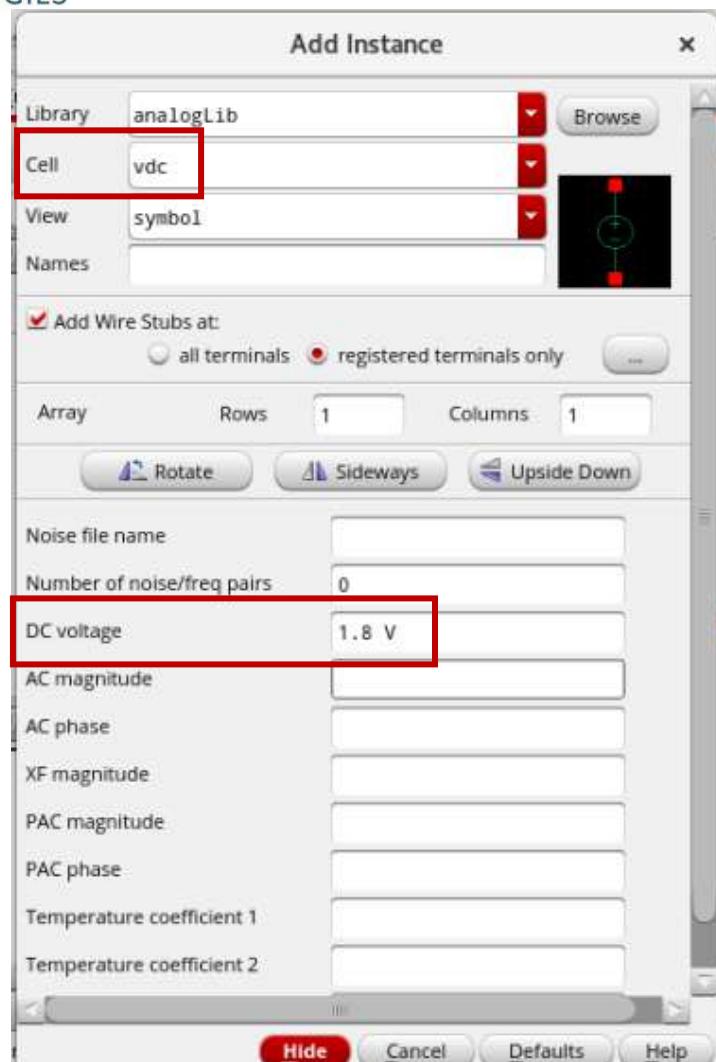


Figure – 1.38: Instantiating “vdc”

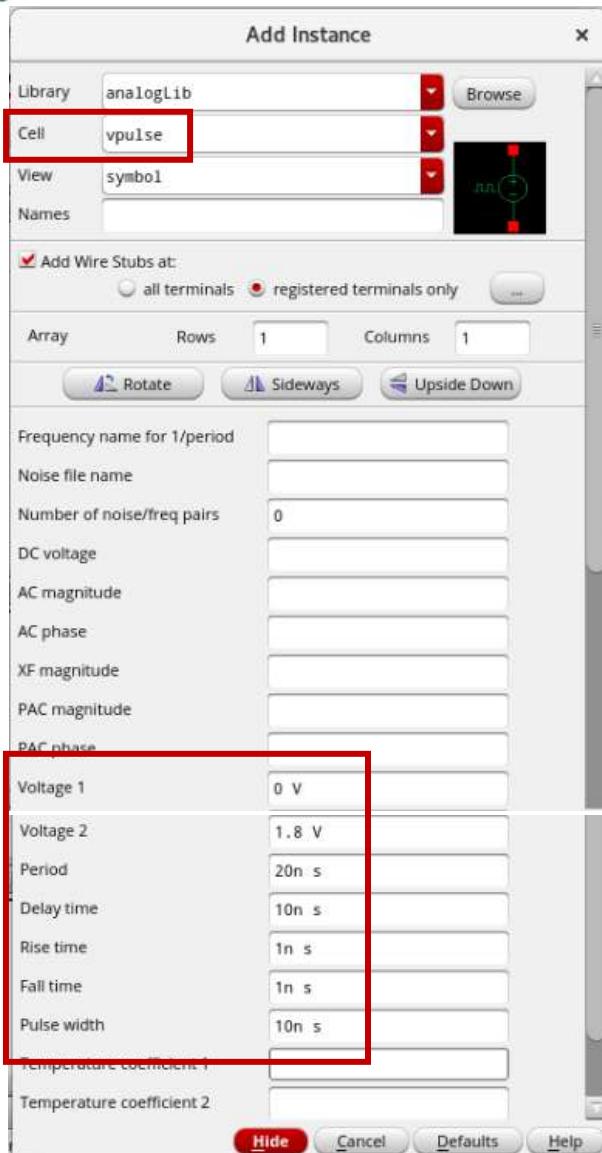


Figure – 1.39: Instantiating “vpulse”

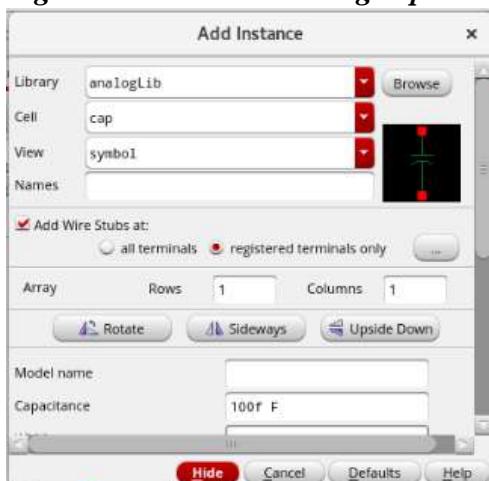


Figure – 1.40: Instantiating “cap”



Figure – 1.41: Instantiating “gnd”

The complete circuit after instantiating all the devices and interconnections is shown in Figure – 1.42.

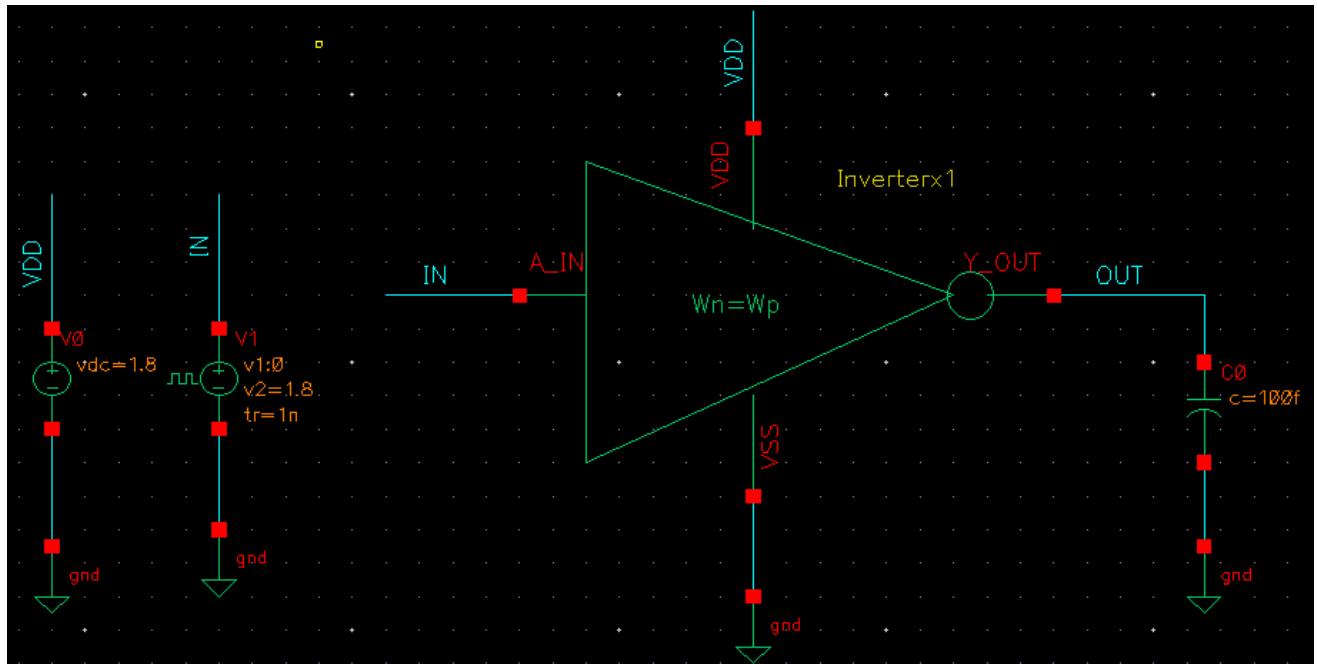


Figure – 1.42: Complete Test Schematic

To **Label** the nets, click on “L” in the keyboard. The “**Create Wire Name**” window pops up as shown in Figure – 1.43. Name the nets, different net names can be mentioned at the same instance of time by separating them with “**Spaces**”, same net names can also be repeated as per the requirement and click on “**Hide**” as shown in Figure – 1.44.

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Figure – 1.43: Create Wire Name Window

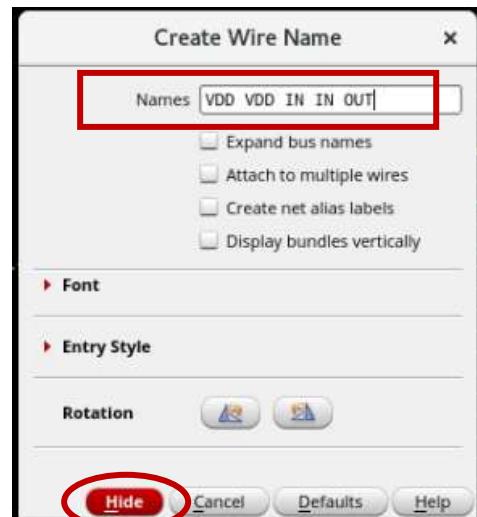


Figure – 1.44: Wire Names

The “Wire Name before placement” can be seen in Figure – 1.45. The “Dot” just under the wire name has to be placed over the “wire” and make a left mouse click to fix it. The “Placed Wire Name” can be seen in Figure – 1.45.

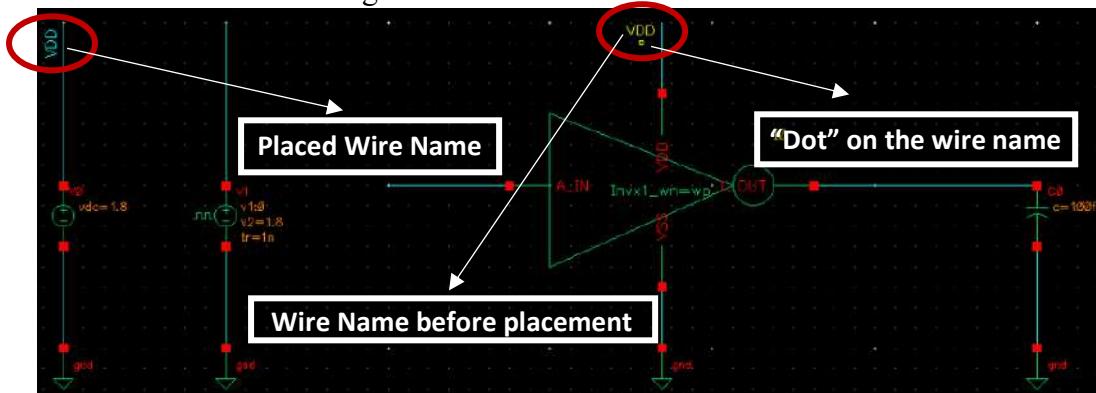


Figure – 1.45: Wire Name before and after its Placement

The complete schematic after placing all the wire names is shown in Figure – 1.46. “Check and Save” the Test Schematic.

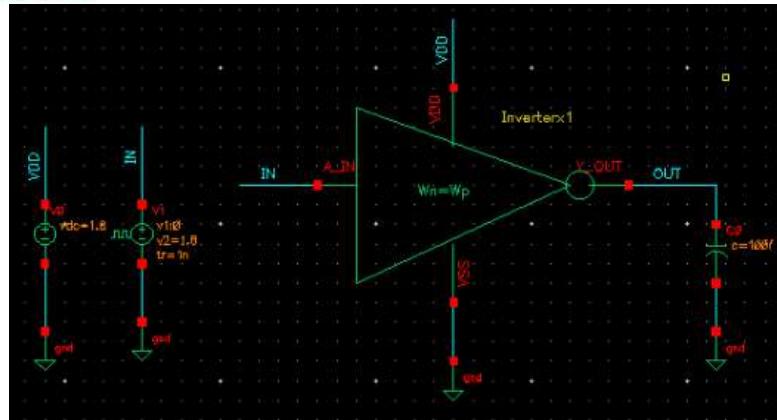


Figure – 1.46: Complete Test Schematic

FUNCTIONAL SIMULATION WITH SPECTRE:

To simulate the design and perform the DC Analysis and Transient Analysis for the CMOS Inverter, click on “**Launch → ADE L**” from the top menu of the Test Schematic Cellview as shown in Figure – 1.47.

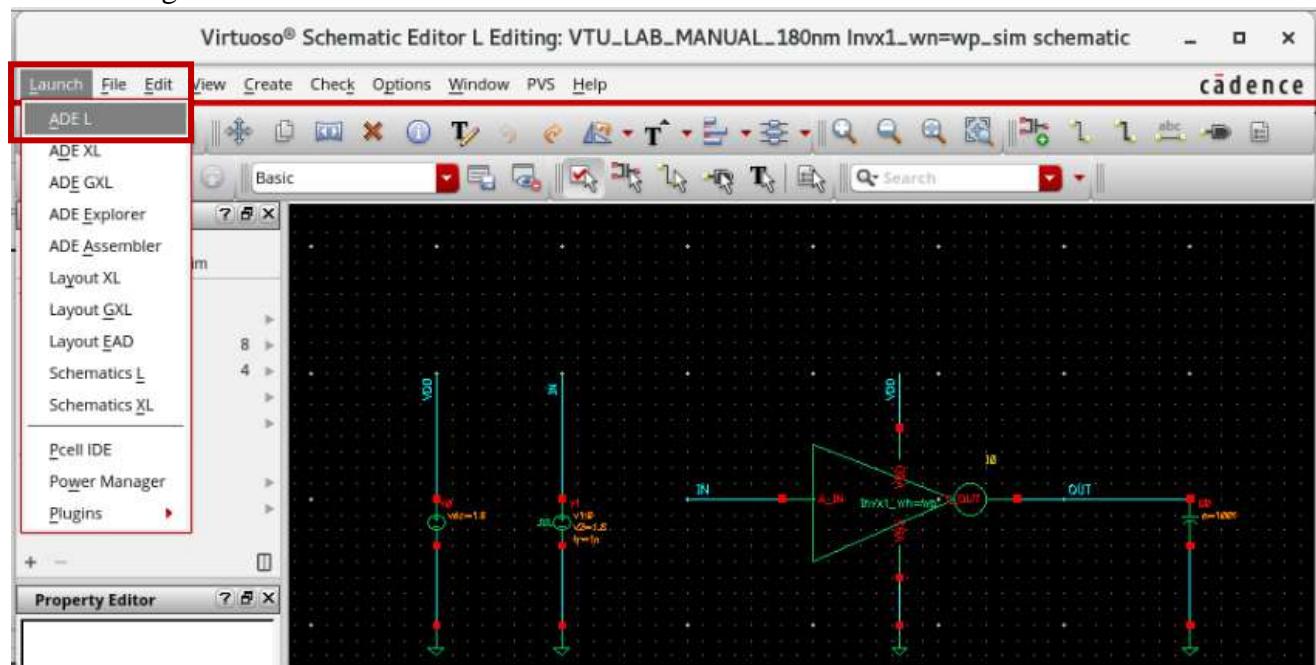


Figure – 1.47: Launch → ADE L

The “ADE L” window pops up as shown in Figure – 1.48.

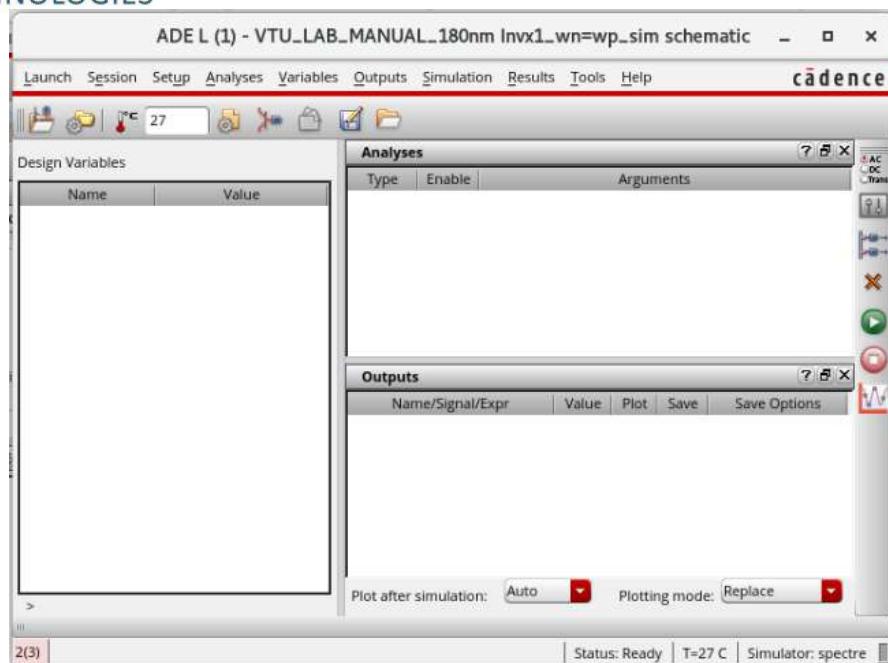


Figure – 1.48: ADE L Window

Before running the simulation, check for the Simulator and Model Libraries.

SELECTING THE SIMULATOR:

To select the Simulator, click on “Setup → Simulator/Directory/Host” as shown in Figure – 1.49.

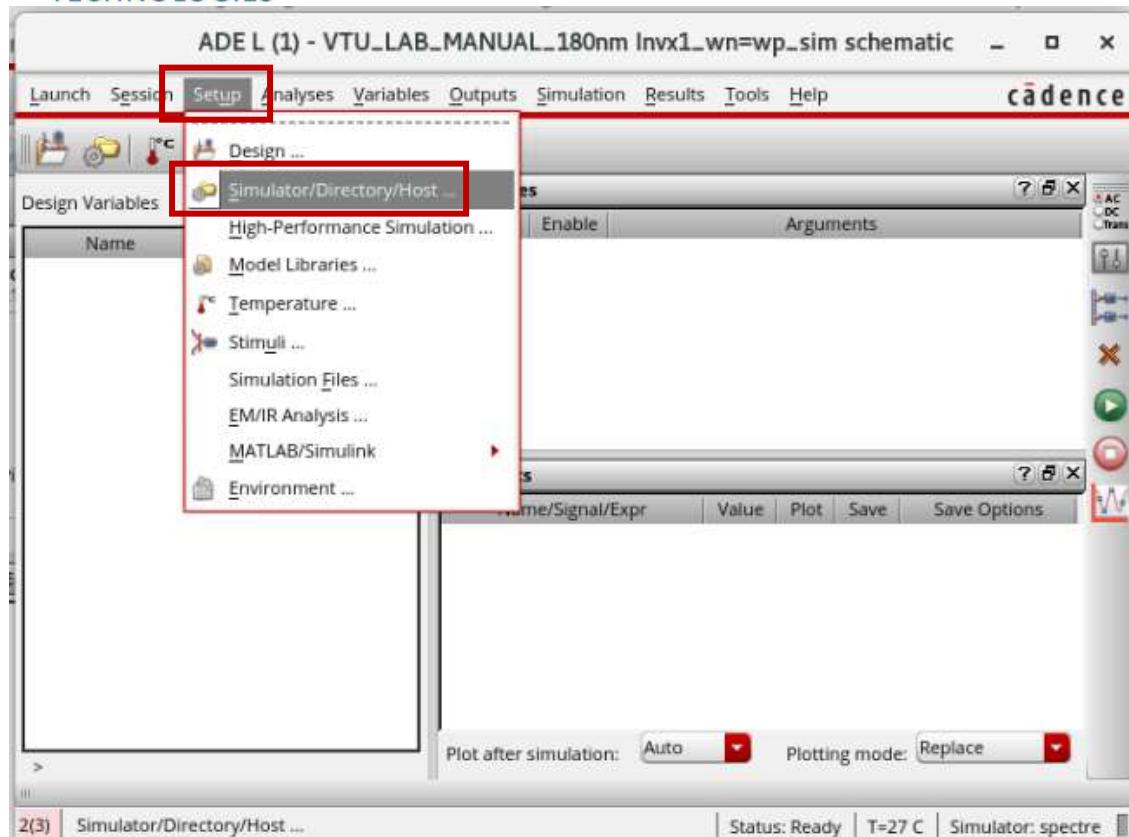


Figure – 1.49: Setup → Simulator/Directory/Host..

The “Choosing Simulator/Directory/Host” window pops up. Select “Simulator → Spectre” and click on “OK” as shown in Figure – 1.50.

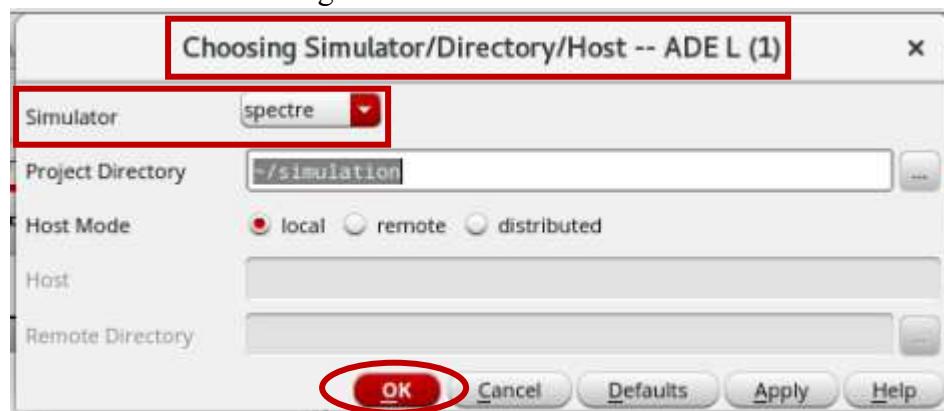


Figure – 1.50: Simulator → Spectre

SELECTING THE MODEL LIBRARIES AND PROCESS CORNERS:

The Model Libraries and Process Corners are important to run the simulation.

To select the “.scs” file with respect to the technology node, select “Setup → Model Libraries” as shown in Figure – 1.51.

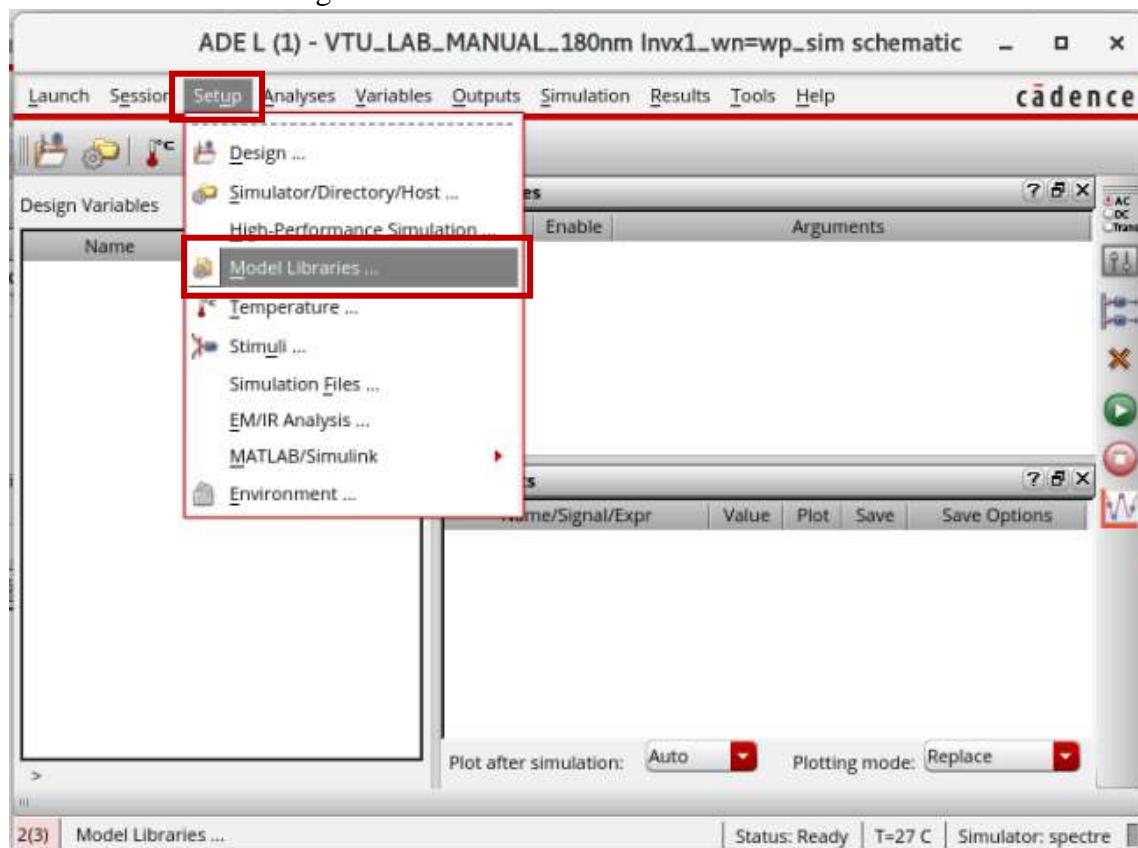


Figure – 1.51: Setup → Model Libraries

The “spectre0: Model Library Setup” window pops up as shown in Figure – 1.52.



Figure – 1.52: “spectre0: Model Library Setup” Window

Select the respective “.scs” file and make a double click under “Section” to select the processing corner of interest using a Left Mouse Click on the drop down and click on “OK” as shown in Figure – 1.53.

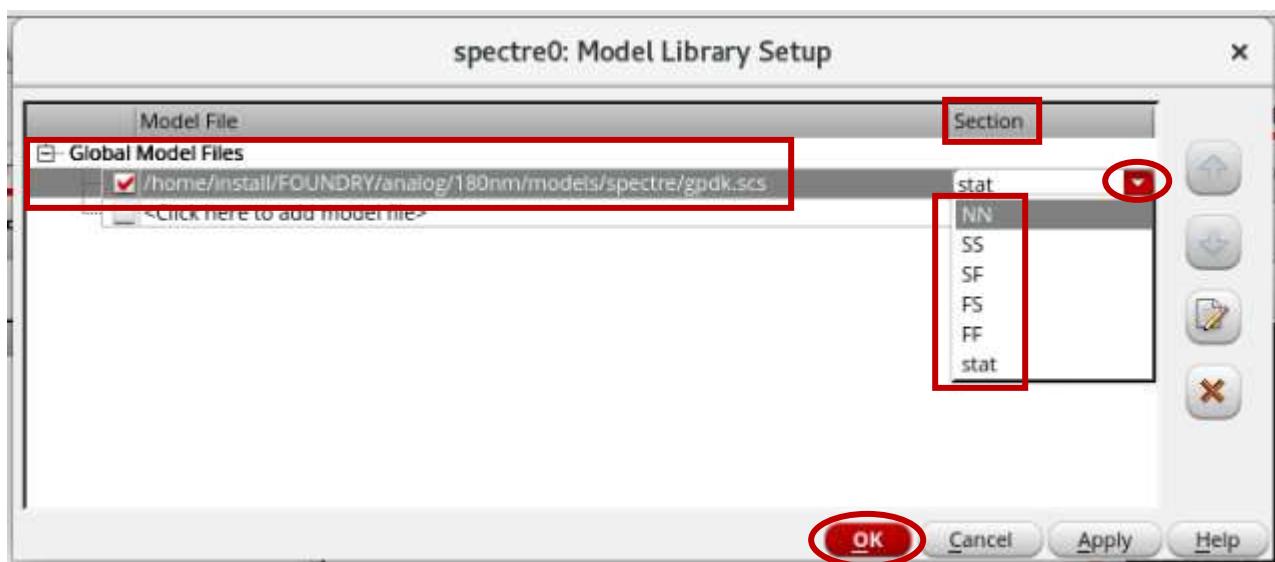


Figure – 1.53: “.scs” file and Processing Corner Selection

SELECTING THE ANALYSIS:

To select the analysis required to be performed on the Test Circuit, select “Analyses → Choose” from the top menu in the ADE L window as shown in Figure – 1.54.

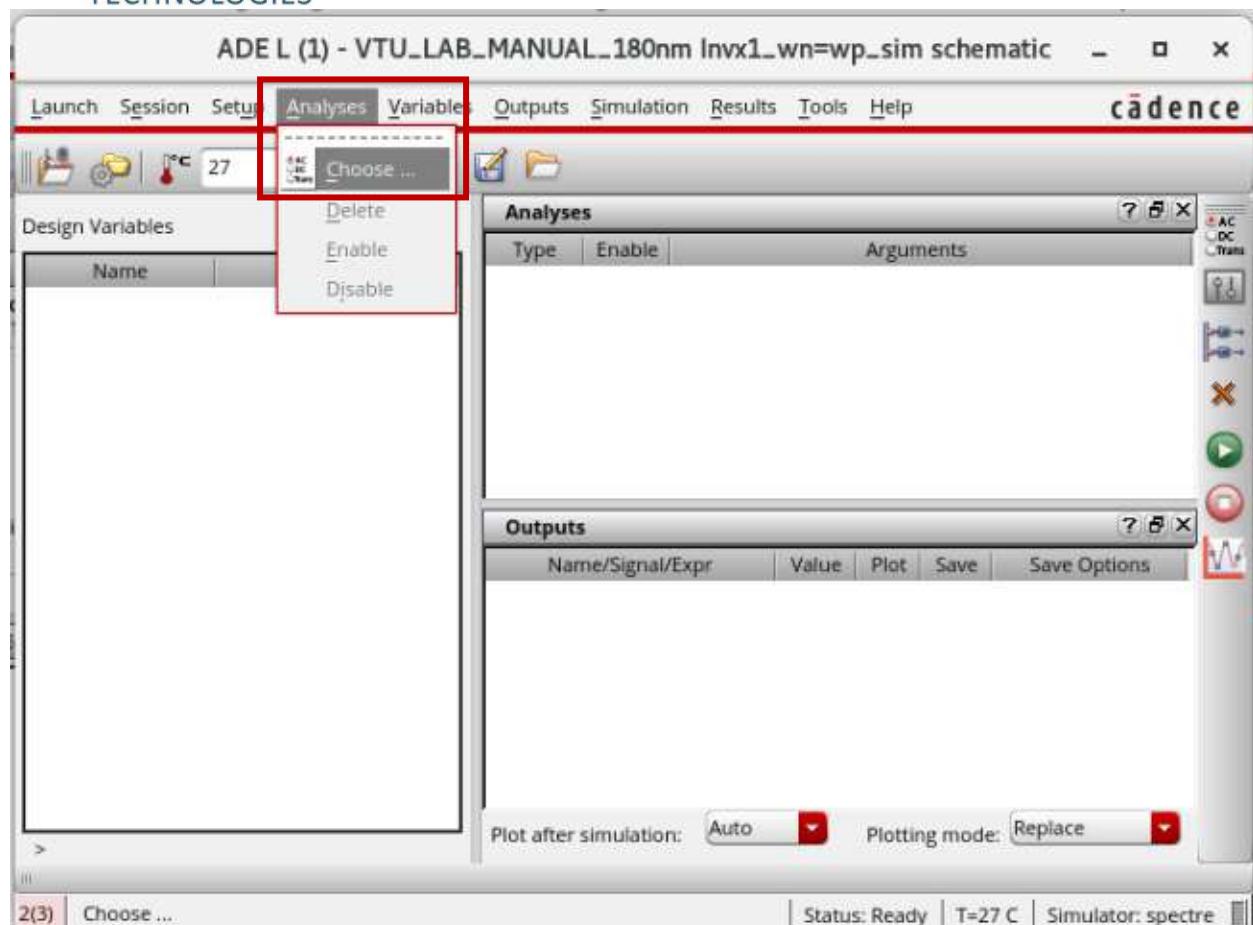


Figure – 1.54: Analyses → Choose

The “Choose Analyses – ADE L” window pops up as shown in Figure – 1.55.

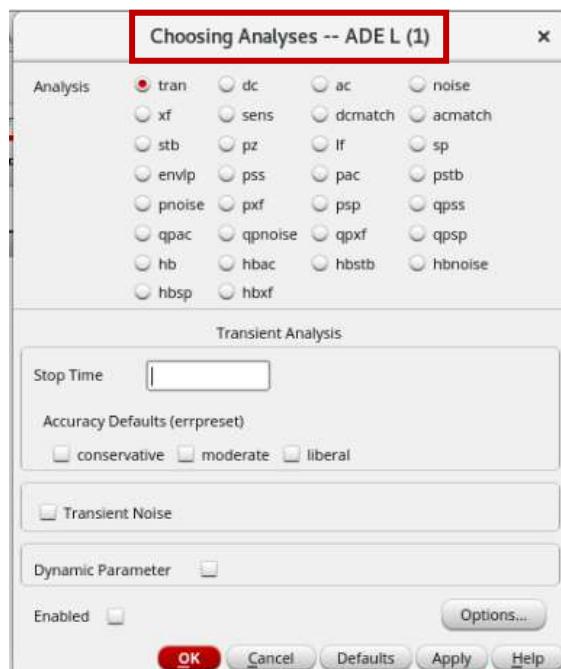


Figure – 1.55: “Choosing Analysis – ADE L” Window

TRANSIENT ANALYSIS:

To set up a “Transient Analysis”, select “tran”, mention the “Stop Time” (for example: 100n), select “Accuracy Defaults” (for example: moderate), click on “Apply” and click on “OK” as shown in Figure – 1.56.

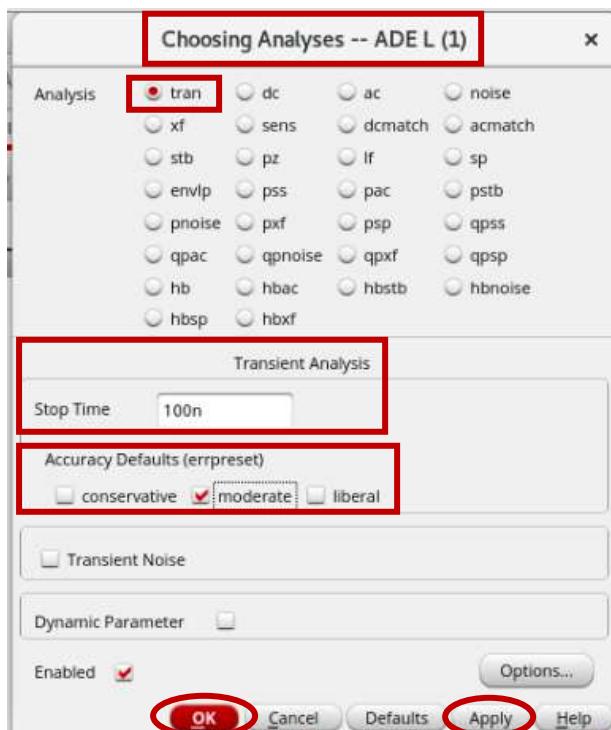


Figure – 1.56: Setup for Transient Analysis

The selected analysis and the arguments can be seen under the “Analyses” tab in the ADE L window as shown in Figure – 1.57.

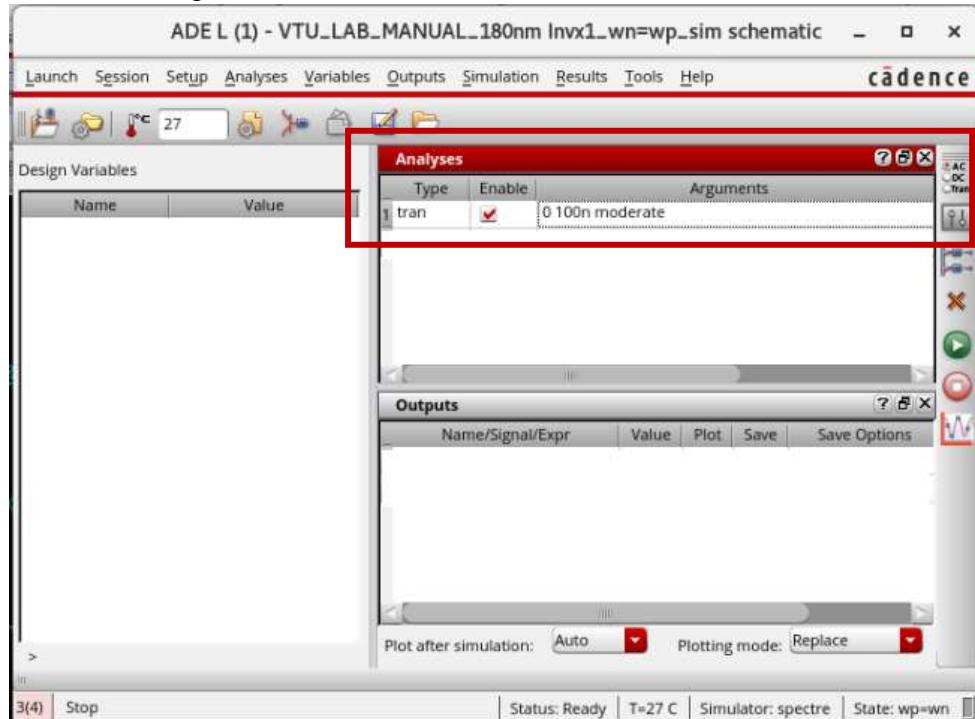


Figure – 1.57: Chosen Analysis in the ADE L window

DC ANALYSIS:

To set up a “DC Analysis”, select “dc” and enable “Save DC Operating Point” as shown in Figure – 1.58.

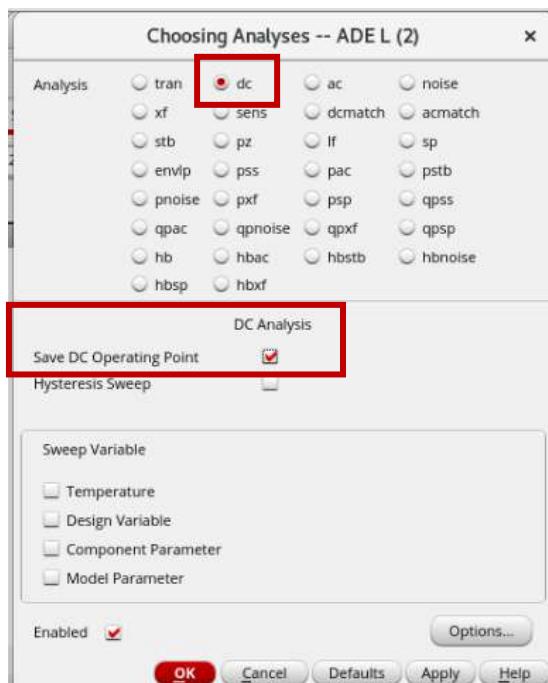


Figure – 1.58: Select “dc”

Enable “Component Parameter”, click on “Select Component” as shown in Figure – 1.59.

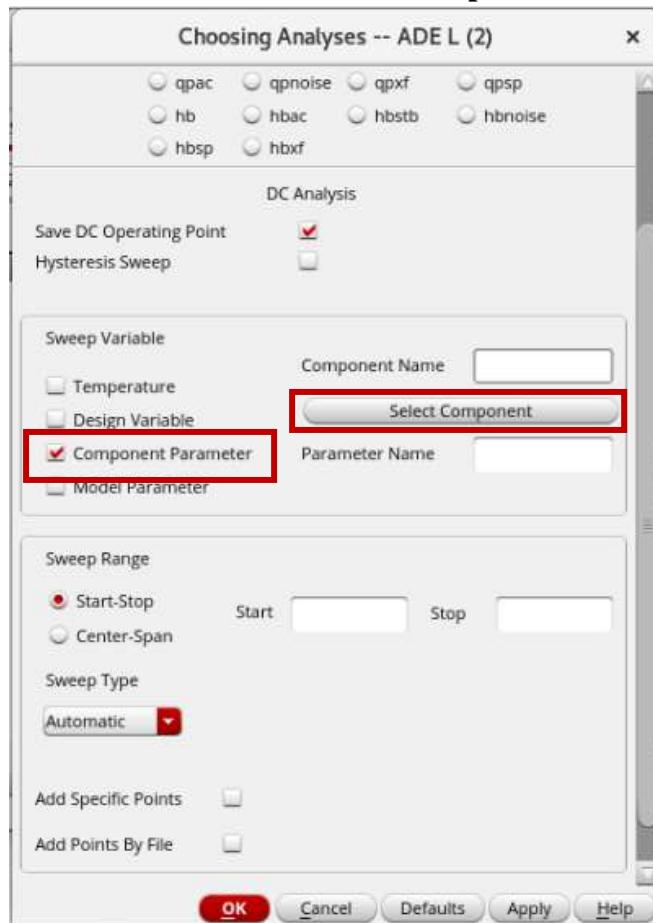


Figure – 1.59: Enable “Component Parameter”

Select the “vpulse” source from the Test Schematic as shown in Figure – 1.60.

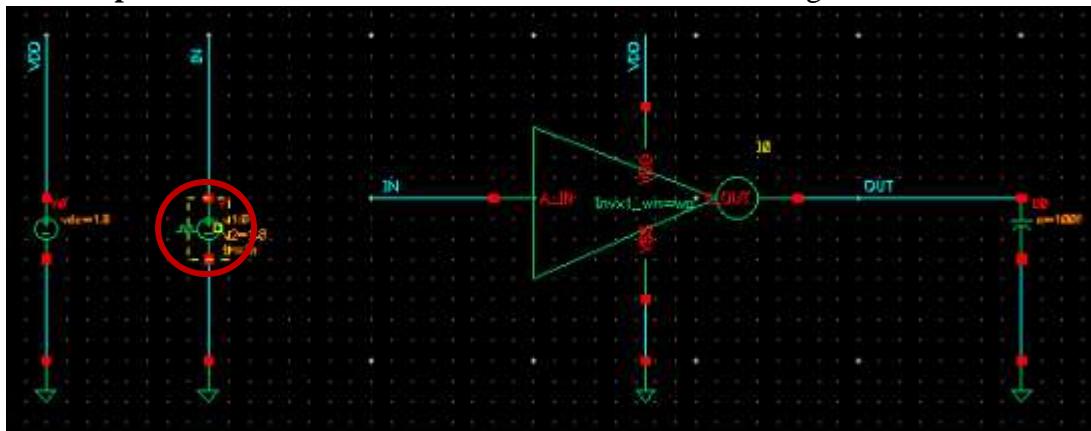


Figure – 1.60: Selecting “vpulse” from the Test Schematic

Select “DC Voltage” from the list of parameters as shown in the “Select Component Parameter” window and click on “OK” as shown in Figure – 1.61.

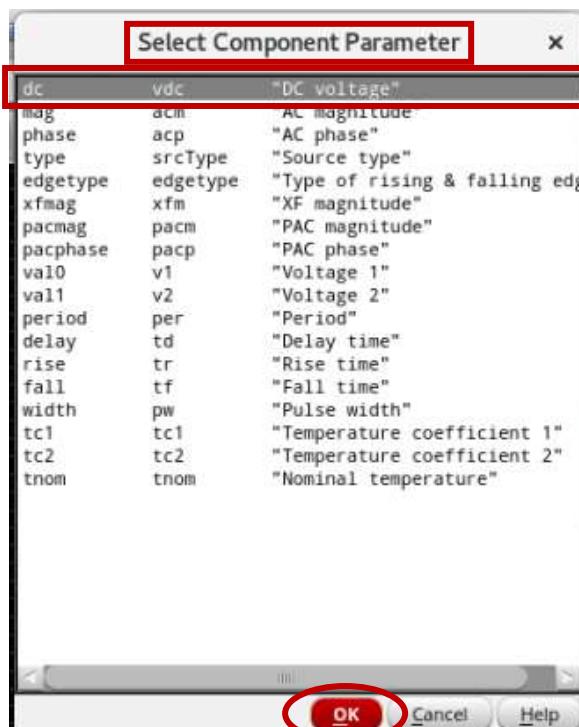


Figure – 1.61: “Select Component Parameter” window

From the “Sweep Range” option, select “Start-Stop” and mention the “Start” value as “0” and “Stop” value as “1.8”, click on “Apply” and click on “OK” as shown in the Figure – 1.62.

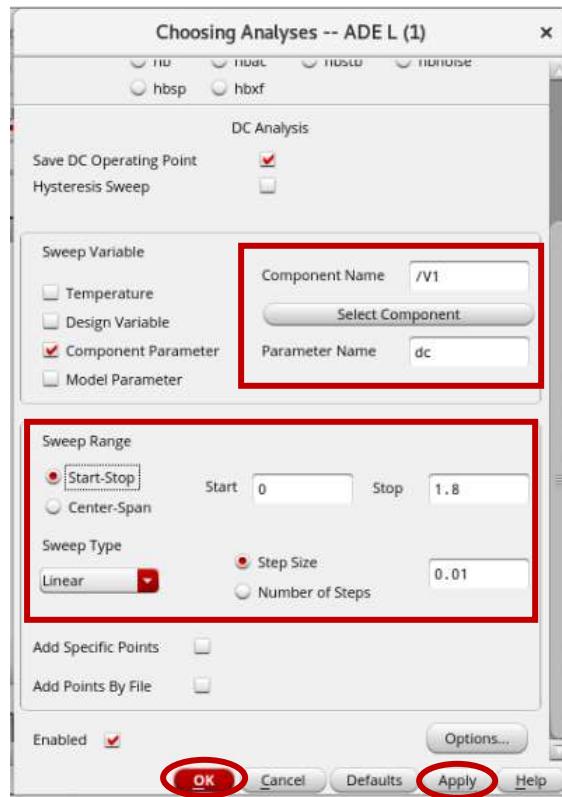


Figure – 1.62: Mention the Sweep Range

The ADE L window is now updated as shown in Figure – 1.63.

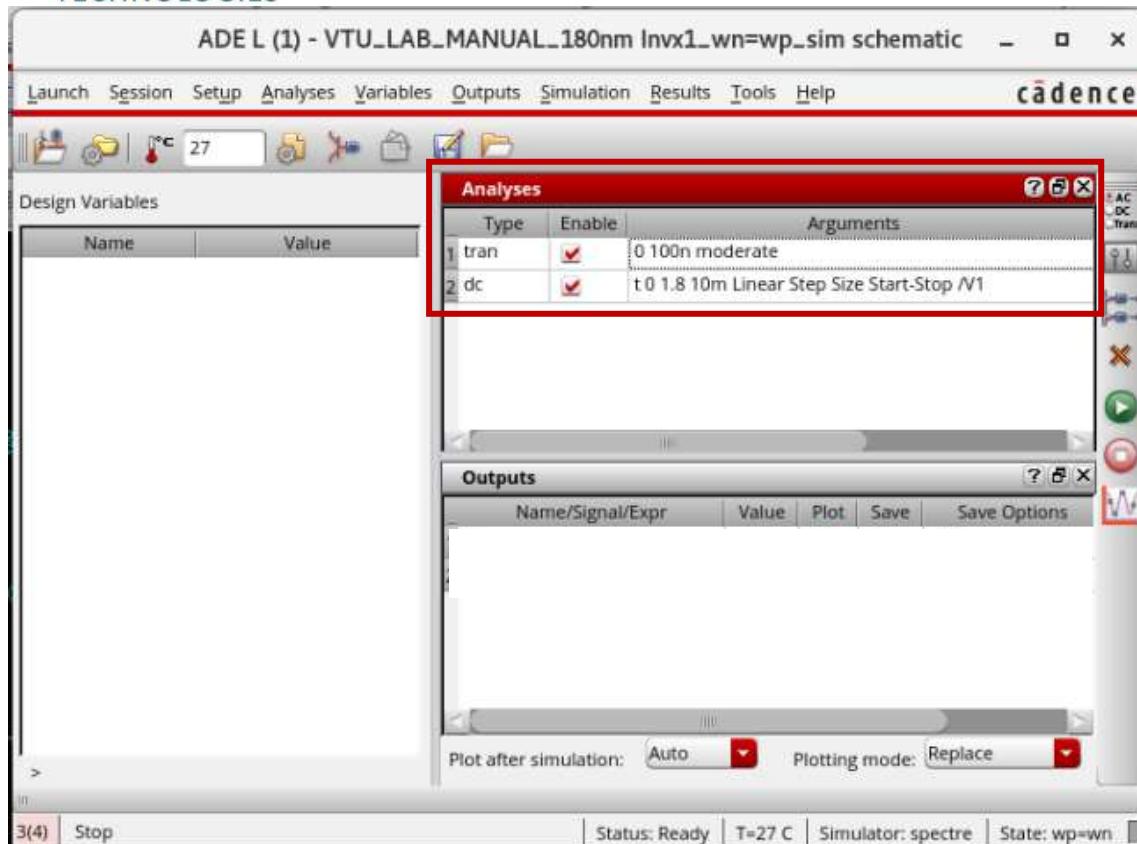


Figure – 1.63: Updated ADE L window

SELECTING THE SIGNALS TO BE PLOTTED:

To select the signals to be plotted, select “Outputs → Setup” from the ADE L window as shown in Figure – 1.64.

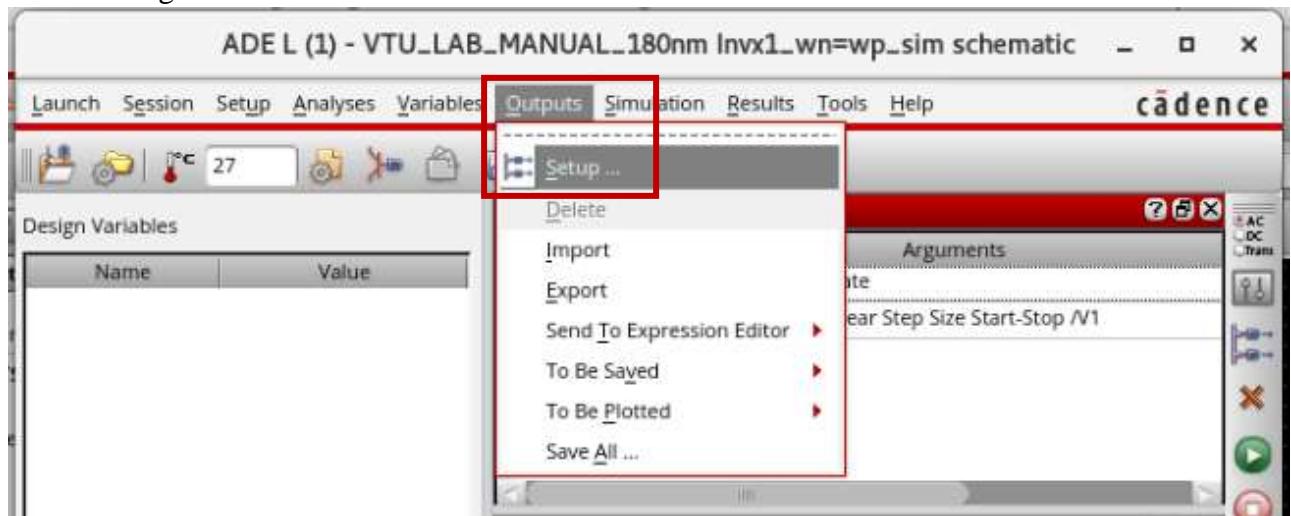


Figure – 1.64: Outputs → Setup

The “Setting Outputs – ADE L” window pops up as shown in Figure – 1.65.

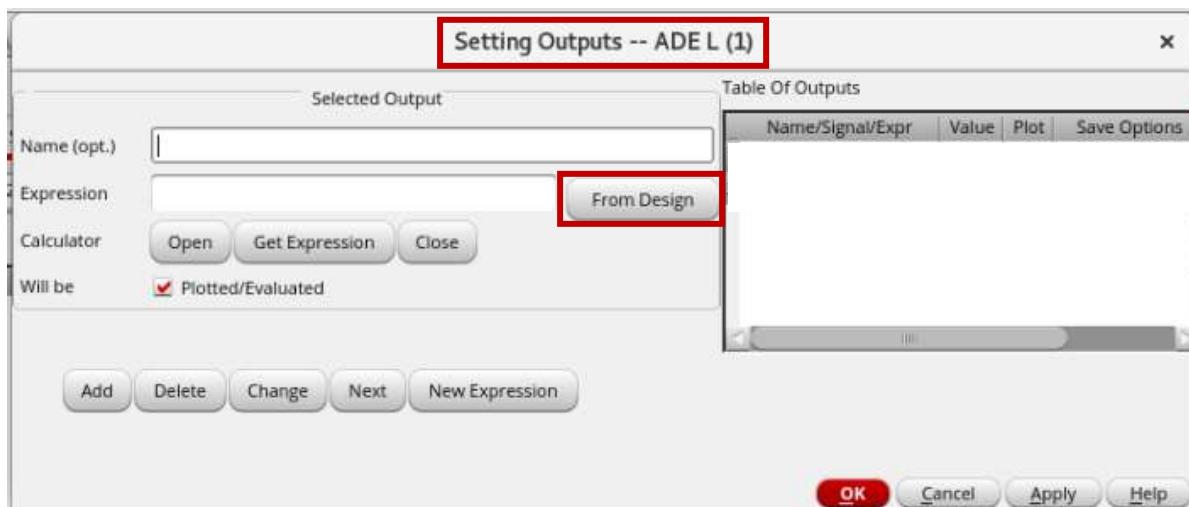


Figure – 1.65: Setting Outputs – ADE L window

Click on “From Design” as shown in the Figure – 1.65. This brings back the Test Schematic as shown in Figure – 1.66.

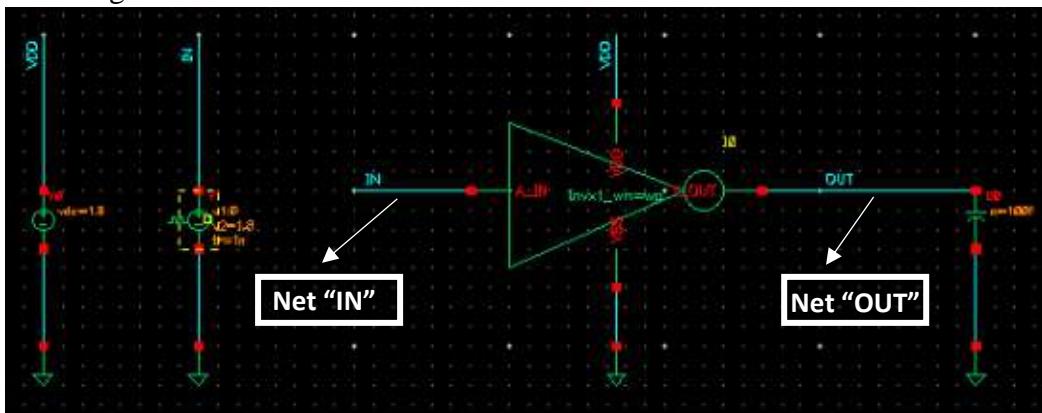


Figure – 1.66: Select the Net “IN” and Net “OUT”

Select the Input Net “IN” and the Output Net “OUT” as shown in Figure – 1.66. The selected Nets will be listed under “Table of Outputs” in the “Setting Outputs – ADE L” window as shown in Figure – 1.67. Click on “OK”.

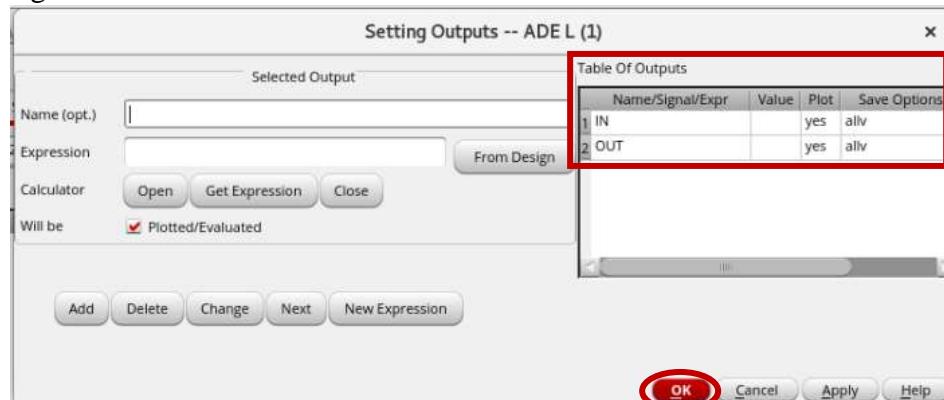


Figure – 1.67: Updated “Setting Outputs” window

The “Outputs” column in the “ADE L” window will be updated as shown in Figure – 1.68.

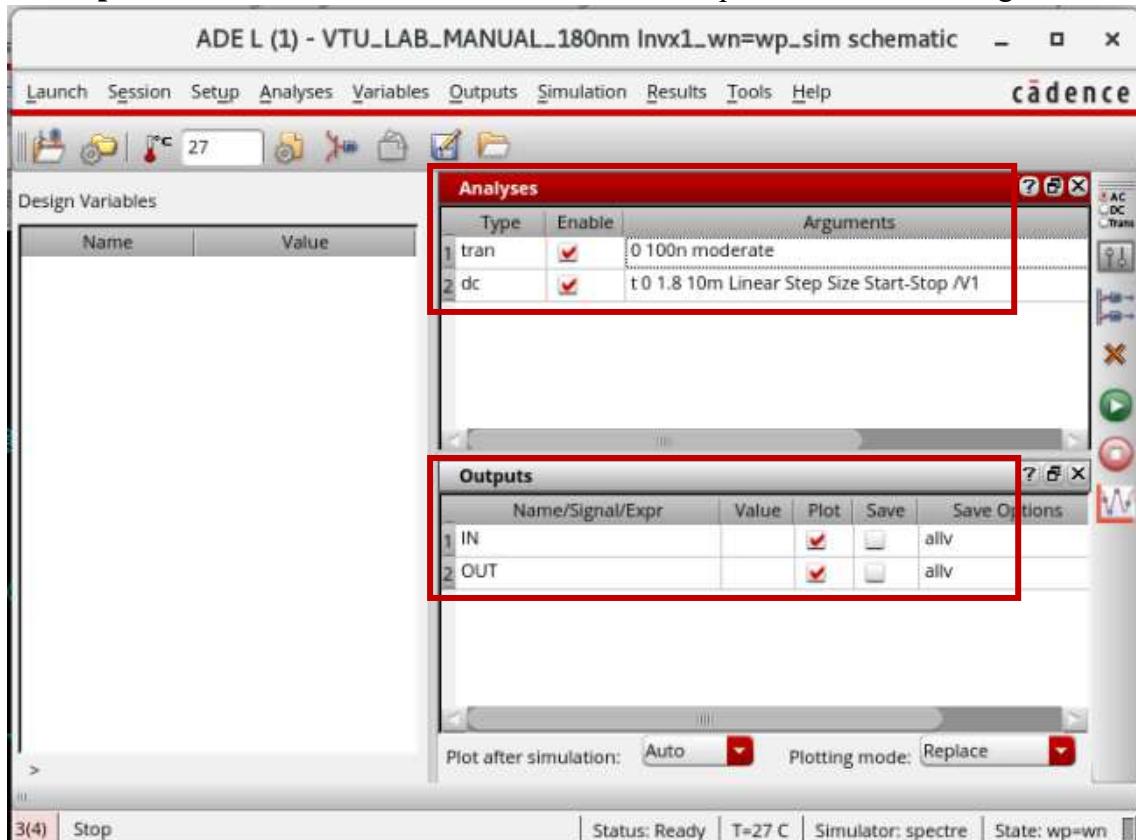


Figure – 1.68: “Outputs” in ADE L window

RUNNING THE SIMULATION:

To run the simulation, click on “**Simulation → Netlist and Run**” from ADE L window as shown in Figure – 1.69.

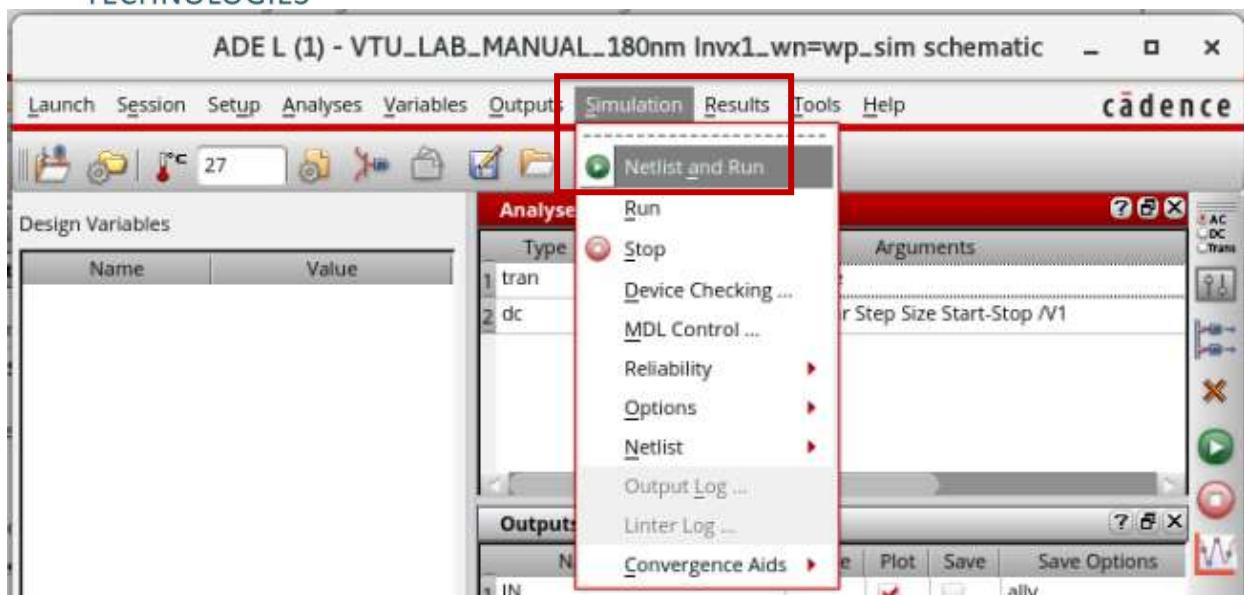


Figure – 1.69: Simulation → Netlist and Run

The simulated waveforms can be seen on the “**Virtuoso Visualization and Analysis XL**” window as shown in Figure – 1.70.

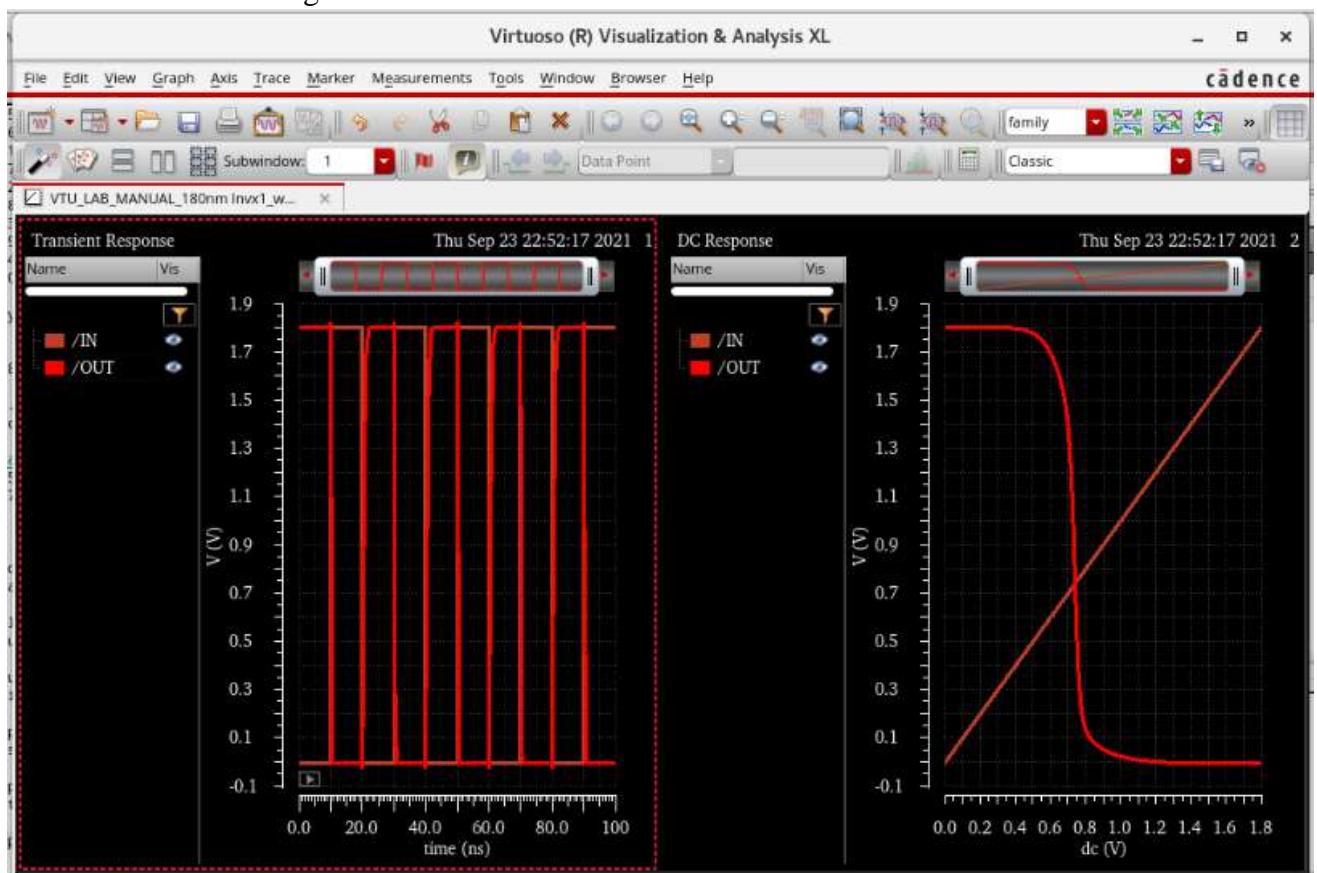


Figure – 1.70: Simulated waveforms

The Input and Output Signals can be split up by selecting “**Graph → Split All Strips**” as in Figure – 1.71.

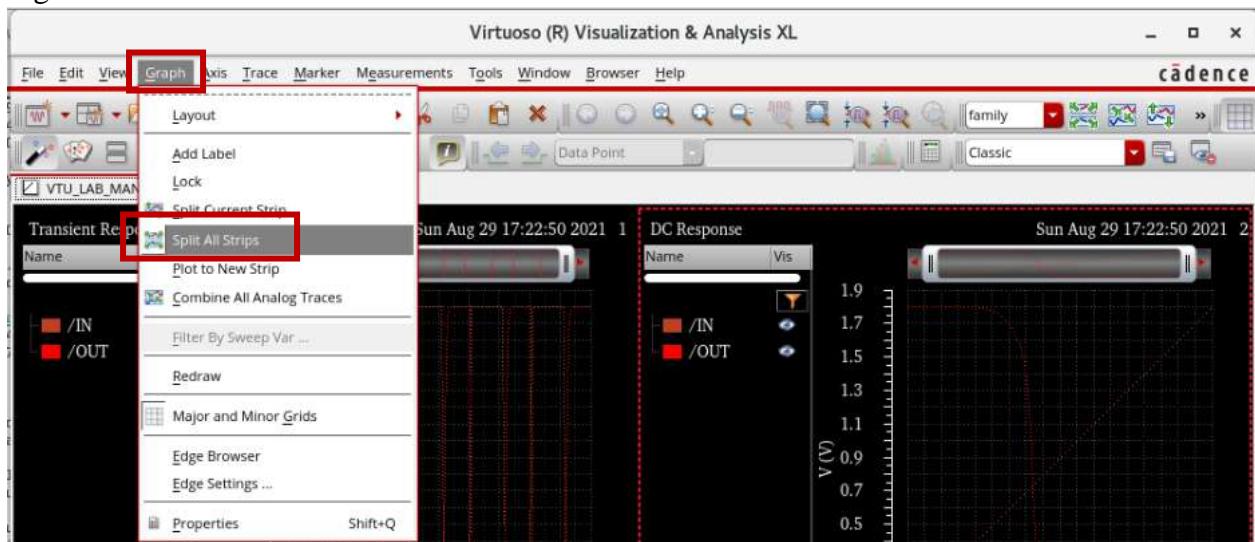


Figure – 1.71: Graph → Split All Strips

SAVING THE ADE L STATE:

To save the current ADE L state, click on “**Session → Save State**” as shown in Figure – 1.72.

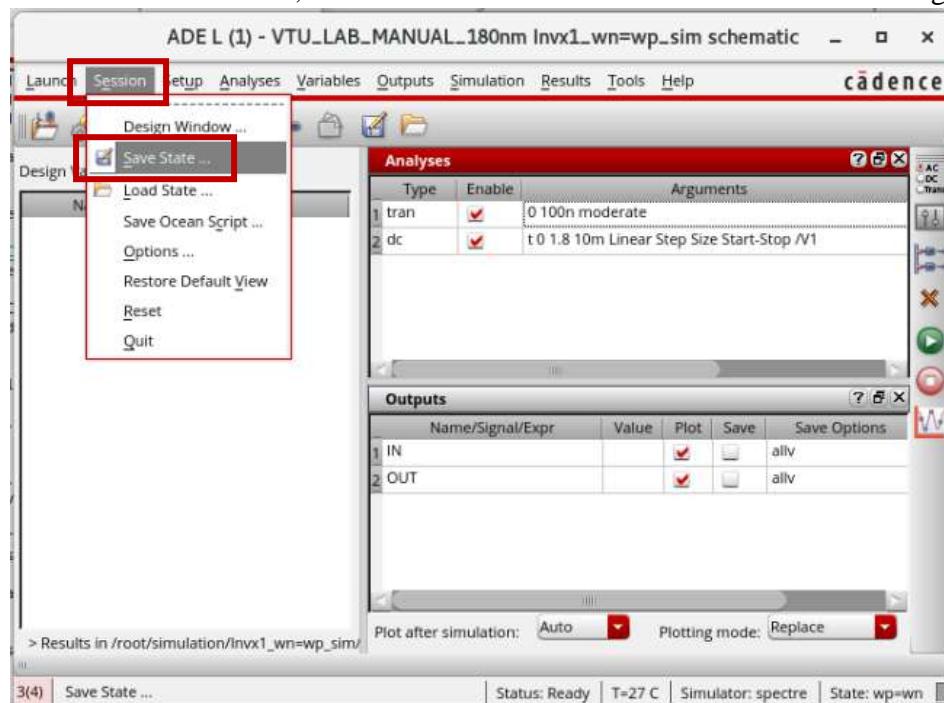


Figure – 1.72: Session → Save State

The “Saving State – ADE L” window pops up. Select the “Save State Option → Cellview” and click on “OK” as shown in Figure – 1.73.

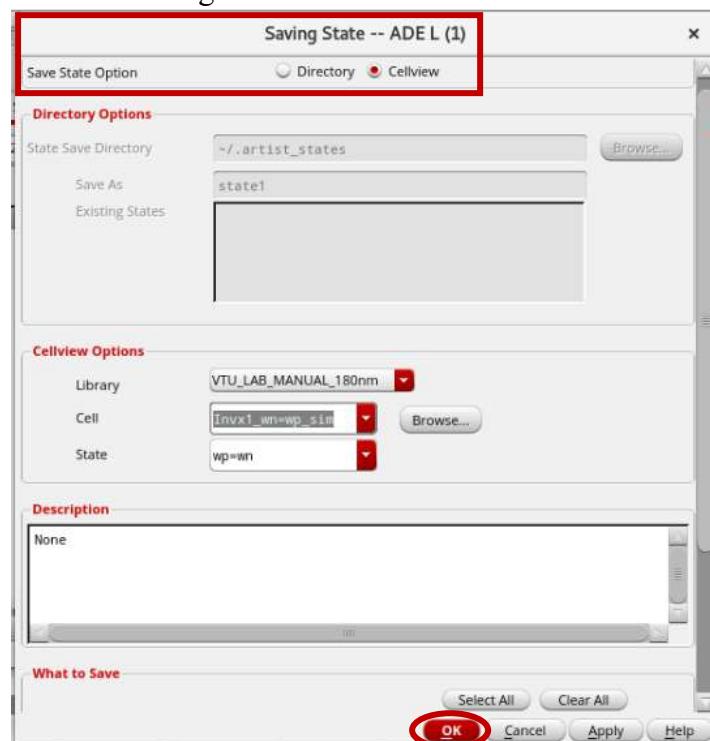


Figure – 1.73: Saving State

The Test Schematic and the State can be seen in the Library Manager as shown in Figure – 1.74.

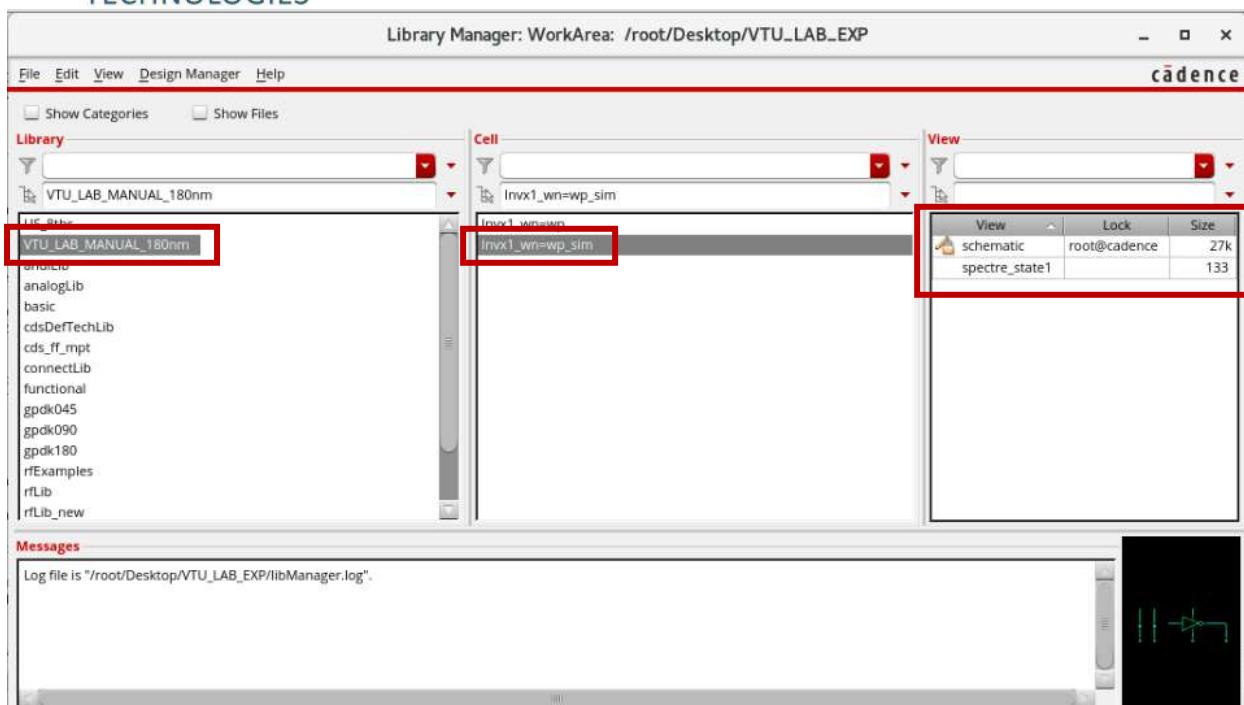


Figure – 1.74: Test Schematic and State in Library Manager

OPEN THE SAVED ADE L STATE:

To open the saved state, click on “Session → Load State” as shown in Figure – 1.75.

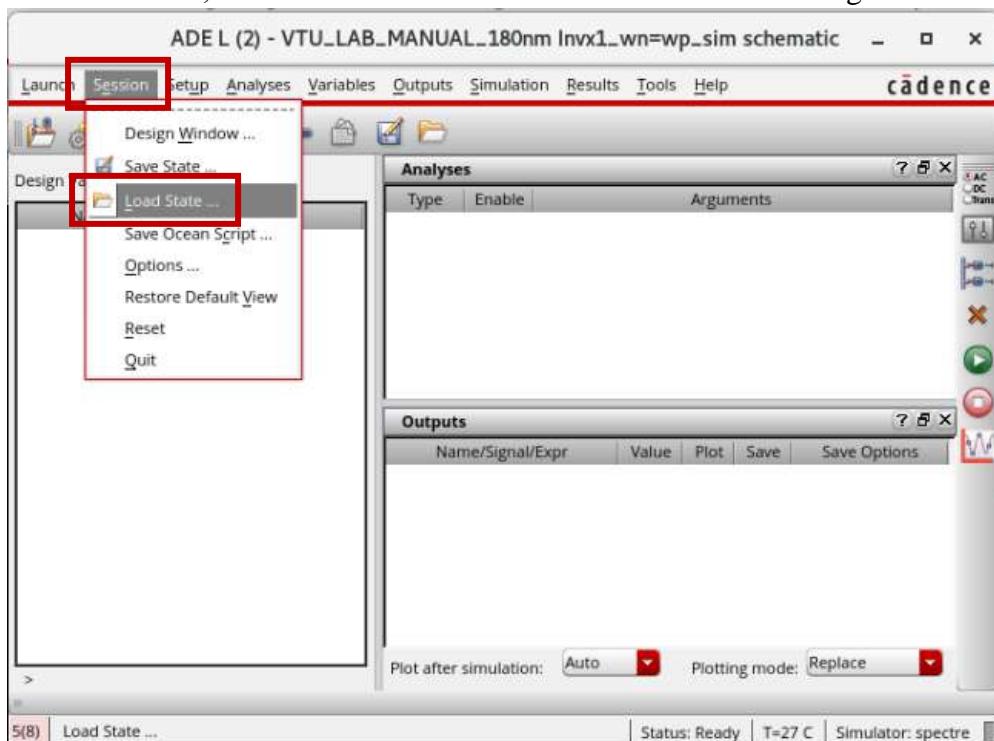


Figure – 1.75: Session → Load State

The “Loading State – ADE L” window pops up. Select the “Load State Option → Cellview” and click on “OK” as shown in Figure – 1.76.



Figure – 1.76: “Loading State – ADE L” window

The Saved ADE L state is loaded as shown in Figure – 1.77.

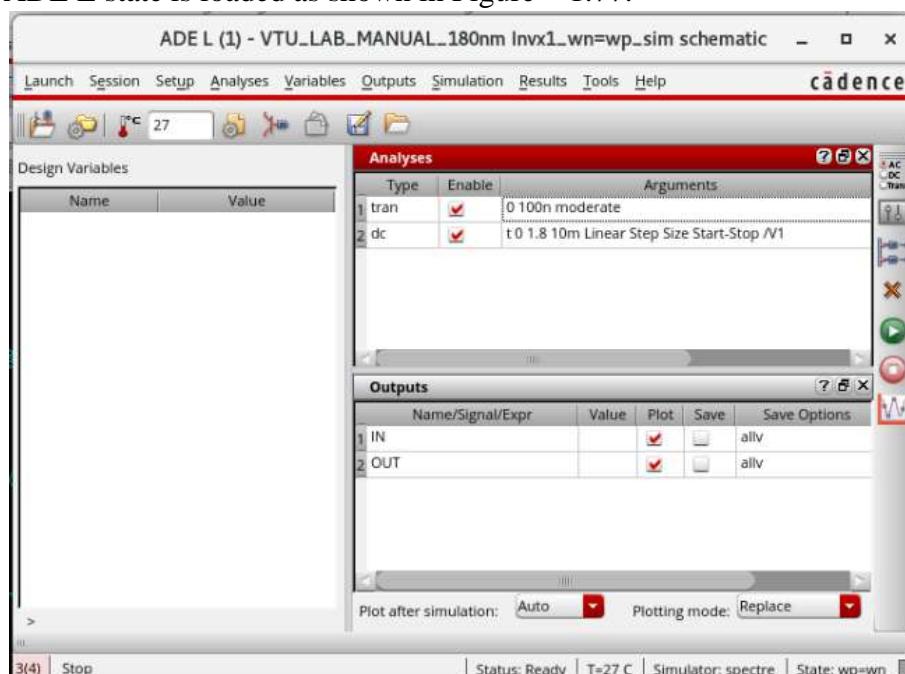


Figure – 1.77: Reloaded ADE L State

(2) CALCULATION OF tp_{HL} , tp_{LH} AND t_{PD} :

To calculate the Propagation Delay (t_{PD}), the formula used is

$$t_{PD} = \frac{(tp_{LH} + tp_{HL})}{2}$$

where, $tp_{LH} \rightarrow$ Low – High Propagation Delay and $tp_{HL} \rightarrow$ High – Low Propagation Delay.

To calculate tp_{LH} and tp_{HL} use the Calculator option from the “Virtuoso (R) Visualization and Analysis” window. So, select “Tools → Calculator” or click on the icon as shown in Figure – 1.78.



Figure – 1.78: Tools → Calculator

The “Virtuoso (R) Visualization and Analysis XL calculator” window pops up as shown in Figure – 1.79.

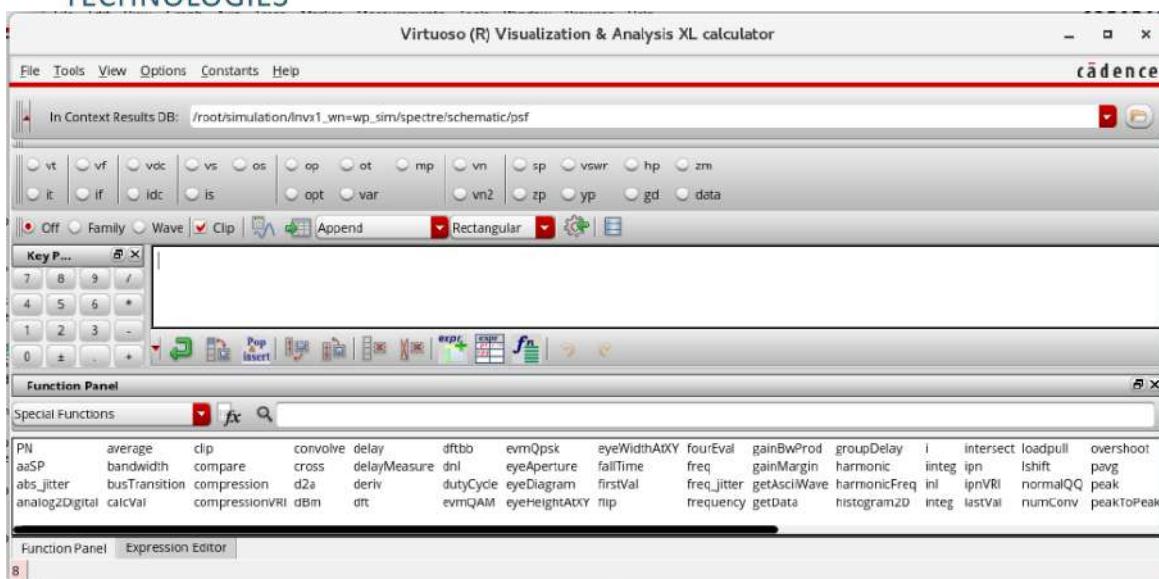


Figure – 1.79: Virtuoso (R) Visualization and Analysis XL calculator window

“Enable → Wave” and “Disable → Clip” as shown in Figure – 1.80.

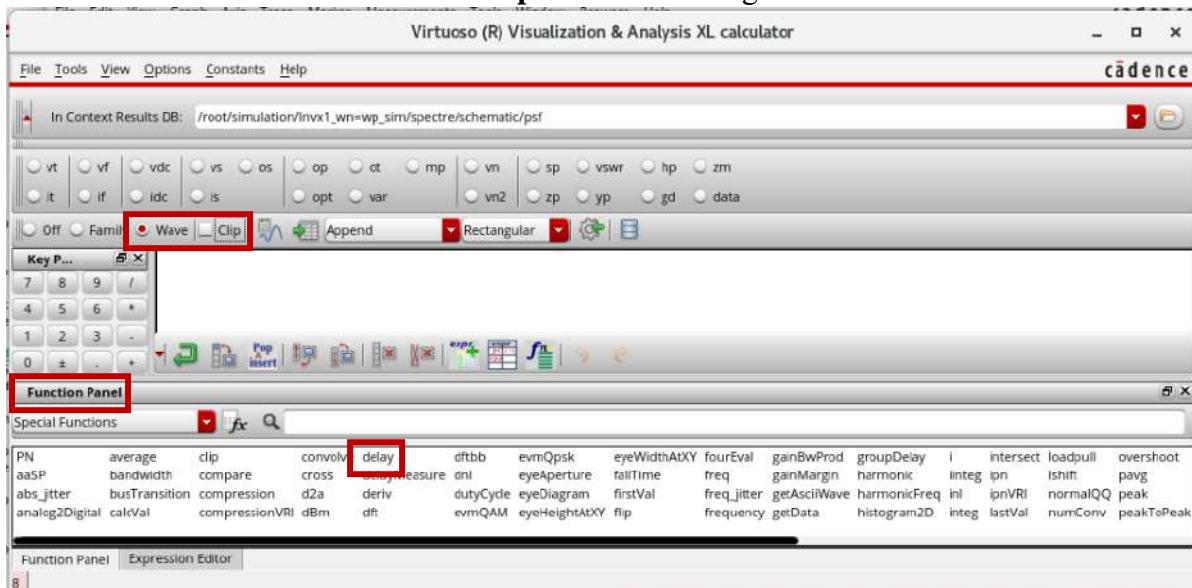


Figure – 1.80: “Enable → Wave” and “Disable → Clip”

Select “delay” from the “Function Panel” as shown in Figure – 1.80. The “Function Panel” gets updated as shown in Figure – 1.81.

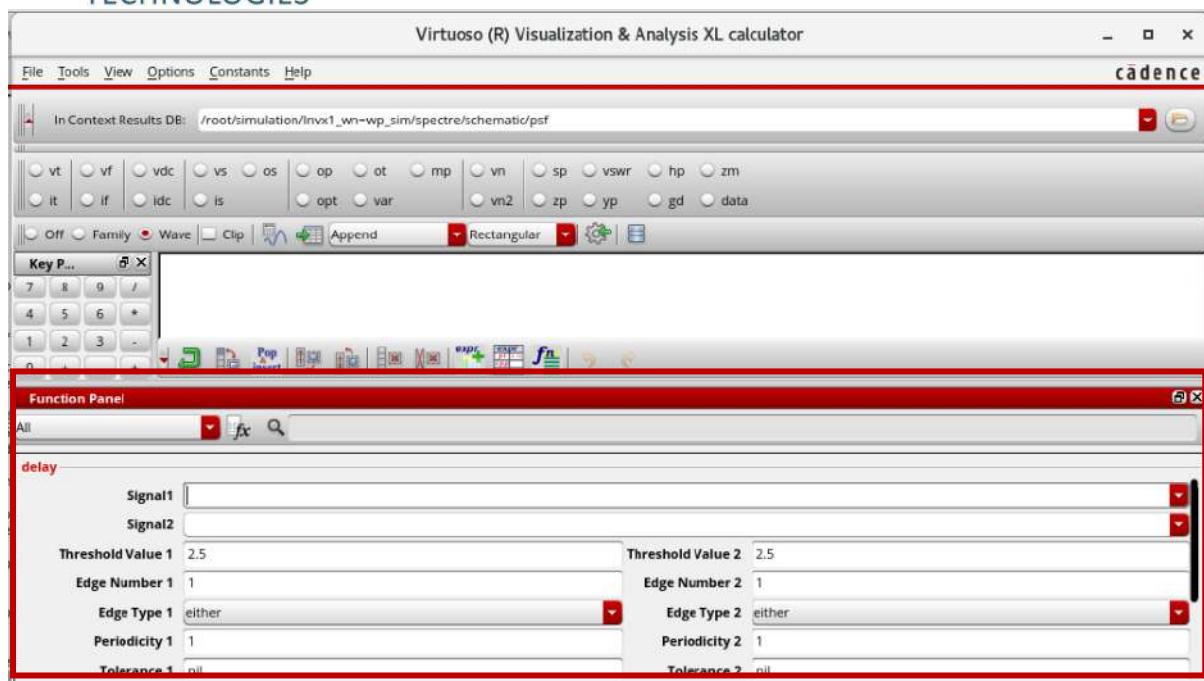


Figure – 1.81: Updated Function Panel

Place the cursor in “Signal 1”, select the signal “IN” from the waveform window as shown in Figure – 1.82.



Figure – 1.82: Selecting “IN” signal from the waveform

Similarly, place the cursor in “Signal 2” and select the “OUT” signal. The Function Panel gets updated as shown in Figure – 1.83.

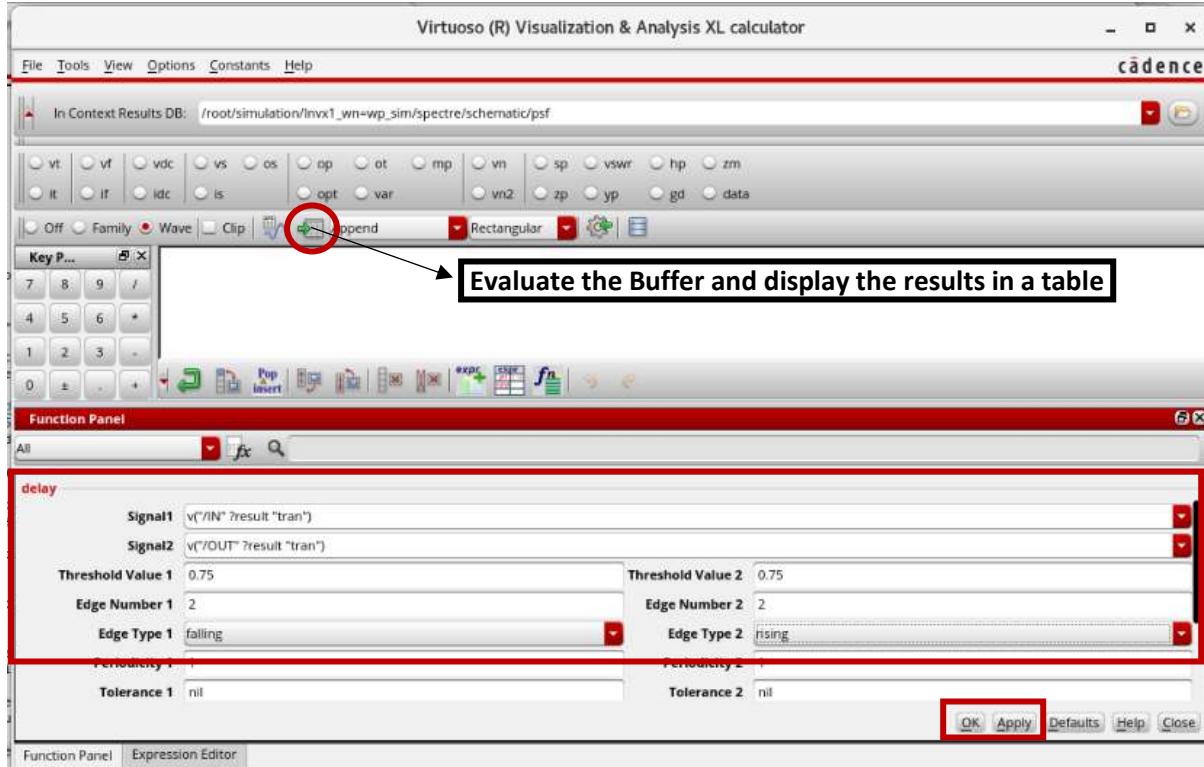


Figure – 1.83: “Signal 2” and other parameter selection

The value of “**Switching Potential**” should be mentioned under “**Threshold Value 1**” and “**Threshold Value 2**”.

Note:

What is Switching Potential?

Switching Potential is defined as the value of Input Voltage for which the Output Voltage is equal to the Input Voltage.

How to obtain the value of Switching Potential?

To obtain the Switching Potential, use the “intersect” option from the Function Panel, select the “Signal 1” and “Signal 2” from the DC Analysis waveform window, click on “Apply”, click on “OK” and click on “Evaluate the buffer and display the results in a table” icon as shown in Figure – 1.83 to obtain the value.

Select “**Edge Number 1**” and “**Edge Number 2**” as “2” (for example). Select “**Edge Type 1 → falling**” and “**Edge Type 2 → rising**” to obtain the value of “ tp_{LH} ” and “**Edge Type 1 → rising**” and “**Edge Type 2 → falling**” to obtain the value of “ tp_{HL} ”.

After the above mentioned selections, click on “**Apply**” and click on “**OK**” to see the “**Buffer**” window in the calculator getting updated as shown in Figure – 1.84.

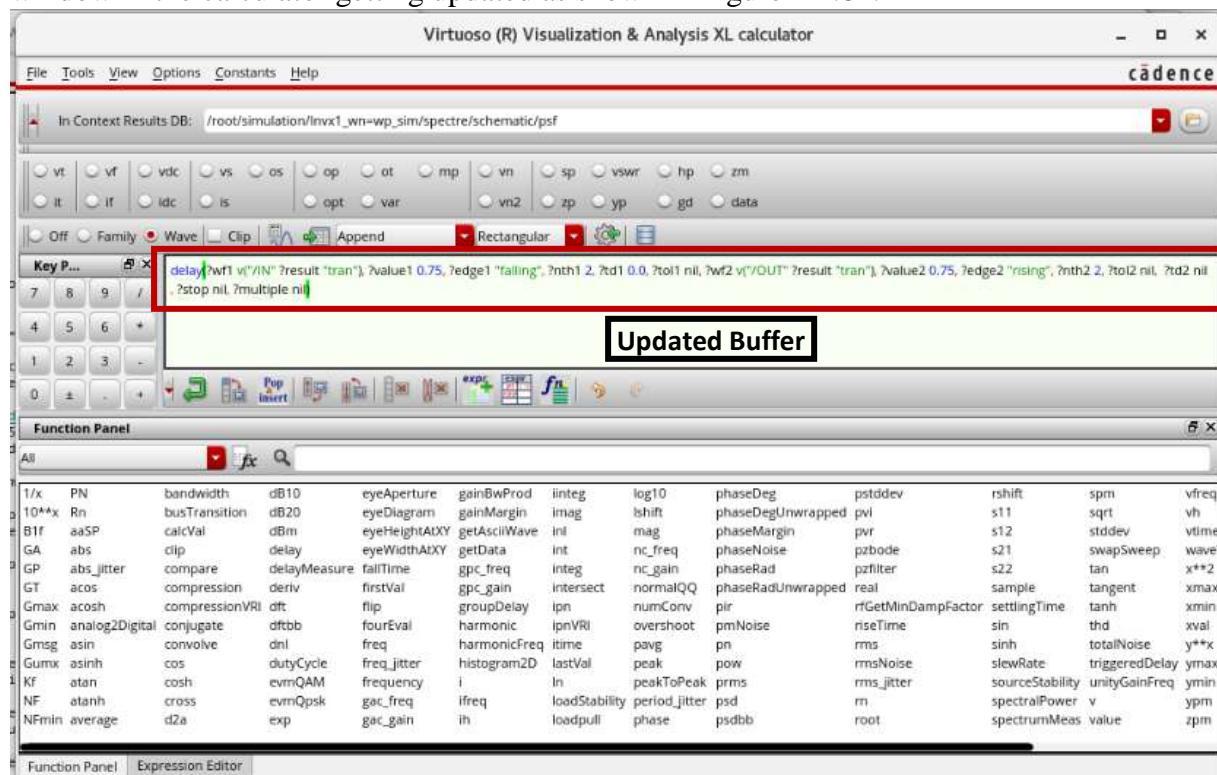


Figure – 1.84: Updated Buffer

Click on the icon “**Evaluate the buffer and display the results in a table**” as shown in Figure – 1.83 to obtain the value of tp_{HL} / tp_{LH} . Use the formula mentioned above to obtain the t_P .

Obtain the values of tp_{HL} , tp_{LH} and t_{PD} for all the three geometrical settings of Width.

(3) TABULATED VALUES OF DELAY:

The results of tp_{HL} , tp_{LH} and t_{PD} for all the required geometrical settings are tabulated below in Table – 5.

Table – 5: Values of tp_{HL} , tp_{LH} and t_{PD} for different geometries

| Width Settings | MOSFET | Width | tpLH | tpHL | tpd |
|----------------|--------|-------|-----------|-----------|-----------|
| $W_p = W_n$ | PMOS | 850n | 3.233E-10 | 7.049E-10 | 5.141E-10 |
| | NMOS | 850n | | | |
| $W_n = 2W_p$ | PMOS | 850n | 3.337E-10 | 4.700E-10 | 4.019E-10 |
| | NMOS | 1.7u | | | |
| $W_n = W_p/2$ | PMOS | 425n | 1.141E-09 | 3.154E-10 | 7.282E-10 |
| | NMOS | 850n | | | |

(b) Layout of CMOS Inverter with $\frac{W_P}{W_N} = \frac{40}{20}$

Objective:

To draw the Layout of CMOS Inverter with $\frac{W_P}{W_N} = \frac{40}{20}$ using optimum Layout Methods. Verify for DRC and LVS, extract the Parasitics and perform the Post-Layout Simulations, compare the results with Pre-Layout Simulations and record the observations.

SCHEMATIC CAPTURE:

Create a New Library, Create a Cellview and instantiate the required devices through “Create → Instance” option. The parameter for PMOS and NMOS Transistors are listed in Table – 6 shown below.

Table – 6: Parameters for NMOS and PMOS Transistors

| Library Name | Cell Name | Comments / Properties |
|--------------|-----------|--|
| gdk180 | Nmos | Width, $W_N = 20 \mu$ Length, $L = 180 n$ |
| gdk180 | Pmos | Width, $W_P = 40 \mu$ Length, $L = 180 n$ |

Follow the techniques demonstrated in Lab – 01 to complete the Schematic. The completed CMOS Inverter circuit is shown in Figure – 1.85.

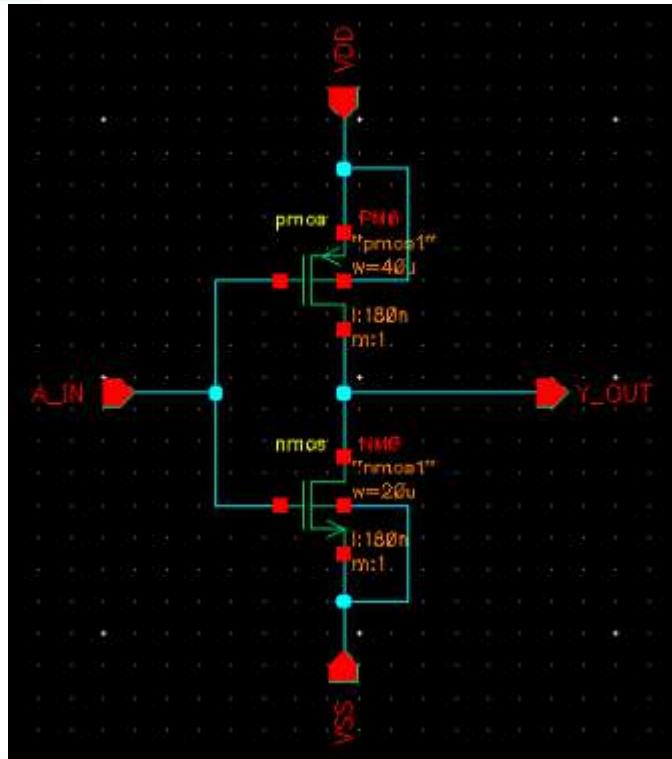


Figure – 1.85: Schematic for CMOS Inverter with $\frac{W_P}{W_N} = \frac{40}{20}$

The symbol for the CMOS Inverter is shown in Figure – 1.86.

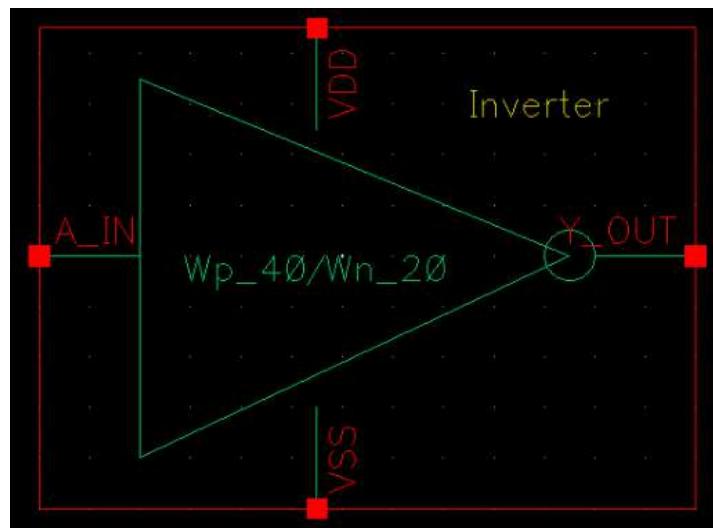


Figure – 1.86: Symbol for CMOS Inverter with $\frac{W_P}{W_N} = \frac{40}{20}$

Create a New Cellview and capture the Test Schematic using the symbol shown in Figure – 1.86. The Test Schematic is shown in Figure – 1.87.

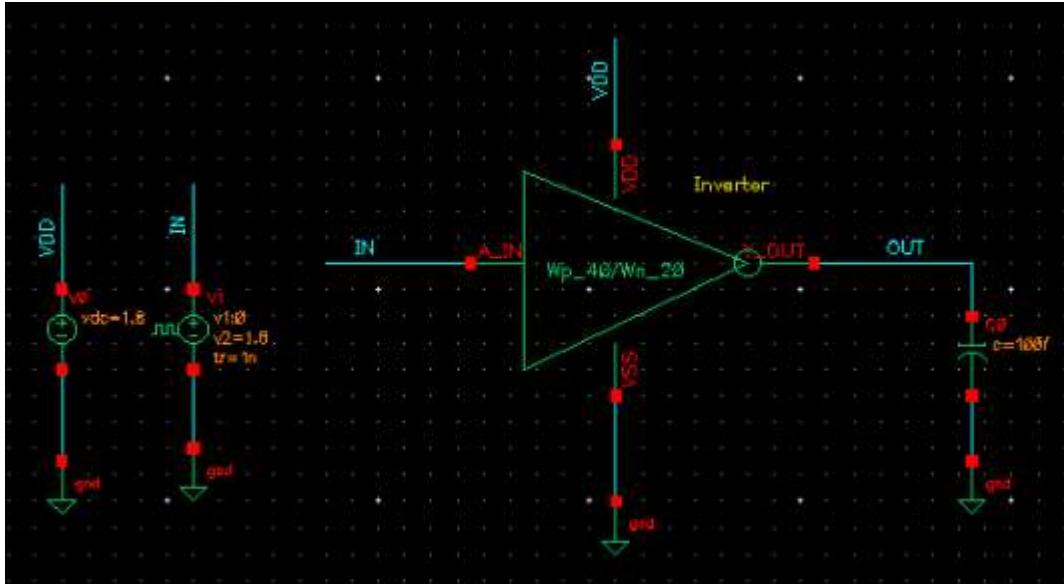


Figure – 1.87: Test Schematic for CMOS Inverter with $\frac{W_P}{W_N} = \frac{40}{20}$

The parameters for “vdc”, “vpulse” and the “capacitor” are the same as shown in Table – 4. Check and Save the design.

SIMULATION:

Launch the ADE L window from the Test Circuit, setup the Simulator, Model Libraries and the Process Corner as shown in Figure – 1.50, Figure – 1.52 and Figure – 1.53.

Setup the DC Analysis and Transient Analysis through the “Choose → Analysis” option and the parameters are the same as shown in Figure – 1.56, Figure – 1.58 and Figure – 1.62.

Select the signals to be plotted and the updated ADE L window is shown in Figure – 1.88.

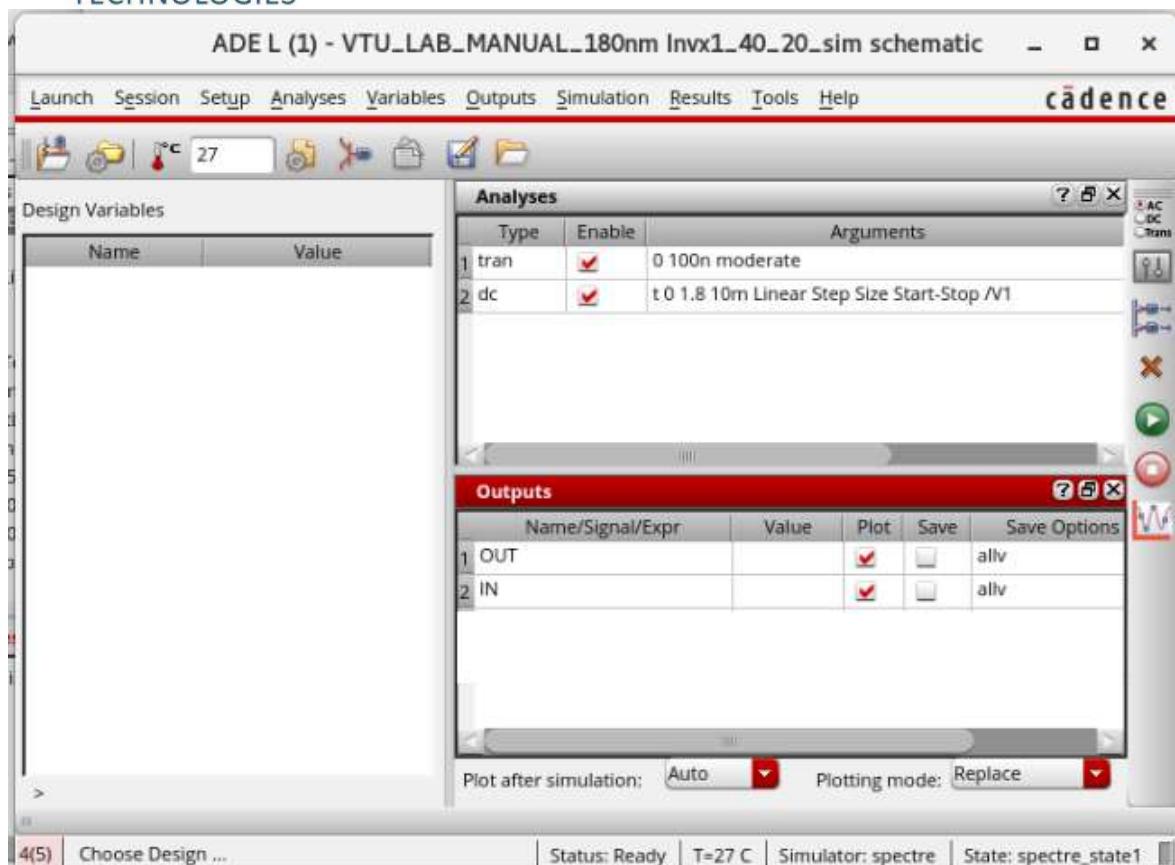


Figure – 1.88: Updated ADE L window

The signals plotted as a result of Transient Analysis is shown in Figure – 1.89.



Figure – 1.89: Transient Analysis for CMOS Inverter with $\frac{W_P}{W_N} = \frac{40}{20}$

Similarly, the signals plotted after DC Analysis are shown in Figure – 1.90.

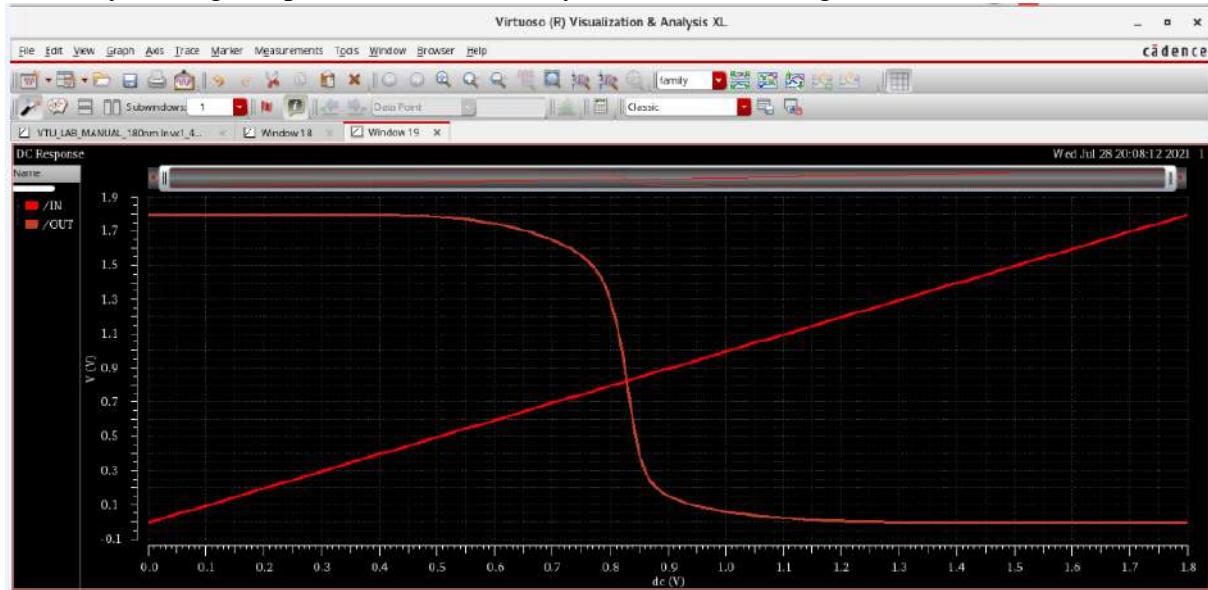


Figure – 1.90: DC Analysis for CMOS Inverter with $\frac{W_P}{W_N} = \frac{40}{20}$

VALUES OF tp_{HL} , tp_{LH} AND t_{PD} :

Obtain the values of tp_{HL} , tp_{LH} and t_{PD} by referring to “**CALCULATION OF tp_{HL} , tp_{LH} AND t_{PD}** ” in the previous section. The values are tabulated as shown in Table – 7.

Table – 7: Values of tp_{HL} , tp_{LH} and t_{PD} for CMOS Inverter with $\frac{W_P}{W_N} = \frac{40}{20}$

| MOSFET | Length | Width | tp_{LH} | tp_{HL} | t_{pd} |
|--------|--------|-------|-----------|-----------|-----------|
| PMOS | 180n | 40u | 1.228E-10 | 3.550E-11 | 7.920E-11 |
| NMOS | 180n | 20u | | | |

LAYOUT FOR CMOS INVERTER WITH $\frac{W_P}{W_N} = \frac{40}{20}$:

From the Virtuoso Schematic Editor as shown in Figure – 1.85, select “Launch → Layout XL” as shown in Figure – 1.91.

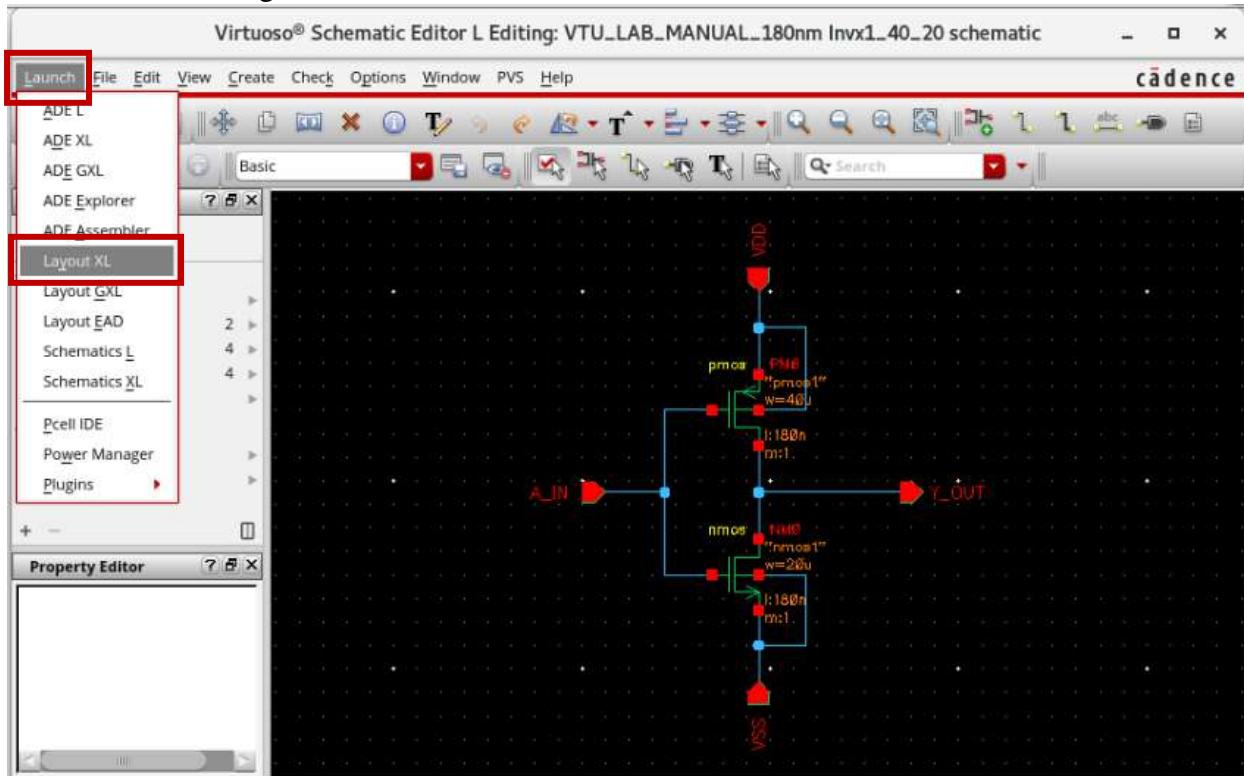


Figure – 1.91: Launch → Layout XL

The “Startup Option” window pops up as shown in Figure – 1.92. Select “Layout → Create New” and “Configuration → Automatic” and click on “OK”.



Figure – 1.92: Startup Option

The “New File” window pops up. Verify the Library Name and Cell Name. “View” and “Type” should be “layout”. Click on “OK” as shown in Figure – 1.93.

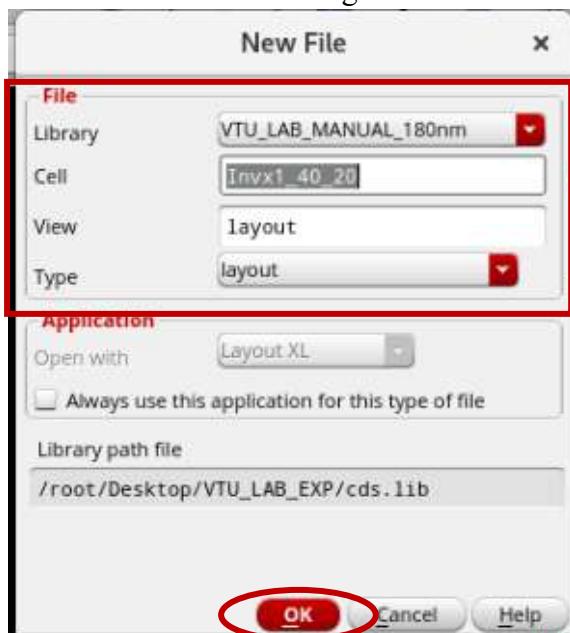


Figure – 1.93: New File window

The “Virtuoso Layout Suite XL Editing” window pops up as shown in Figure – 1.94. Click on “F” to fit the cross wire to the center of the Virtuoso Layout Editor.

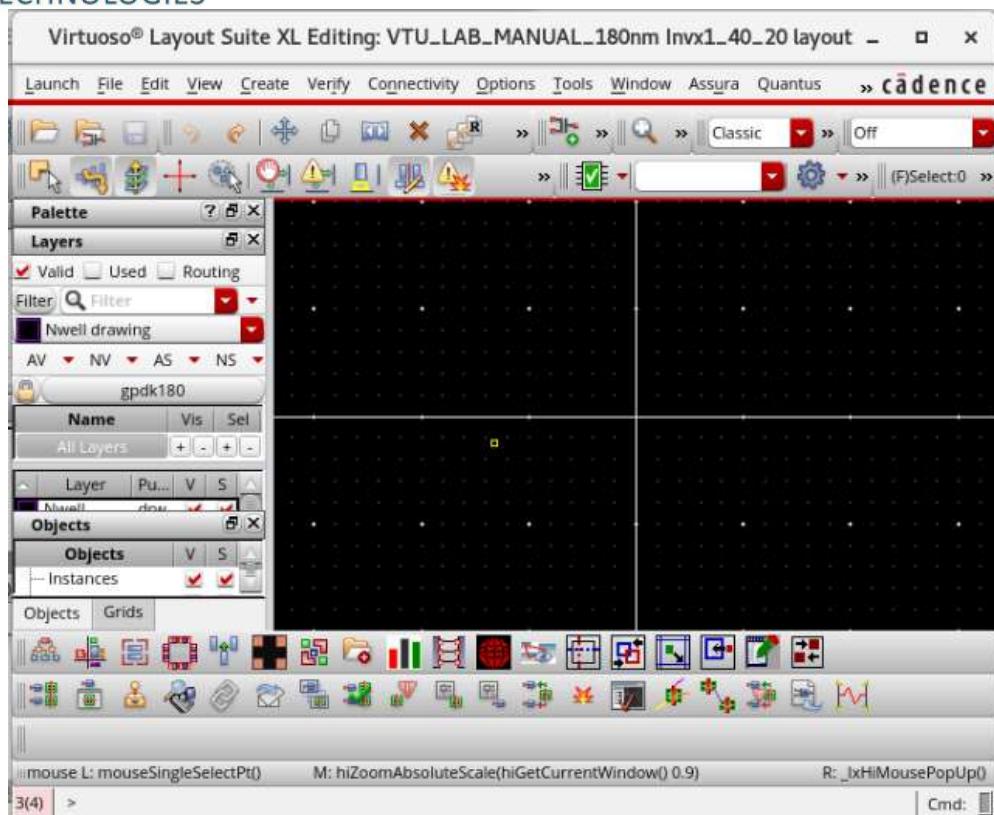


Figure – 1.94: Virtuoso Layout Suite XL Editing

Note:

We have created a Template for gpdk180.

To instantiate all the devices from the Virtuoso Schematic Editor, select “**Connectivity → Generate → All From Source**” as shown in Figure – 1.95.

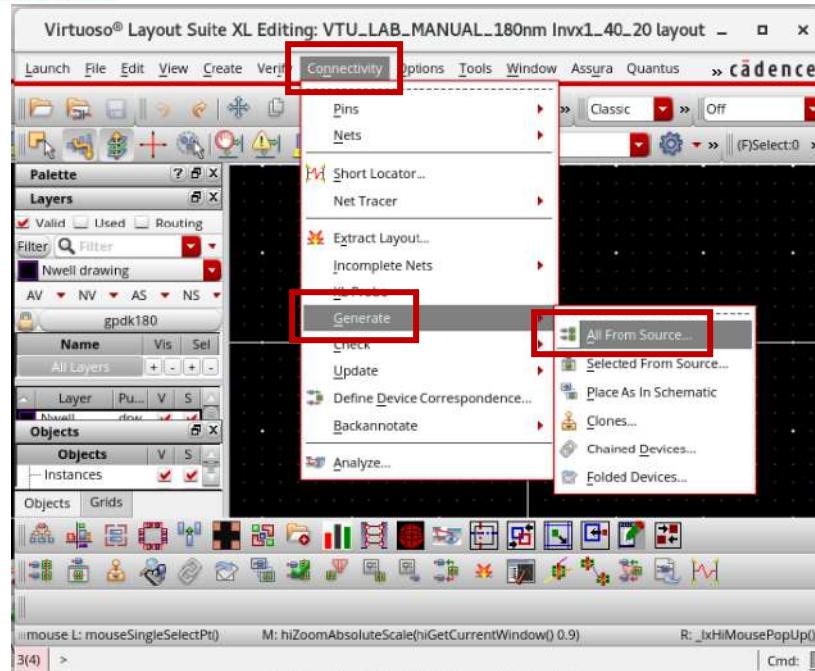


Figure – 1.95: Connectivity → Generate → All From Source

The “Generate Layout” window pops up. Click on “OK” as shown in Figure – 1.96.

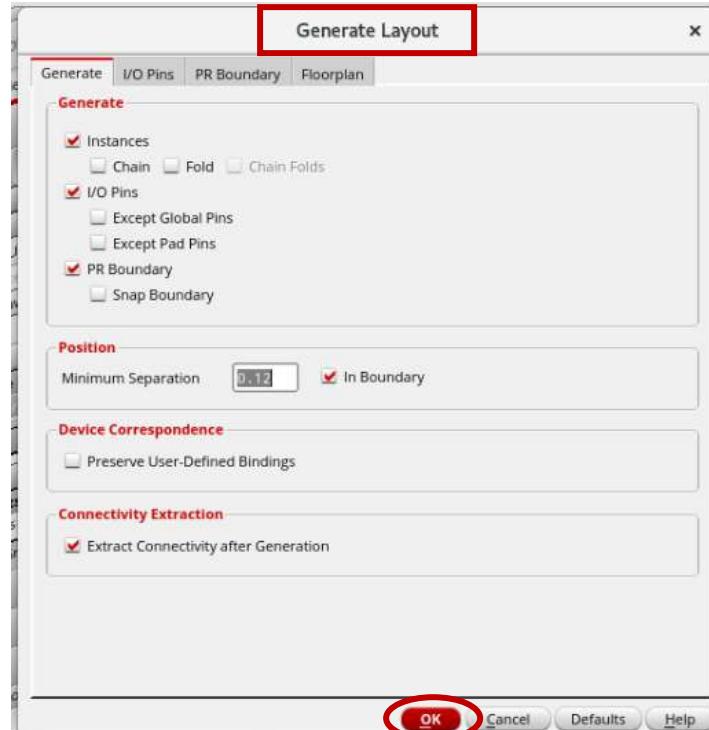


Figure – 1.96: Generate Layout window

The Virtuoso Layout Editor gets updated as shown in Figure – 1.97.

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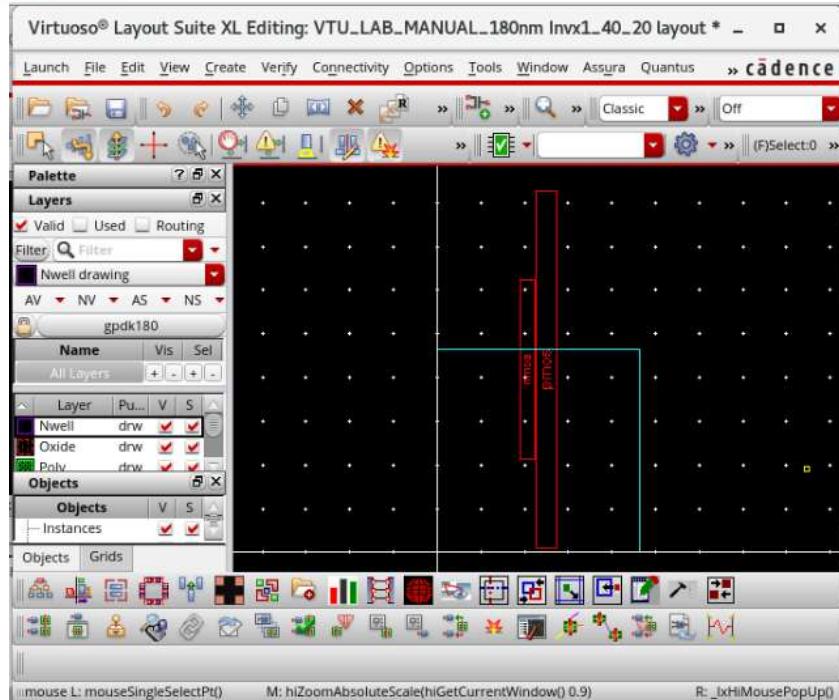


Figure – 1.97: Updated Virtuoso Layout Editor

To view the terminals of the devices, click on “Shift + F” and the devices in the Virtuoso Layout Editor gets updated as shown in Figure – 1.98.

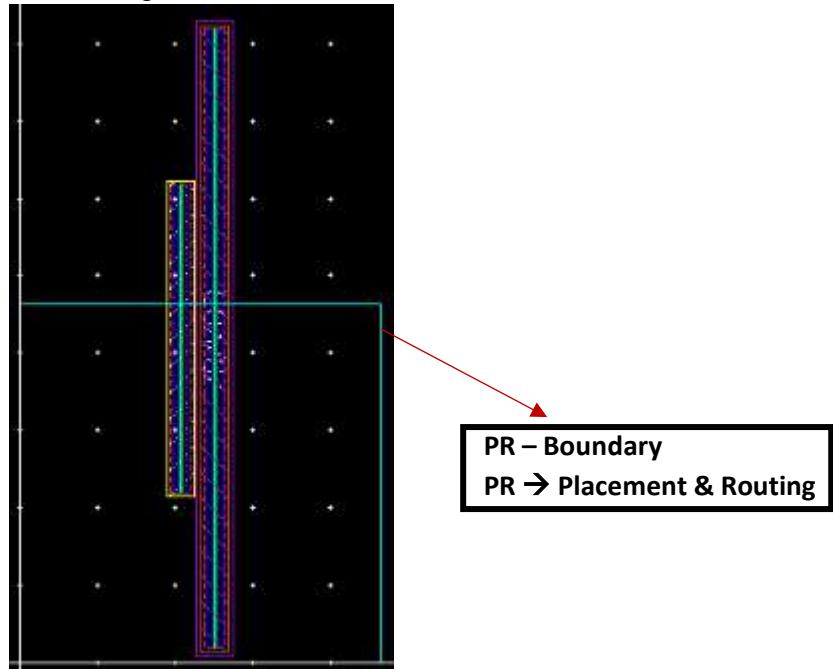


Figure – 1.98: Updated devices after “Shift + F”

The blue colored box that is seen in the Layout is the **PR – Boundary (PR → Placement and Routing)**. Since the devices have to be fixed within the size of the Template, the properties of NMOS and PMOS transistors have to be changed.

To change the device properties, select the device using a Left Mouse Click (for eg: NMOS transistor) and it gets highlighted as shown in Figure – 1.99.

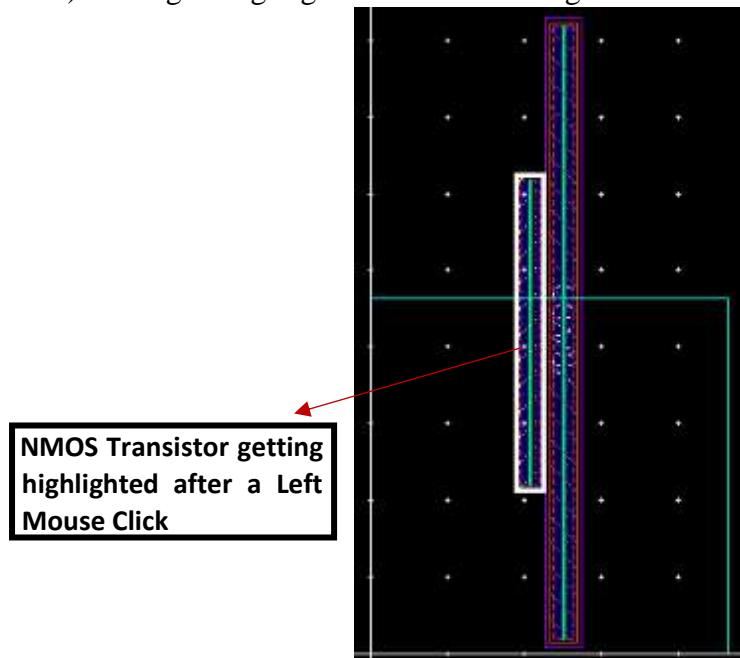


Figure – 1.99: NMOS Transistor after Left Mouse Click

To edit the device properties, use a Right Mouse Click and select “Properties” as shown in Figure – 1.100 (or) use the bind key “Q”.

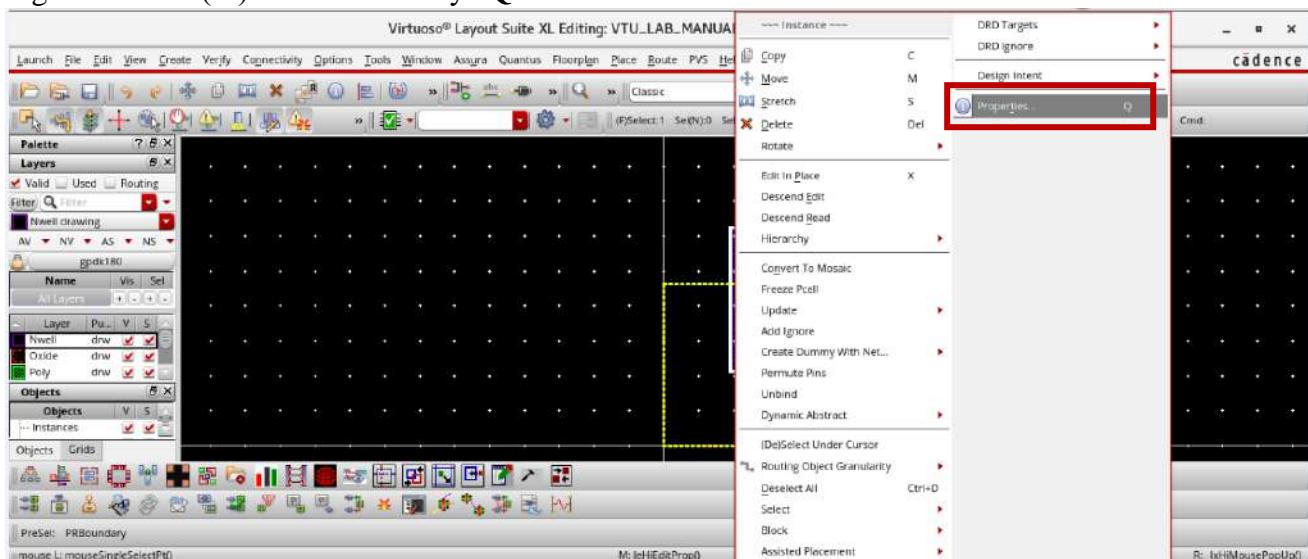


Figure – 1.100: Select “Properties” after a Right Mouse Click

The “Edit Instance Properties” window pops up as shown in Figure – 1.101.

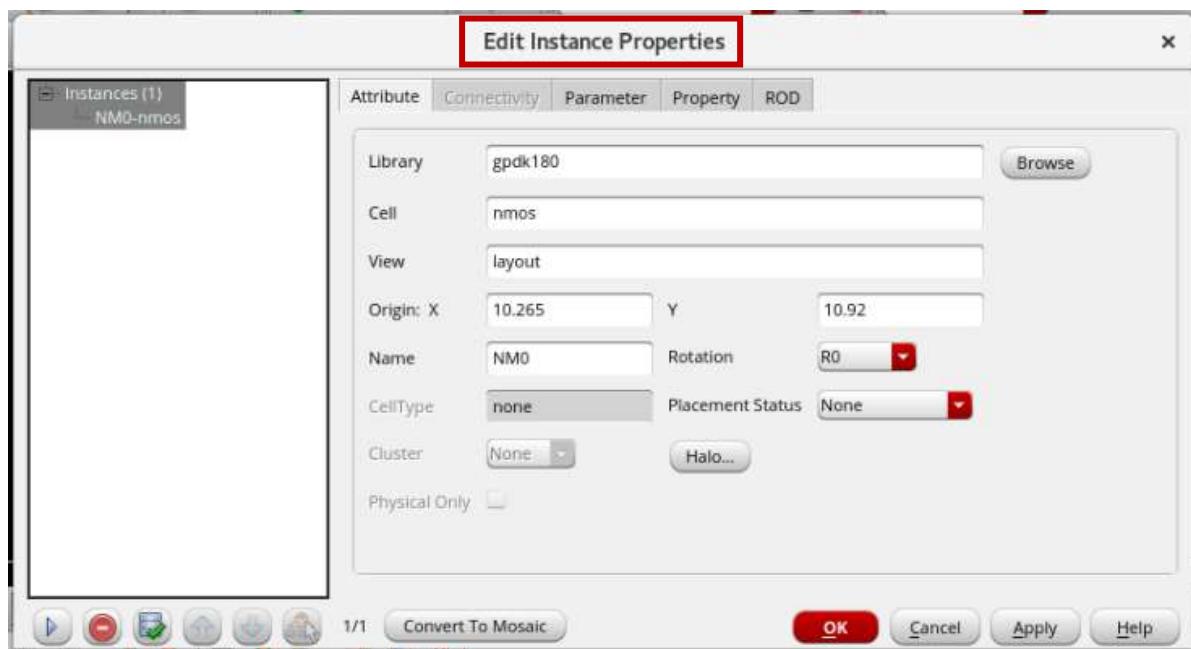


Figure – 1.101: Edit Instance Properties window

Click on “**Parameter**” tab to visualize the parameters of the selected device (for example: NMOS transistor) like Length, Multiplier, Total Width, Finger Width, Fingers and most importantly Bodytie Type as shown in Figure – 1.102. Initially, the “**Bulk**” won’t be included to the layout view of Transistors and the “**Bodytie Type**” option helps in including that.

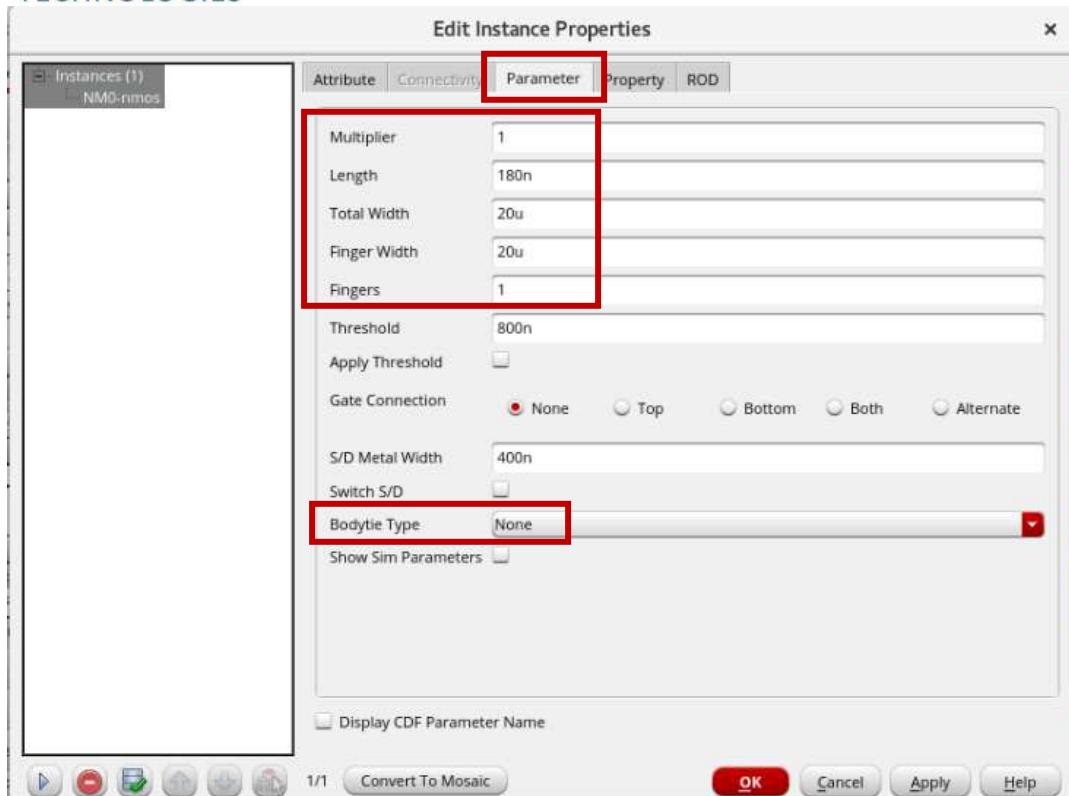


Figure – 1.102: Parameter tab before update

The Parameter tab after updating the values is shown in Figure – 1.103.

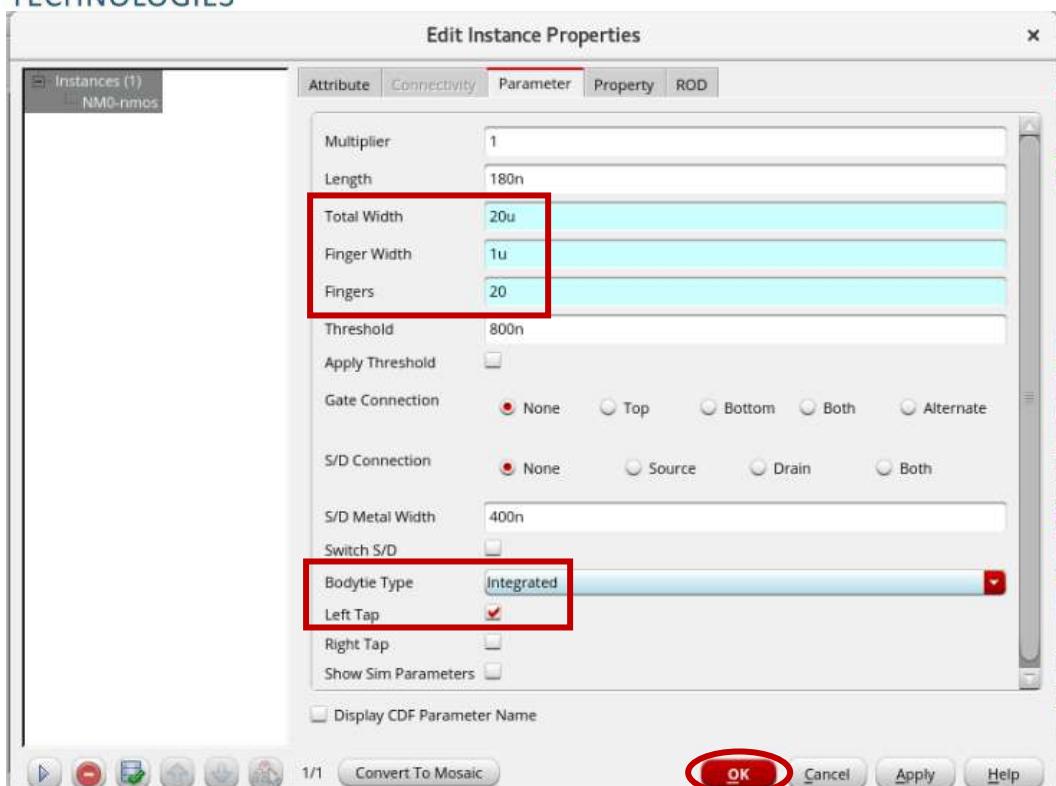


Figure – 1.103: Parameter tab after updating the values for NMOS transistor

In order to fix the device within the Template, the parameter “**Finger → 20**” and “**Finger Width → 1u**” are changed but the “**Total Width**” should remain the same. The “**Bodytie Type → Integrated**” option will have the Bulk terminal integrated to the Source terminal of the device on the left side “**Left Tap**” of the device. Click on “**OK**” and the device gets updated as shown in Figure – 1.104.

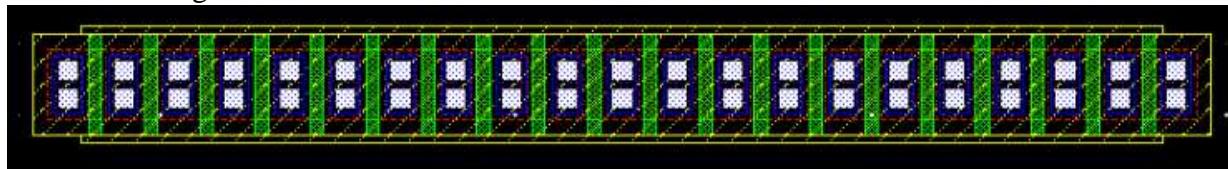


Figure – 1.104: Updated NMOS Transistor

Similarly, the parameters for the PMOS transistors are given as “**Finger → 20**”, “**Finger Width → 2u**” and “**Bodytie Type → Integrated**”. The updated parameter tab is shown in Figure – 1.105.

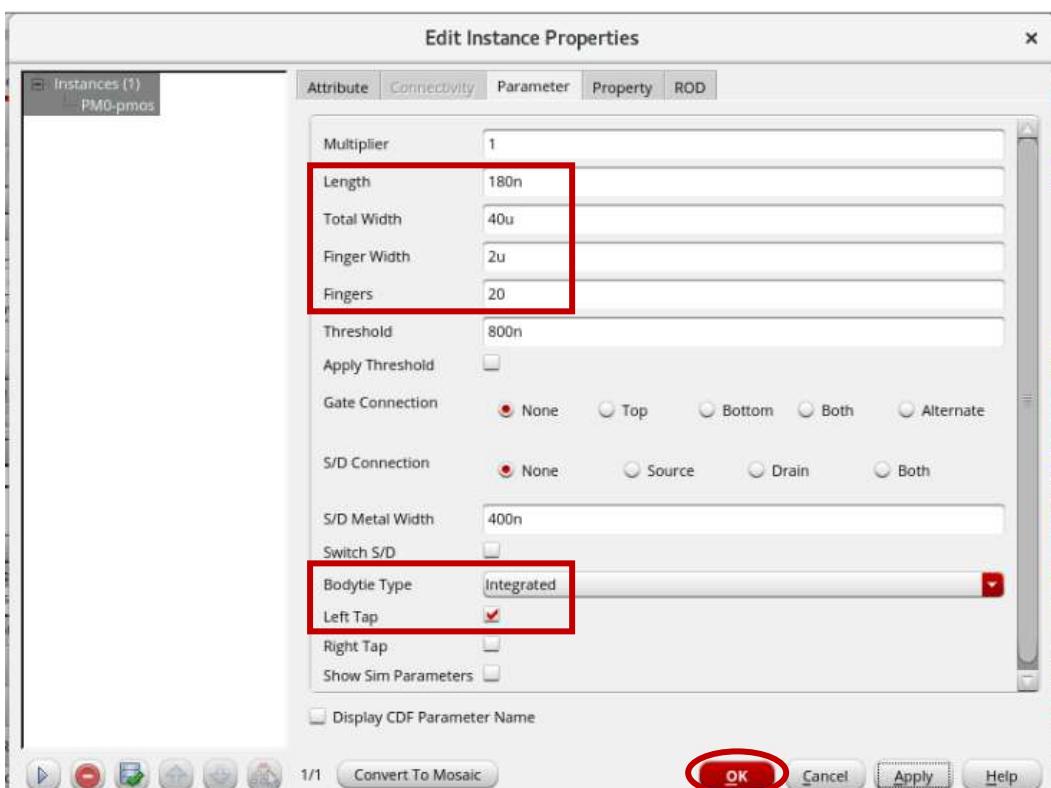


Figure – 1.105: Parameter tab after updating the values for PMOS transistor

Click on “OK” and the device gets updated as shown in Figure – 1.106.

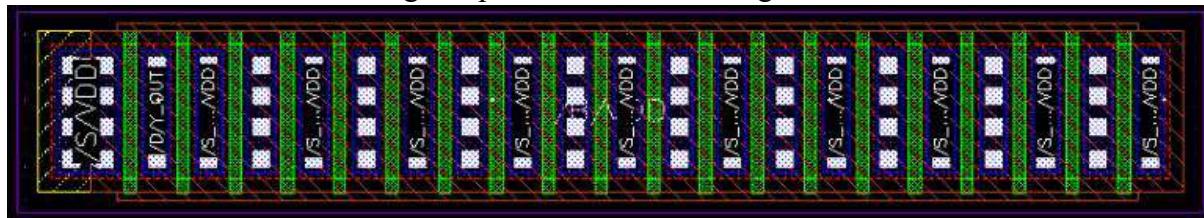


Figure – 1.106: Updated PMOS Transistor

To have an idea of the interconnections, select the layout using “Ctrl + A”. The entire layout gets highlighted as shown in Figure – 1.107.

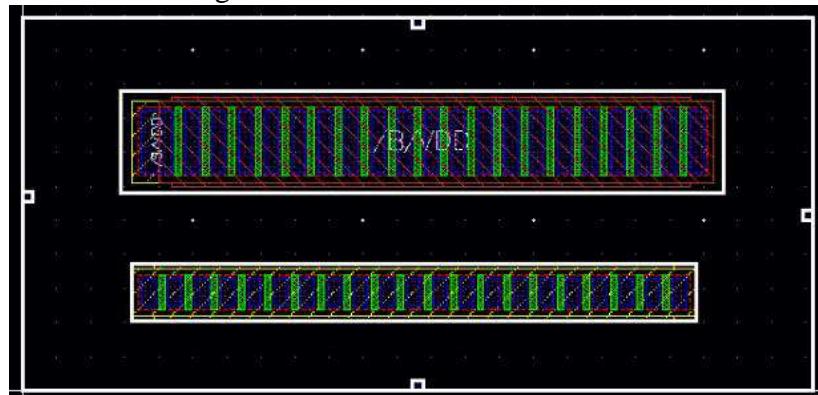


Figure – 1.107: Selecting the layout using “Ctrl + A”

Select “**Connectivity → Incomplete Nets → Show/Hide Selected..**” as shown in Figure – 1.108.

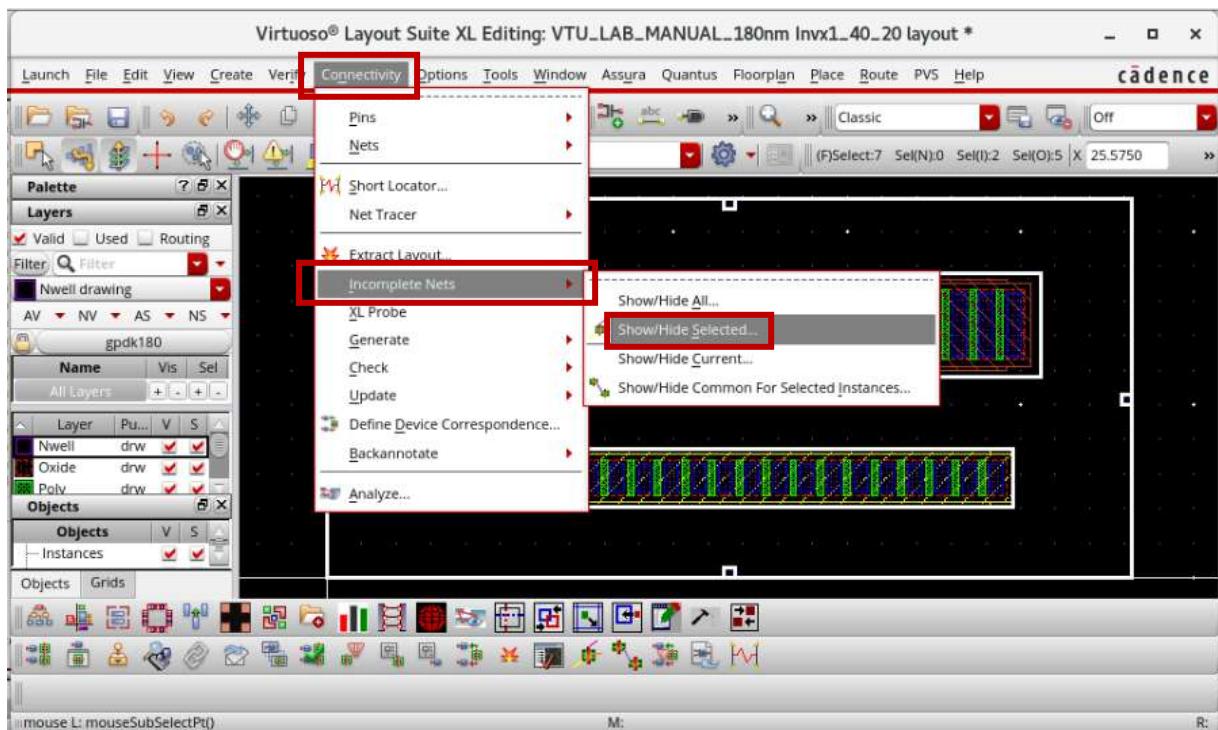


Figure – 1.108: Connectivity → Incomplete Nets → Show/Hide Selected..

The layout gets updated as shown in Figure – 1.109. The lines visible in the layout are called the Rat Lines. These lines give an idea about the missing interconnections in the layout.

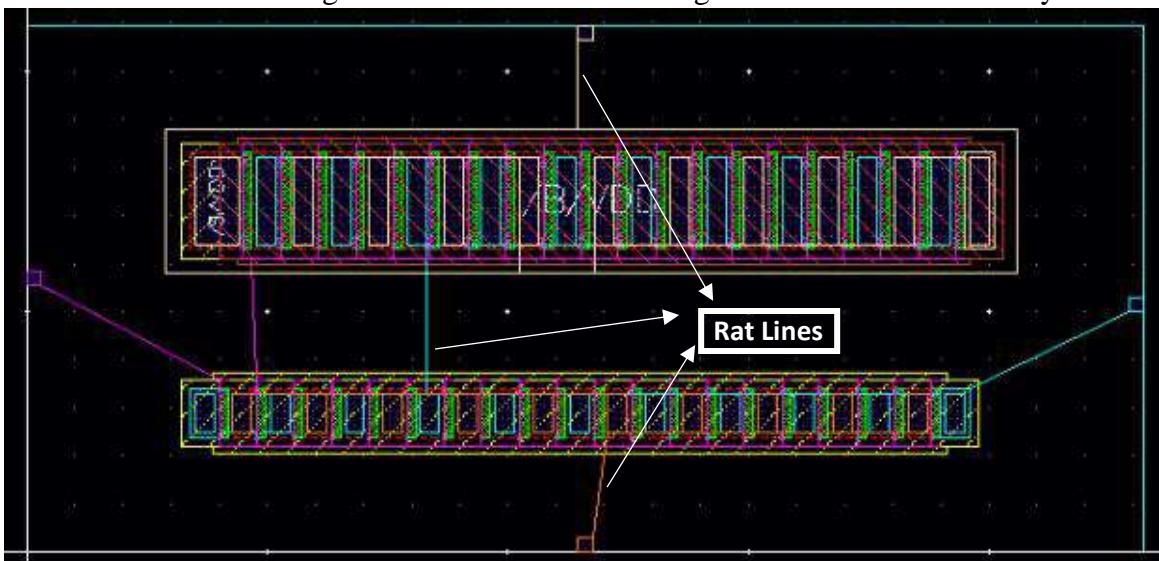


Figure – 1.109: Layout with Rat Lines

Use the bind key “P” for the interconnections. After the click on “P” in the keyboard, if the mouse pointer is taken close to the terminals in the transistor, it gets highlighted as shown in Figure – 1.110.

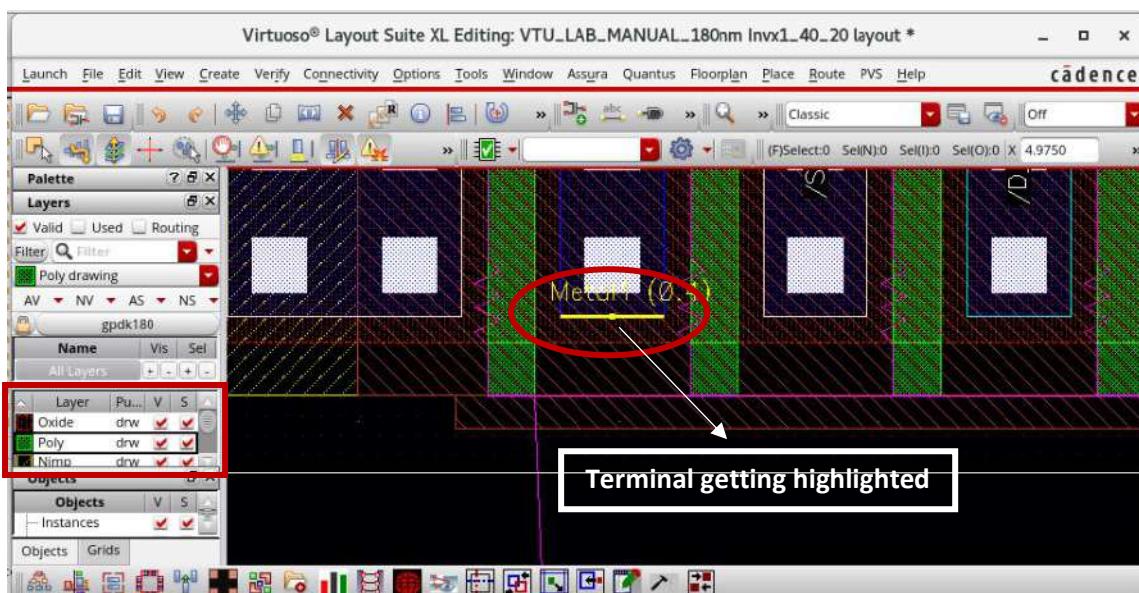


Figure – 1.110: Terminal getting highlighted

Use Left Mouse Click to start the interconnection from the terminal as shown in Figure – 1.111. The option “**Rectangle**” with bind key “**R**” can also be used for interconnections. In case of “**Rectangle**” option, select the respective layer from the “**Layer Palette**” as shown in Figure – 1.110 and then click on “**R**” in the keyboard, use Left Mouse Click to draw the respective layers. Similarly, use the option “**Shift + P**” to create “**Polygon**” which is useful in creating the layers in different shapes other than Rectangle and Square.

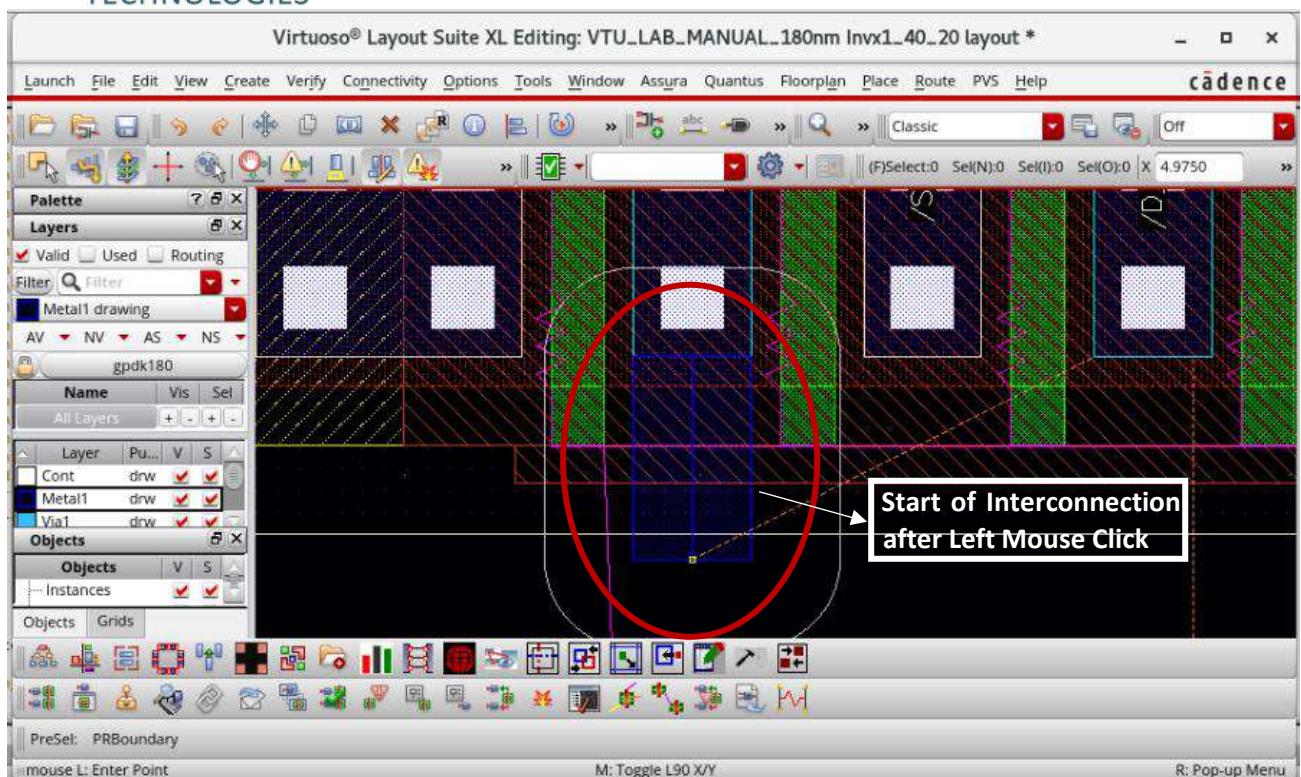


Figure – 1.111: Start of Interconnection after Left Mouse Click

Use the Left Mouse Click at the point where the interconnection has to end. The layout is updated as shown in Figure – 1.112.

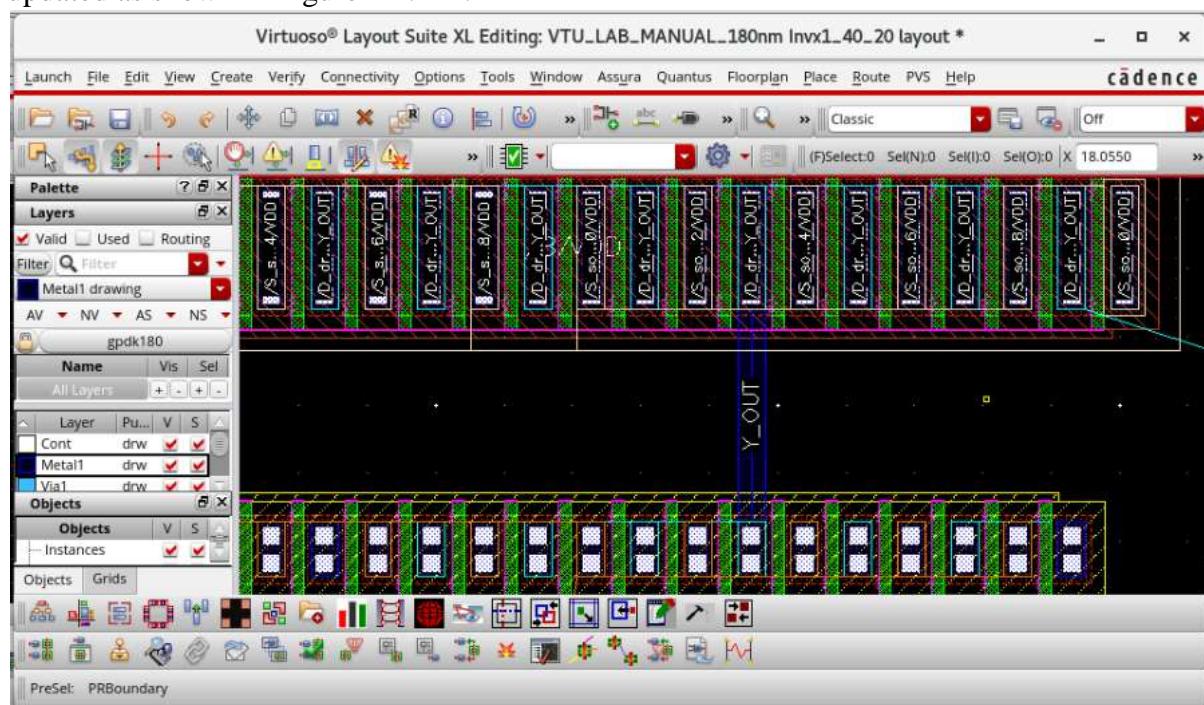


Figure – 1.112: Layout after the interconnections

Repeat the steps to complete the remaining connections in the layout.

For interconnections between two different layers, use a “Via”. Via has to be selected according to the layers present at the Start and End of the interconnections. To include a Via in the layout, select “Create → Via” as shown in Figure – 1.113.

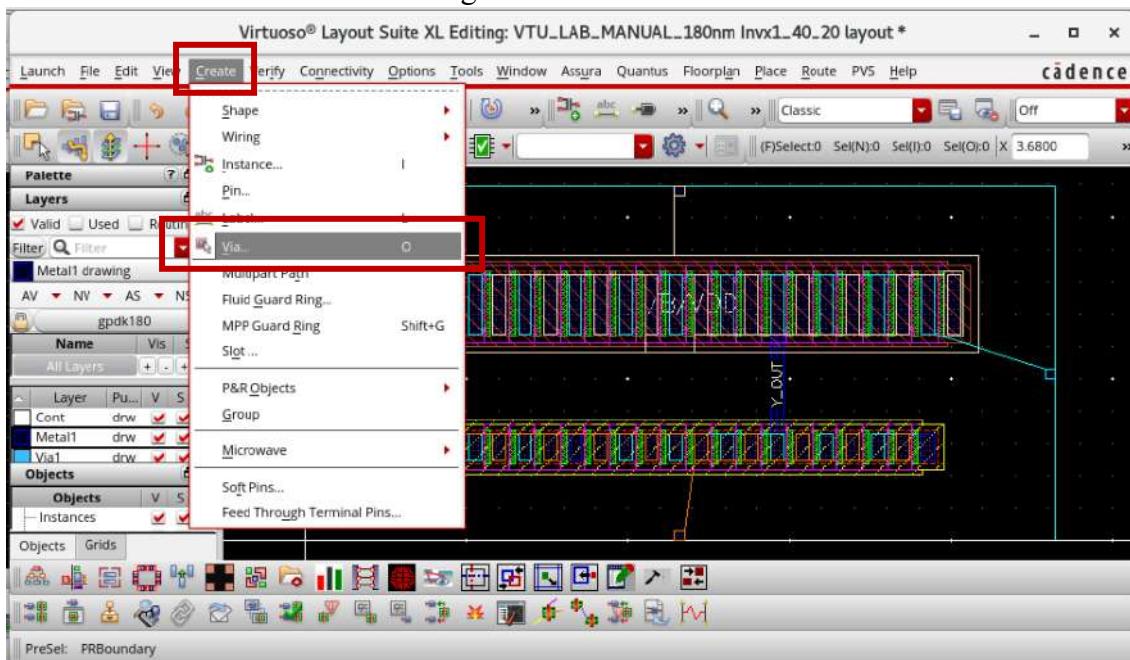


Figure – 1.113: Create → Via

The “Create Via” window pops up as shown in Figure – 1.114.

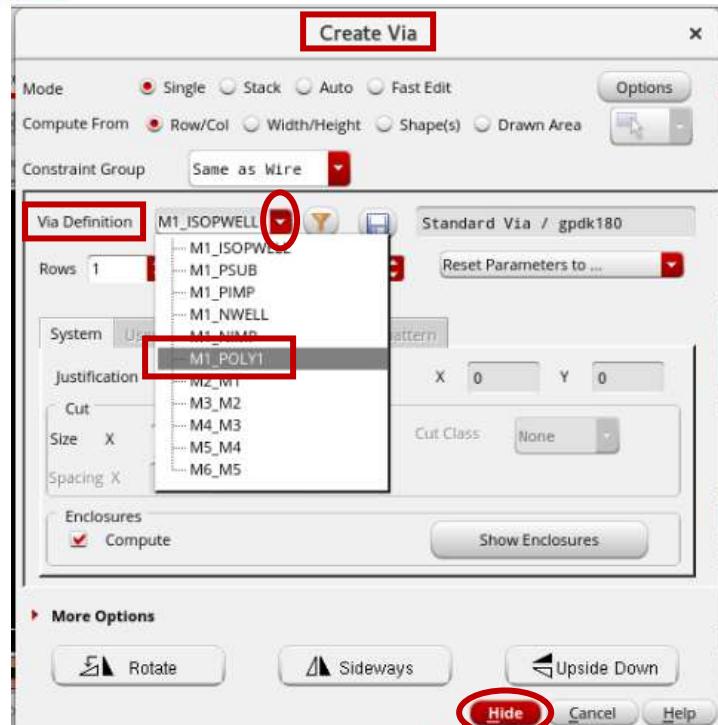


Figure – 1.114: Create Via window

The required Via can be selected through the “**Via Definition**” option as shown in Figure – 1.114. Click on the drop down and select the required Via. For example, in the CMOS Inverter design, the Input pin “A_IN” is of **Metal 1** layer and it has to be connected to the Gate terminal of PMOS and NMOS Transistors which is a **Poly** layer. So, from the Via Definition, **M1_POLY1** is selected as shown in Figure – 1.114. Click on “**Hide**” to visualize the Via on the Virtuoso Layout Editor as shown in Figure – 1.115. Use a Left Mouse Click to place the Via.

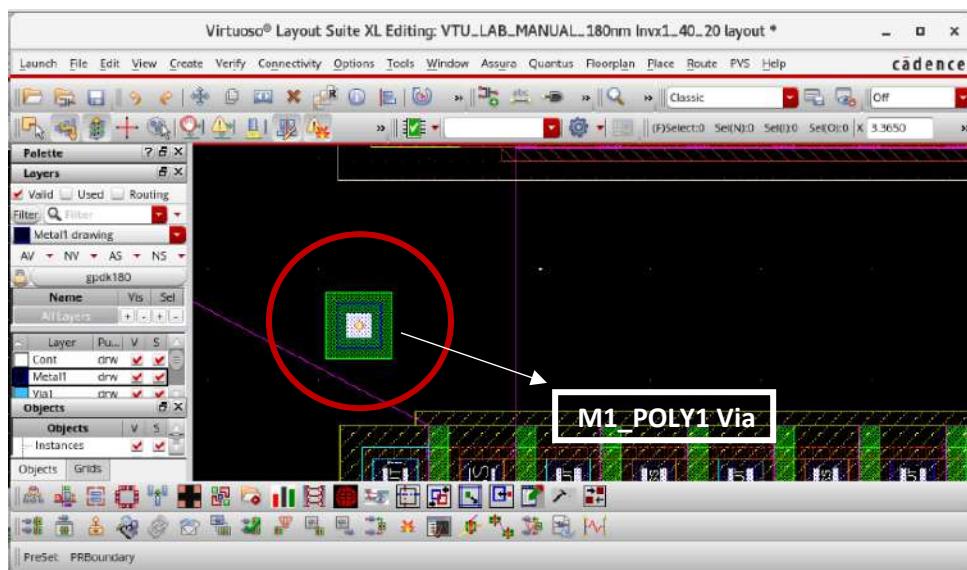


Figure – 1.115: Selected Via

Use the bind key “P” to complete the connections between the Input Pin and Via and between Via and Gate Terminal of the transistor. The completed layout can be visualized as shown in Figure – 1.116(a).

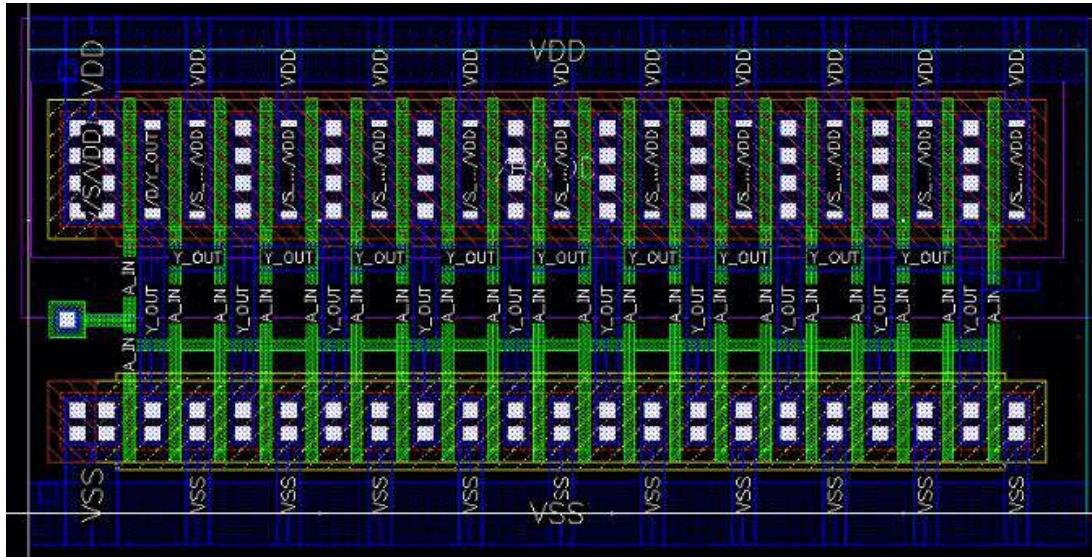


Figure – 1.116(a): Completed Layout

With the Template shown, the layout can be visualized as shown in Figure – 1.116(b).

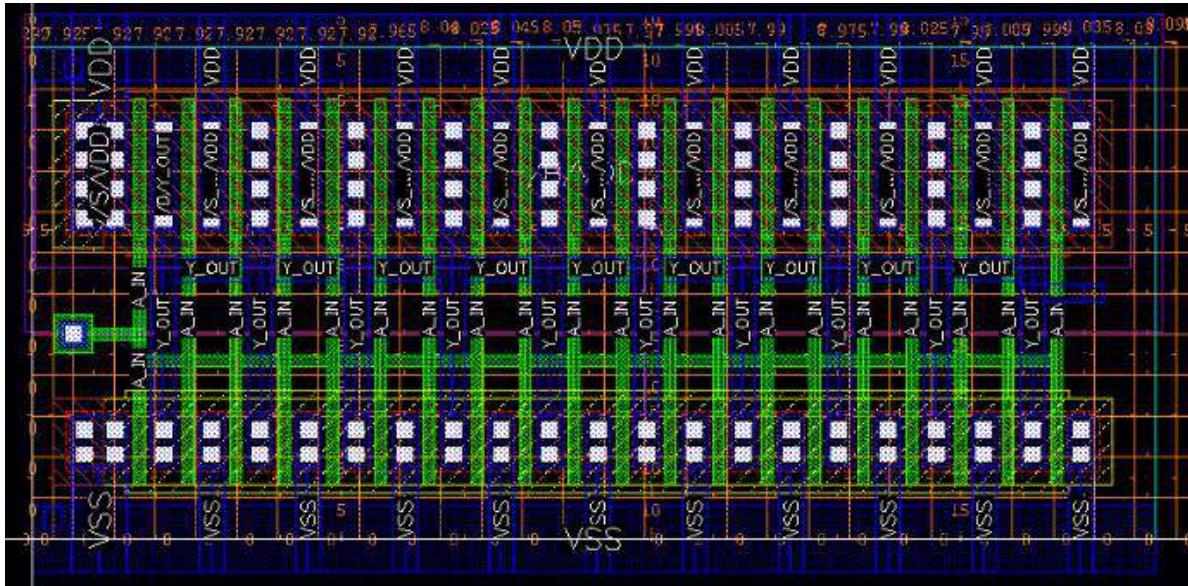


Figure – 1.116(b): Completed Layout with Template

Click on “File → Save” to Save the layout.

PHYSICAL VERIFICATION WITH ASSURA:

Physical Verification involves **DRC** (Design Rule Check) and **LVS** (Layout versus Schematic) checks on the layout. These checks are performed using Assura.

TECHNOLOGY LIBRARY (`assura_tech.lib`) MAPPING:

To map the library file, select “**Assura → Technology..**” as shown in Figure – 1.117.

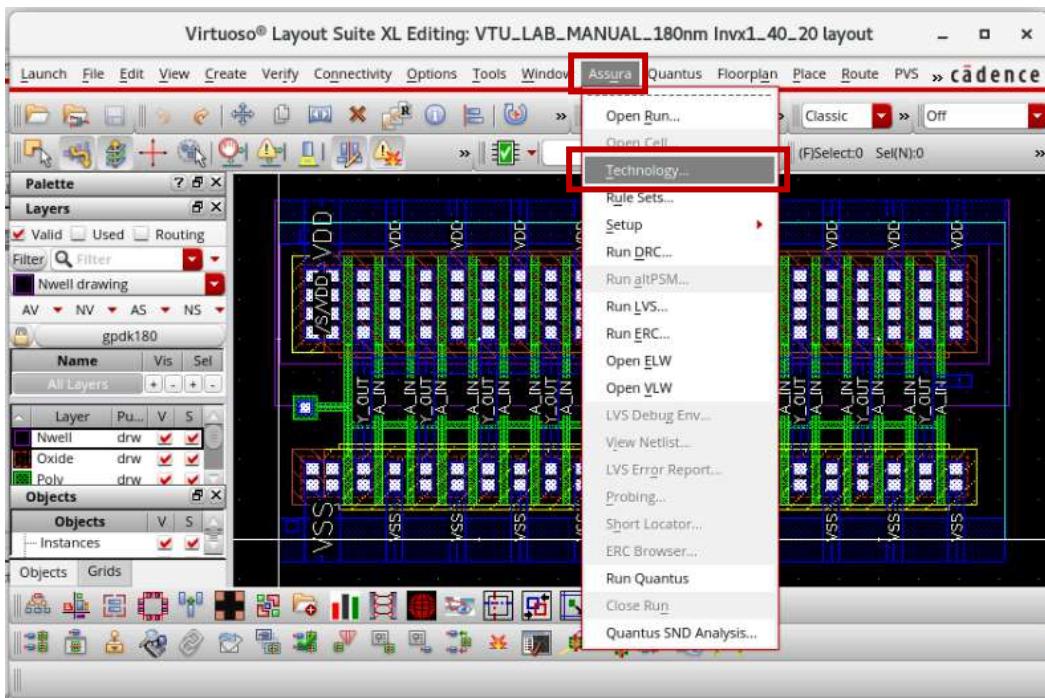


Figure – 1.117: Assura → Technology..

'The “Assura Technology Lib Select” window pops up as shown in Figure – 1.118.

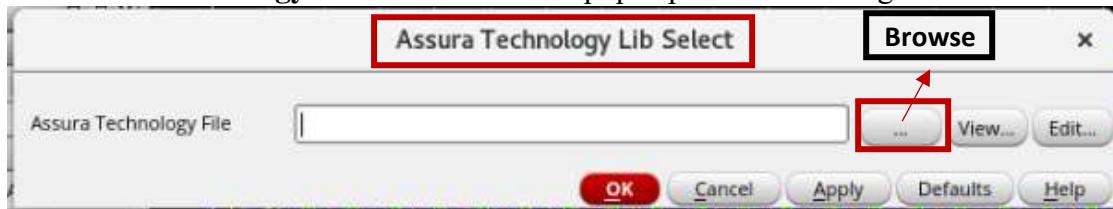


Figure – 1.118: Assura Technology Lib Select

Click on “Browse” option as shown in Figure – 1.118. The “File Selector” window pops up as shown in Figure – 1.119.

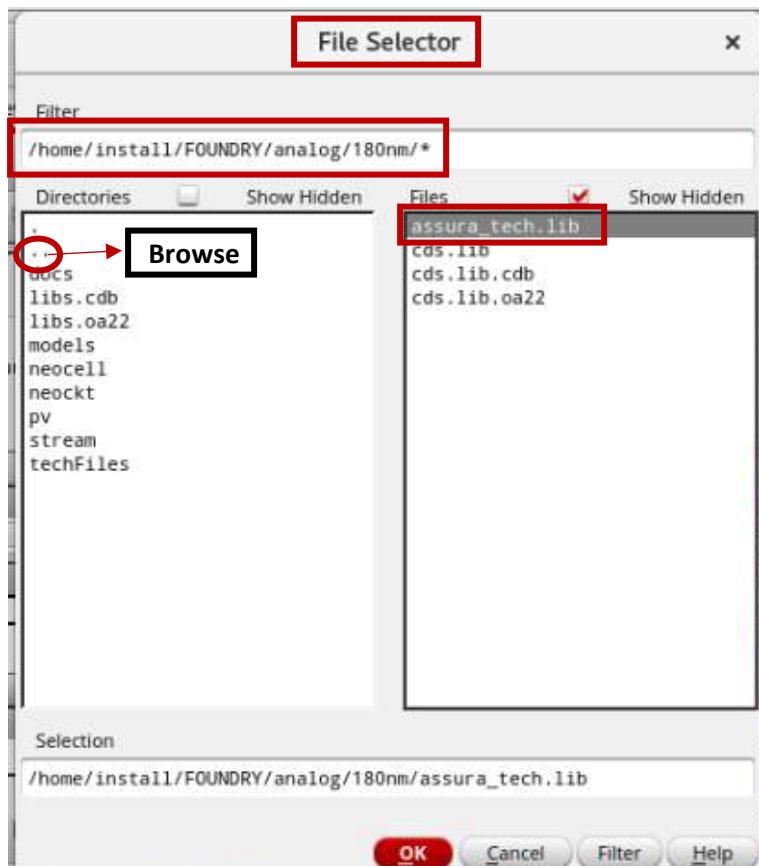


Figure – 1.119: File Selector window

Click on the “Browse” as shown in Figure – 1.119 to select the file “**assura_tech.lib**” from the location “**/home/install/FOUNDRY/analog/180nm/**”. Once a double-mouse click in done on “**assura_tech.lib**”, the path gets completed as shown in Figure – 1.120. Click on “**OK**”.

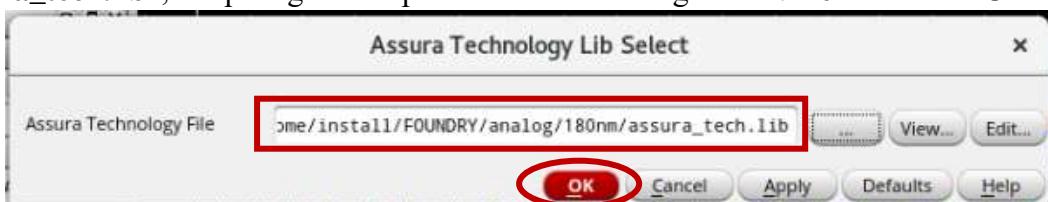


Figure – 1.120: Assura Technology Lib Select window after file selection

DRC (DESIGN RULE CHECK):

To run DRC check using Assura, select “**Assura → Run DRC**” as shown in Figure – 1.121.

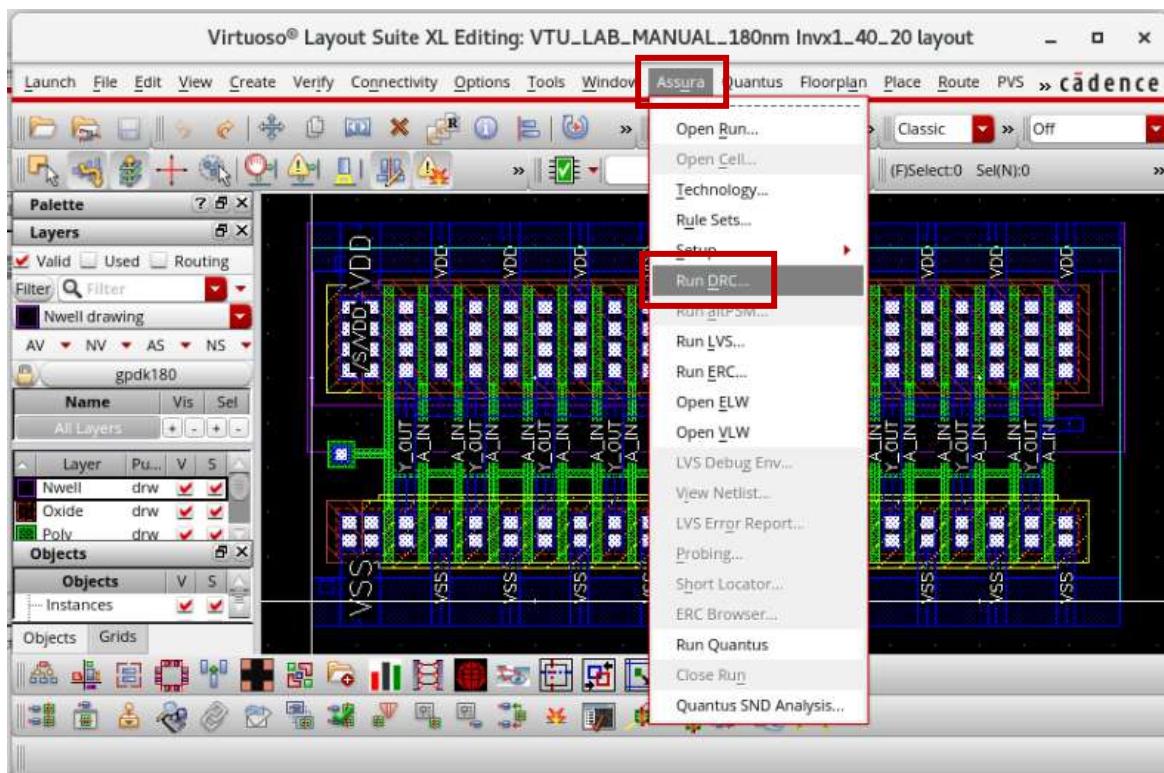


Figure – 1.121: Assura → Run DRC

The “Run Assura DRC” window pops up as shown in Figure – 1.122.

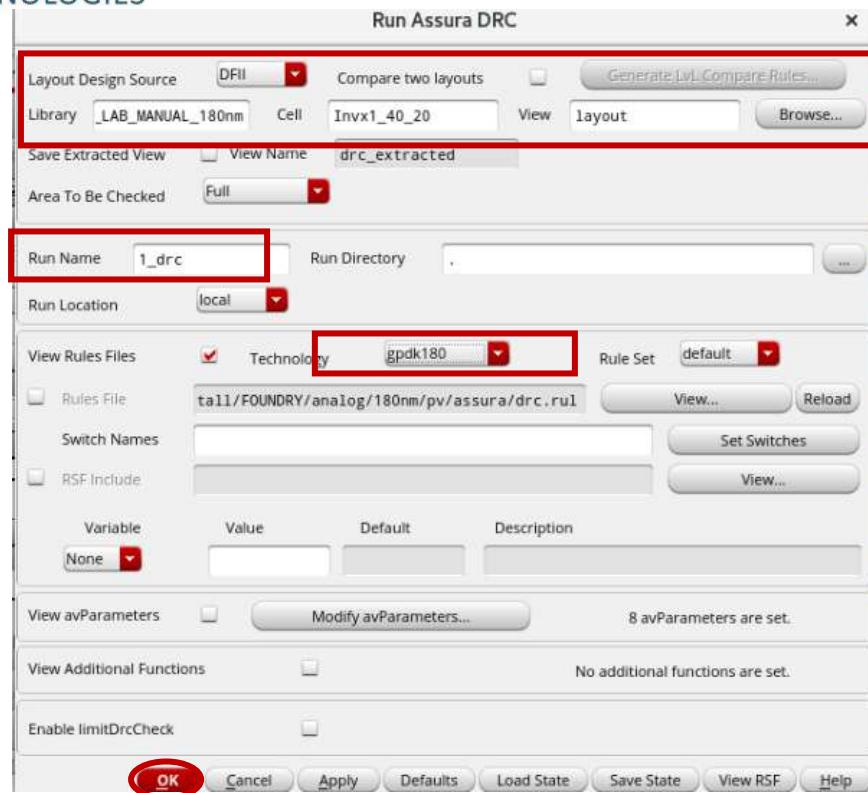


Figure – 1.122: Run Assura DRC window

Check for the “Layout Design Source”, mention a “Run Name” (it can be any name) and select “Technology → gpdk180” from the drop down and click on “OK” as shown in Figure – 1.122. The “Progress” window pops up as shown in Figure – 1.123.

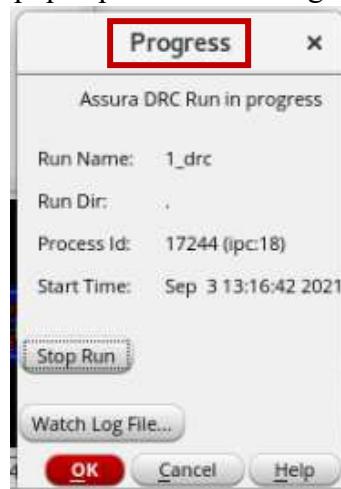


Figure – 1.123: “Progress” window

Once the DRC check is over, we get the DRC check completion window as shown in Figure – 1.124.

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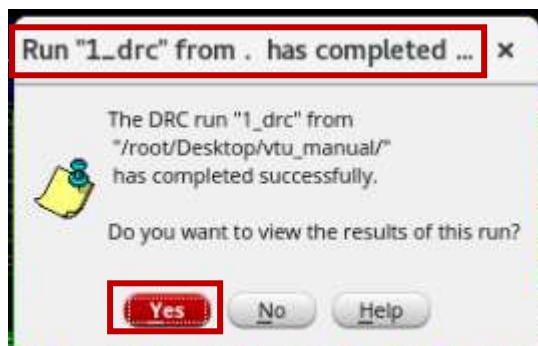


Figure – 1.124: DRC Check completion window

Click on “Yes” to get the results of DRC Check as shown in Figure – 1.125.



Figure – 1.125: Result of DRC Check if the layout is DRC clean

In case of errors, the error information will be shown. If the error is selected, it points out the issue which has to be reworked on the layout. Once done, Save the layout and re-run the DRC check to make sure that the layout is DRC clean.

LVS (LAYOUT VERSUS SCHEMATIC):

To run the LVS check using Assura, select “**Assura → Run LVS**” as shown in Figure – 1.126.

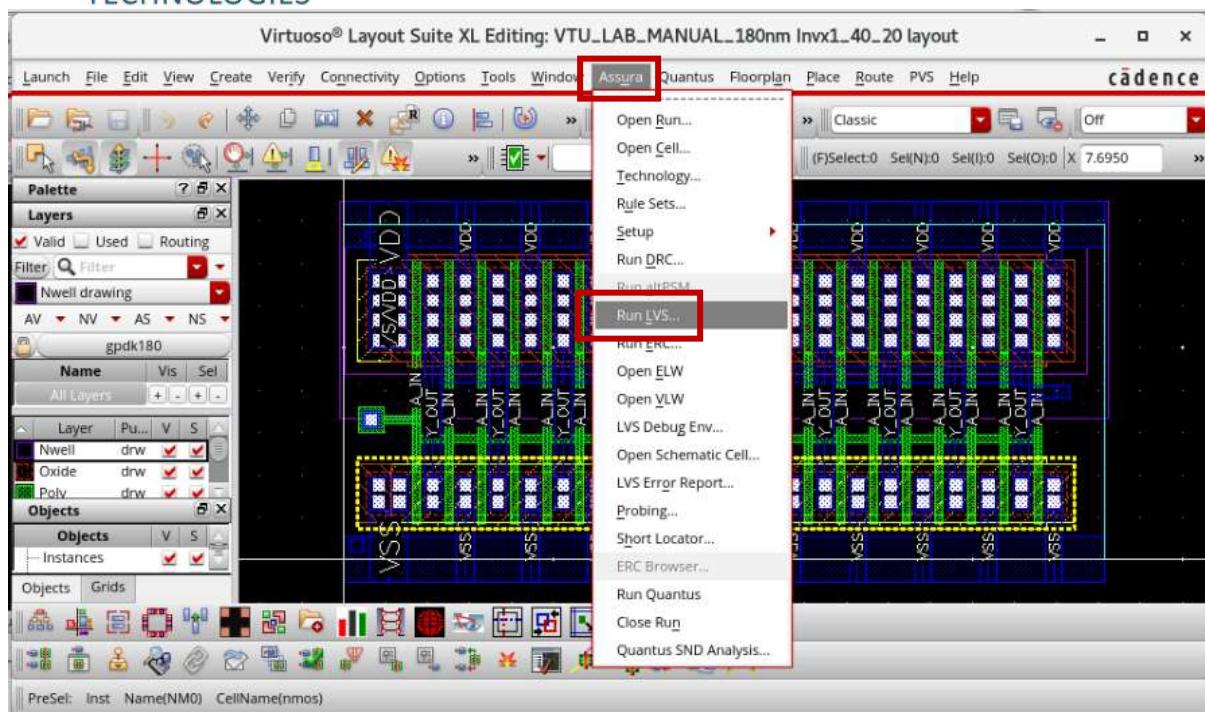


Figure – 1.126: Assura → Run LVS

The “Run Assura LVS” window pops up as shown in Figure – 1.127.

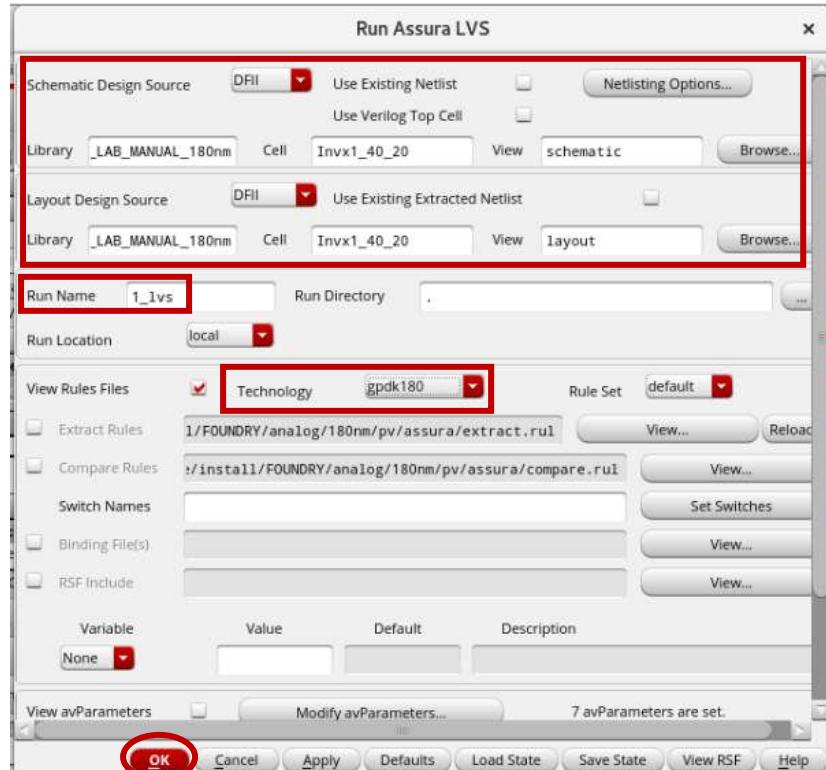


Figure – 1.127: Run Assura LVS window

Check for the correctness of the Schematic and Layout to be compared in the “**Schematic Design Source**” and the “**Layout Design Source**”, mention a “**Run Name**” (it can be any name but avoid space) and select the **Technology** (for example: gpdk180) as shown in Figure – 136. Click on “**OK**”. The progress of “**LVS**” check can be seen as shown in Figure – 137.

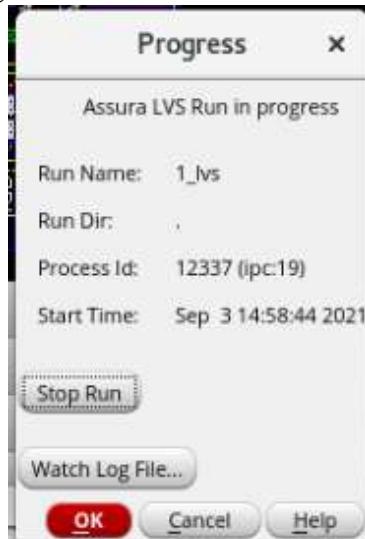


Figure – 1.128: LVS “Progress” window

After the LVS check gets completed, the “**Run: “1_lvs”**” window pops up. In case of violations in LVS check, the total number of violations can be seen as shown in Figure – 1.129. Since there are no violations, it shows as “**0**”.

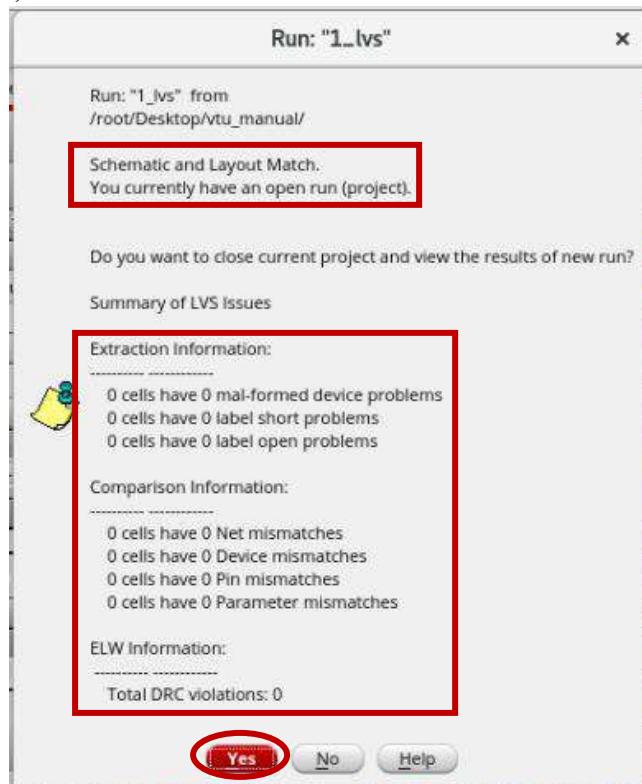


Figure – 1.129: “Run: “1_lvs”” window

Click on “Yes” to see the result in the “LVS Debug” window as shown in Figure – 1.130.

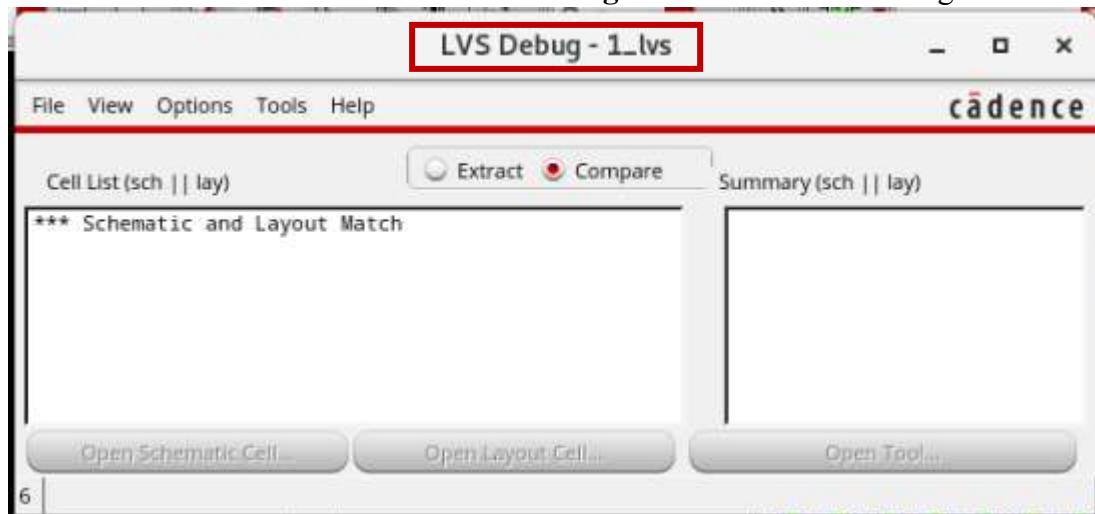


Figure – 1.130: “LVS Debug” window

Since the design is LVS clean, the message “**Schematic and Layout Match**” can be seen. In case of violations, the respective messages are listed out.

QRC (RC / PARASITIC EXTRACTION):

The tool used for Parasitic Extraction process is “**Quantus**”. Select “**Assura → Run Quantus**” as shown in Figure – 1.131 to invoke the tool and enter the “**Quantus (Assura) Parasitic Extraction Run Form**”.

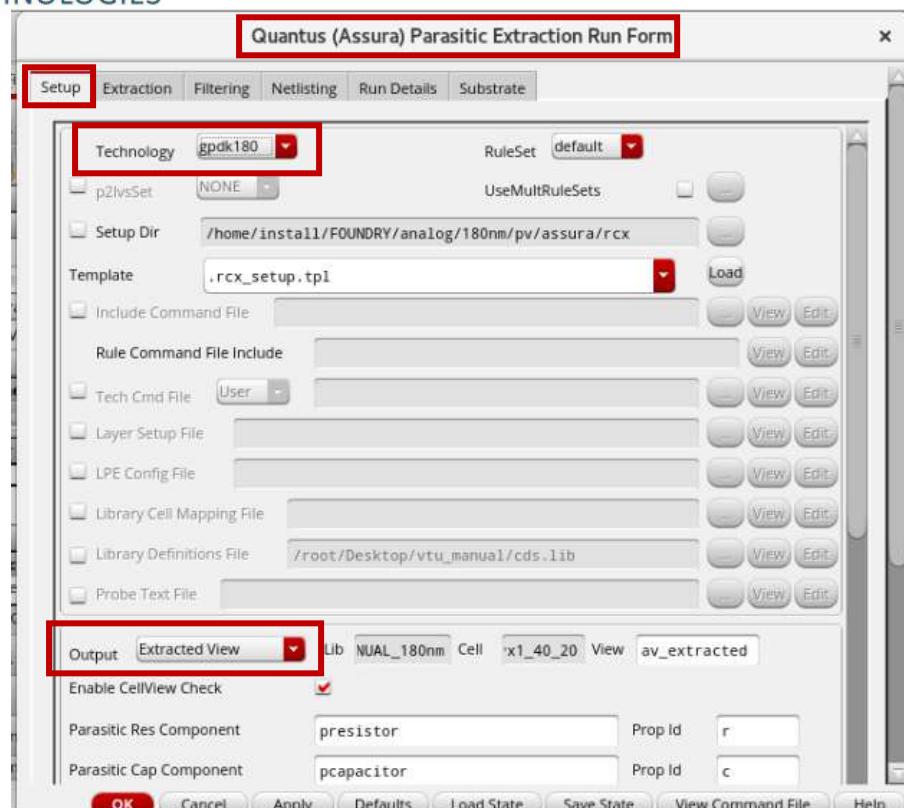


Figure – 1.131: Quantus (Assura) Parasitic Extraction Run Form

Click on the “Setup” tab, check for “Technology → gdk180” and select “Output → Extracted View” as shown in Figure – 1.131. Click on “Extraction” tab and the options can be seen as shown in Figure – 1.132.

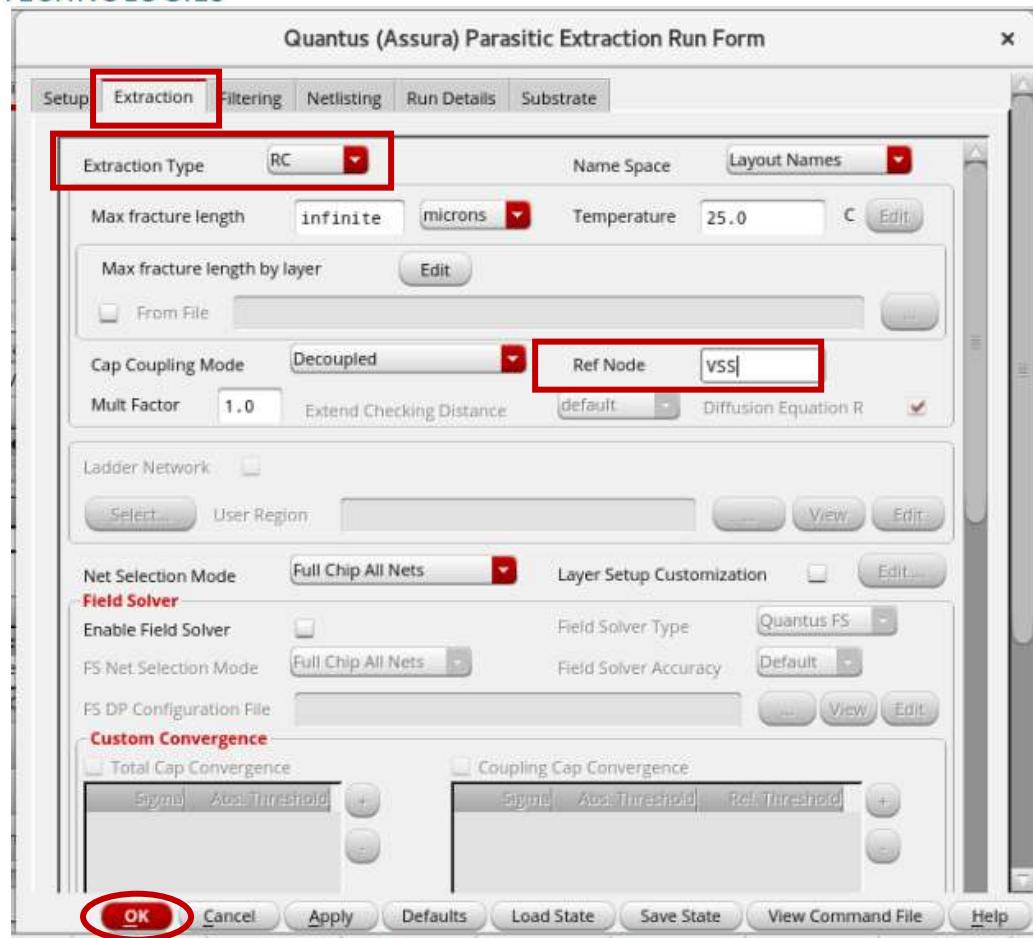


Figure – 1.132: “Extraction” Tab

Select “**Extraction Type → RC**” and the other options like “**R only**”, “**C only**” and others can be checked as per the requirements. Select the “**Ref Node → VSS**” and click on “**OK**” as shown in Figure – 1.132. The “**Quantus Progress Form**” can be seen as shown in Figure – 1.133.

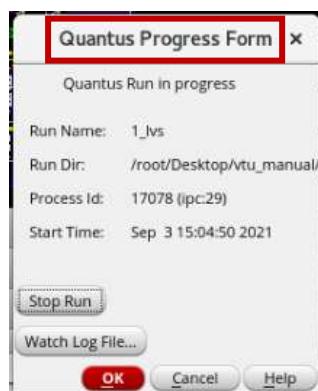


Figure – 1.133: Quantus Progress Form

After Extraction, the “Quantus Run” form pops up with the “av_extracted” file’s location as shown in Figure – 1.134.

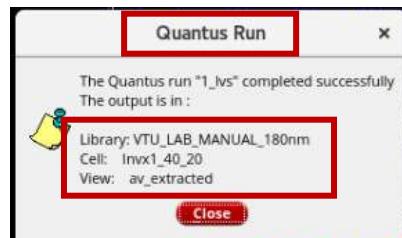


Figure – 1.134: Quantus Run form

The details of Extracted Parasitics are available with the av_extracted view and the file can be opened from the Library Manager as shown in Figure – 1.135.

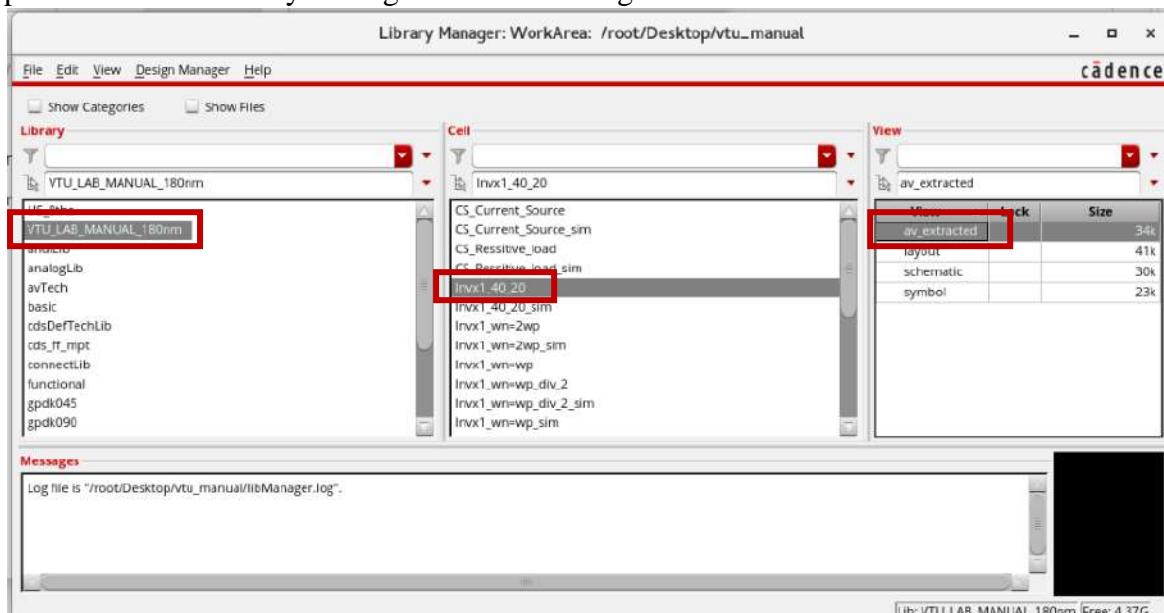


Figure – 1.135: “av_extracted” view from Library Manager

Double Click on “av_extracted” view to see the Extracted View of the layout as shown in Figure – 1.136.

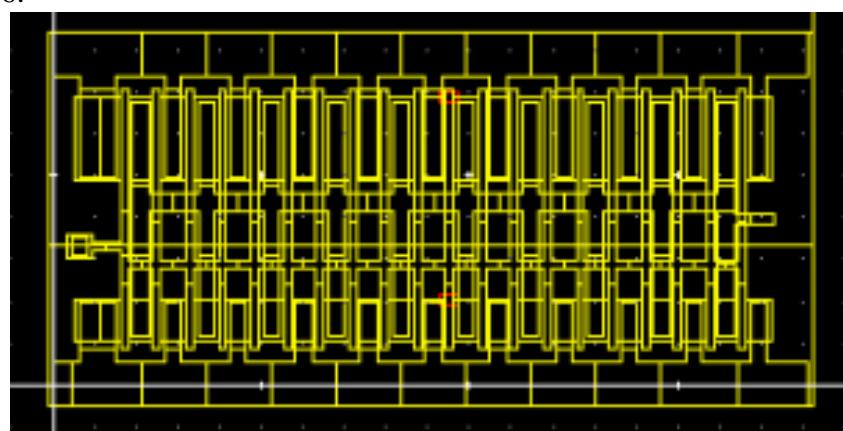


Figure – 1.136: Extracted View

Use the Mouse Scroller to “Zoom In” and “Zoom out” in order to view the parasites as shown in Figure – 1.137.

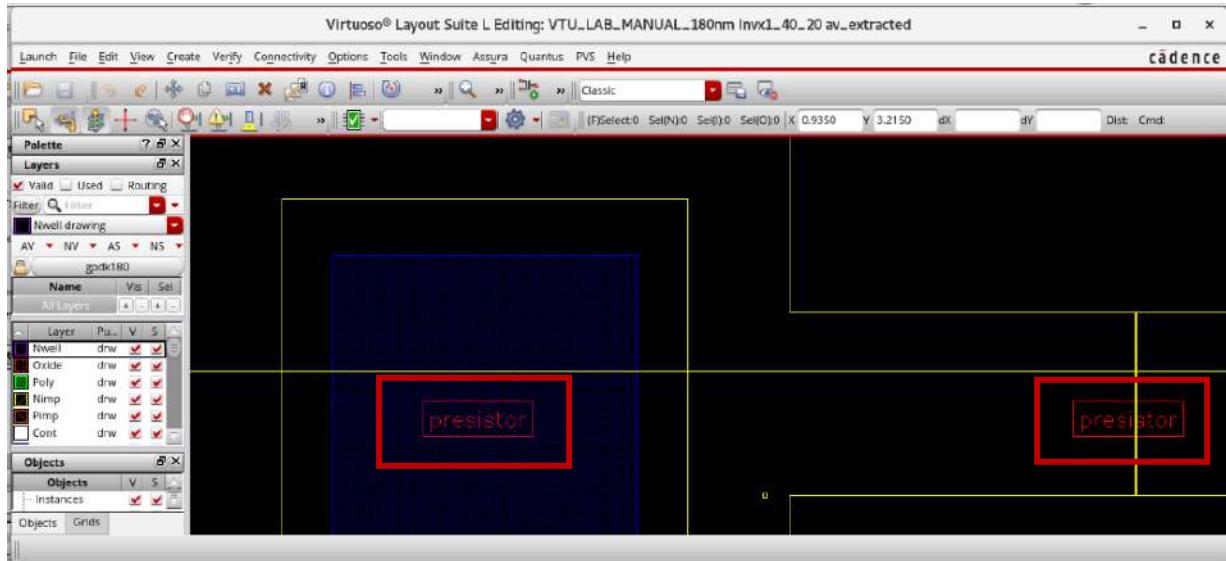


Figure – 1.137: Parasitic Resistance (presistor) after Zoom In

To check out the values of these Parasitic Resistance, click on “Shift + F”. By zooming in further, the values can be checked out as shown in Figure – 1.138.

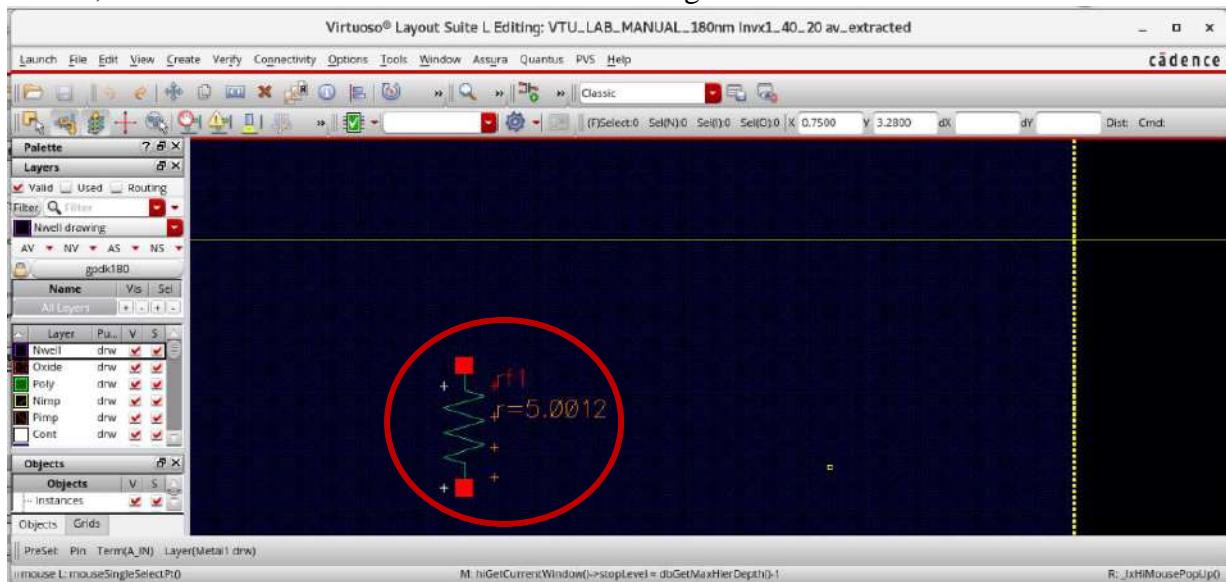


Figure – 1.138: Value of Parasitic Resistance

The impact of these parasitic devices can be checked out through the Backannotation (Post Layout Simulation) process.

BACKANNOTATION (POST LAYOUT SIMULATION):

To run the Post Layout Simulation, the extracted Parasitics have to be imported into the Test Schematic. So, a New Configuration has to be created.

To create a “New Configuration” select the Cell which has the Test Schematic and select its “Schematic” view as shown in Figure – 1.139.

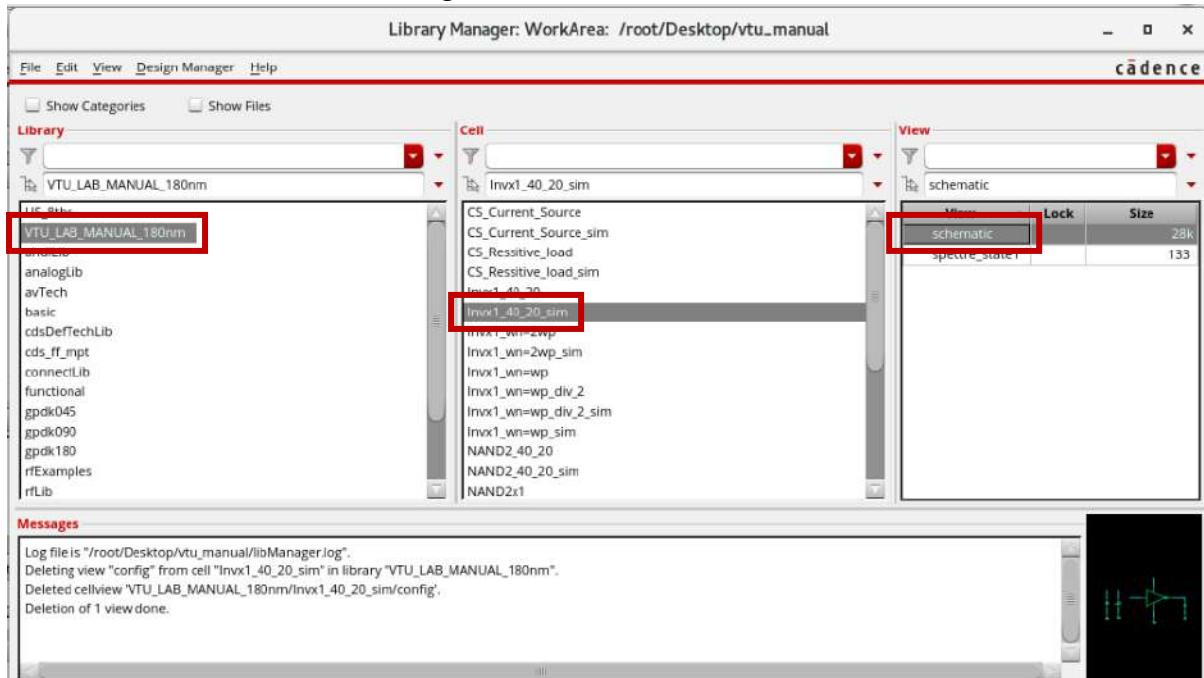


Figure – 1.139: Selecting the “Schematic” view

Click on “File → New → Cell View” as shown in Figure – 1.140.

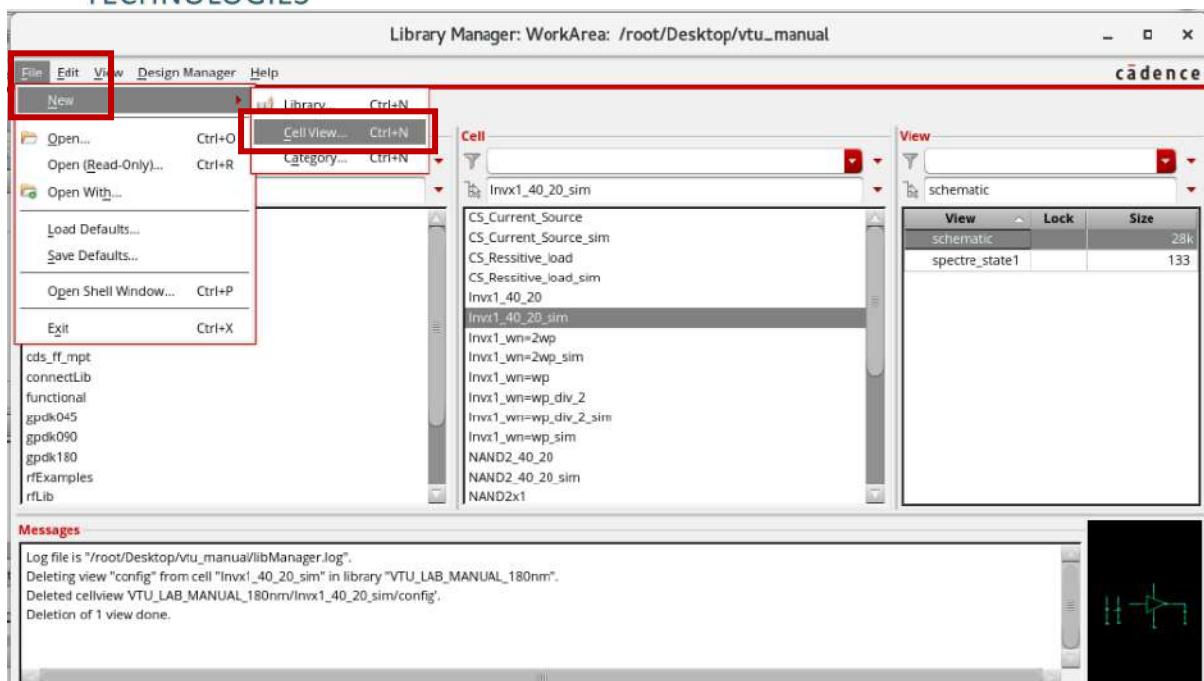


Figure – 1.140: File → New → Cell View

The “New File” window pops up. Select the “Type → config” from the drop down as shown in Figure – 1.141. Soon as the “Type → config” is selected, “View → config” and in “Application”, “Open with → Hierarchy Editor” gets updated. Click on “OK”.



Figure – 1.141: “New File” window

The “New Configuration” window pops up as shown in Figure – 1.142. Click on “Use Template”.



Figure – 1.142: “New Configuration” window

The “Use Template” window pops up as shown in Figure – 1.143.

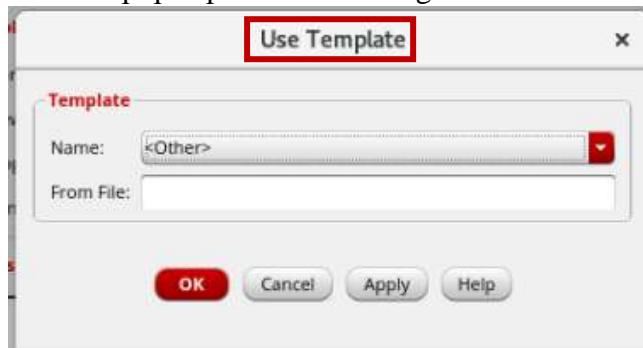


Figure – 1.143: Use Template window

Click on the drop down and select “**Name → Spectre**”, the name of the Simulator and click on “**OK**” as shown in Figure – 1.144.

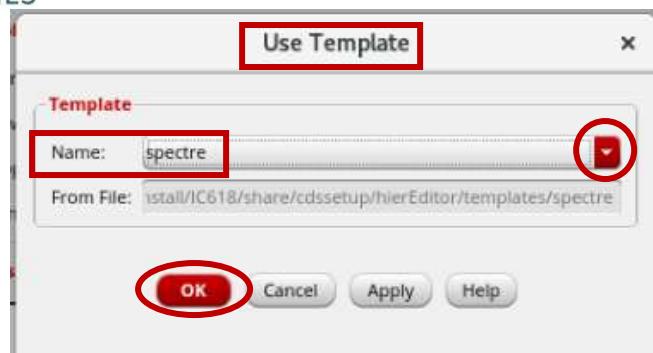


Figure – 1.144: Name → Spectre

The updated “New Configuration” window pops up as shown in Figure – 1.145.

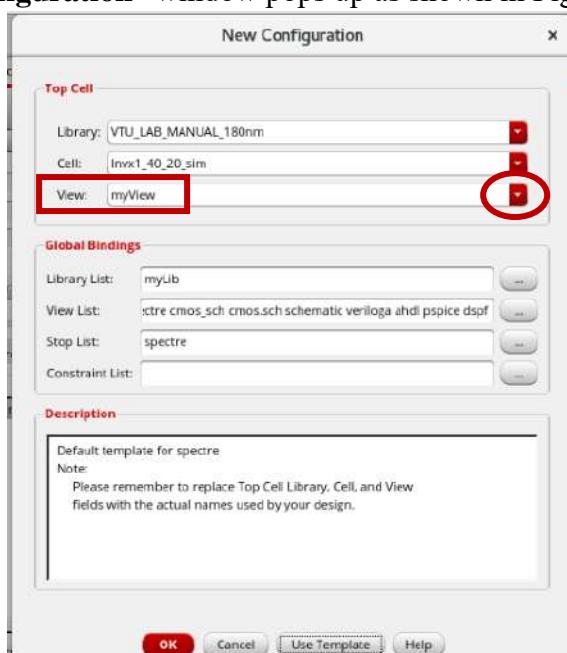


Figure – 1.145: New Configuration window

The “Top Cell → View → Schematic” has to be selected using the drop down as shown in Figure – 1.145. The “New Configuration” window gets updated as shown in Figure – 1.146.

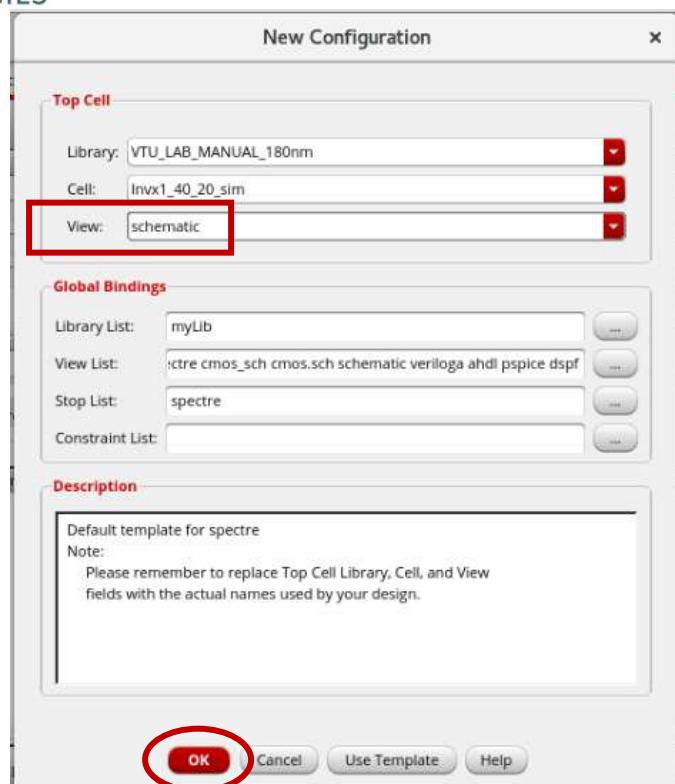


Figure – 1.146: Top Cell → View → Schematic

Click on “OK” and the “Virtuoso Hierarchy Editor: New Configuration” window pops up as shown in Figure – 1.147.

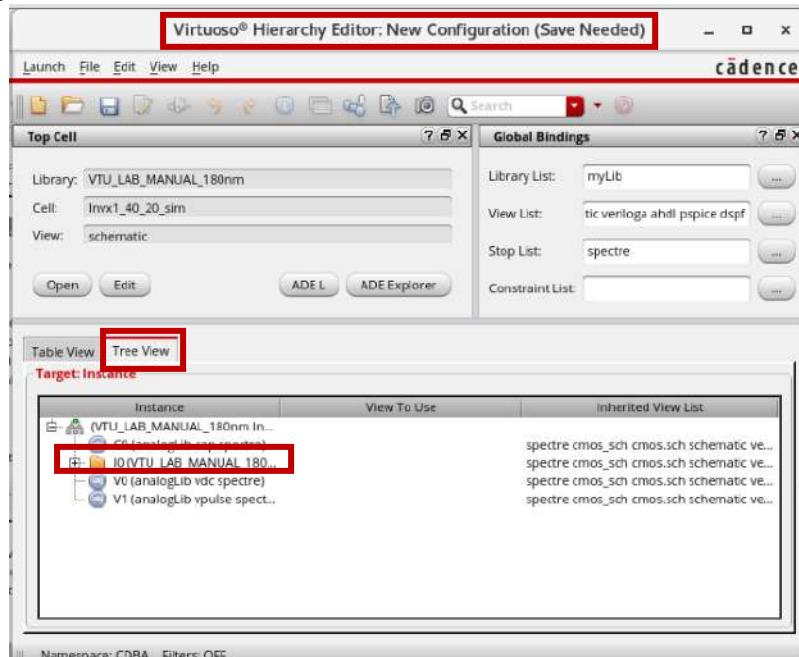


Figure – 1.147: Virtuoso Hierarchy Editor: New Configuration window

Two types of views, “**Table View**” and “**Tree View**” can be seen. Select “**Tree View**” as shown in Figure – 1.147, the instance “**I0**” which is the Instance number of the Symbol with which we had created the Test Schematic can be seen.

Select the Instance “**I0**” as shown in Figure – 1.148, make a Right Click, select “**Set Instance View → av_extracted**”.

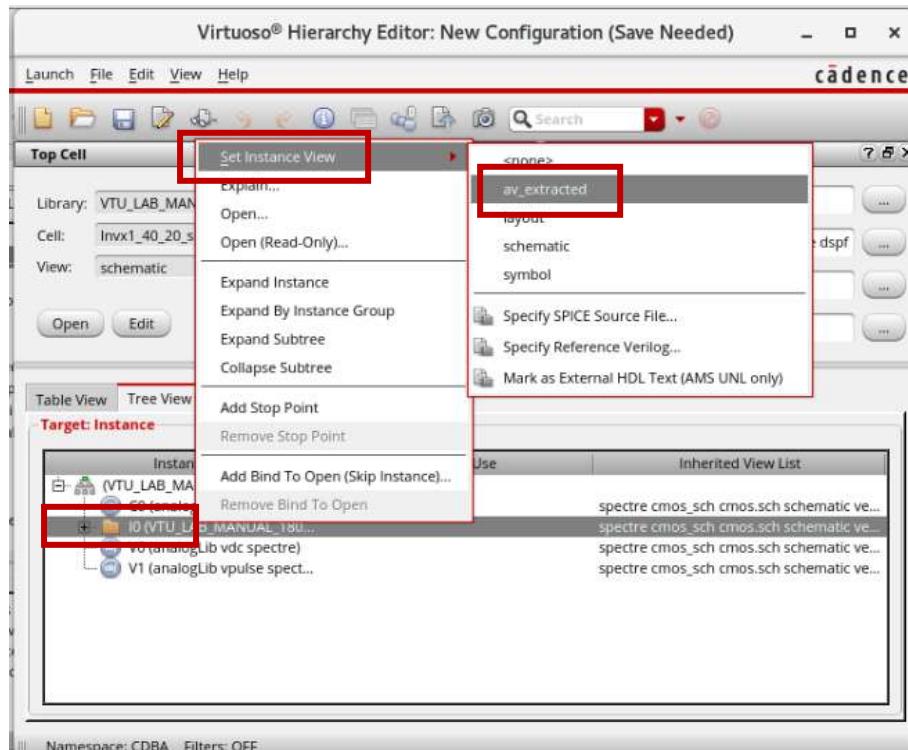


Figure – 1.148: Set Instance View → av_extracted

Click on the “+“ sign before the instance “**I0**” to see the imported parasitics as shown in Figure – 1.149.

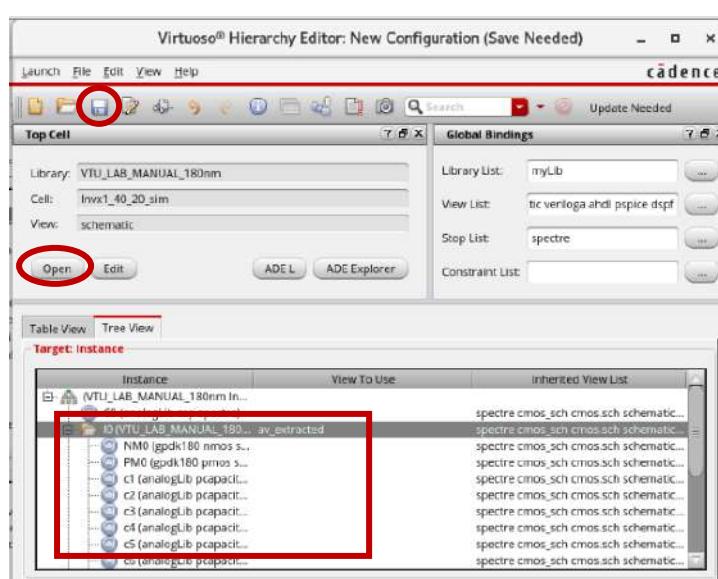


Figure – 1.149: Imported Parasitics

Click on the “Save” option, click on “Open” to bring back the Test Schematic as shown in Figure – 1.150.

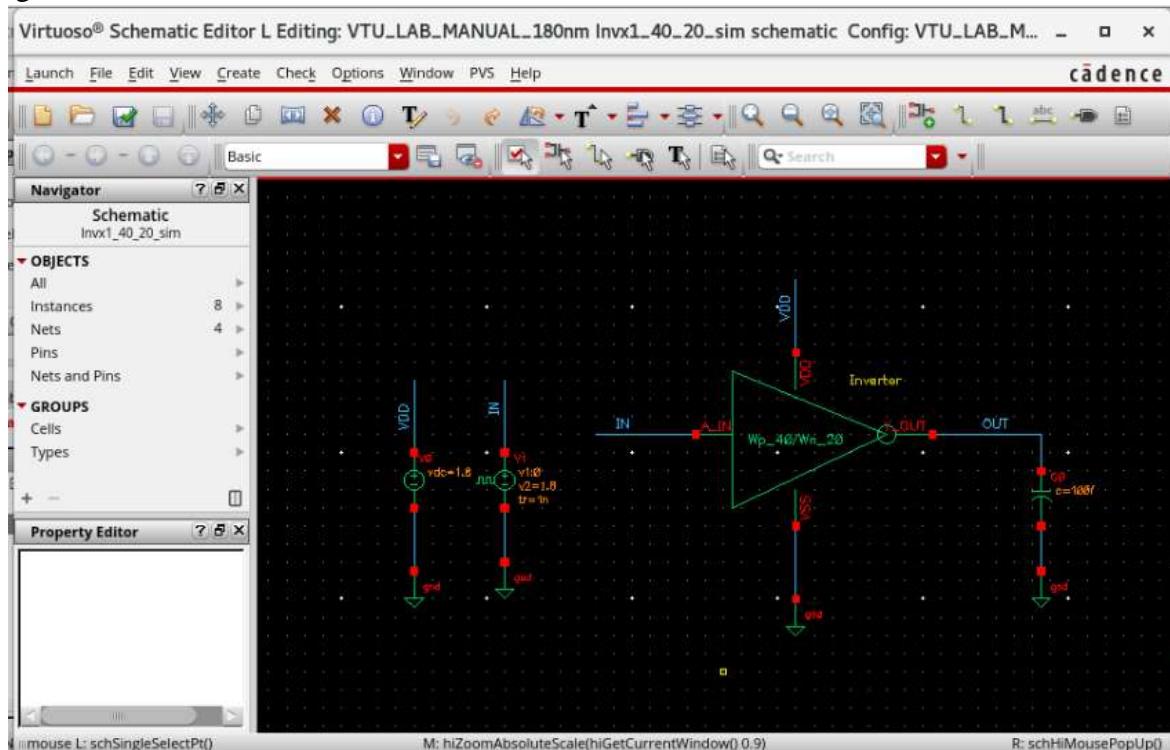


Figure – 1.150: Test Schematic

To verify if the parasitics are imported, double click on the Inverter symbol, the “**Descend**” window pops up as shown in Figure – 1.151. Check if “**View → av_extracted**” and select “**Open in → new tab**” and click on “**OK**”

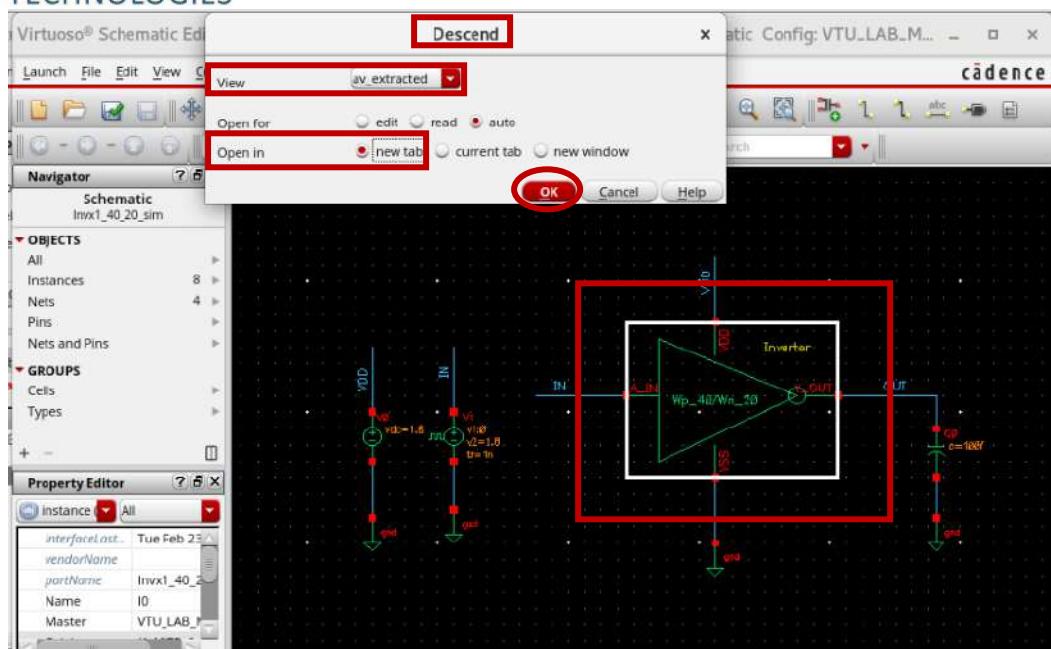


Figure – 1.151: Descend window

This should open the av_extracted view as we had seen in Figure -1.139 in a new tab as shown in Figure – 1.152.

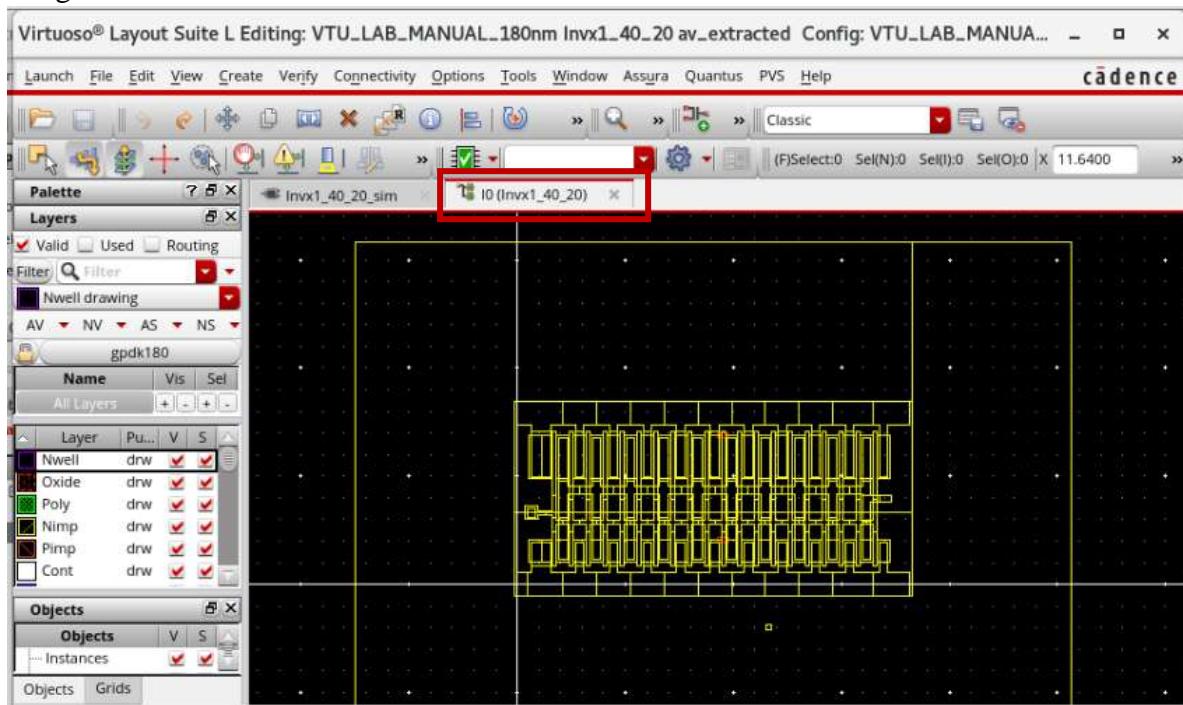


Figure – 1.152: av_extracted view in a new tab

Click on “Launch → ADE L” and select “Session → Load State” to open the Saved State as shown in Figure – 1.153.

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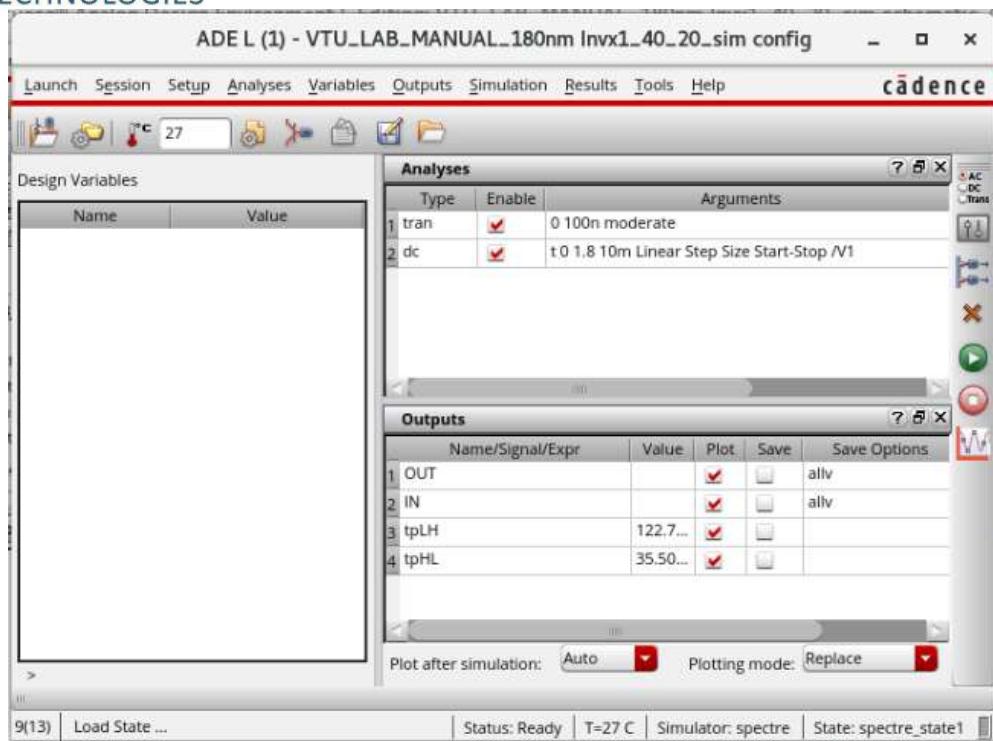


Figure – 1.153: Saved State

Re-run the Simulation and check for the waveforms of Transient Analysis and DC Analysis as shown in Figure – 1.154.



Figure – 1.154: Waveforms of Transient Analysis and DC Analysis

Using the Calculator, obtain the Switching Potential, tp_{HL} , tp_{LH} and t_{PD} . The results are tabulated in Table – 8.

Table – 8: Values of tp_{HL} , tp_{LH} and t_{PD} for CMOS Inverter with $\frac{W_P}{W_N} = \frac{40}{20}$

| MOSFET | Length | Width | tpLH | tpHL | tpd |
|--------|--------|-------|----------|----------|----------|
| PMOS | 180n | 40u | 1.23E-10 | 3.55E-11 | 7.78E-11 |
| NMOS | 180n | 20u | | | |

LAB – 02: 2 – INPUT CMOS NAND GATE

Objective:

- (a) Capture the Schematic of a 2 – input CMOS NAND Gate having similar delay as that of CMOS Inverter computed in Lab – 01. Verify the functionality of the NAND Gate and also find out the delay for all the four possible combinations of input vectors. Tabulate the results. Increase the drive strength to 2X and 4X and tabulate the results.
- (b) Draw the layout of NAND with $\frac{W_P}{W_N} = \frac{40}{20}$, use optimum layout methods. Verify DRC and LVS, extract the parasitics and perform the post layout simulation, compare the results with pre layout simulations. Record the observations.

Solution – (a):

SCHEMATIC CAPTURE:

Following the techniques demonstrated in Lab – 01, Create a New Library using the option “File → New → Library”, create a New Cell View upon selecting the newly created library using the option “File → New → Cell View” and instantiate the required devices using the “Create → Instance” option.

The device parameters are listed in Table – 9.

Table – 9: Width and Length of NMOS and PMOS Transistors for CMOS NAND Gate

| Library Name | Cell Name | Comments / Properties |
|--------------|-----------|---|
| gdk180 | Nmos | Width, $W_N = 1.7 \mu$ Length, $L = 180 \text{ n}$ |
| gdk180 | Pmos | Width, $W_P = 1.275 \mu$ Length, $L = 180 \text{ n}$ |

Similarly, the device parameters for the 2 – input CMOS NAND Gate with drive strength 2 and drive strength 4 are listed in Table – 10 and Table – 11.

Table – 10: Width and Length of NMOS and PMOS Transistors for CMOS NAND Gate with Drive Strength “2”

| Library Name | Cell Name | Comments / Properties |
|--------------|-----------|--|
| gdk180 | Nmos | Width, $W_N = 3.4 \mu$ Length, $L = 180 \text{ n}$ |
| gdk180 | Pmos | Width, $W_P = 2.55 \mu$ Length, $L = 180 \text{ n}$ |

Table – 11: Width and Length of NMOS and PMOS Transistors for CMOS NAND Gate with Drive Strength “4”

| Library Name | Cell Name | Comments / Properties |
|--------------|-----------|---|
| gdk180 | Nmos | Width, $W_N = 6.8 \mu$ Length, $L = 180 \text{ n}$ |
| gdk180 | Pmos | Width, $W_P = 5.1 \mu$ Length, $L = 180 \text{ n}$ |

The completed Schematic for all the three dimensions are shown in Figure – 2.1, Figure – 2.2 and Figure – 2.3.

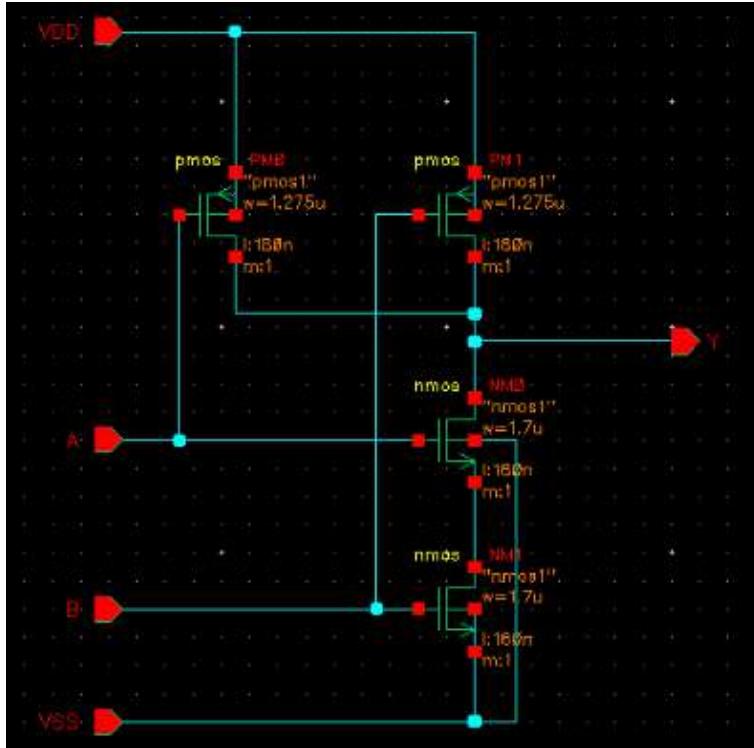


Figure – 2.1: Schematic Capture of 2 – input CMOS NAND Gate (NAND2X1)

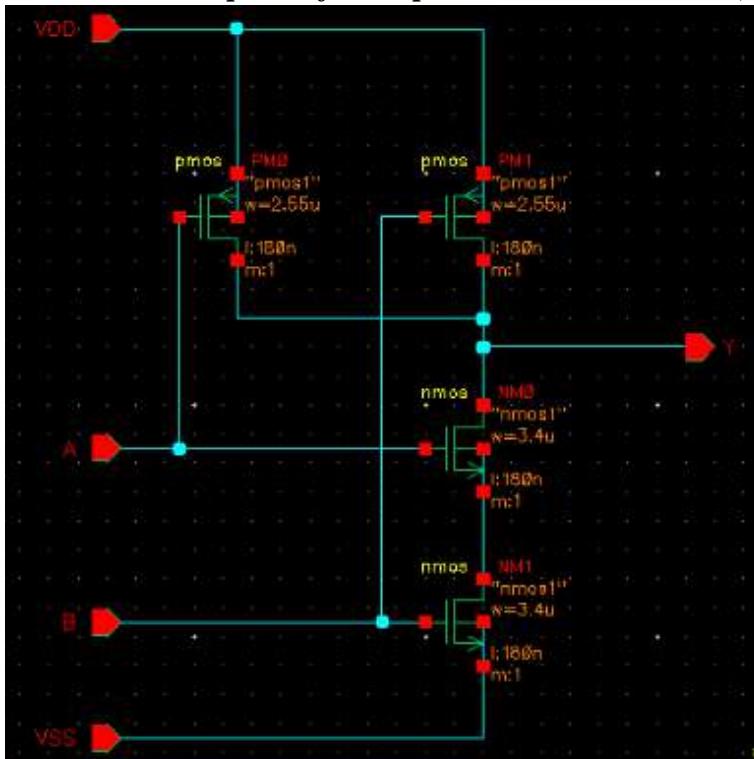


Figure – 2.2: Schematic Capture of 2 – input CMOS NAND Gate with drive strength 2 (NAND2X2)

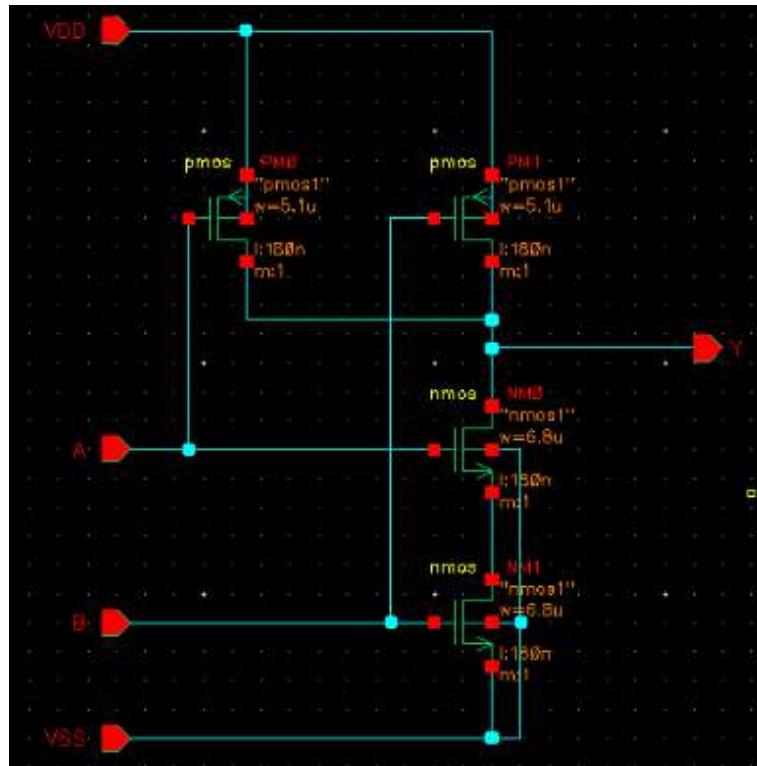


Figure – 2.3: Schematic Capture of 2 – input CMOS NAND Gate with drive strength 2 (NAND2X4)

The symbol for the CMOS NAND Gate is shown in Figure – 2.4.

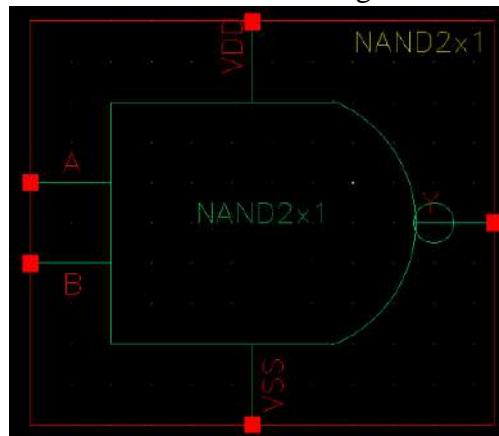


Figure – 2.4: Symbol of 2 – input NAND Gate

FUNCTIONAL SIMULATION:

Using the symbol created, build the Test Schematic. Create a New Cell View, instantiate the symbol of 2 – input NAND Gate, DC Voltage Source, Capacitance and Ground, connect the using wires. Create two input pins for the circuit A and B and connect them to the input of the

NAND gate as shown in Figure – 2.5. Repeat the same procedure for creating the Test Schematic for the 2 – input CMOS NAND Gate with drive strength 2 and drive strength 4.

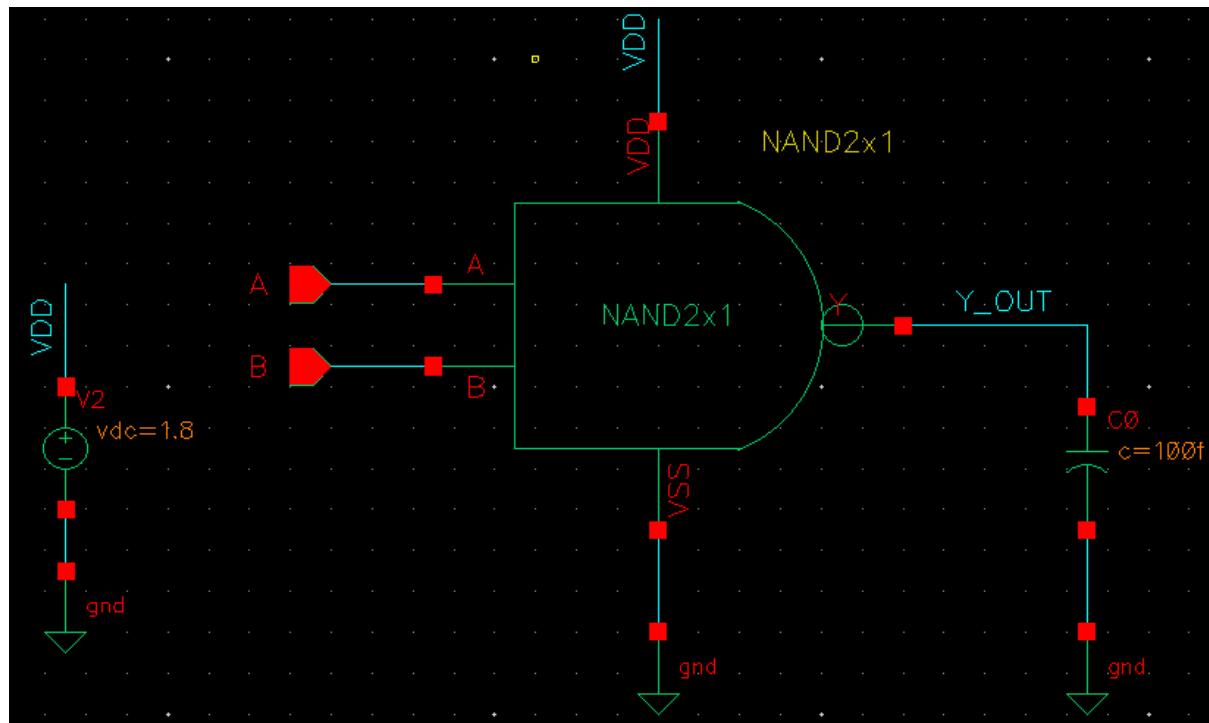


Figure – 2.5: Test Schematic for 2 – input CMOS NAND Gate

Launch ADE L, select “Setup → Stimuli” as shown in Figure – 2.6 to give the required sequence of inputs to pins A and B.

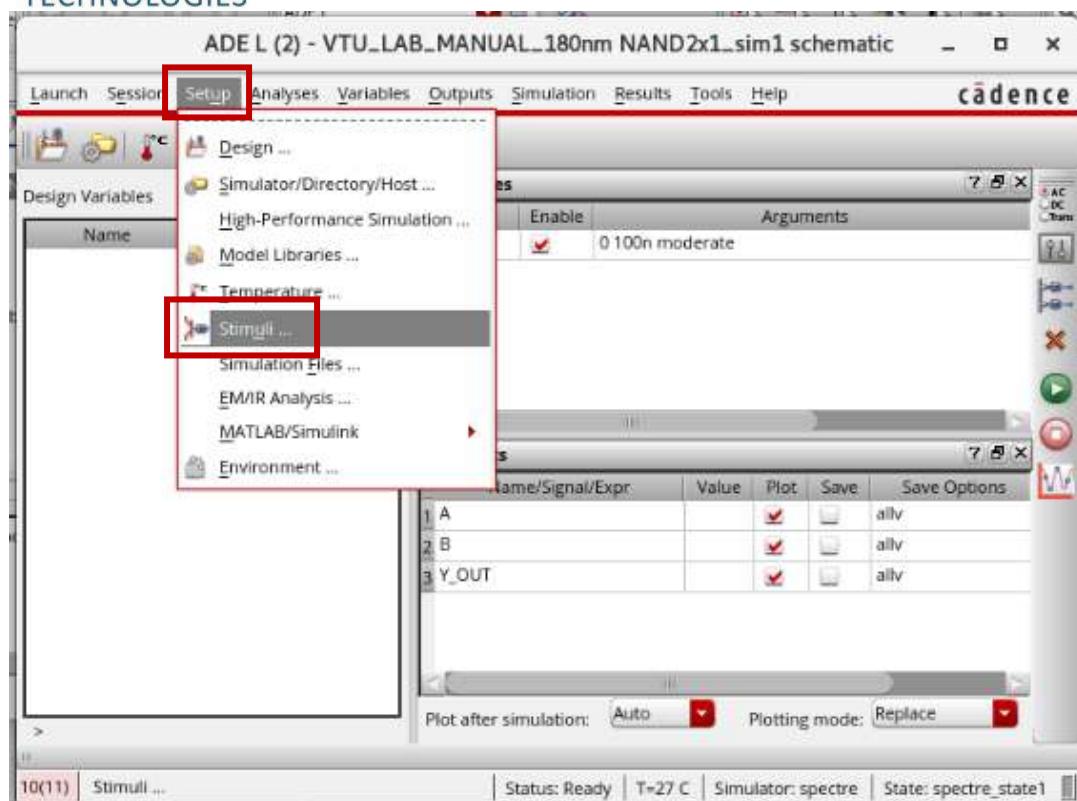


Figure – 2.6: Setup → Stimuli

The “Setup Analog Stimuli” window pops up as shown in Figure – 2.7.

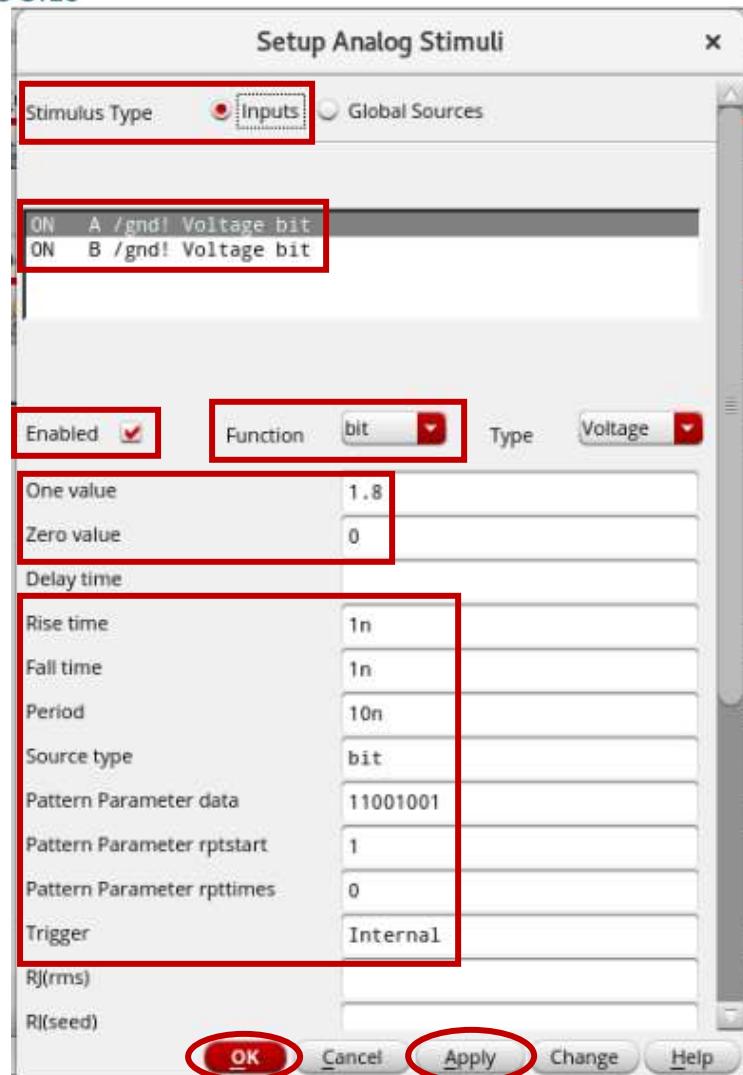


Figure – 2.7: Setup Analog Stimuli window

Select “**Stimulus Type → Inputs**” and the input pins A and B get listed out as shown in Figure – 2.7. Select any one of the Inputs, click on “**Enabled**” and select “**Function → bit**”.

Mention the value of voltages for “**Logic 0**” and “**Logic 1**” in “**One value → 1.8**” and “**Zero value → 0**”.

Consider the values of Rise time, Fall time and Period similar to that considered in Lab – 01. Select “**Source type → bit**”, “**Pattern Parameter data → 11001001**”, “**Pattern Parameter rptstart → 1**”, “**Pattern Parameter rpttimes → 0**” and “**Trigger → Internal**”, click on “**Apply**” to “**Turn ON**” the input and click on “**OK**”.

Select the type of Analysis to be performed on the 2 – input CMOS NAND Gate.

Select the Input and Output Signals to be plotted.

The ADE L window gets updated as shown in Figure – 2.8.

Run the Simulation to check for the functionality of the NAND Gate.

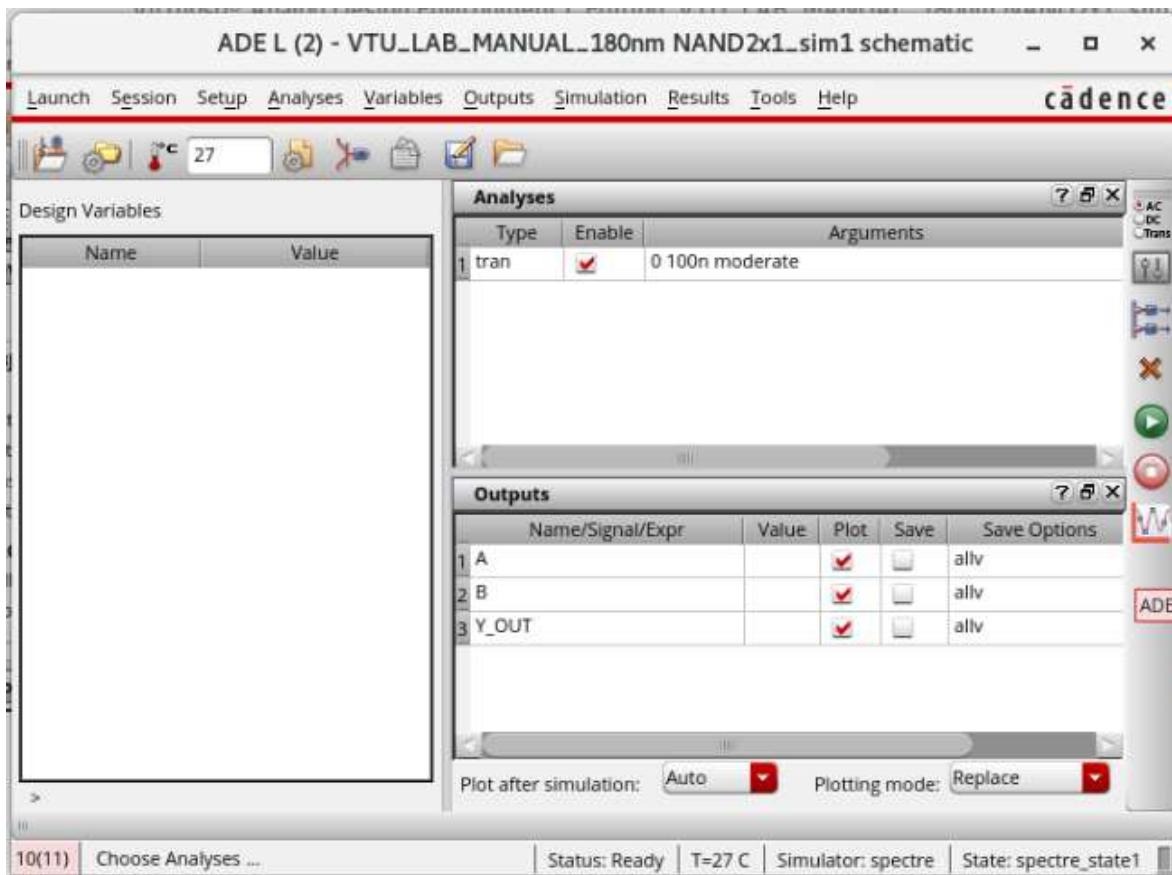


Figure – 2.8: Updated ADE L window

The Simulated waveforms can be seen as shown in Figure – 2.9.

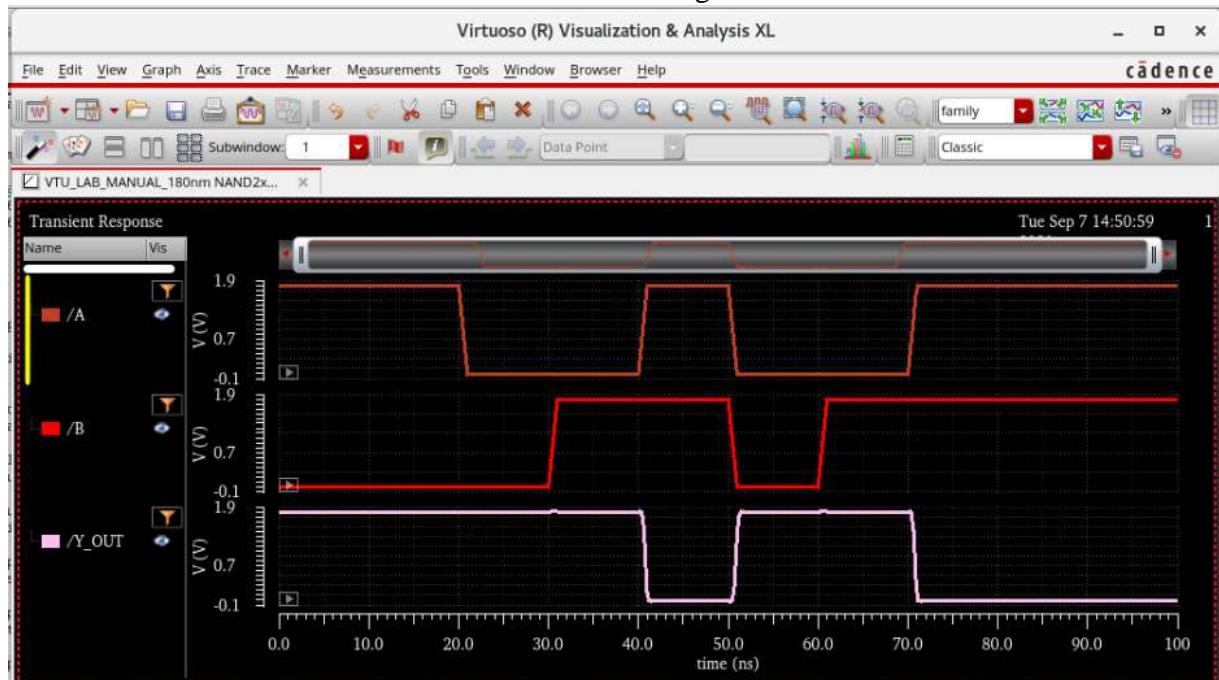


Figure – 2.9: Transient Analysis of 2 – input CMOS NAND Gate

The delay values are obtained using the “**Calculator**” option as demonstrated in Lab – 01. The results are tabulated as shown in Table – 12.

Table – 12: Values of Delay for 2 – input CMOS NAND2X1, NAND2X2 and NAND 2X4

| NAND Type | MOSFET | Length | Width | tpLH | tpHL | tpd |
|----------------|--------|--------|------------------------|-----------|-----------|-----------|
| NAND2X1 | PMOS | 180n | 1.5 * 850n = 1.275u | 3.720E-10 | 3.340E-10 | 3.530E-10 |
| | NMOS | | 2 * 850n = 1.7u | | | |
| NAND2X2 | PMOS | 180n | 1.5 * 850n * 2 = 2.55u | 2.610E-10 | 2.200E-10 | 2.400E-10 |
| | NMOS | | 2 * 850n * 2 = 3.4u | | | |
| NAND2X4 | PMOS | 180n | 1.5 * 850n * 4 = 5.1u | 1.900E-10 | 1.650E-10 | 1.780E-10 |
| | NMOS | | 2 * 850n * 4 = 6.8u | | | |

Solution – (b):
SCHEMATIC CAPTURE:

Following the techniques demonstrated in Lab – 01, Create a New Library, a New Cell View and instantiate the devices as per the Schematic of 2 – input CMOS NAND Gate.

The device parameters for the NMOS and PMOS Transistors are listed in Table – 13.

Table – 13: Device parameters for 2 – input CMOS NAND Gate with $\frac{W_P}{W_N} = \frac{40}{20}$

| Library Name | Cell Name | Comments / Properties |
|--------------|-----------|--|
| gdk180 | Nmos | Width, $W_N = 20 \mu$ Length, $L = 180 n$ |
| gdk180 | Pmos | Width, $W_P = 40 \mu$ Length, $L = 180 n$ |

The Schematic as per the dimensions of NMOS and PMOS transistors listed above is shown in Figure – 2.10.

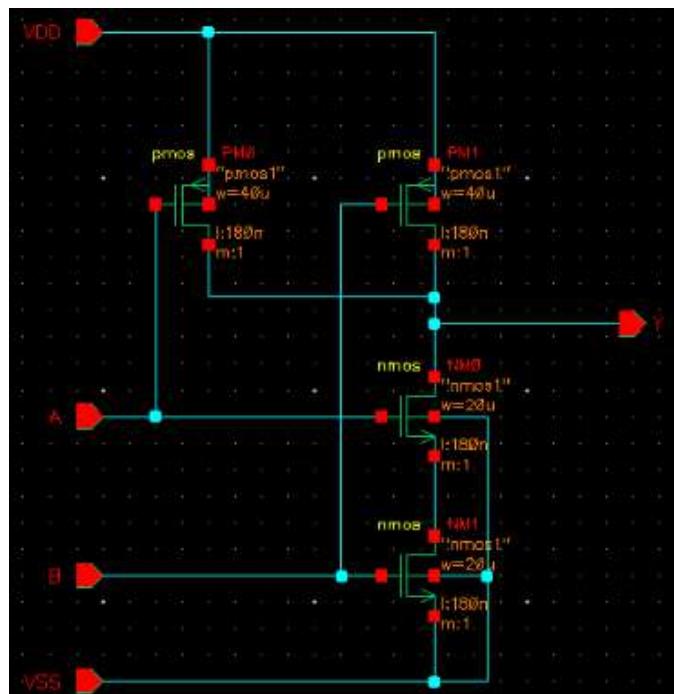


Figure – 2.10: Schematic for 2 – input CMOS NAND with $\frac{W_P}{W_N} = \frac{40}{20}$

Symbol for the Schematic in Figure – 2.10 is shown in Figure – 2.11.

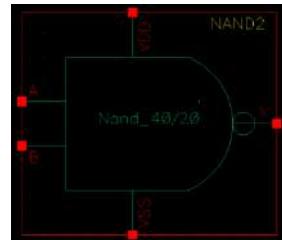


Figure – 2.11: Symbol for 2 – input CMOS NAND with $\frac{W_P}{W_N} = \frac{40}{20}$

FUNCTIONAL SIMULATION:

The Test Schematic for the functionality check of the 2 – input CMOS NAND Gate is shown in Figure – 2.12.

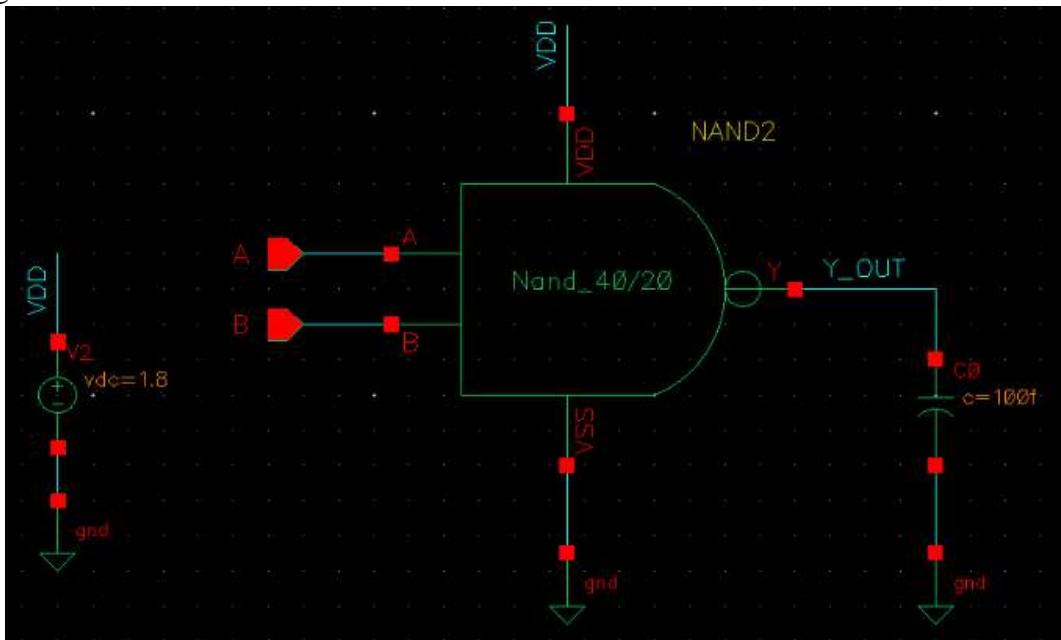


Figure – 2.12: Test Schematic for 2 – input CMOS NAND with $\frac{W_P}{W_N} = \frac{40}{20}$

The ADE L window after choosing the Analysis and the Signals to be plotted is shown in Figure – 2.13.

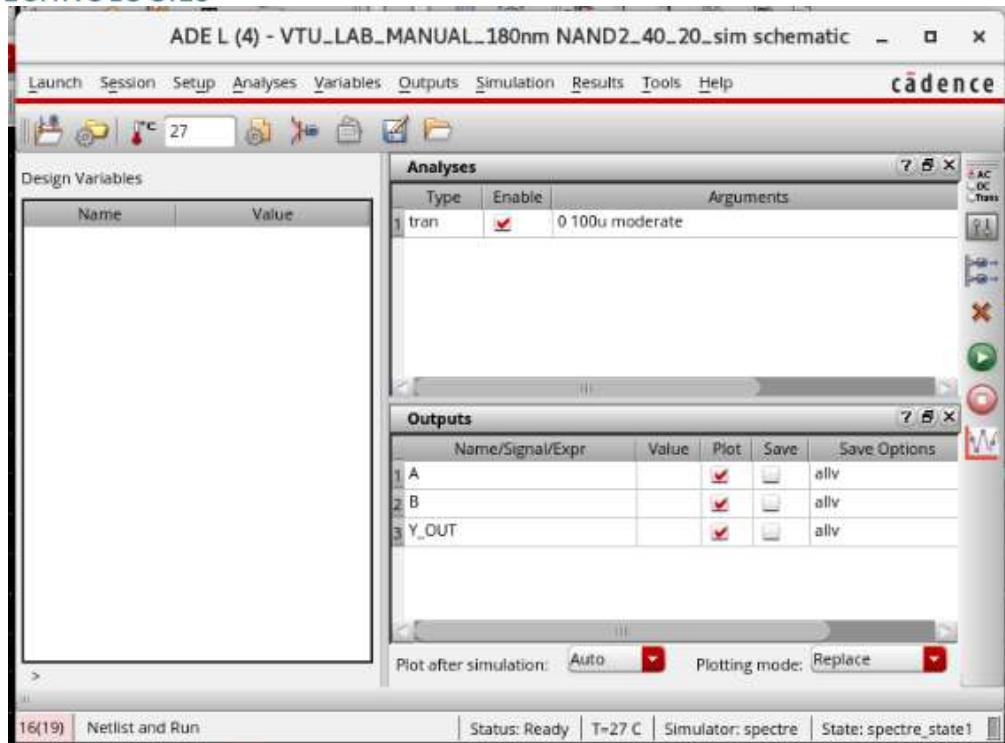


Figure – 2.13: Updated ADE L window

The waveforms after simulation is shown in Figure – 2.14.



Figure – 2.14: Simulated Waveforms for 2 – input CMOS NAND with $\frac{W_P}{W_N} = \frac{40}{20}$

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The values of delay elements are tabulated in Table – 14.

Table – 14: Delay Elements for 2 – input CMOS NAND Gate with $\frac{W_P}{W_N} = \frac{40}{20}$ (Pre Layout Simulation)

| MOSFET | Length | Width | tpLH | tpHL | tpd |
|--------|--------|-------|----------|----------|----------|
| PMOS | 180n | 40u | 3.64E-11 | 1.55E-10 | 9.57E-11 |
| NMOS | 180n | 20u | | | |

LAYOUT:

Follow the techniques demonstrated in Lab – 01 to open the Layout Editor, import the devices from the Schematic, place the devices as per the requirement and complete the routing. The completed layout can be seen as shown in Figure – 2.15.

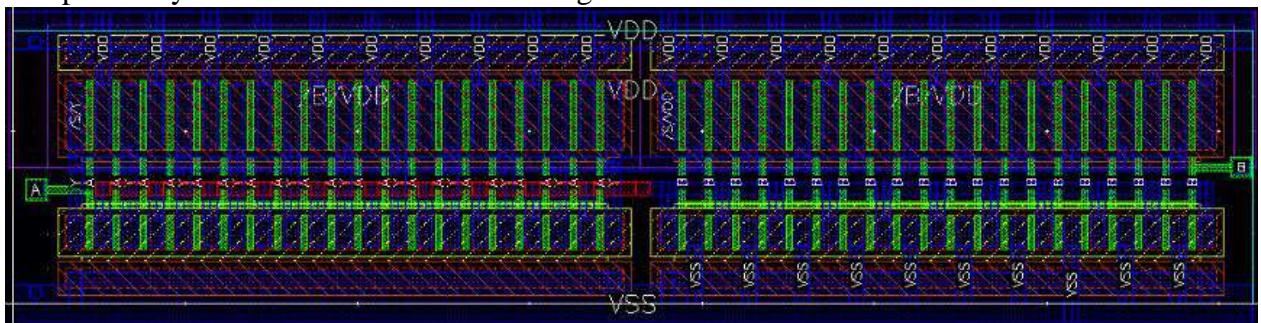


Figure – 2.15: Layout for 2 – input CMOS NAND Gate with $\frac{W_P}{W_N} = \frac{40}{20}$

DRC:

To check for the DRC violations, browse the “assura_tech.lib” file, select “Assura → Run DRC”, verify the Layout Design Source, mention a “Run Name”, select “Technology → gpdk180” and click on “OK” as demonstrated in Lab – 01.

LVS:

To check for the LVS violations, select “**Assura → Run LVS**”, verify the Schematic Design Source and the Layout Design Source, mention a “**Run Name**”, select “**Technology → gpdk180**” and click on “**OK**” as demonstrated in Lab – 01.

QRC:

To extract the Parasitics, select “**Assura → Quantus**”, select “**Technology → gpdk180**”, “**Output → Extracted View**” from the “**Setup**” option, select “**Extraction Type → RC**” and “**Ref Node → VSS**” from the “**Extraction**” and click on “**OK**” as demonstrated in Lab – 01.

The result can be checked from the Library Manager.

BACKANNOTATION:

Import the parasitics into the Test Schematic and re-run the simulation to check their impact by calculating the delay elements as demonstrated in Lab – 01.

The values of delay are shown in Table – 15.

Table – 15: Delay Elements for 2 – input CMOS NAND Gate with $\frac{W_P}{W_N} = \frac{40}{20}$ (Post Layout Simulation)

| MOSFET | Length | Width | tpLH | tpHL | tpd |
|--------|--------|-------|----------|----------|----------|
| PMOS | 180n | 40u | | | |
| NMOS | 180n | 20u | 3.64E-11 | 1.55E-10 | 9.57E-11 |

LAB – 03: COMMON SOURCE AMPLIFIER WITH PMOS CURRENT MIRROR LOAD

Objective:

- (a) Capture the Schematic of a Common Source Amplifier with PMOS Current Mirror Load and find its Transient Response and AC Response. Measure the UGB and Amplification Factor by varying transistor geometries, study the impact of variation in width to UGB.
- (b) Draw the layout of Common Source Amplifier, use optimum layout methods. Verify DRC and LVS, extract the parasitics and perform the post layout simulation, compare the results with pre layout simulations. Record the observations.

Solution – (a):

SCHEMATIC CAPTURE:

Following the techniques demonstrated in Lab – 01, Create a New Library using the option “File → New → Library”, create a New Cell View upon selecting the newly created library using the option “File → New → Cell View” and instantiate the required devices using the “Create → Instance” option.

The device parameters are listed in Table – 16.

Table – 16: Width and Length of NMOS and PMOS Transistors

| Library Name | Cell Name | Comments / Properties |
|--------------|-----------|--|
| gdk180 | Nmos | Width, $W_N = 6 \mu$ Length, $L = 180 n$ |
| gdk180 | Pmos | Width, $W_P = 8.85 \mu$ Length, $L = 180 n$ |

The completed Schematic is shown in Figure – 3.1.

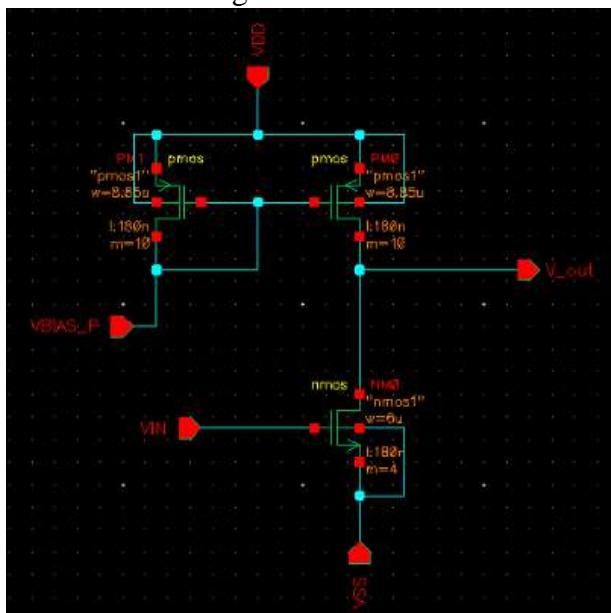


Figure – 3.1: Schematic of Common Source Amplifier with PMOS Current Mirror Load

The symbol for the Common Source Amplifier with PMOS Current Mirror Load is shown in Figure – 3.2.

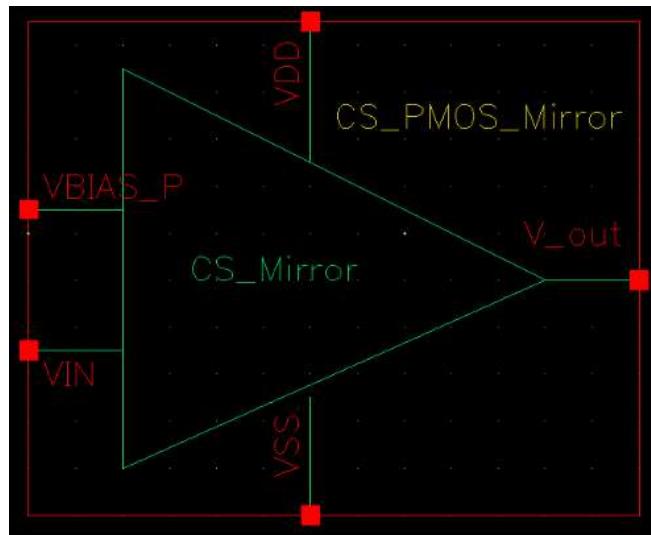


Figure – 3.2: Symbol of Common Source Amplifier with PMOS Current Mirror Load

FUNCTIONAL SIMULATION:

Using the symbol created, build the Test Schematic. Create a New Cell View, instantiate the symbol of Common Source Amplifier with PMOS Current Mirror Load, DC Voltage Source, Current Source, AC Voltage Source, Capacitance, Resistance and Ground, connect the using wires.

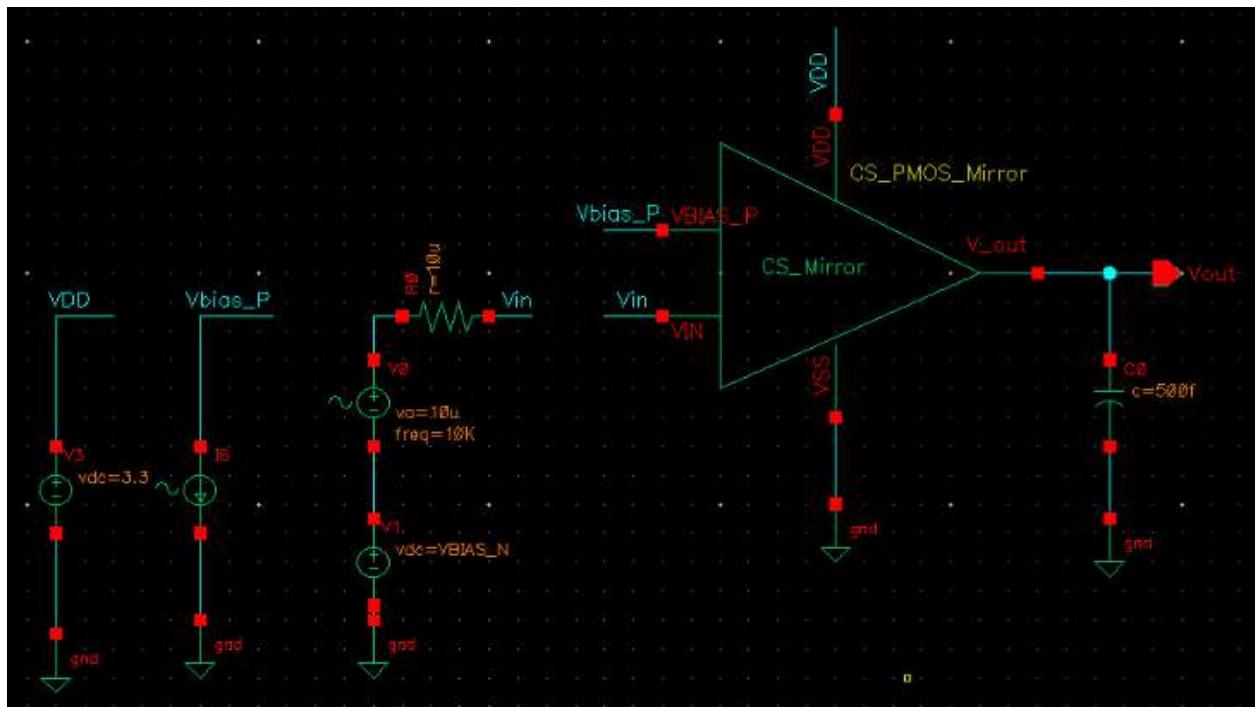


Figure – 3.3: Test Schematic for 2 – input CMOS NAND Gate

The parameters for remaining devices are shown in Table – 17.

| Library Name | Cell Name | Comments / Properties |
|--------------|-----------|---|
| analogLib | vdc | DC voltage = 3.3 V (VDD) |
| analogLib | vdc | DC voltage = VBIAS_N V (Vin) |
| analogLib | isin | DC current = 100u A (Vbias_P) |
| analogLib | vsin | AC Magnitude = 1 V, Amplitude = 10u V, Frequency = 10K Hz (Vin) |
| analogLib | cap | Capacitance = 500f F |
| analogLib | res | Resistance = 10u Ohms |
| analogLib | gnd | |

Table – 17: Parameters for the devices used in Test Schematic

Launch ADE L, import the design variables, mention the values and select the Transient Analysis, DC Analysis and AC Analysis, mention the parameters and choose the signals to be plotted as shown in Figure – 3.4.

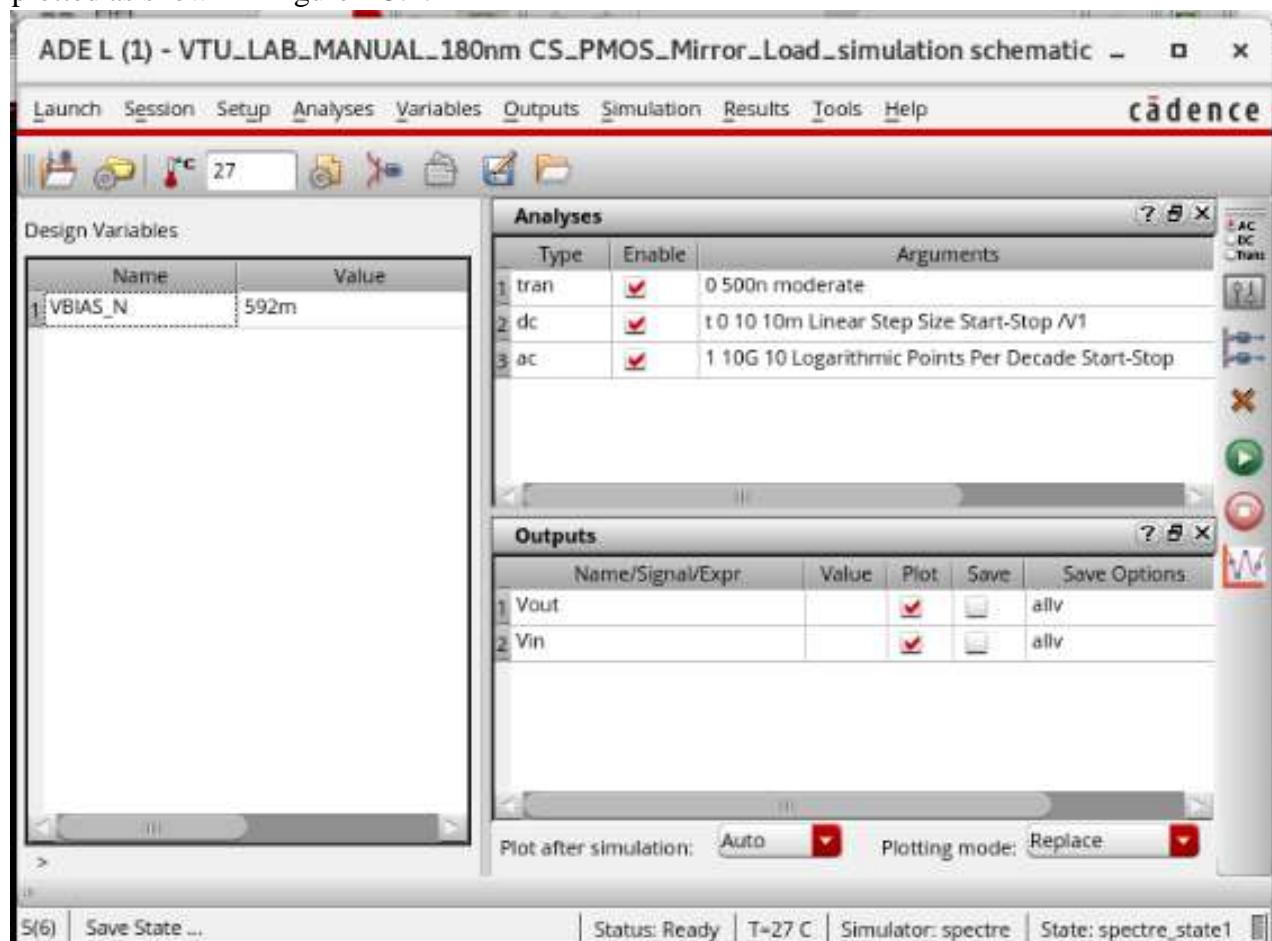


Figure – 3.4: Updated ADE L window

The Simulated waveforms can be seen as shown in Figure – 3.5 and Figure – 3.6.

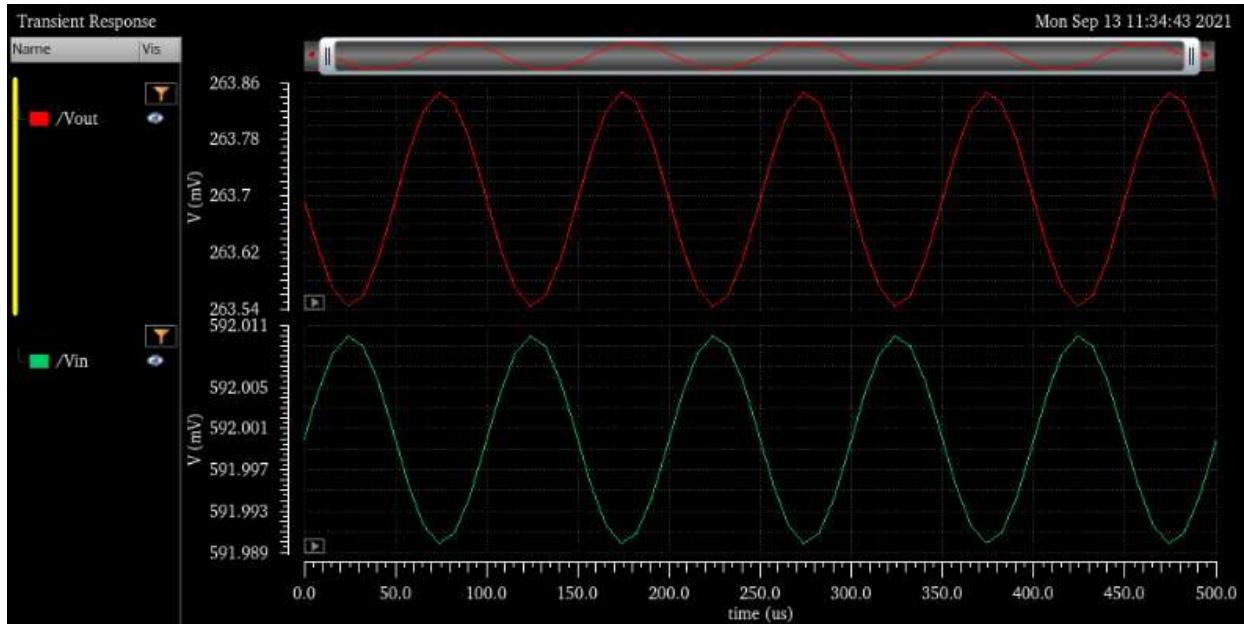


Figure – 3.5: Transient Analysis

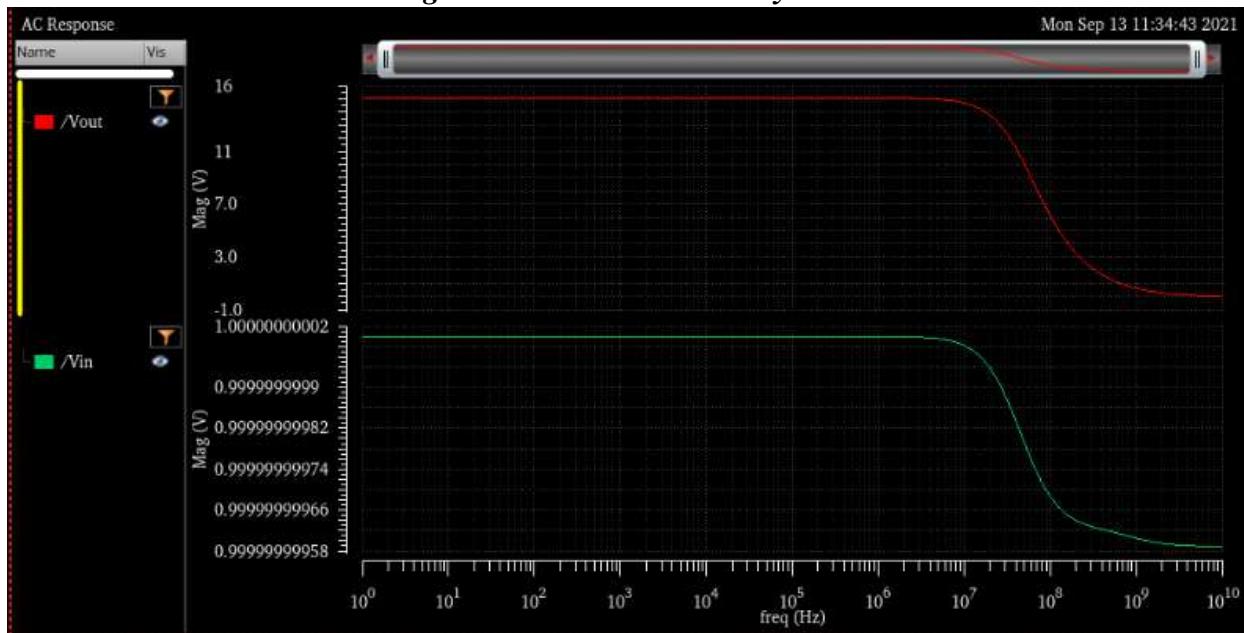


Figure – 3.6: AC Analysis

To measure the Gain and Unity Gain Bandwidth, go back to the ADE L window, select “Results → Direct Plot → AC Magnitude & Phase” as shown in Figure – 3.7.

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The Test Schematic window pops up, select the output net as shown in Figure – 3.8 and click on “Esc” key on the keyboard.

The waveform can be seen as shown in Figure – 3.9. The marker placed on the low frequency part of the response gives the DC Gain, use the bind key “M” to place the marker.

Place a horizontal cursor at “0 dB” and the crossing frequency gives the Unity Gain Bandwidth (UGB) as shown in Figure 3.9.

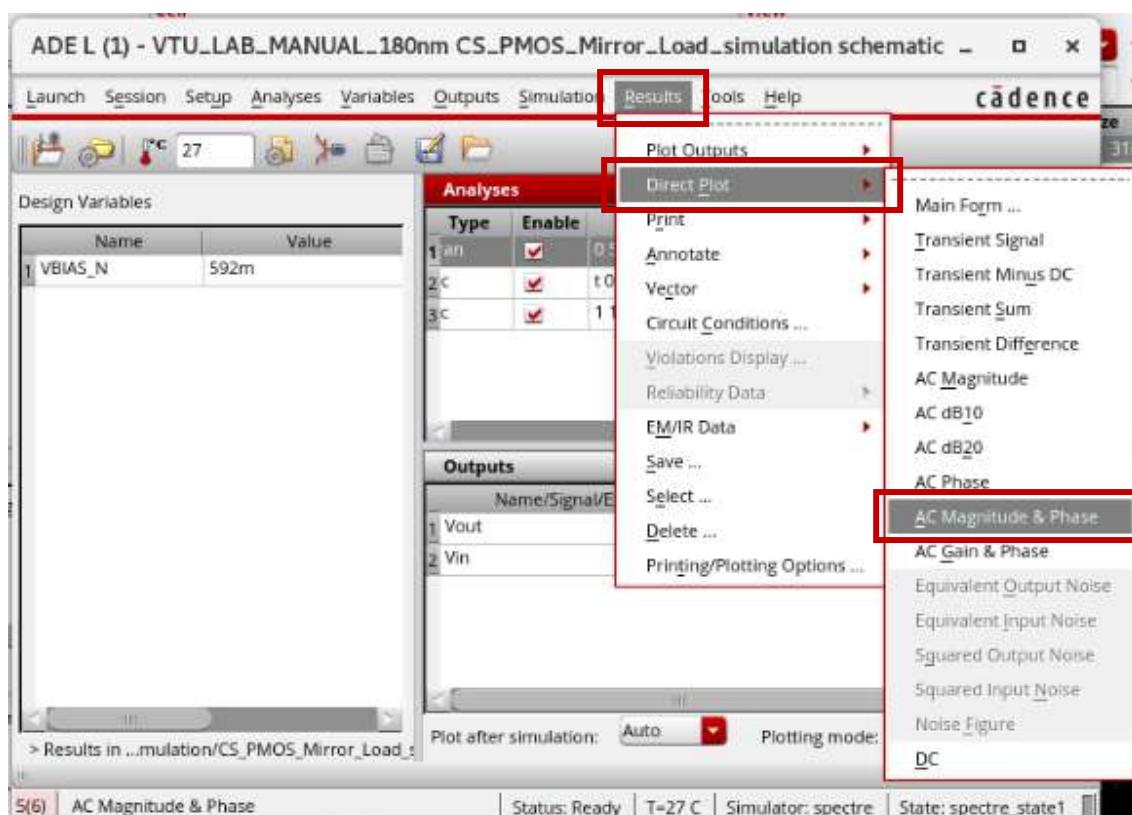


Figure – 3.7: Results → Direct Plot → AC Magnitude & Phase

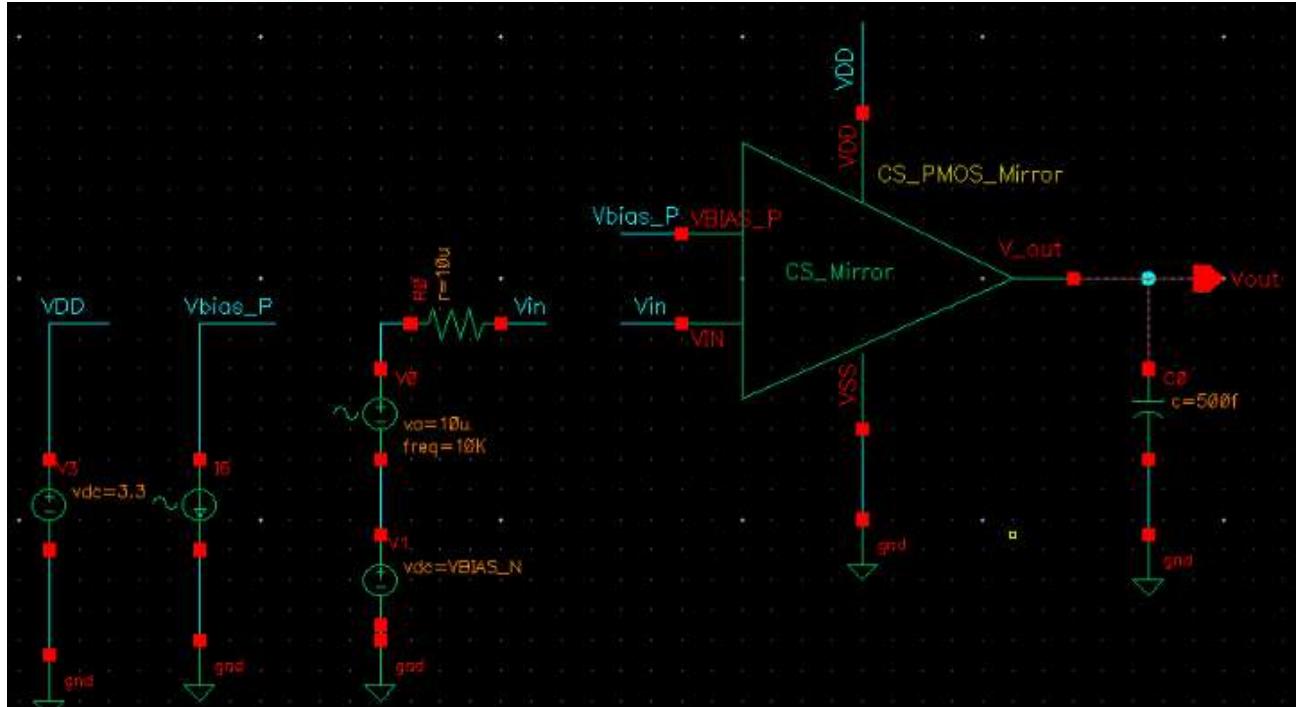


Figure – 3.8: Selecting Output Net from the Test Schematic

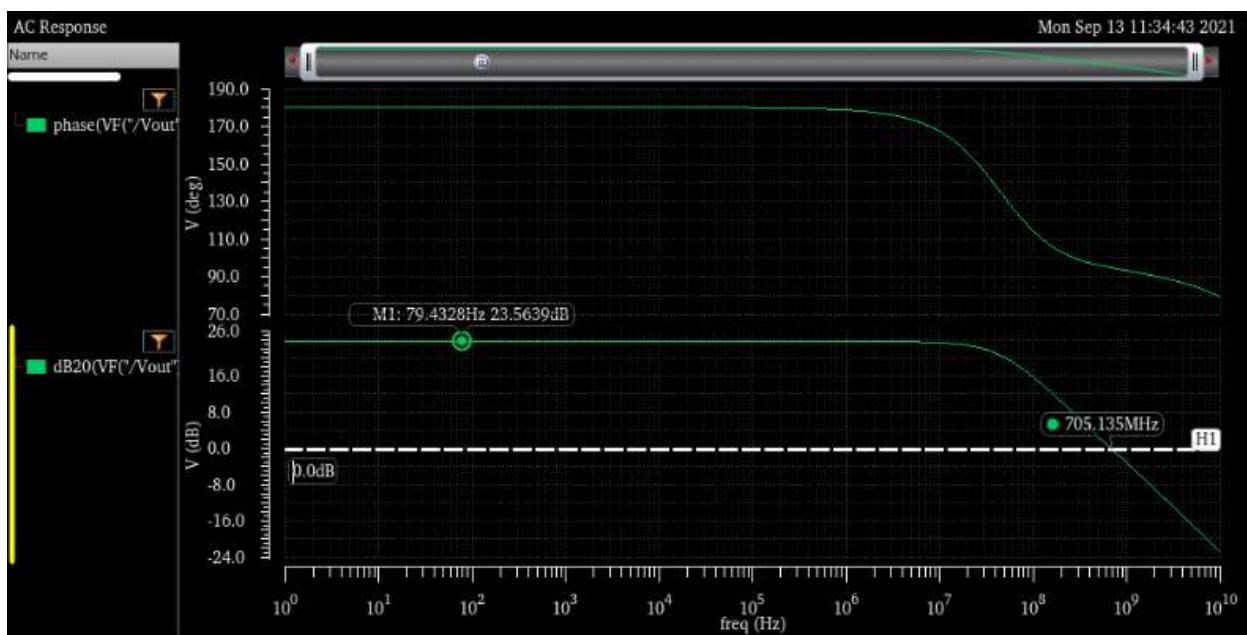


Figure – 3.9: Gain and Phase plot

Solution – (b):

LAYOUT:

Follow the techniques demonstrated in Lab – 01 to open the Layout Editor, import the devices from the Schematic, place the devices as per the requirement and complete the routing. The completed layout can be seen as shown in Figure – 3.10.



Figure – 3.10: Layout for Common Source Amplifier with PMOS Current Mirror Load

DRC:

To check for the DRC violations, browse the “assura_tech.lib” file, select “Assura → Run DRC”, verify the Layout Design Source, mention a “Run Name”, select “Technology → gpd़k180” and click on “OK” as demonstrated in Lab – 01.

LVS:

To check for the LVS violations, select “Assura → Run LVS”, verify the Schematic Design Source and the Layout Design Source, mention a “Run Name”, select “Technology → gpd़k180” and click on “OK” as demonstrated in Lab – 01.

QRC:

To extract the Parasitics, select “Assura → Quantus”, select “Technology → gpd़k180”, “Output → Extracted View” from the “Setup” option, select “Extraction Type → RC” and “Ref Node → VSS” from the “Extraction” and click on “OK” as demonstrated in Lab – 01.

The result can be checked from the Library Manager.

BACKANNOTATION:

Import the parasitics into the Test Schematic and re-run the simulation to check their impact by calculating the delay elements as demonstrated in Lab – 01.

LAB – 04: 2 – STAGE OPERATIONAL AMPLIFIER

Objective:

- (a) Capture the Schematic of a 2 – Stage Operational Amplifier and measure the following:
1. UGB
 2. dB Bandwidth
 3. Gain Margin and Phase Margin with and without coupling capacitance
 4. Use the Op-Amp in the Inverting and Non-Inverting configuration and verify its functionality
 5. Study the UGB, 3 dB Bandwidth, Gain and Power Requirement in Op-Amp by varying the stage wise transistor geometries and record the observations
- (b) Draw the layout of 2 – stage Operational Amplifier with the maximum transistor width set to 300 (in 180 / 90/ 45n m Technology), choose appropriate transistor geometries as per the results obtained in 4(a). Use optimum layout methods. Verify DRC and LVS, extract the parasitics and perform the post layout simulation, compare the results with pre layout simulations. Record the observations.

Solution – (a):

SCHEMATIC CAPTURE:

Create a New Library, select the Technology Node as “**gpdk045**” (Technology Node used for this demonstration is 45 nm), Create a New Cell View, instantiate the devices as demonstrated in Lab – 01. Use the “**Sideways**” option as shown in Figure – 4.1 to flip the Transistor.

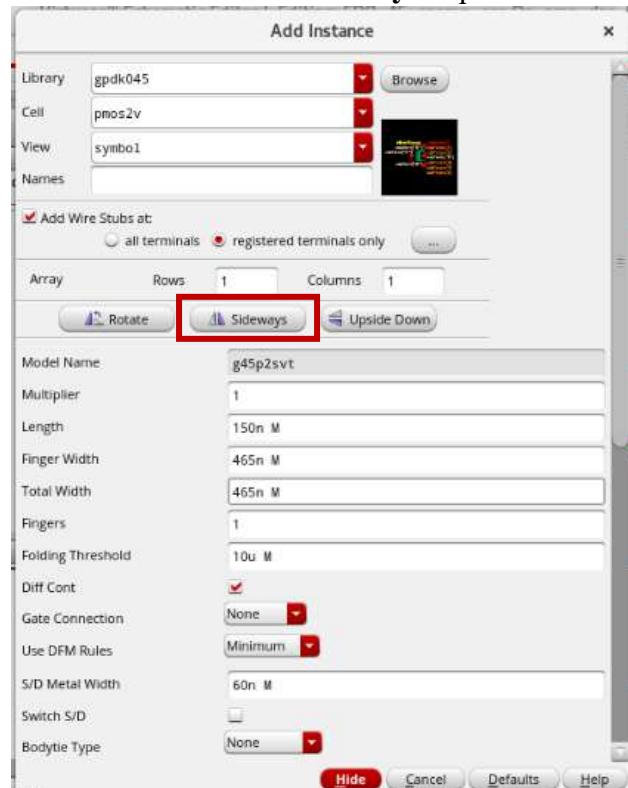


Figure – 4.1: “Sideways” option to flip the Transistors



Figure – 4.1(a): Before
Figure – 4.1(b): After selecting “Sideways”

The Transistors before and after flipping are shown in Figure – 4.1(a) and Figure – 4.1(b). The dimensions of all the devices are given in Table – 18 as shown below.

Table – 18: Device Parameters for 2 – Stage Operational Amplifier

| Library Name | Transistor | Cell Name | Comments / Properties |
|--------------|------------|-----------|--|
| gdk045 | M0, M1 | pmos2v | Width, W = 465 n Length, L = 150 n |
| gdk045 | M3, M4 | nmos2v | Width, W = 490 n Length, L = 150 n |
| gdk045 | M5, M7 | nmos2v | Width, W = 1.09 u Length, L = 150 n |
| gdk045 | M2 | pmos2v | Width, W = 10 u Length, L = 150 n |
| gdk045 | M6 | nmos2v | Width, W = 6.88 u Length, L = 150 n |
| gdk045 | M8 | pmoscap2v | Calculated Parameter = Capacitance Capacitance = 250.043 f |

The completed Schematic as per the dimensions mentioned in Table – 18 is shown in Figure – 4.2.

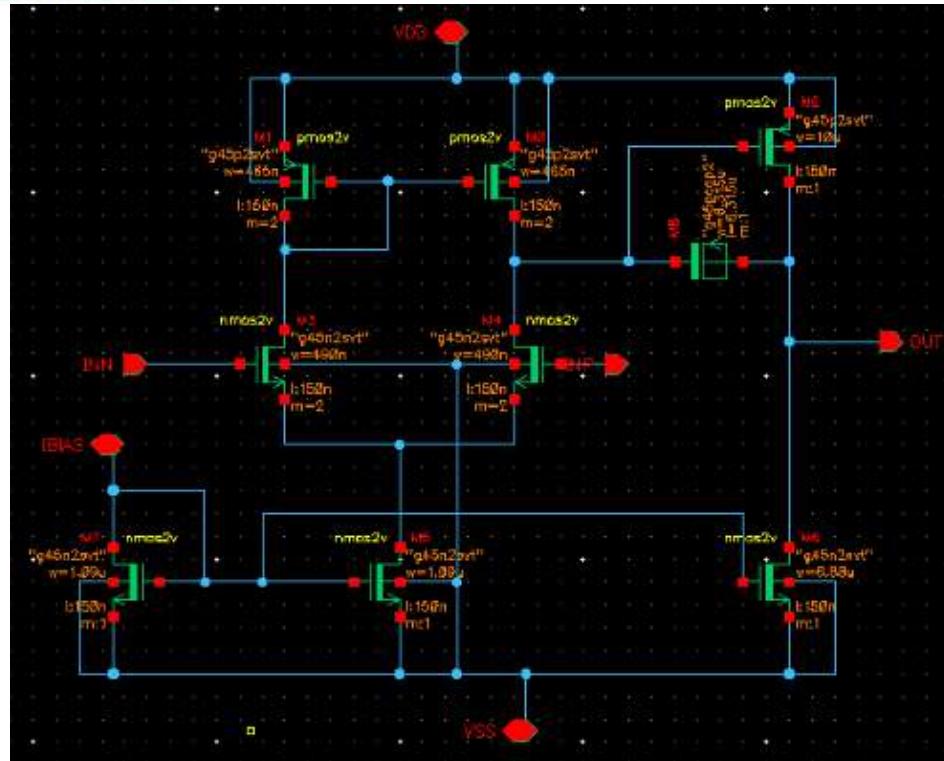


Figure – 4.2: Schematic of 2 – Stage Operational Amplifier

The Symbol created according to the Techniques demonstrated in Lab – 01 is shown in Figure – 4.3.

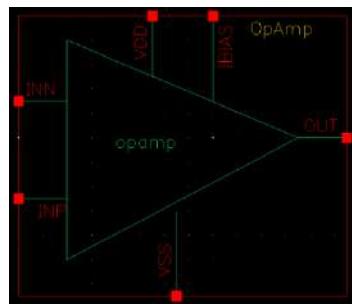


Figure – 4.3: Symbol for 2 – Stage Operational Amplifier

FUNCTIONAL SIMULATION USING ADE EXPLORER AND ASSEMBLER:

To test the functionality of Operational Amplifier, build a Test Schematic using the Symbol that was created as shown in Figure – 4.3. Create a New Cell View, instantiate the symbol. Instantiate the other devices required for testing the circuit, mention the device parameters as shown in Table – 19.

Table – 19: Device Parameters for 2 – Stage Operational Amplifier Test Schematic

| Library Name | Cell Name | Comments / Properties |
|--------------|-----------|-----------------------|
| analogLib | vdc | DC voltage = vdd V |
| analogLib | vdc | DC voltage = vss V |

| | | |
|-----------|--------|--|
| analogLib | vpulse | Voltage 1 = vdc + 0.3 V, Voltage 2 = vdc - 0.3 V, Period = 10u s, Rise time = 10p s, Fall time = 10p s |
| analogLib | idc | DC current = ibias A |
| analogLib | cap | Capacitance = CL F |
| analogLib | gnd | |

The Test Schematic after completion of all the interconnections can be seen as shown in Figure – 4.4.

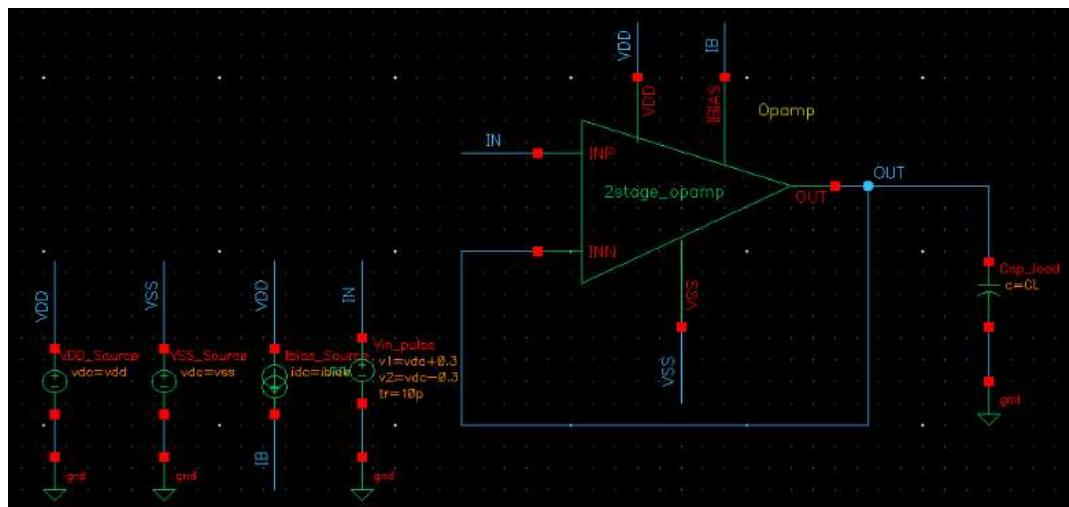


Figure – 4.4: Test Schematic for 2 – Stage Operational Amplifier

The specification that has to be achieved on simulating the design are as follows:

- Slew Rate $\geq 50 \text{ MV/s}$
- DC Open Loop Gain $\geq 60 \text{ dB} (1000 \text{ V/V})$
- Unity Gain Bandwidth $\geq 50 \text{ MHz}$
- Output Offset $\leq \pm 10 \text{ mV}$
- Settling Time $\leq 50 \text{ ns}$

The steps to be carried out are listed below:

Step – 1:

Select “Launch → ADE Explorer” as shown in Figure – 4.5.

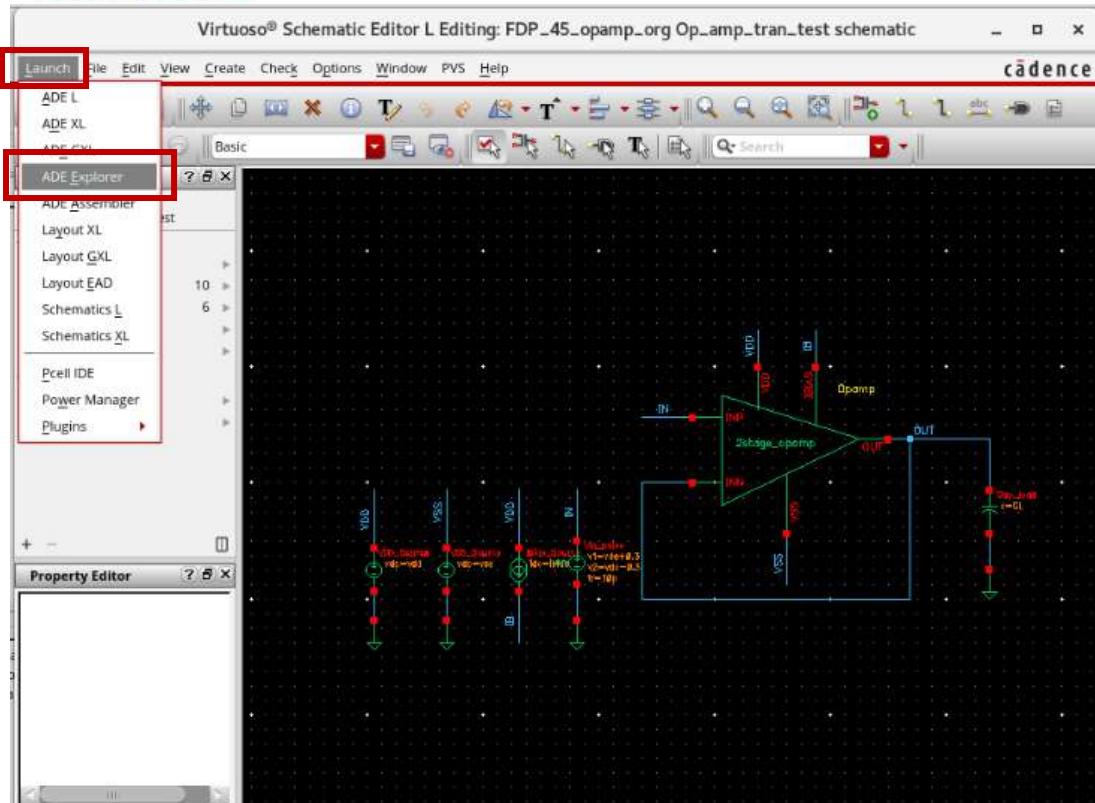


Figure – 4.5: **Launch → ADE Explorer**

The “Launch ADE Explorer” window pops up, select “Create New View” and click on “OK” as shown in Figure – 4.6.

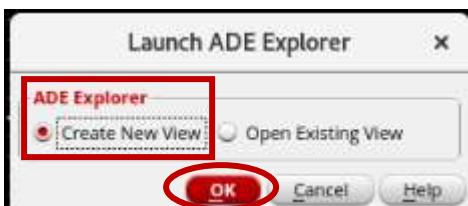


Figure – 4.6: “**Launch ADE Explorer**” window

The “Create new ADE Explorer view” window pops up as shown in Figure – 4.7. Select the Cell View Name, “Open in → new tab” and click on “OK”.

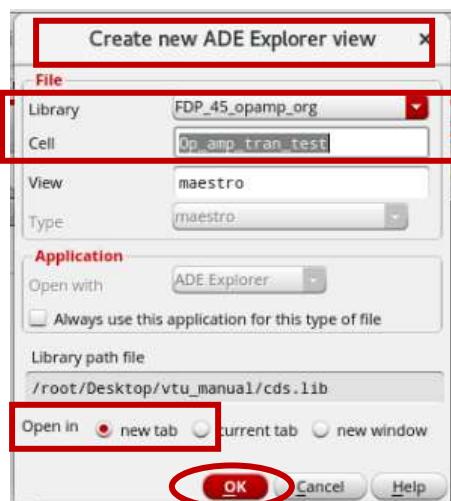


Figure – 4.7: “Create new ADE Explorer view” window

The “Virtuoso ADE Explorer Editing” window pops up as shown in Figure – 4.8.

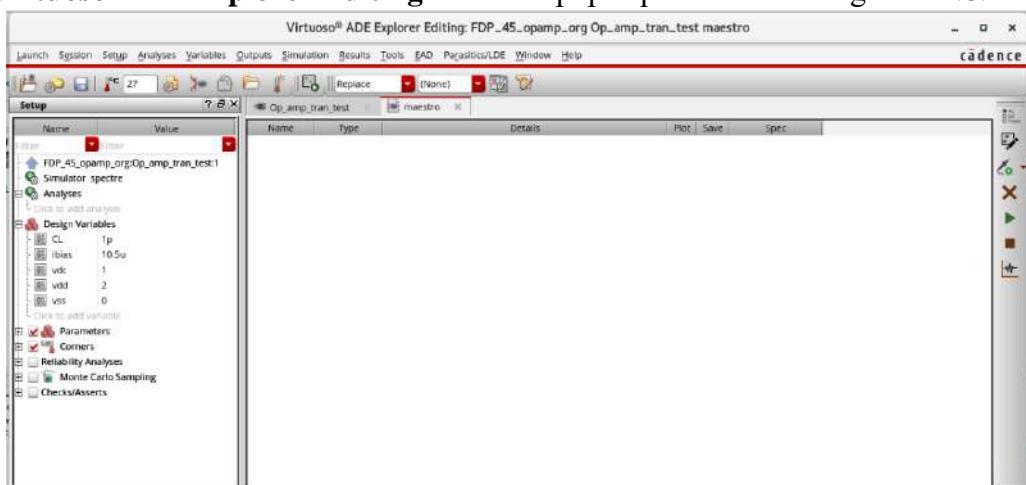


Figure – 4.8: “Virtuoso ADE Explorer Editing” window

Select “Setup → Model Libraries” as shown in Figure – 4.9.

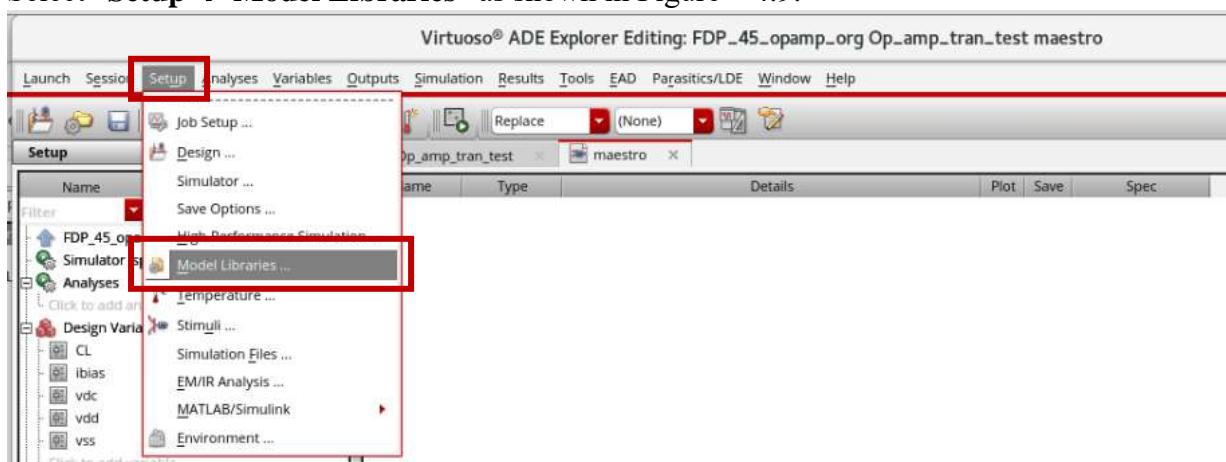


Figure – 4.9: Setup → Model Libraries

The “spectre1: Model Library Setup” window pops up as shown in Figure – 4.10. Select the respective “.scs” file and the process corner as “tt”. Click on “OK”

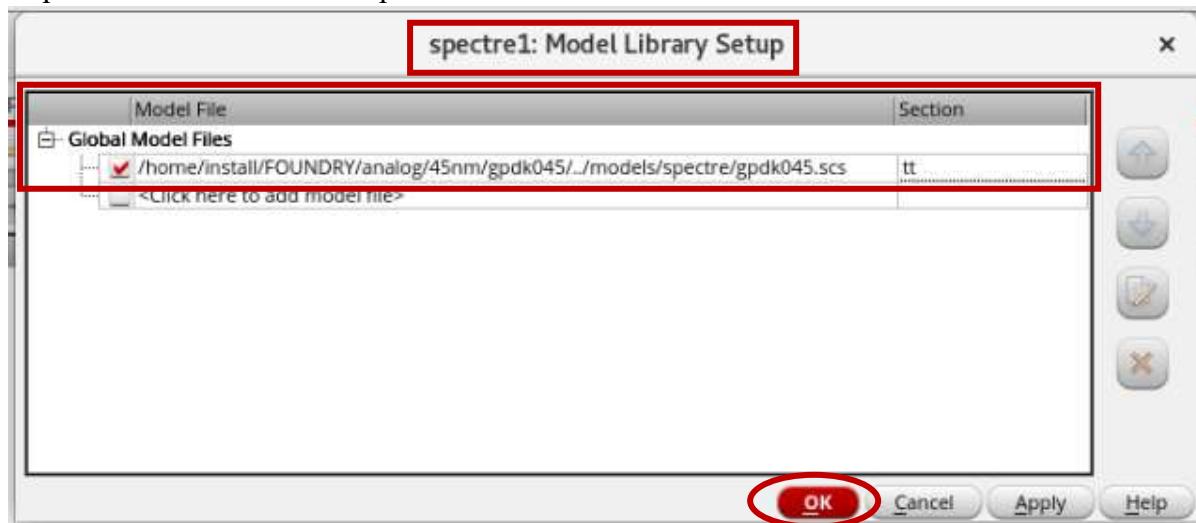


Figure – 4.10: “spectre1: Model Library Setup” window

To analyze the circuit through Transient Analysis and AC Analysis, select “Click to add analysis” just below the “Analyses” option in the “Setup” window as shown in Figure – 4.11.

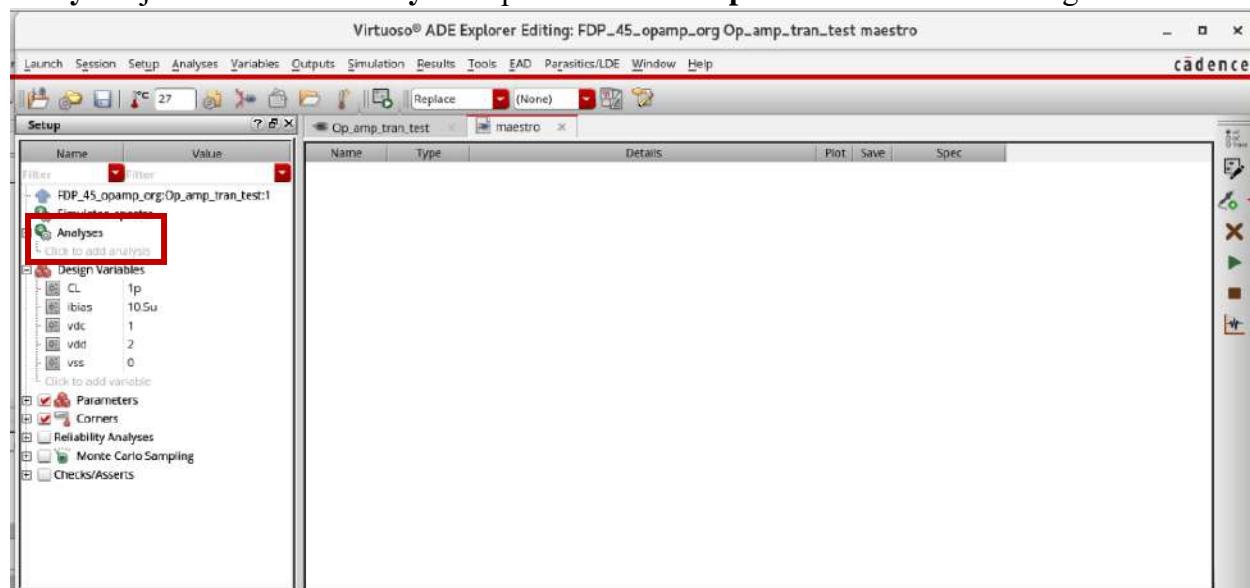


Figure – 4.11: Analyses → Click to add analysis

The “Choosing Analyses – ADE Explorer” window pops up as shown in Figure – 4.12. Select the “tran” for the “Transient Analysis” and “dc” for the “DC Analysis”.

The ADE Explorer window gets updated as shown in Figure – 4.13.

Mention the values for the Design Variables defined in the Schematic of the 2 – Stage Operational Amplifier.

The defined values for the respective Design Variables are given in Table – 20. The Design Variables along with the values in ADE Explorer window is shown in Figure – 4.13.

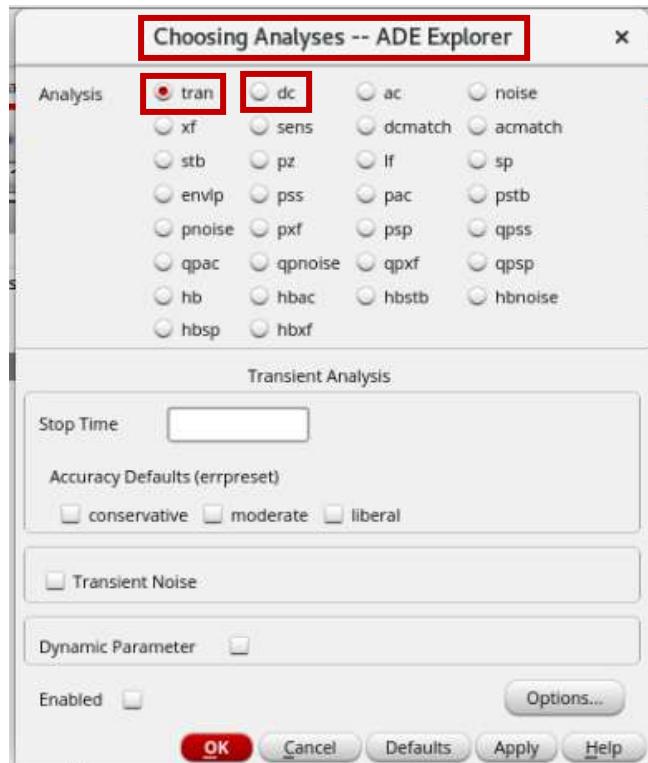


Figure – 4.12: “Choosing Analyses – ADE Explorer” window

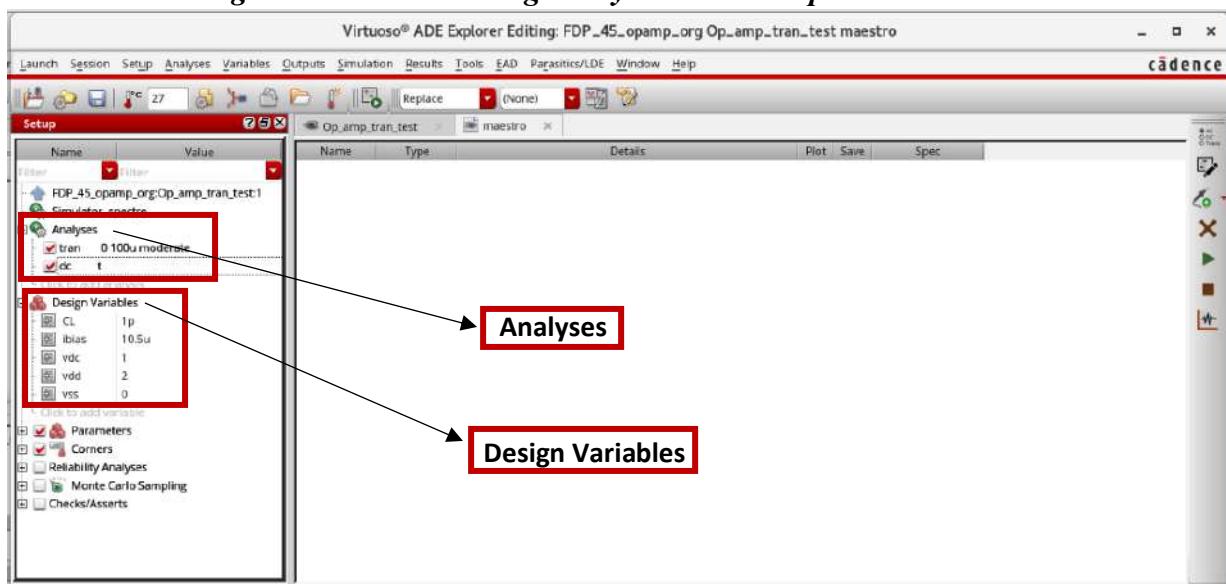


Figure – 4.13: Updated ADE Explorer

| Name of the Variable | Value |
|----------------------|-------|
| CL | 1p |

| | |
|-------|-----|
| ibias | 10u |
| vdc | 1 |
| vdd | 2 |
| vss | 0 |

Table – 20: Design Variables and its Values

To specify the outputs for the simulation, select “Tools → Calculator” as shown in Figure – 4.14.

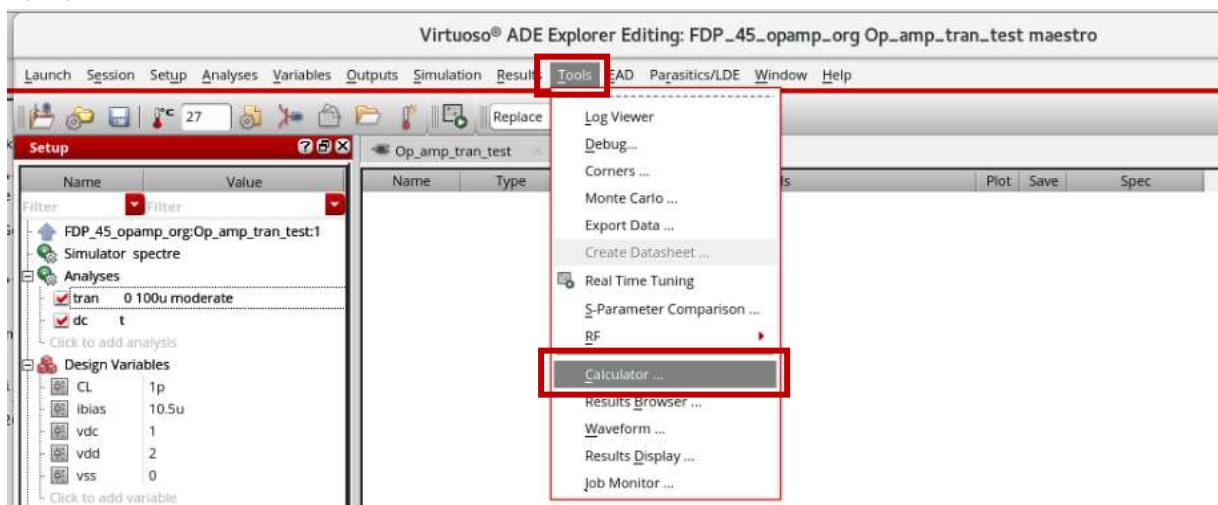


Figure – 4.14: Tools → Calculator

The “Virtuoso Visualization & Analysis XL calculator” window pops up as shown in Figure – 4.15.

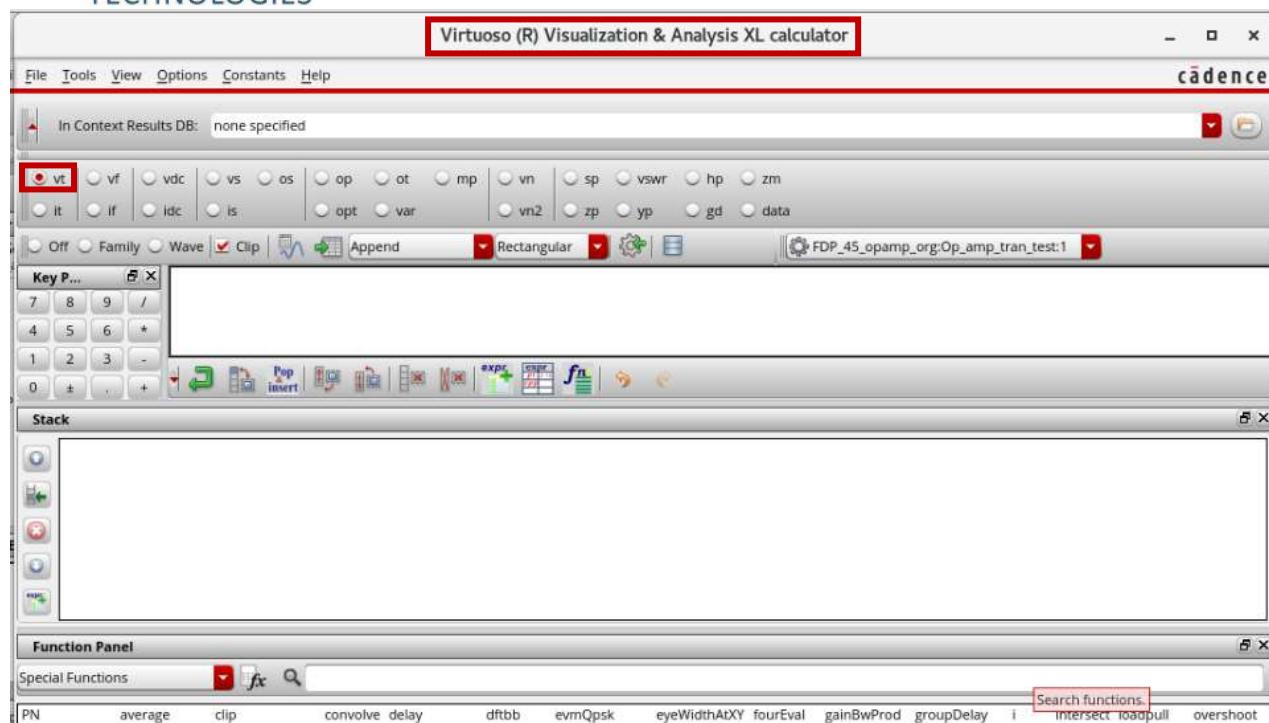


Figure – 4.15: “Virtuoso Visualization & Analysis XL calculator” window

Select “vt” as shown in Figure – 4.15. The Test Schematic pops up as shown in Figure – 4.16. Select the output net “OUT” from the Schematic and the Buffer window in the Calculator gets updated as shown in Figure – 4.17.

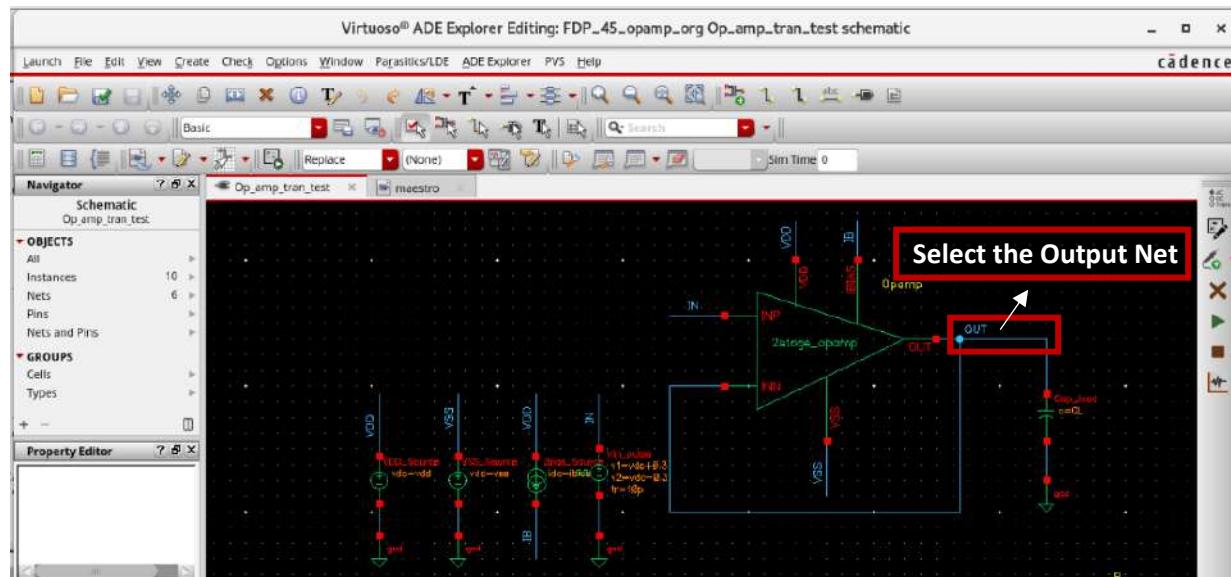


Figure – 4.16: Test Schematic

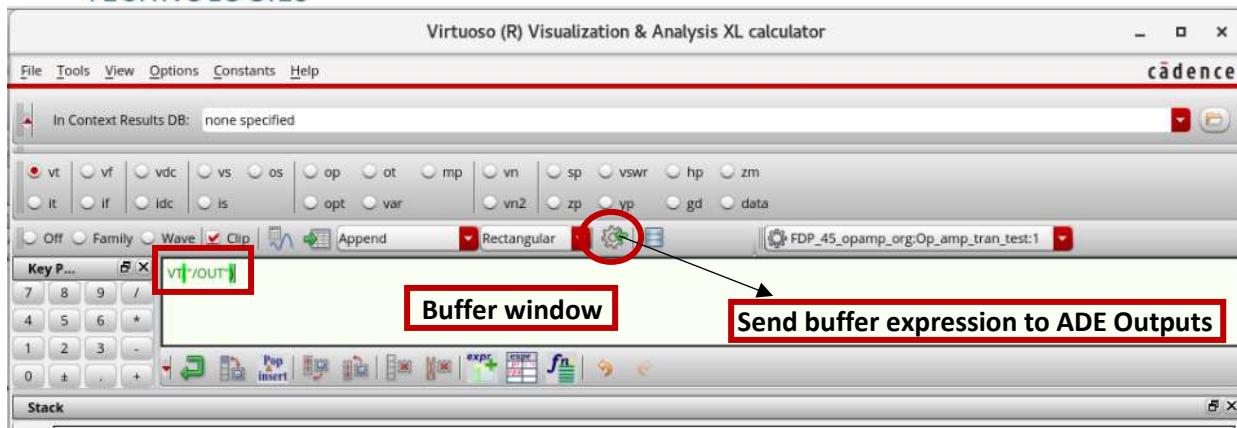


Figure – 4.17: Updated Buffer window

Click on “Send buffer expression to ADE Outputs” option to get the expression from the Buffer window into ADE Explorer as shown in Figure – 4.18.

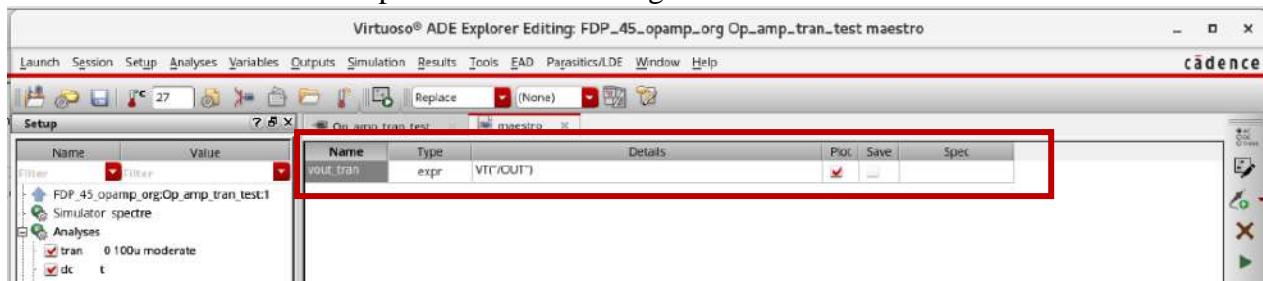


Figure – 4.18: Updated ADE Explorer

Initially, the “Name” column would be blank, use the left mouse click to rename (for eg: vout_tran). Similarly, select “vt” again, to select the input net “IN” and then select “vdc” from the calculator, select the input net and the output net from the Test Schematic, rename it for easier identification. The updated ADE Explorer can be seen as shown in Figure – 4.19.

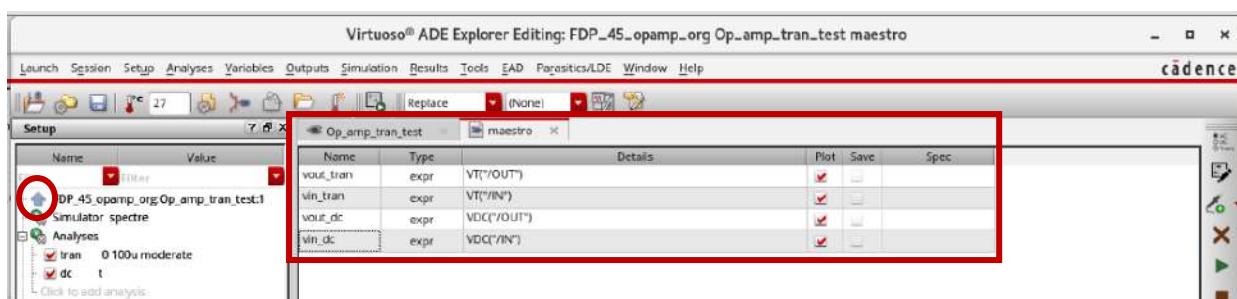


Figure – 4.19: Updated ADE Explorer

Click on the “Upward Arrow” just before the Test Circuit name in the **Setup** tab to invoke the **ADE Assembler** as shown in Figure – 4.20. The ADE Assembler allows multiple tests to be simulated on the same environment.

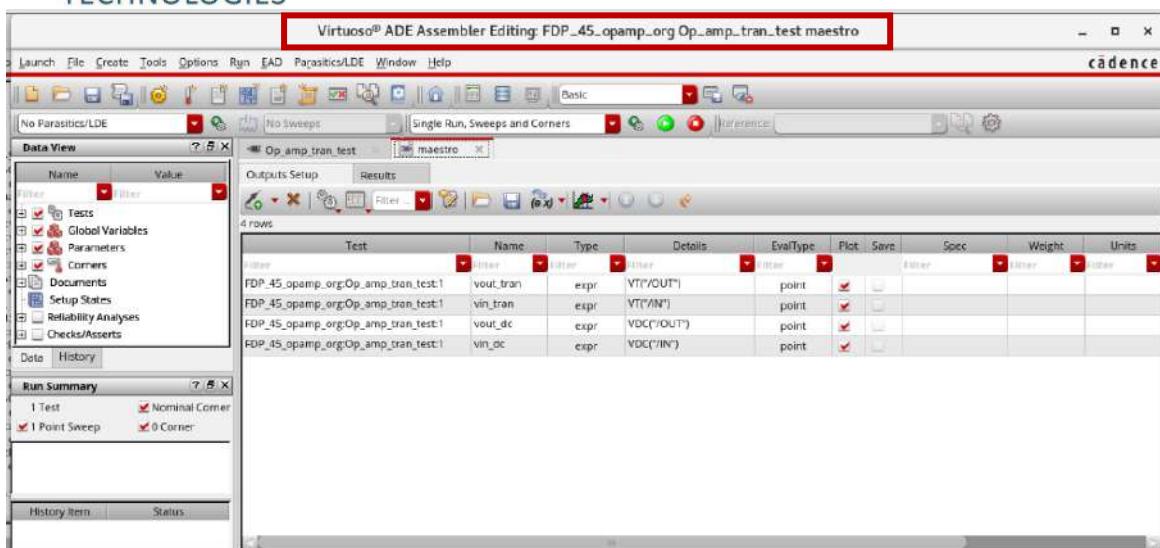


Figure – 4.20: ADE Assembler invoked

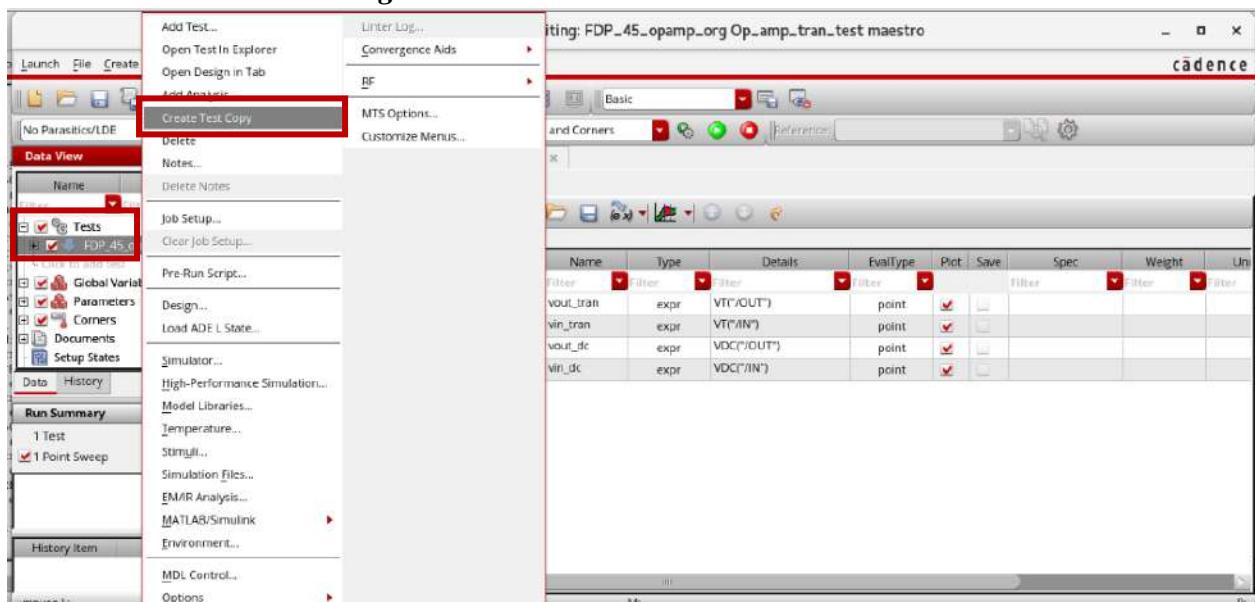


Figure – 4.21: Create Test Copy

Expand “**Tests**” and use the left mouse click to select the Test Circuit and use the right mouse click to select “**Create Test Copy**” as shown in Figure – 4.21.

Use a left mouse click to select the “**Copied Test**” (for eg: **FDP_45_opamp_org:Op_amp_tran_test:1:1**) as shown in Figure – 4.22. Left mouse click again to rename it to **FDP_45_opamp_org:Op_amp_ac_test:1** as shown in Figure – 4.22.

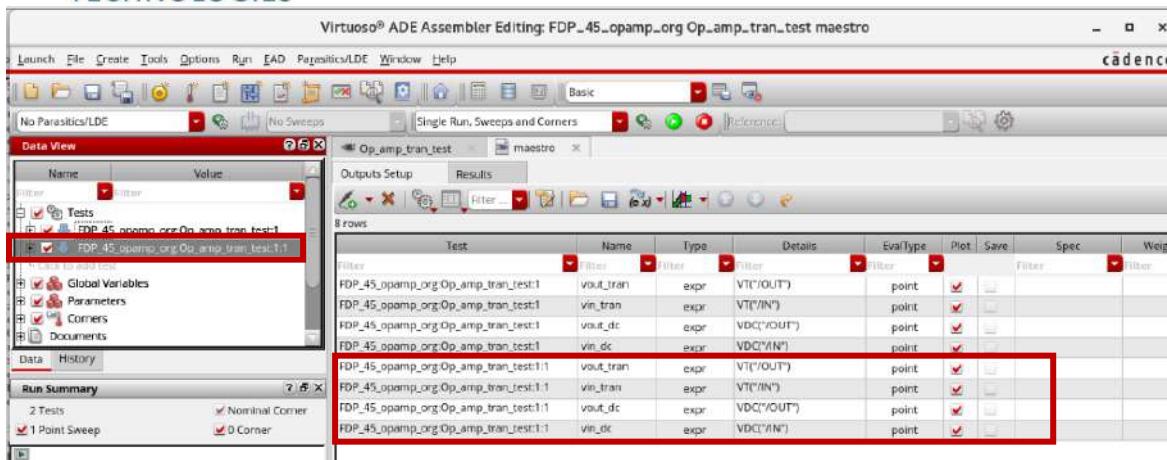


Figure – 4.22: Copied Test

Left mouse click again to rename it to **FDP_45_opamp_org:Op_amp_ac_test:1** as shown in Figure – 4.23.

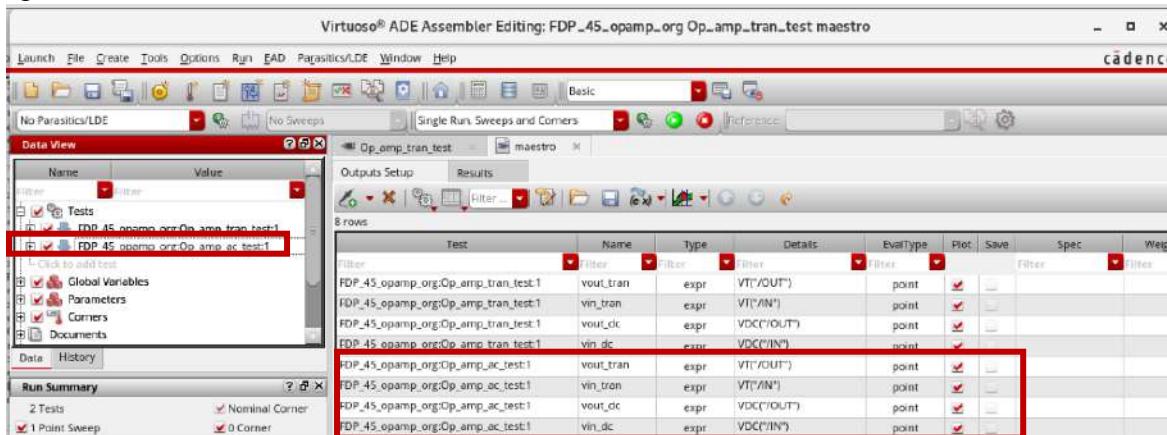


Figure – 4.23: Renamed Test

To verify the selected design for “ac” test, right mouse click on the test and select “Design” as shown in Figure – 4.24.

The “Choose Design – ADE Assembler” window pops up as shown in Figure – 4.25.

Select the Library, Cell Name, “View Name → Schematic” and click on “OK”.

Select all the tests related to “ac” from the “Outputs Setup” and delete them.

Select the “ac” test from the “Data View” window, expand, select “Analyses” and remove the “tran” and “dc” analysis that were copied.

The updated ADE Assembler window is shown in Figure – 4.26.

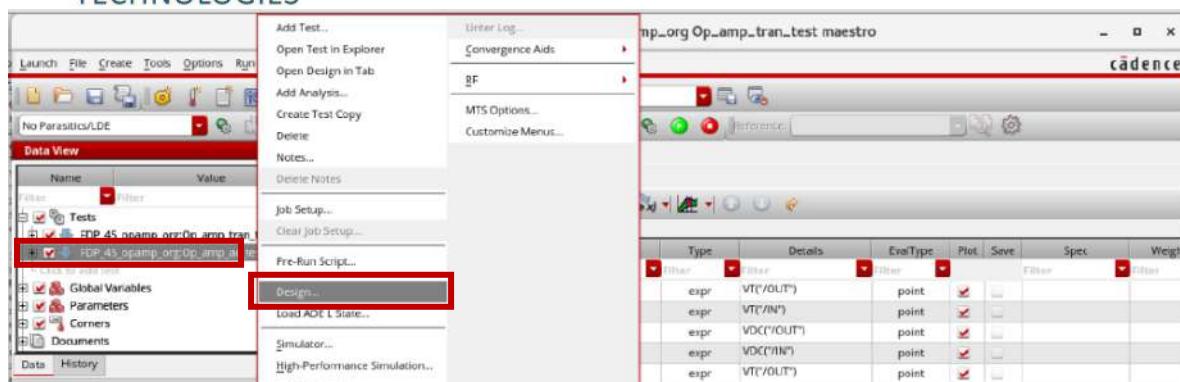


Figure – 4.24: Select “Design” option

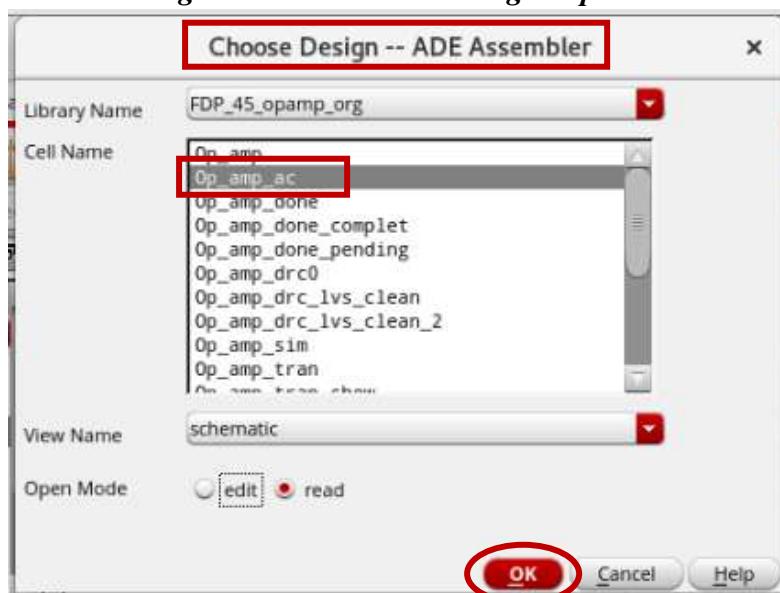


Figure – 4.25: Select the “Op_amp_ac” Cell Name

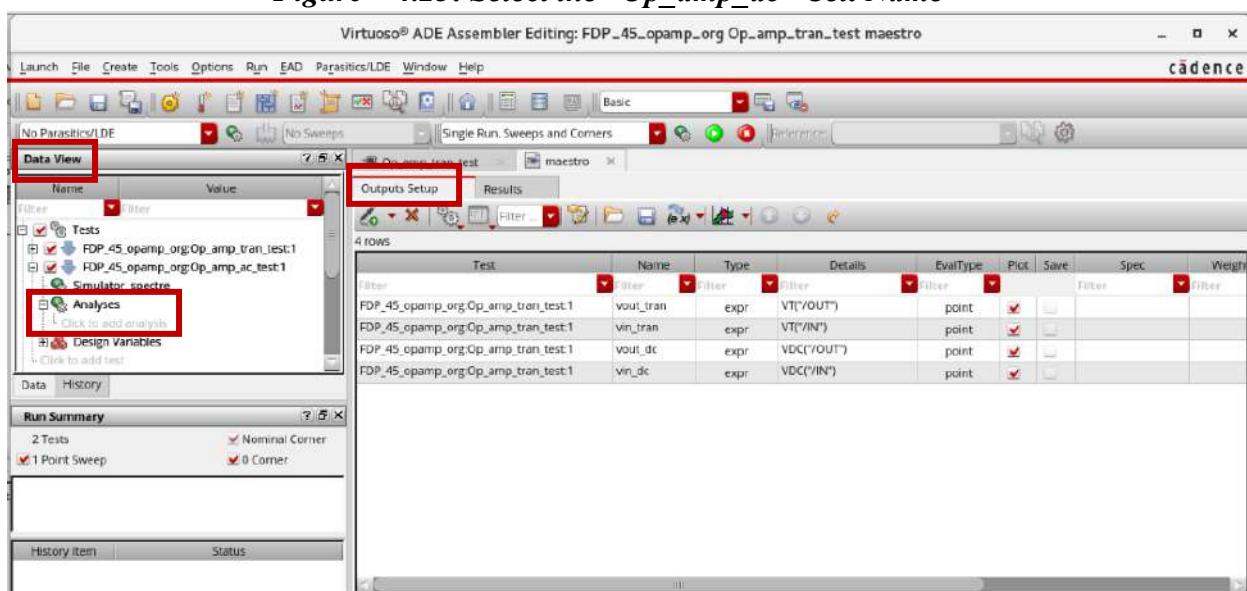


Figure – 4.26: Updated ADE Assembler

Select “Click to add analysis” option from the **Analyses** option to select the “ac” analysis for the Test Schematic. The parameters are shown in Figure – 4.27.

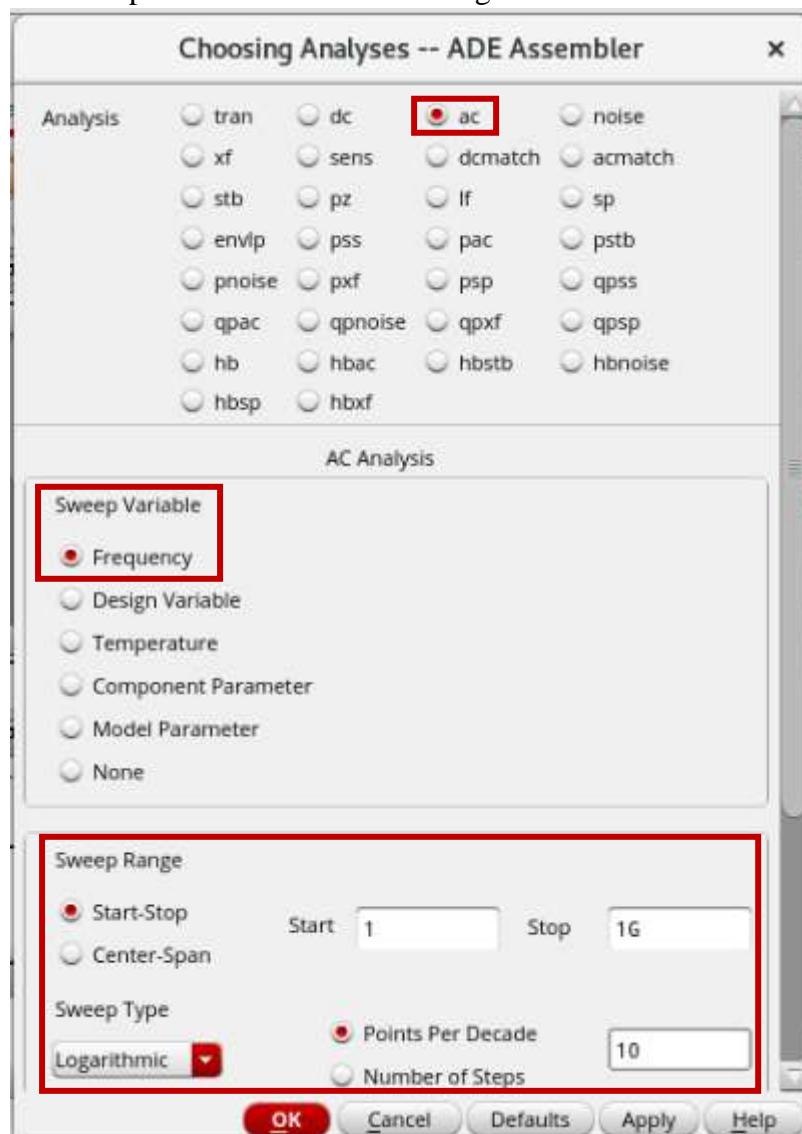


Figure – 4.27: “ac” analysis

Click on “Apply”, click on “OK” to see the ADE Assembler updated as shown in Figure – 4.28.

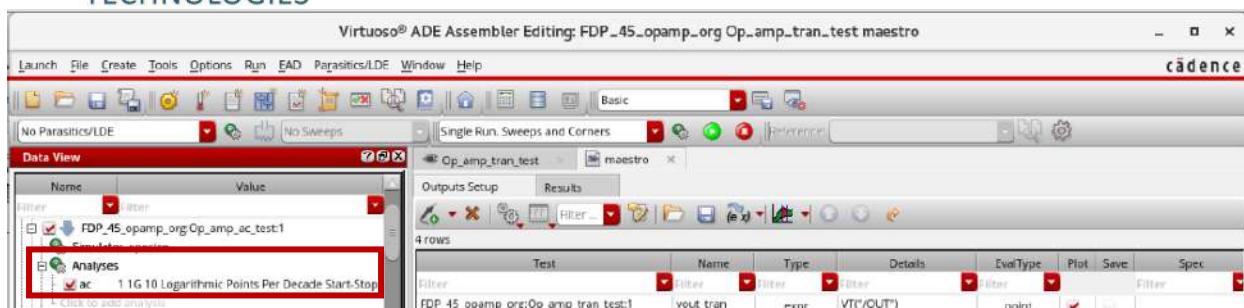


Figure – 4.28: Updated ADE Assembler with “ac” analysis

Expand the “Design Variables”, add “vac” as the variable and “100m” as its value by selecting the “Click to add variable” option. The updated Design Variables are shown in Figure – 4.29.

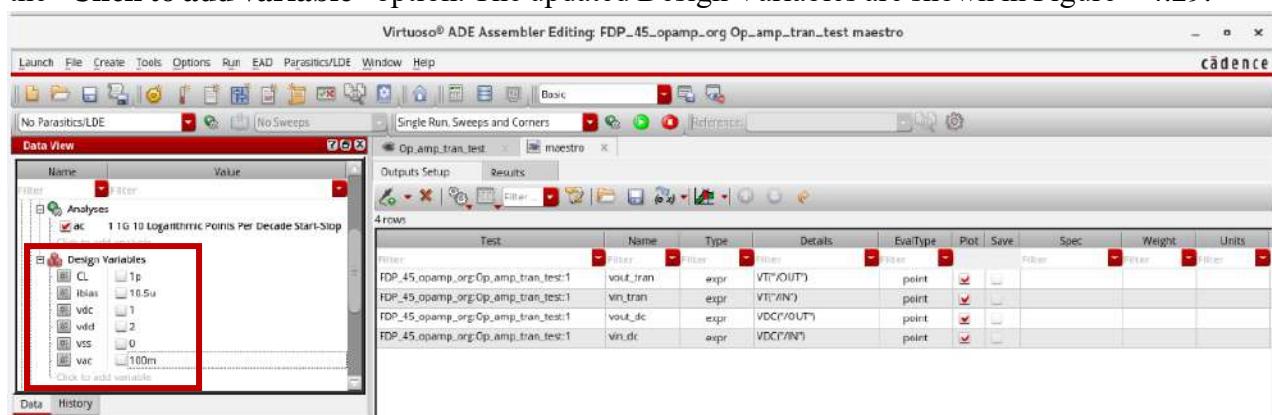


Figure – 4.29: Updated Design Variables

Select “Tools → Calculator” and select the “ac” analysis test circuit as shown in Figure – 4.30.

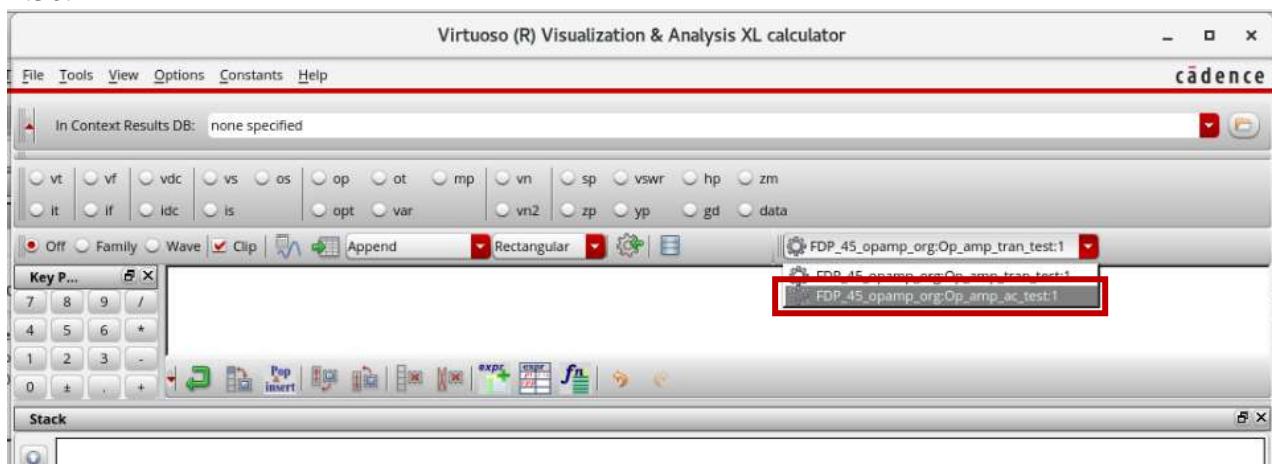


Figure – 4.30: Selecting “ac” test from calculator

Select “vf” which accesses voltage over frequency and select the output net from the Test Schematic. The updated Buffer can be seen in Figure – 4.31.

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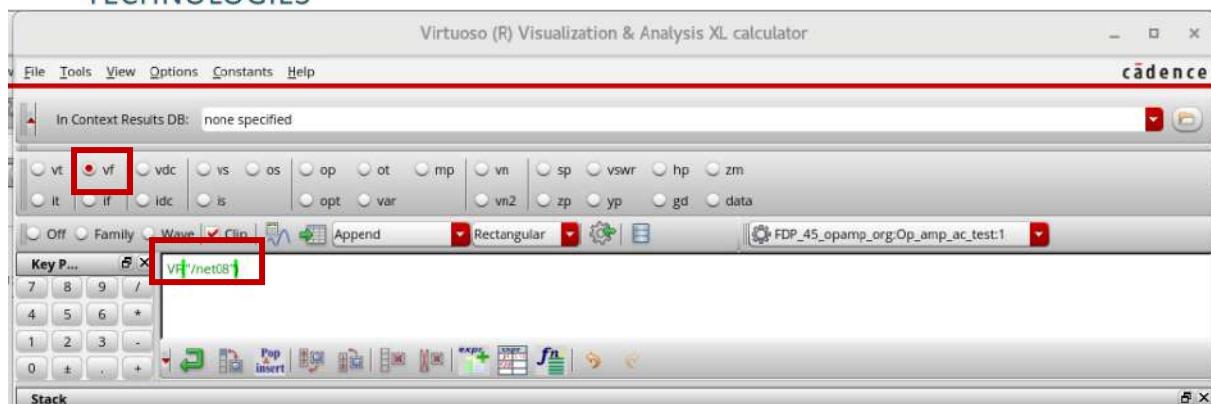


Figure – 4.31: Updated Buffer after “vf” and output net selection

Similarly, select the input net from the Test Schematic. The buffer and stack gets updated as shown in Figure – 4.32.

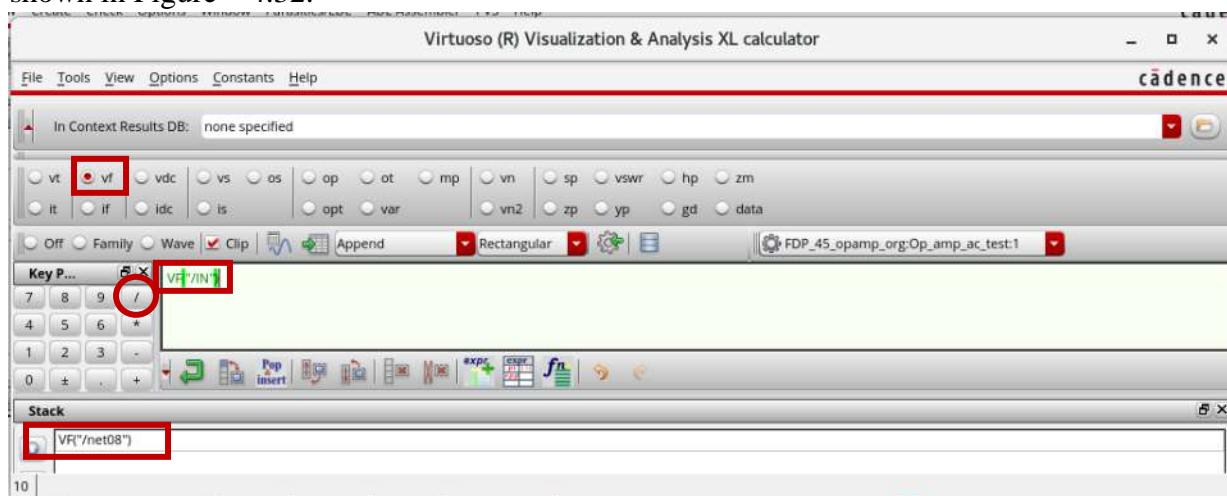


Figure – 4.32: Updated Buffer and Stack

Click on “ / “ from the keypad as shown in Figure – 4.32. The expression in the Buffer gets updated as shown in Figure – 4.33.

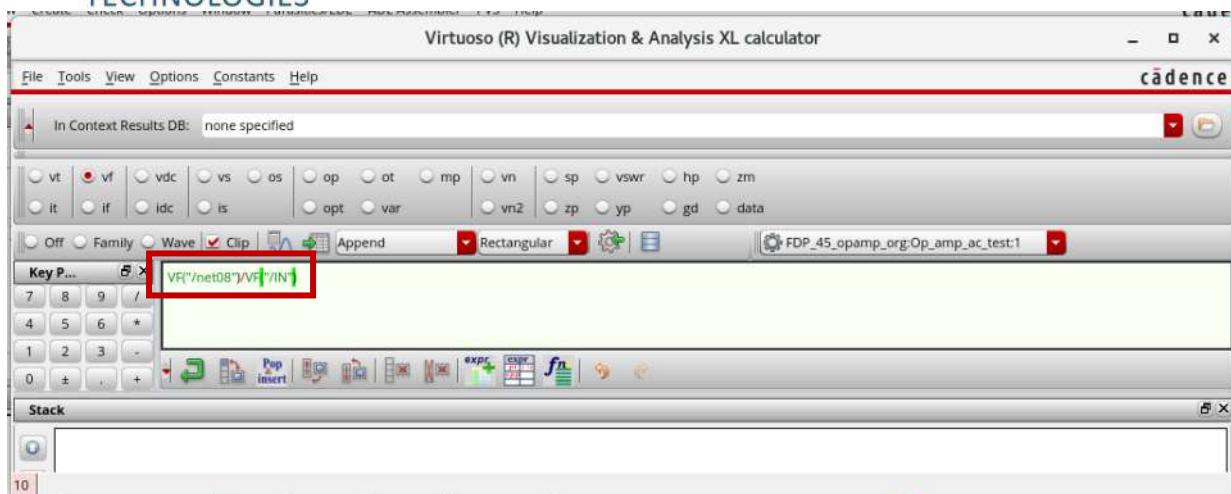


Figure – 4.33: Updated Buffer and Stack

Select “dB20” from the Function Panel, the expression in buffer gets updated as shown in Figure – 4.34.

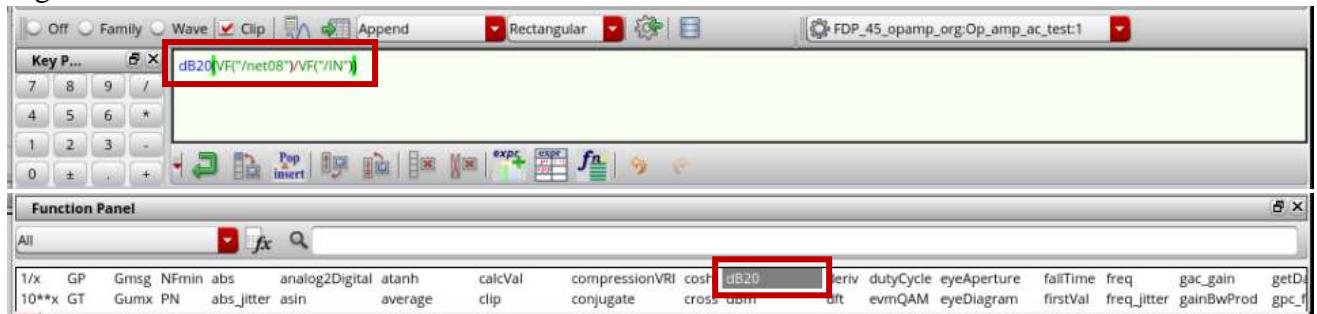


Figure – 4.34: Updated Buffer after selecting “dB20”

This expression calculates the Gain in dB for the Amplifier. Click on “Send buffer expression to ADE Outputs”. Rename the expression and the updated ADE Assembler can be seen as shown in Figure – 4.35.

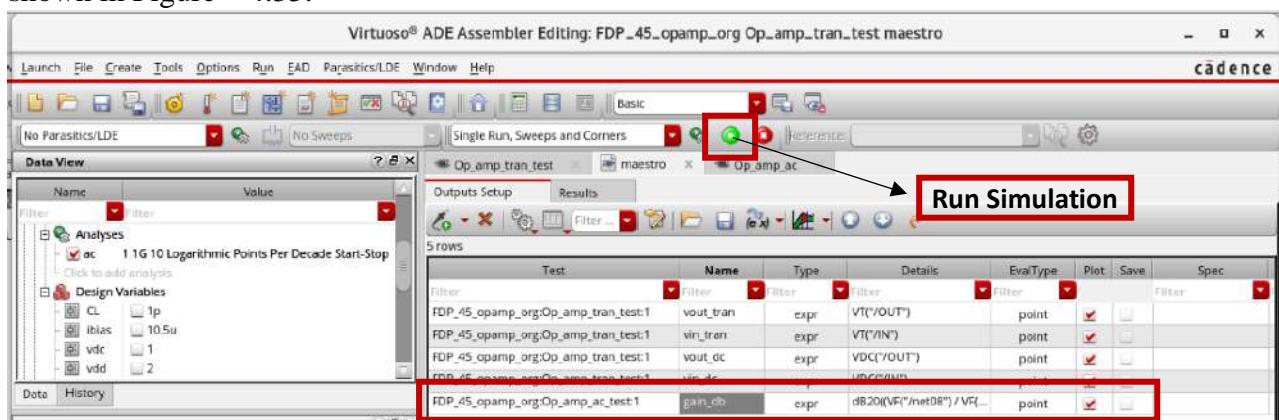


Figure – 4.35: Expression from the Calculator

Click on “Run Simulation” option as shown in Figure – 4.35 to simulate the design. The ADE Assembler after simulation is shown in Figure – 4.36.

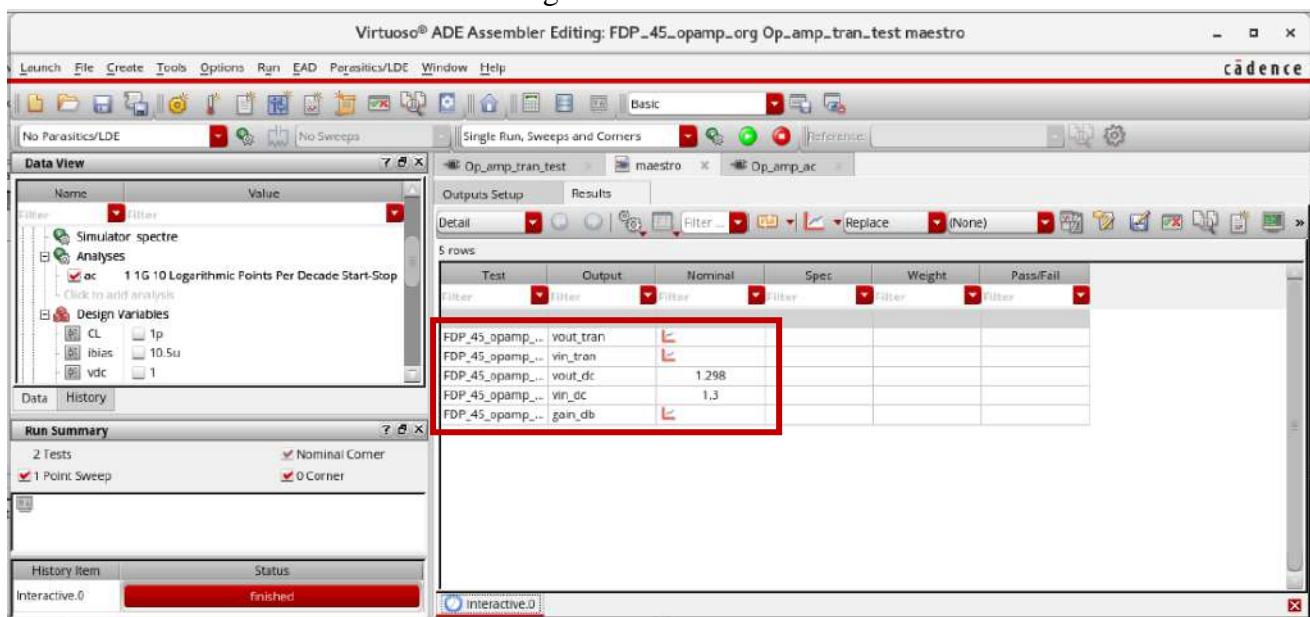


Figure – 4.36: ADE Assembler after simulation

Select “Options → Plotting/Printing” as shown in Figure – 4.37.

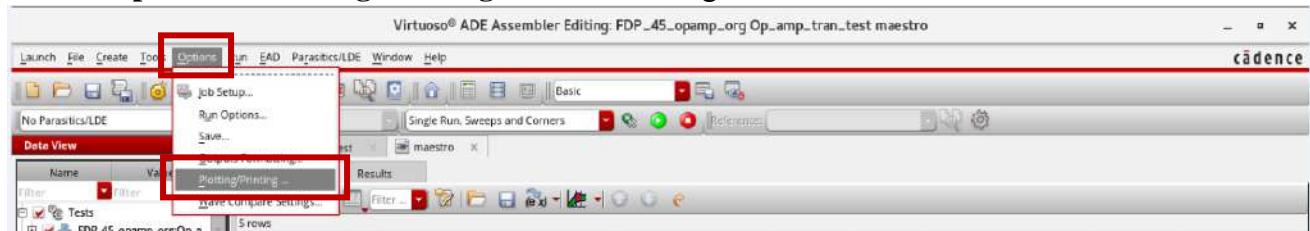


Figure – 4.37: Options → Plotting/Printing

The “ADE Assembler Plotting/Printing Options” window pops up as shown in Figure – 4.38. Select “Plotting Option → Auto” and uncheck “Plot Scalar Expressions”, click on “OK” as shown in Figure – 4.38.

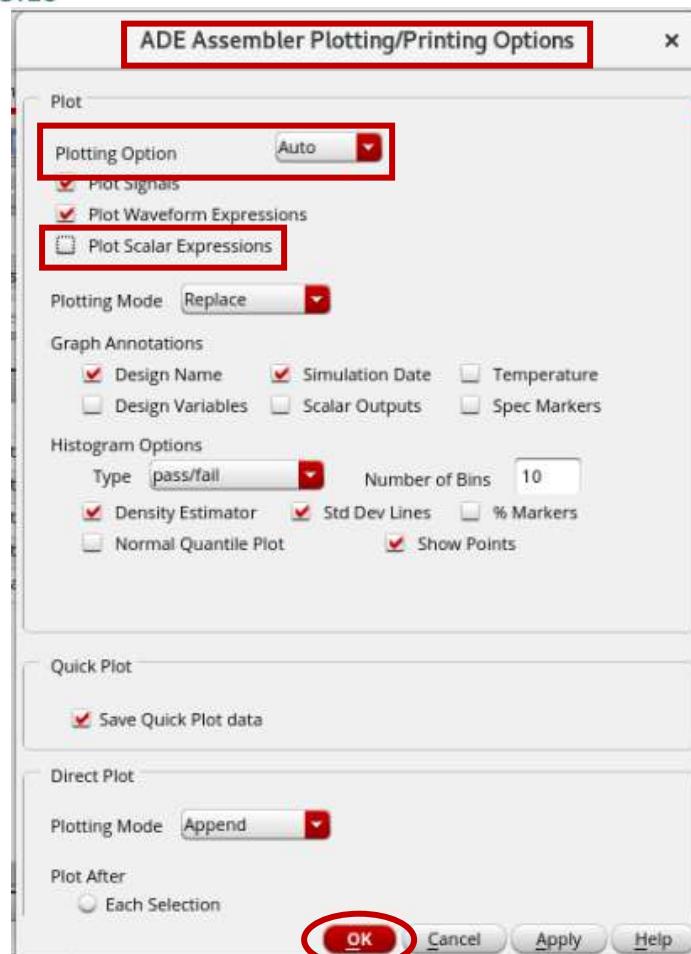


Figure – 4.38: ADE Assembler Plotting/Printing Options” window

Click on “Plot All” to see the waveforms as shown in Figure – 4.39.

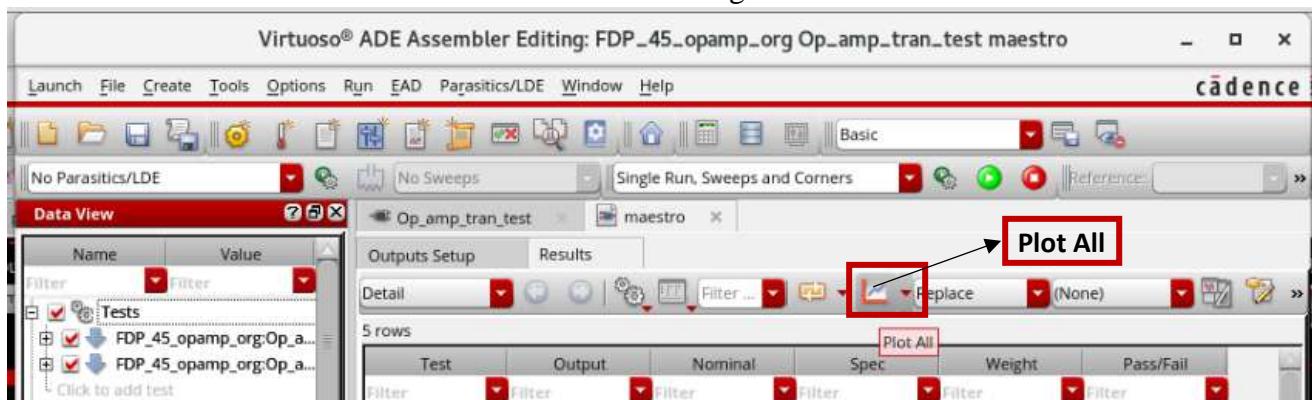


Figure – 4.39: “Plot All” option

The plotted waveforms can be visualized in the “Virtuoso Visualization & Analysis XL” window as shown in Figure – 4.40.

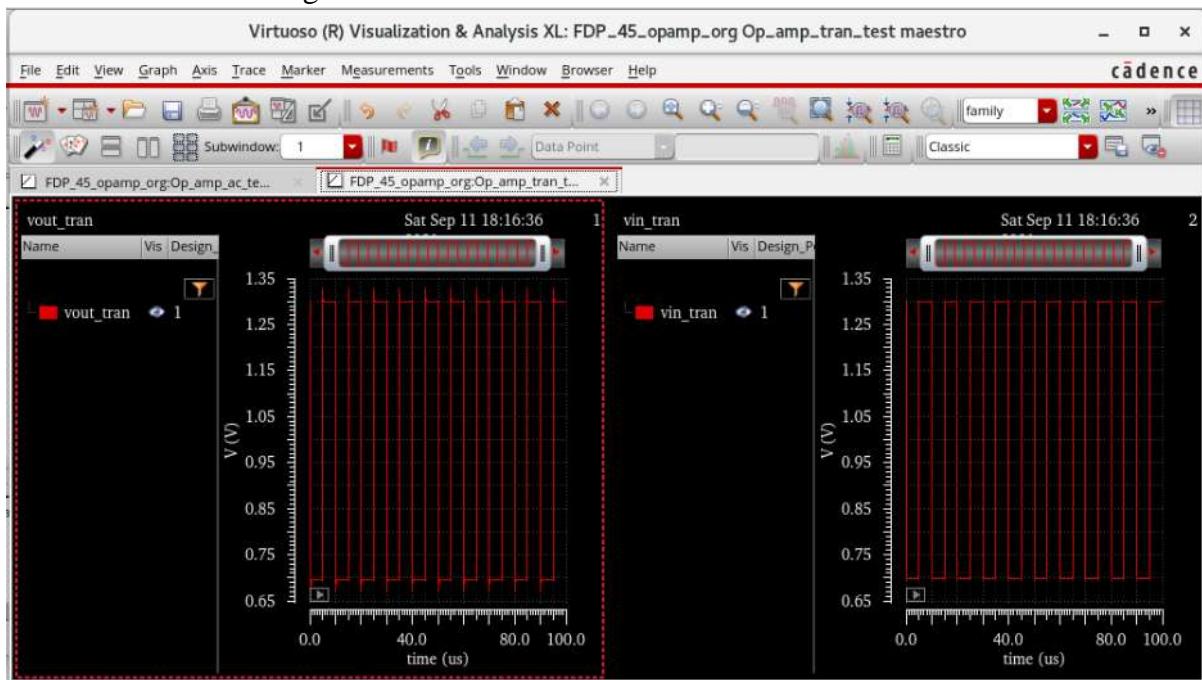


Figure – 4.40: Plotted Waveforms

Select “Measurements → Transient Measurement” as shown in Figure – 4.41.

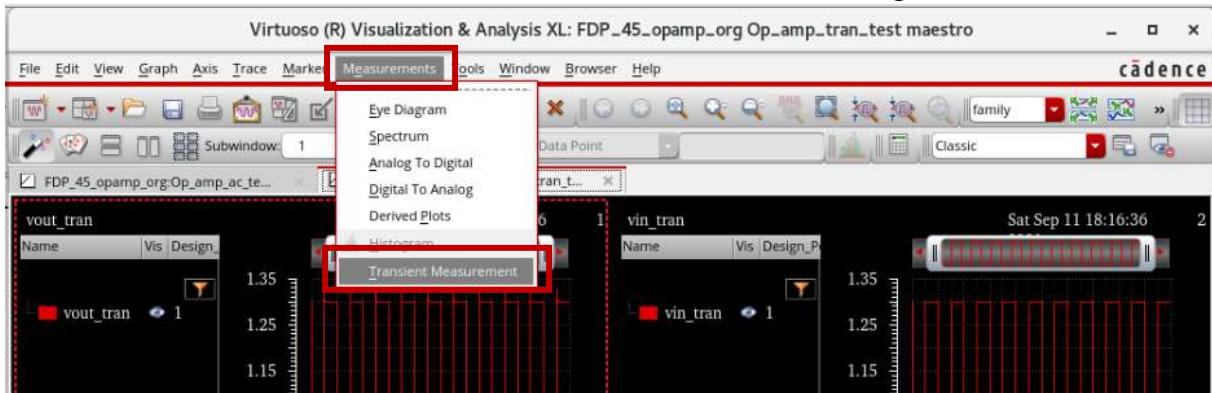


Figure – 4.41: Measurements → Transient Measurement

The **Slew Rate** can be checked out as shown in Figure – 4.42.

To calculate the **Settling Time**, consider the time the wave takes to reach and stay between (+/- 1%) of its final value in comparison with the initial value. This is calculated as follows:

$$\text{Lower Bound} = 99\% * (1.3 \text{ V} - 0.7 \text{ V}) + 0.7 \text{ V} = 1.294 \text{ V}$$

$$\text{Upper Bound} = 101\% * (1.3 \text{ V} - 0.7 \text{ V}) + 0.7 \text{ V} = 1.306 \text{ V}$$

Right Mouse click on X-axis properties, “Independent Axis Properties for time” window pops up as shown in Figure – 4.43.

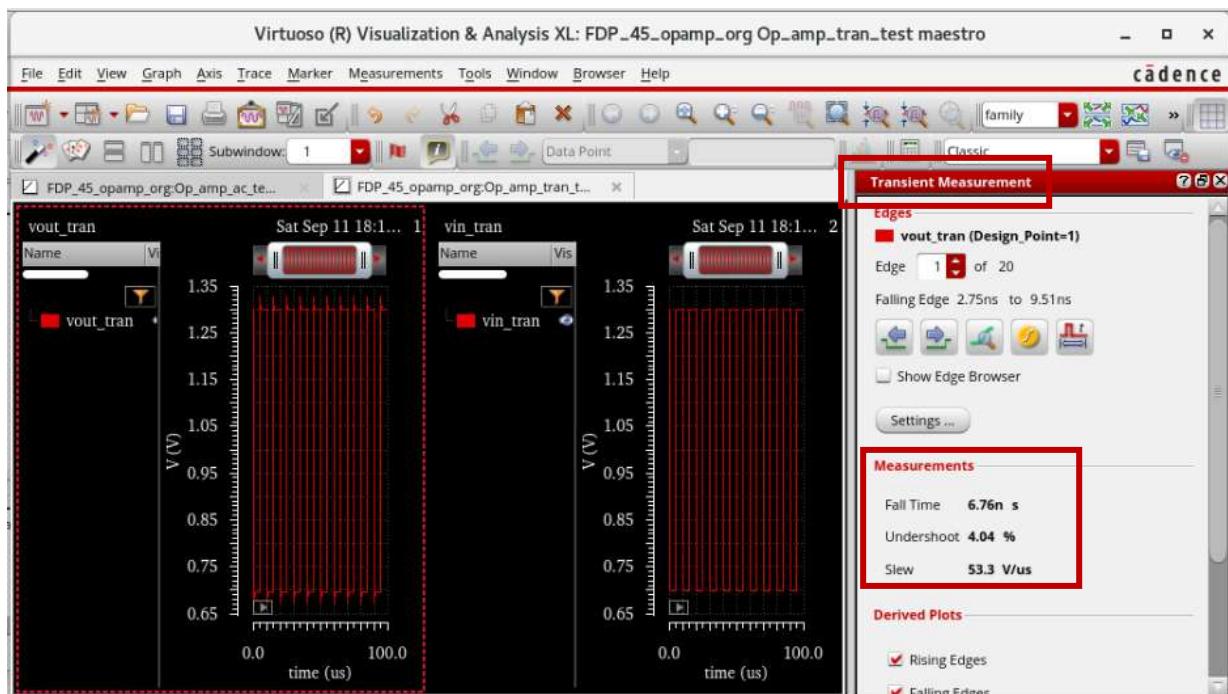


Figure – 4.42: Transient Measurement tab

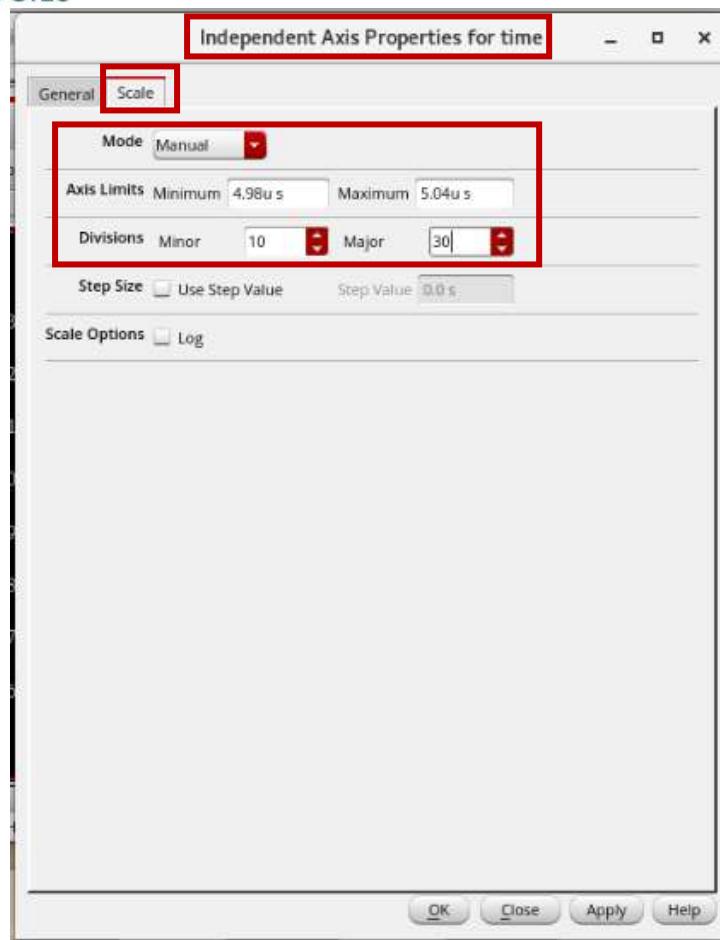


Figure – 4.43: “Independent Axis Properties for time” window

Select the “Scale” tab, select “Mode → Manual”, mention Axis Limits “Minimum → 4.98u s”, “Maximum → 5.04u s” and Divisions “Minor → 10”, “Major → 30”, click on “OK” as shown in Figure – 4.43. This will isolate the edges that are to be analyzed as shown in Figure – 4.44.



Figure – 4.44: Isolated Waveforms

Use left mouse click and drag and drop to combine the waveforms as shown in Figure – 4.45.

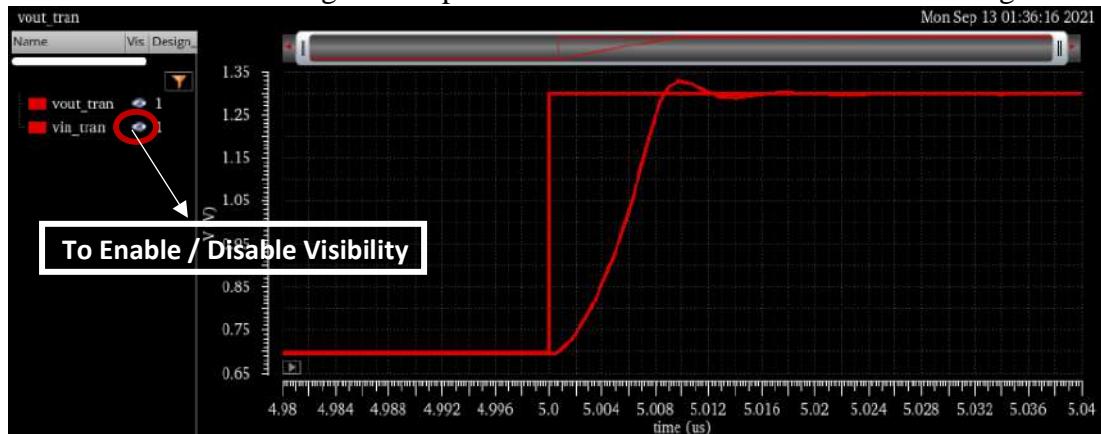


Figure – 4.45: Combined Waveforms

Use the bind key “M” to setup a Marker at the required time instance as shown in Figure – 4.46.

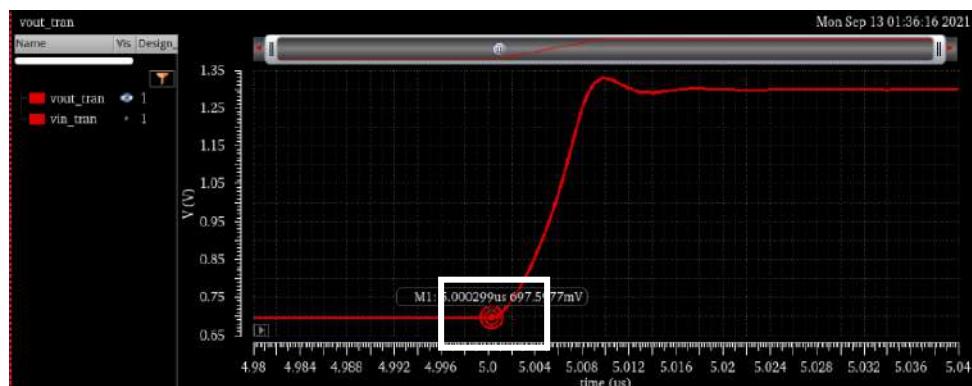


Figure – 4.46: Waveform with Marker

Use the bind key “H” to setup horizontal cursors at **1.294 V** and **1.306 V** as shown in Figure – 4.47.

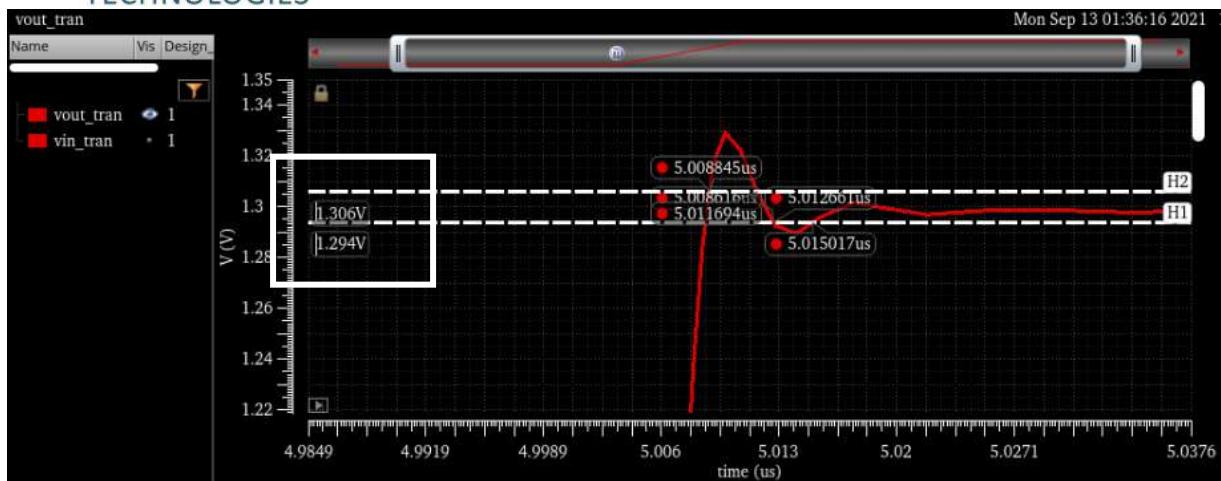


Figure – 4.47: Horizontal cursors at 1.294 V and 1.306 V

Use the zooming options to zoom-in and zoom-out as and when required. Setup a marker on the lower horizontal cursor as shown in Figure – 4.48.



Figure – 4.48: Marker on the 2nd horizontal cursor

The difference between the timing instances gives the **Settling Time** as **12.5n s**.

Without closing the waveform window, open the “maestro” in the ADE Assembler.

For this simulation, the output dc value is 1.298 V and the input dc value is 1.3 V.

The difference gives the **DC Offset (1.298 V – 1.3 V = 2m V)**.

From the AC Analysis curve, set the marker on the low frequency portion of the signal as shown in Figure – 4.49.

The marker reading gives the **DC Open Loop Gain** which is **50.98 dB**.

Setup a horizontal cursor at **0 dB** as shown in Figure – 4.50. The point of intersection of the cursor with the AC Analysis curve gives the Unity Gain Bandwidth.

The **Unity Gain Bandwidth** is measured as **84.51M Hz**.

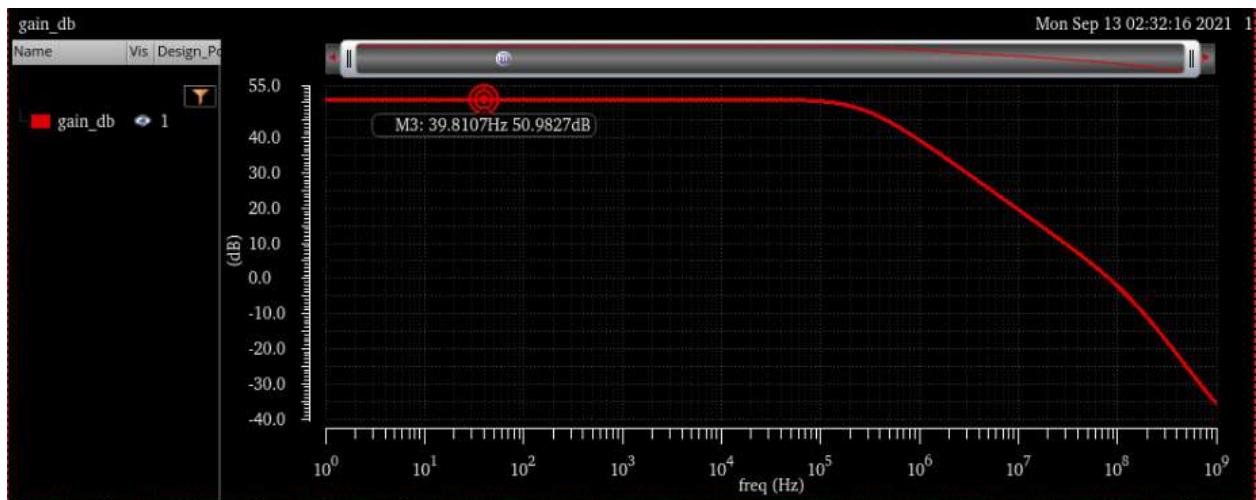


Figure – 4.49: DC Open Loop Gain – 50.98 dB

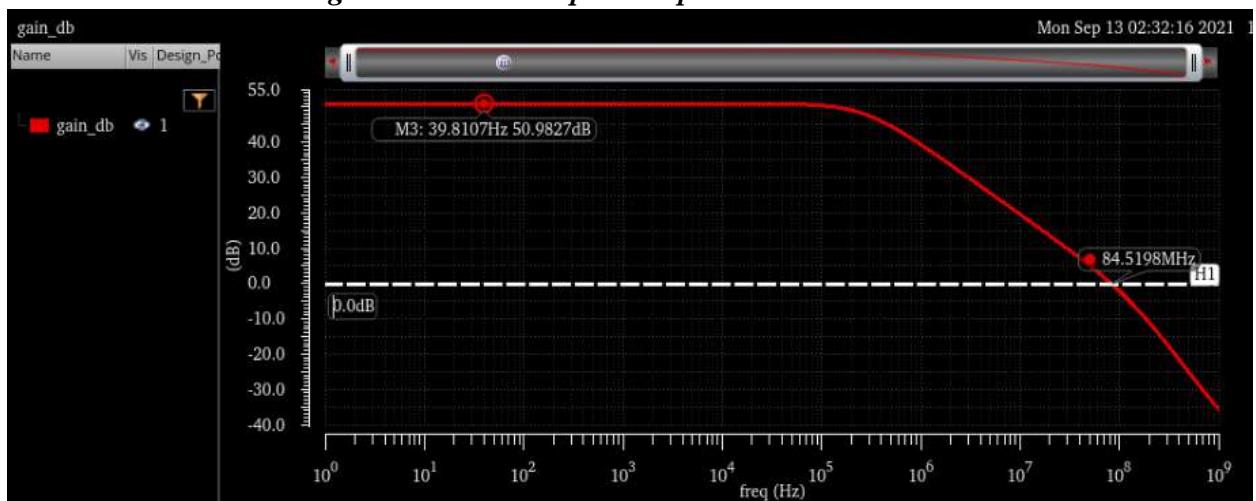


Figure – 4.50: Unity Gain Bandwidth – 84.51M Hz

GENERATING THE EXPRESSIONS:

To improve productivity, create reusable expressions rather than using the measurements from waveforms.

To generate the expressions, open the “Outputs Setup” tab from ADE Assembler, click on “Add new output” as shown in Figure – 4.51.

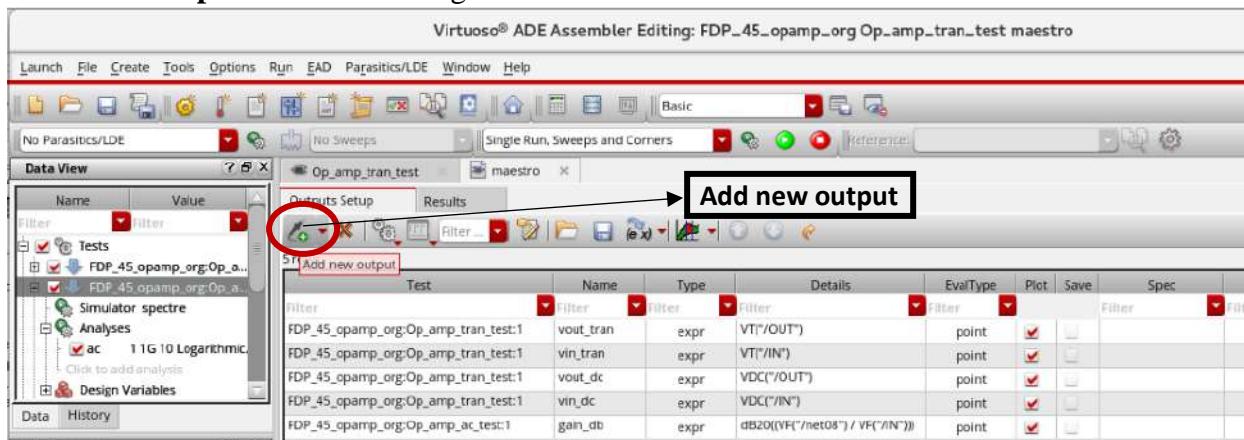


Figure – 4.51: “Add new output” option

Select “FDP_45_opamp_org:Op_amp_tran_test → Expression” as shown in Figure – 4.52.

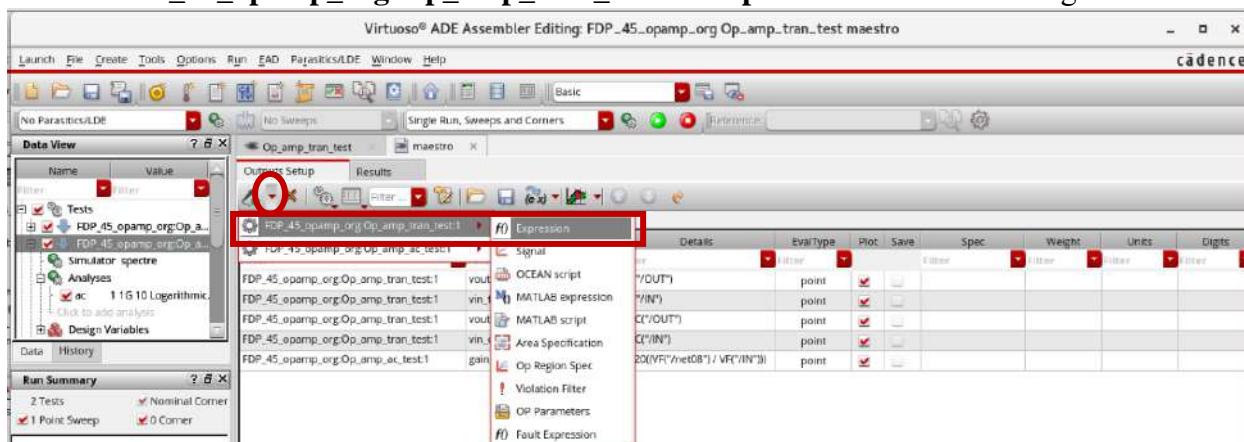


Figure – 4.52: FDP_45_opamp_org:Op_amp_tran_test → Expression

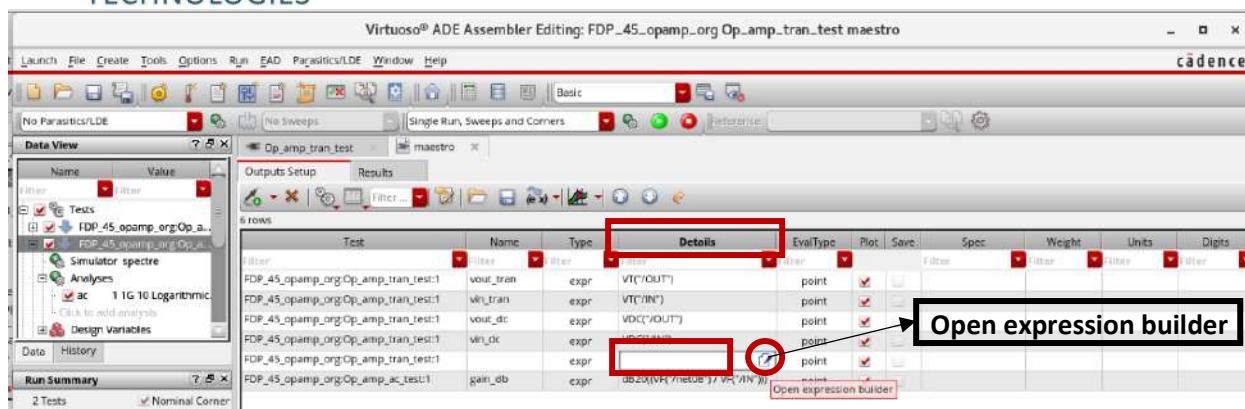


Figure – 4.53: Open expression builder

For the new expression, click on the “**Details**” column and click on “**Open expression builder**” as shown in Figure – 4.53.

Type “**Slew**” and the auto-completion can be seen. Select “**slewRate**” as shown in Figure – 4.54.

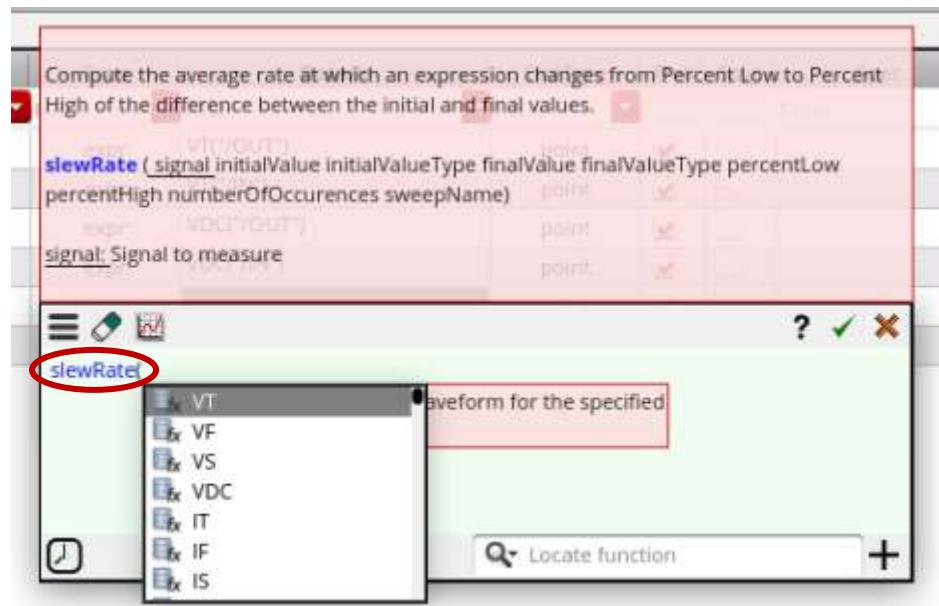


Figure – 4.54: “slewRate” auto-completion

Scroll down and select “**vout_tran**”, it points to the next parameter. Mention the values and the completed expression can be seen as shown in Figure – 4.55.



Figure – 4.55: Completed expression

The values for the remaining parameters are given below:

| | |
|------------------|-------|
| initialValue | - 1.3 |
| initialValueType | - nil |
| finalValue | - 0.7 |
| finalValueType | - nil |

| | |
|---------------------|--------|
| percentLow | - 20 |
| percentHigh | - 80 |
| numberOfOccurrences | - nil |
| sweepName | - time |

Click on the “closing parenthesis” to complete the expression. Click on the “Green” colored tick mark to update the expression in the “Details” tab as shown in Figure – 4.56.

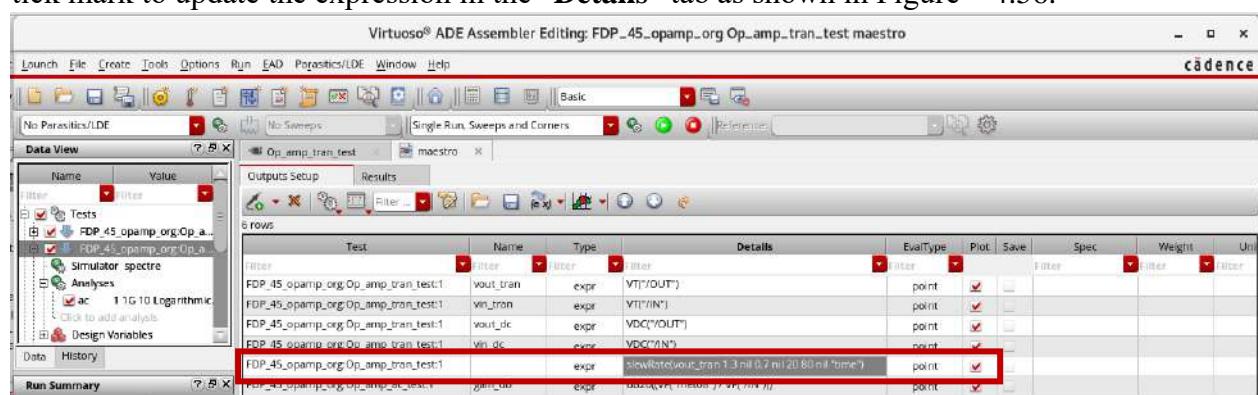


Figure – 4.56: Expression updated in ADE Assembler

Mention a “Name” for the created expression as shown in Figure – 4.57.

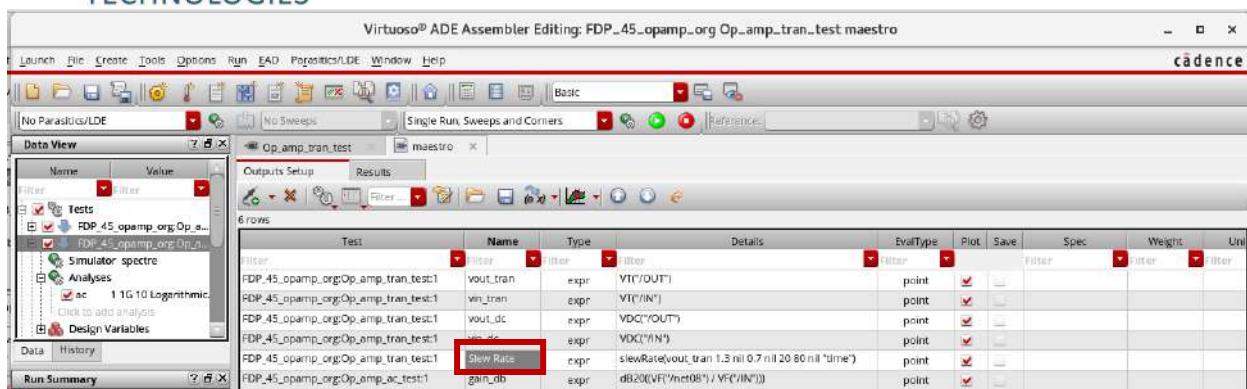


Figure – 4.57: Naming the expression

Similarly, include the expression for Settling Time. After completion, ADE Assembler is updated as shown in Figure – 4.58.

| Test | Name | Type | Details | EvalType | Plot | Save | Spec | Weight | Unit |
|-------------------------------------|---------------|------|---|----------|-------------------------------------|--------------------------|------|--------|------|
| FDP_45_opamp_org:Op_amp_tran_test:1 | vout_tran | expr | VIT("OUT") | point | <input checked="" type="checkbox"/> | <input type="checkbox"/> | | | |
| FDP_45_opamp_org:Op_amp_tran_test:1 | vin_tran | expr | VIT("IN") | point | <input checked="" type="checkbox"/> | <input type="checkbox"/> | | | |
| FDP_45_opamp_org:Op_amp_tran_test:1 | vout_dc | expr | VDC("OUT") | point | <input checked="" type="checkbox"/> | <input type="checkbox"/> | | | |
| FDP_45_opamp_org:Op_amp_tran_test:1 | vin_dc | expr | VDC("IN") | point | <input checked="" type="checkbox"/> | <input type="checkbox"/> | | | |
| FDP_45_opamp_org:Op_amp_tran_test:1 | Slew Rate | expr | slewRate(vout_tran 1.3 nV 0.7 nV 20.80 nV "time") | point | <input checked="" type="checkbox"/> | <input type="checkbox"/> | | | |
| FDP_45_opamp_org:Op_amp_tran_test:1 | Settling Time | expr | settlingTime(vout_tran 0 1.2e-06 t 1 nV "time") | point | <input checked="" type="checkbox"/> | <input type="checkbox"/> | | | |
| FDP_45_opamp_org:Op_amp_ac_test:1 | gain_db | expr | dB20((VH"/net08" / VH"/IN")) | point | <input checked="" type="checkbox"/> | <input type="checkbox"/> | | | |

Figure – 4.58: ADE Assembler updated with Settling Time

The expression for DC Offset is shown in Figure – 4.59.



Figure – 4.59: DC Offset

The expression for dissipated power is shown in Figure – 4.60. After typing “ 2 * ”, select “IDC” from the list (“2” → Total Supply voltage range applied on the op-amp). Click on “Select from design” and select the top pin of the “DC Voltage Source” instantiated for “VDD”.



```
2 * IDC("/VDD_Source/PLUS")
```

Figure – 4.60: Dissipated Power

To include the expression for DC Gain and Bandwidth, select the AC Analysis and mention the expressions. The expression for Bandwidth is shown in Figure – 4.61.



```
cross(gain_db 0 1 "falling" nil nil nil)
```

Figure – 4.61: Bandwidth

The expression for DC Gain is shown in Figure – 4.62.



```
value(gain_db 0 ?scale '(roundDown))
```

Figure – 4.62: DC Gain

After defining all the expressions, the ADE Assembler gets updated as shown in Figure – 4.63.

| Test | Name | Type | Details | EvalType | Plot |
|-------------------------------------|-------------------|--------|---|----------|--------|
| Filter | Filter | Filter | Filter | Filter | Filter |
| FDP_45_opamp_org:Op_amp_tran_test:1 | vout_tran | expr | VT("OUT") | point | ✓ |
| FDP_45_opamp_org:Op_amp_tran_test:1 | vin_tran | expr | VT("IN") | point | ✓ |
| FDP_45_opamp_org:Op_amp_tran_test:1 | vout_dc | expr | VDC("OUT") | point | ✓ |
| FDP_45_opamp_org:Op_amp_tran_test:1 | vin_dc | expr | VDC("IN") | point | ✓ |
| FDP_45_opamp_org:Op_amp_tran_test:1 | Slew Rate | expr | slewRate(vout_tran 1.3 nill 0.7 nill 20 80 nill "time") | point | ✓ |
| FDP_45_opamp_org:Op_amp_tran_test:1 | Settling Time | expr | settlingTime(vout_tran 0 t 2e-06 t 1 nill "time") | point | ✓ |
| FDP_45_opamp_org:Op_amp_tran_test:1 | DC Offset | expr | (vout_dc - vin_dc) | point | ✓ |
| FDP_45_opamp_org:Op_amp_tran_test:1 | Power Dissipation | expr | (2 * IDC("/VDD_Source/PLUS")) | point | ✓ |
| FDP_45_opamp_org:Op_amp_ac_test:1 | gain_db | expr | dB20(VF("/net08") / VF("IN")) | point | ✓ |
| FDP_45_opamp_org:Op_amp_ac_test:1 | Bandwidth | expr | cross(gain_db 0 1 "falling" nill nill) | point | ✓ |
| FDP_45_opamp_org:Op_amp_ac_test:1 | DC Gain | expr | value(gain_db 0 ?scale '(roundDown)) | point | ✓ |

Figure – 4.63: Updated ADE Assembler with expressions

Go back to the “Results” tab in the “maestro” and click on “Re-evaluates results using current settings from the outputs setup table or with partial simulation data” option as shown in Figure – 4.64 to re-simulate the expressions and evaluate the data.

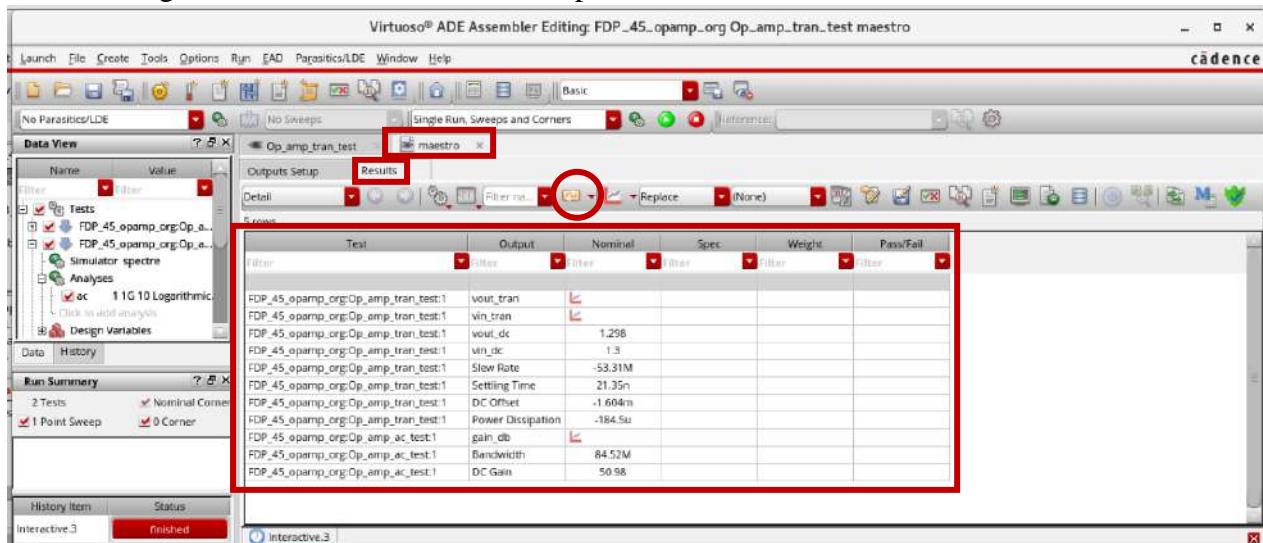


Figure – 4.64: Evaluated Results after re-simulation

Slew Rate and Power Dissipation are seen as negative values after re-simulation. To get the positive values, change the expression on the Outputs Setup as shown in Figure – 4.65.

| | | | |
|-------------------------------------|-------------------|------|--|
| FDP_45_opamp_org:Op_amp_tran_test:1 | vin_dc | expr | VDC("IN") |
| FDP_45_opamp_org:Op_amp_tran_test:1 | Slew Rate | expr | abs(slewRate(vout_tran 1.3 nill 0.7 nill 20 80 nill "time")) |
| FDP_45_opamp_org:Op_amp_tran_test:1 | Settling Time | expr | settlingTime(vout_tran 0 t 2e-06 t 1 nill "time") |
| FDP_45_opamp_org:Op_amp_tran_test:1 | DC Offset | expr | (vout_dc - vin_dc) |
| FDP_45_opamp_org:Op_amp_tran_test:1 | Power Dissipation | expr | abs(2 * IDC("/VDD_Source/PLUS")) |
| FDP_45_opamp_org:Op_amp_ac_test:1 | gain_db | expr | dB20(VF("/net08") / VF("IN")) |

Figure – 4.65: Modified expressions to get positive values

Specifications can be mentioned as shown in Figure – 4.66.

| Test | Name | Type | Details | EvalType | Plot | Save | Spec |
|-------------------------------------|-------------------|--------|--|----------|-------------------------------------|--------------------------|---|
| Filter | Filter | Filter | Filter | Filter | Filter | Filter | Filter |
| FDP_45_opamp_org:Op_amp_tran_test:1 | vout_tran | expr | VT("//OUT") | point | <input checked="" type="checkbox"/> | <input type="checkbox"/> | |
| FDP_45_opamp_org:Op_amp_tran_test:1 | vin_tran | expr | VT("//IN") | point | <input checked="" type="checkbox"/> | <input type="checkbox"/> | |
| FDP_45_opamp_org:Op_amp_tran_test:1 | vout_dc | expr | VDC("//OUT") | point | <input checked="" type="checkbox"/> | <input type="checkbox"/> | |
| FDP_45_opamp_org:Op_amp_tran_test:1 | vin_dc | expr | VDC("//IN") | point | <input checked="" type="checkbox"/> | <input type="checkbox"/> | |
| FDP_45_opamp_org:Op_amp_tran_test:1 | Slew Rate | expr | abs(slewRate(vout_tran 1.3 n1 0.7 n1 20 80 n1 "time")) | point | <input checked="" type="checkbox"/> | <input type="checkbox"/> | |
| FDP_45_opamp_org:Op_amp_tran_test:1 | Settling Time | expr | settlingTime(vout_tran 0 t 2e-06 t 1 n1 "time") | point | <input checked="" type="checkbox"/> | <input type="checkbox"/> | |
| FDP_45_opamp_org:Op_amp_tran_test:1 | DC Offset | expr | (vout_dc - vin_dc) | point | <input checked="" type="checkbox"/> | <input type="checkbox"/> | |
| FDP_45_opamp_org:Op_amp_tran_test:1 | Power Dissipation | expr | abs((2 * IDC("VDD_Source/PLUS"))) | point | <input checked="" type="checkbox"/> | <input type="checkbox"/> | |
| FDP_45_opamp_org:Op_amp_ac_test:1 | gain_db | expr | dB20((VF("//net08") / VF("//IN"))) | point | <input checked="" type="checkbox"/> | <input type="checkbox"/> | |
| FDP_45_opamp_org:Op_amp_ac_test:1 | Bandwidth | expr | cross(gain_db 0 1 "falling" n1 n1 n1) | point | <input checked="" type="checkbox"/> | <input type="checkbox"/> | |
| FDP_45_opamp_org:Op_amp_ac_test:1 | DC Gain | expr | valueof(gain_db 0 ?scale '(roundDown)) | point | <input checked="" type="checkbox"/> | <input type="checkbox"/> | |
| | | | | | | | > 50M < 50n < 200u > 50M > 60 |

Figure – 4.66: Specifications

After re-evaluation, the results can be seen as shown in Figure – 4.67.

| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|-------------------------------------|-------------------|---------|--------|--------|-----------|
| Filter | Filter | Filter | Filter | Filter | Filter |
| FDP_45_opamp_org:Op_amp_tran_test:1 | vout_tran | | | | |
| FDP_45_opamp_org:Op_amp_tran_test:1 | vin_tran | | | | |
| FDP_45_opamp_org:Op_amp_tran_test:1 | vout_dc | 1.298 | | | |
| FDP_45_opamp_org:Op_amp_tran_test:1 | vin_dc | 1.3 | | | |
| FDP_45_opamp_org:Op_amp_tran_test:1 | Slew Rate | 53.31M | > 50M | | pass |
| FDP_45_opamp_org:Op_amp_tran_test:1 | Settling Time | 21.35n | < 50n | | pass |
| FDP_45_opamp_org:Op_amp_tran_test:1 | DC Offset | -1.604m | | | |
| FDP_45_opamp_org:Op_amp_tran_test:1 | Power Dissipation | 184.5u | < 200u | | pass |
| FDP_45_opamp_org:Op_amp_ac_test:1 | gain_db | | | | |
| FDP_45_opamp_org:Op_amp_ac_test:1 | Bandwidth | 84.52M | > 50M | | pass |
| FDP_45_opamp_org:Op_amp_ac_test:1 | DC Gain | 50.98 | > 60 | | fail |

Figure – 4.67: Results after re-evaluation

GAIN MARGIN AND PHASE MARGIN:

The Schematic for measuring the Gain Margin and Phase Margin is shown in Figure – 4.68.

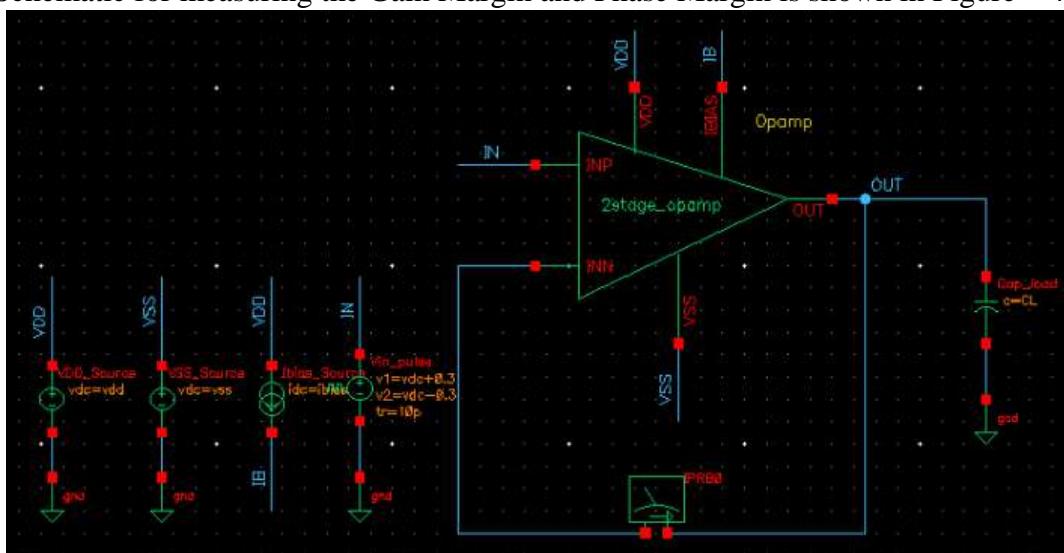


Figure – 4.68: Schematic for Gain Margin and Phase Margin measurement

The “**iprobe**” (available in “**analogLib**”) acts as a signal source for the stability analysis. Create a Test Copy for the Stability Analysis as shown in Figure – 4.69.

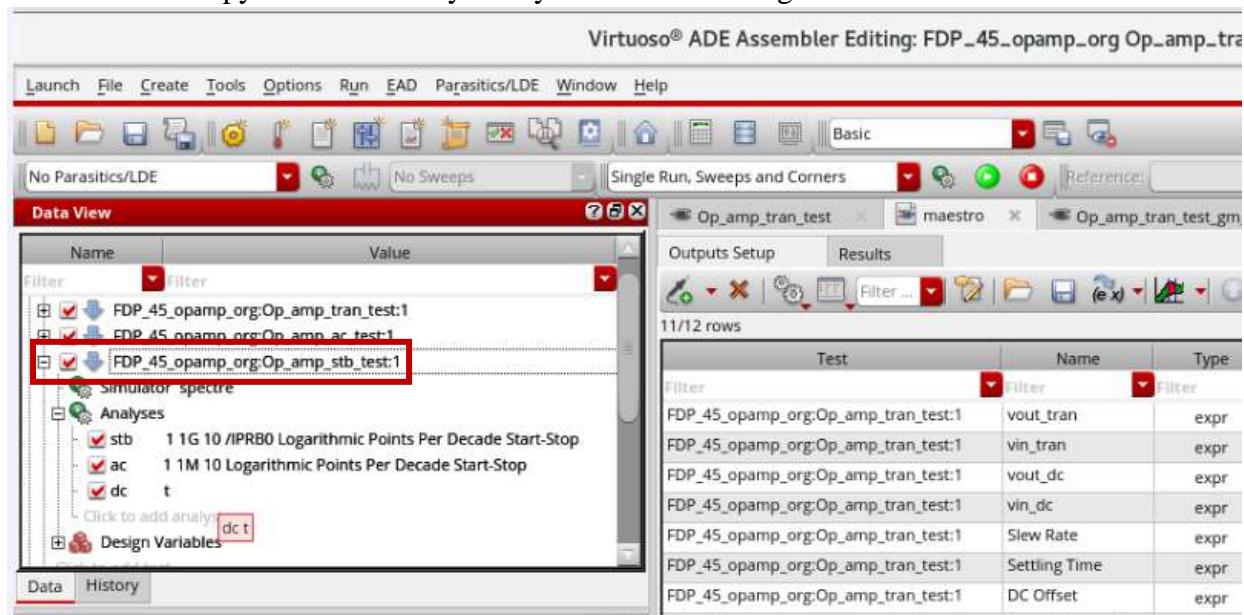


Figure – 4.69: Test Creation for Stability Analysis

Browse “**Design → Op_amp_tran_gm_pm**” as shown in Figure – 4.70.

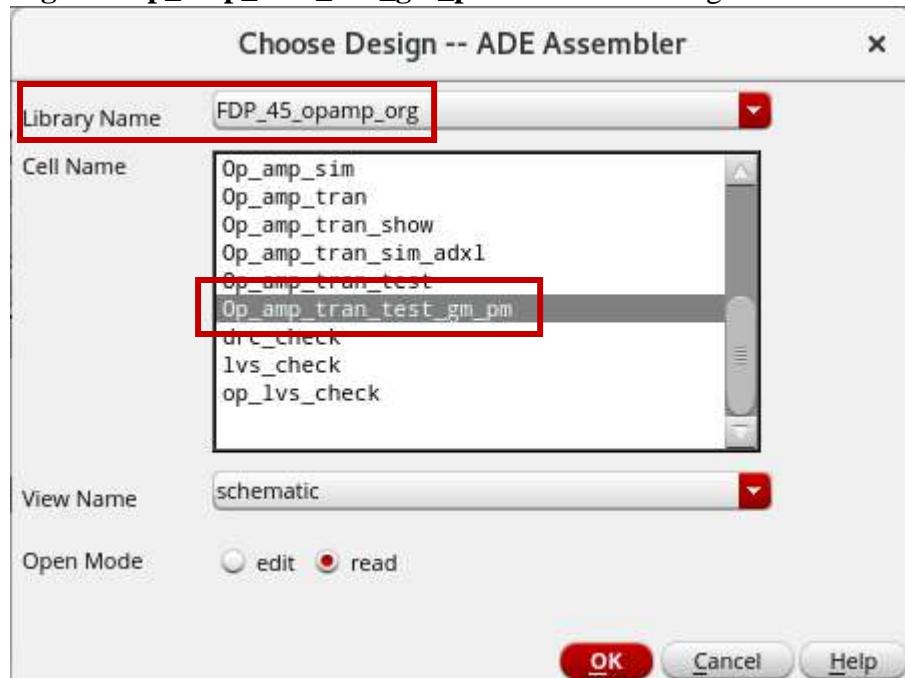


Figure – 4.70: Design Selection

Choose “stb” through “Analyses → Click to add analysis → Choosing Analyses – ADE Assembler”. The parameters are shown in Figure – 4.71.



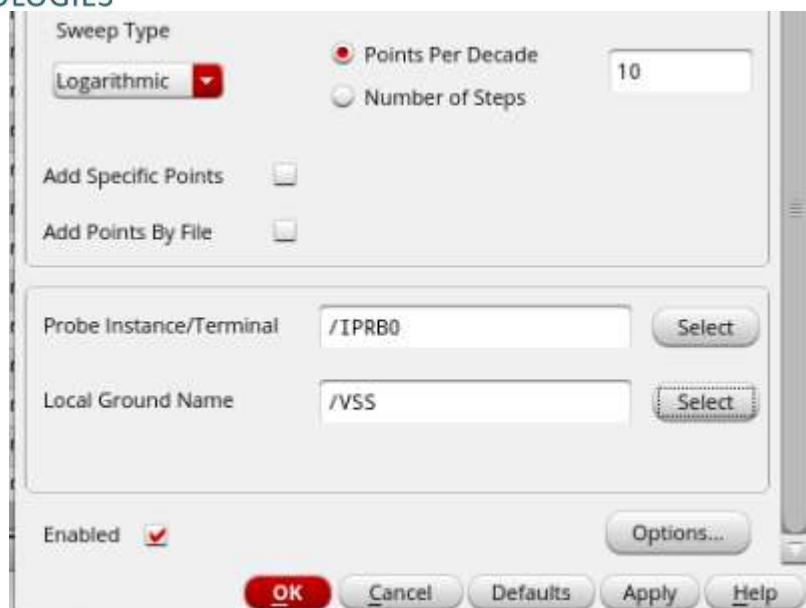


Figure – 4.71: “stb” selection and its parameters

Click on the “**downward arrow**” just before the test name as shown in Figure – 4.72 to go back to the ADE Explorer.

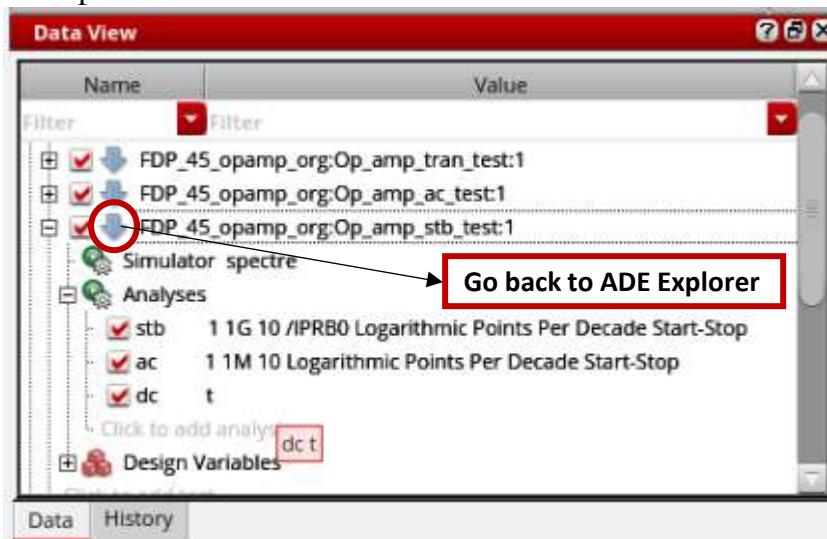


Figure – 4.72: Click on downward arrow

The ADE Explorer window pops up as shown in Figure – 4.73.

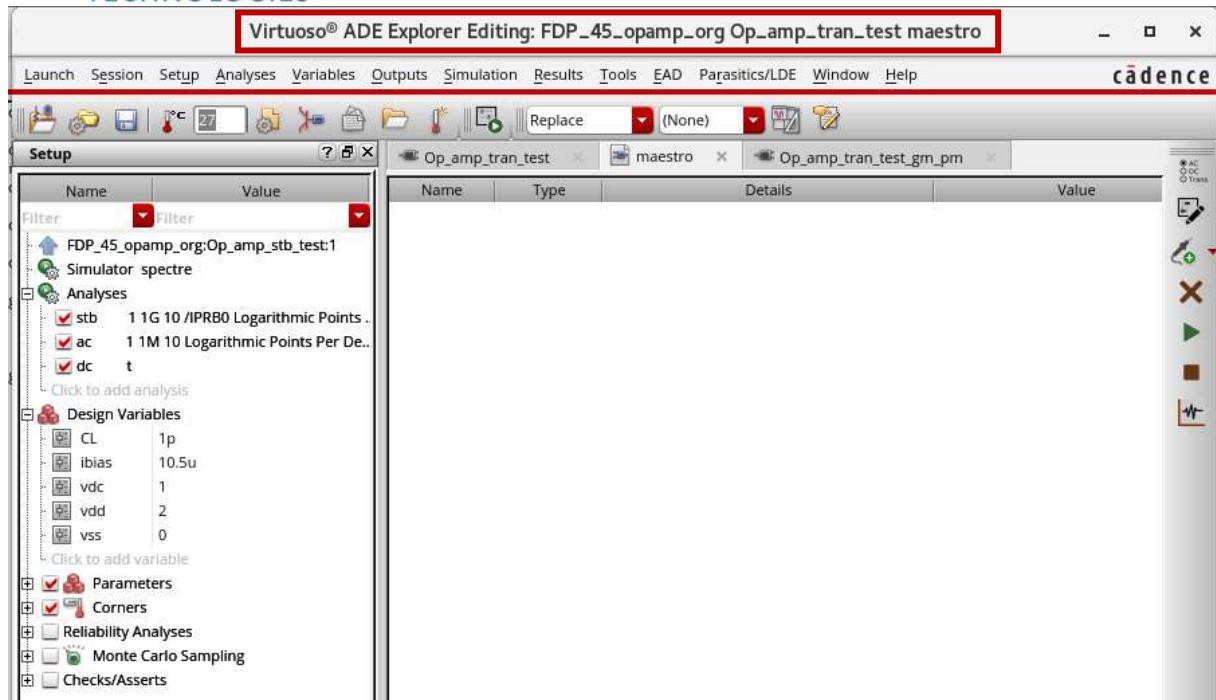


Figure – 4.73: ADE Explorer

Click on “**Simulation → Netlist and Run**” similar to the selection in ADE L window. After the simulation, select “**Results → Direct Plot → Main Form**” as shown in Figure – 4.74. The “**Direct Plot Form**” pops up as shown in Figure – 4.75. Click on “**Stability Summary**” to print the values of Gain Margin and Phase Margin. Click on “**Plot**” to plot the graph.

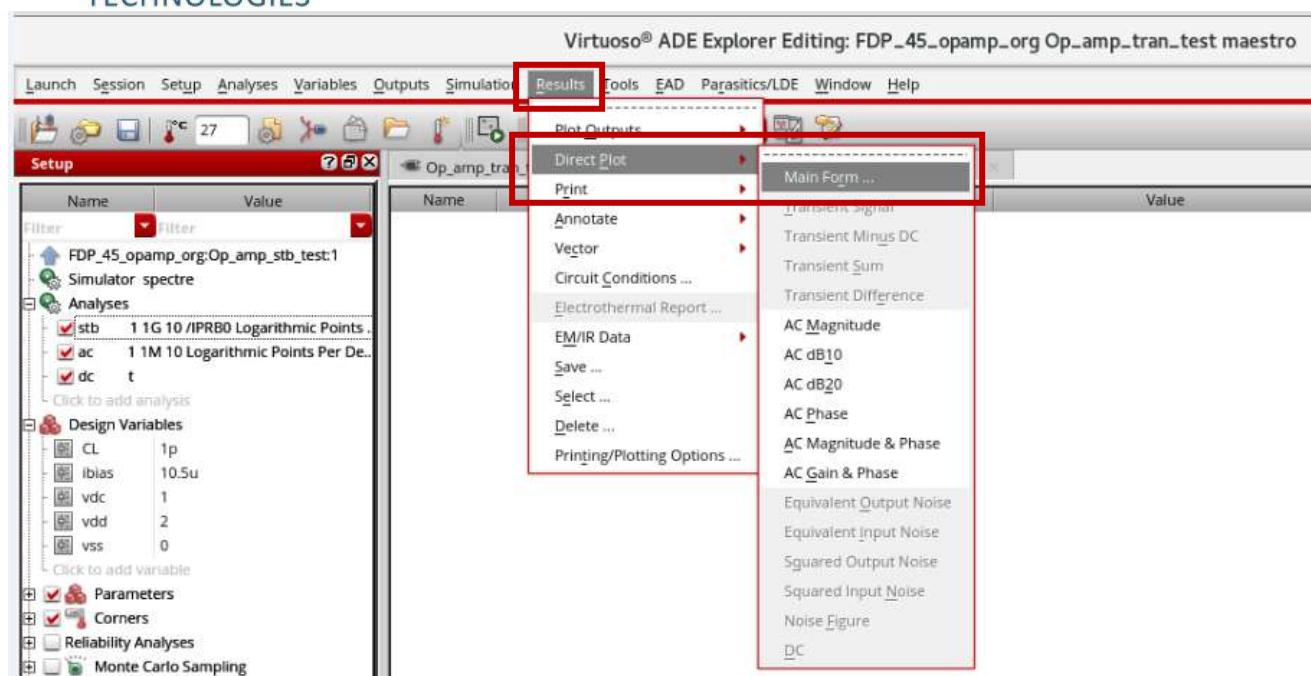


Figure – 4.74: Results → Direct Plot → Main Form

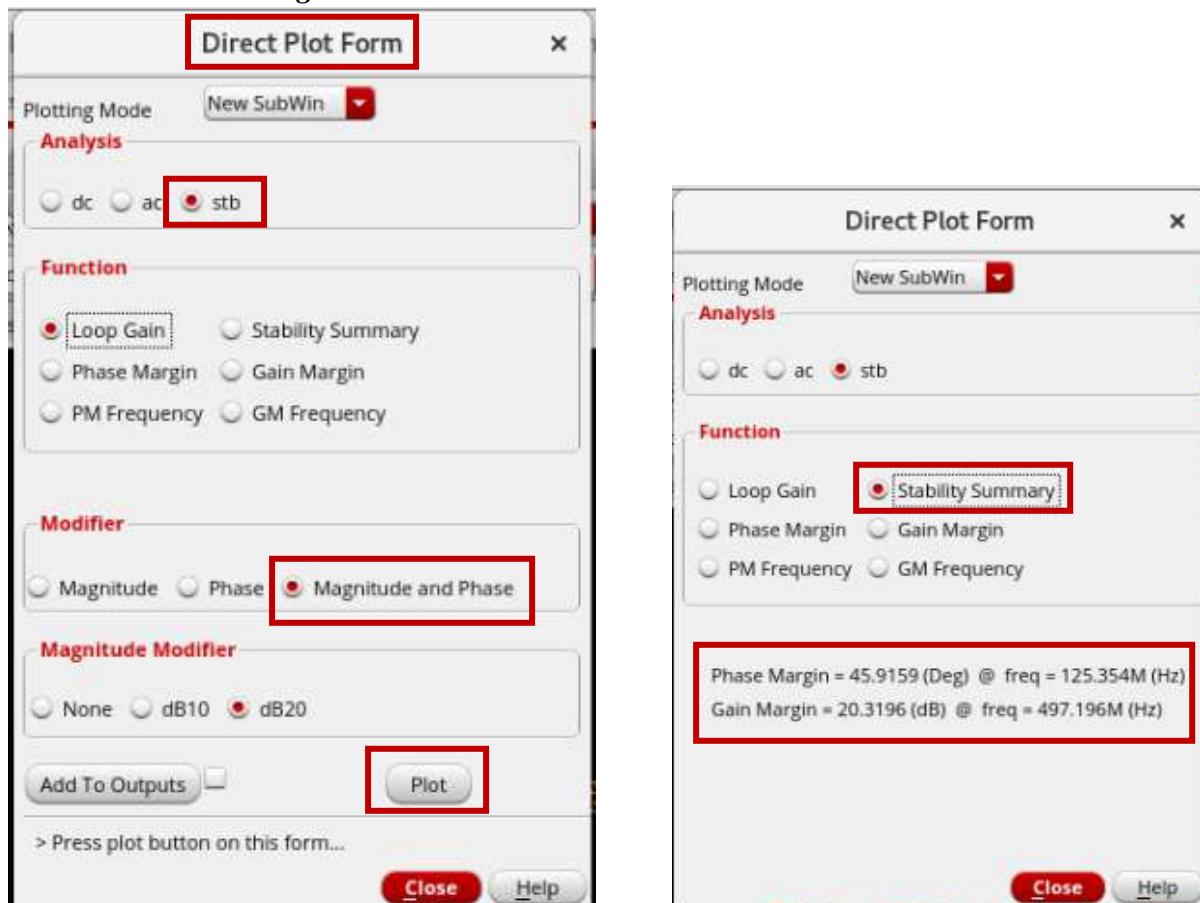


Figure – 4.75: Direct Plot Form and Stability Summary with Gain Margin and Phase Margin

LAYOUT:

Follow the techniques demonstrated in Lab – 01 to open the Layout Editor, import the devices from the Schematic, place the devices as per the requirement and complete the routing. The completed layout can be seen as shown in Figure – 4.76.

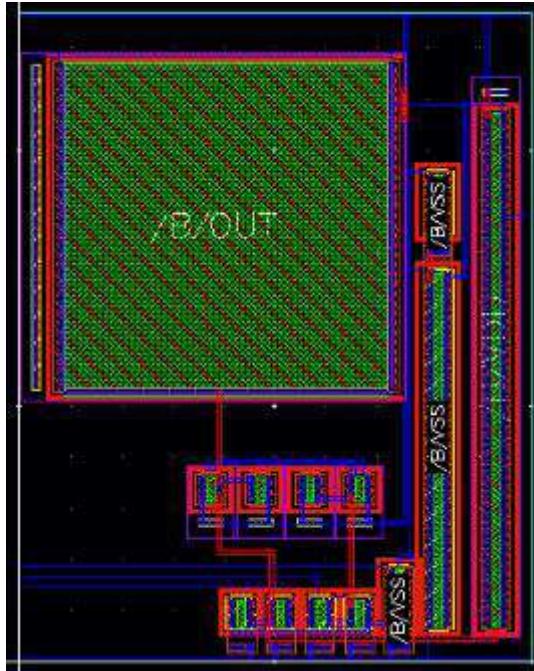


Figure – 4.76: Layout for 2 – Stage Operational Amplifier

DRC:

To check for the DRC violations, browse the “assura_tech.lib” file, select “**Assura → Run DRC**”, verify the Layout Design Source, mention a “Run Name”, select “**Technology → gdk045**” and click on “OK” as demonstrated in Lab – 01.

LVS:

To check for the LVS violations, select “**Assura → Run LVS**”, verify the Schematic Design Source and the Layout Design Source, mention a “Run Name”, select “**Technology → gdk045**” and click on “OK” as demonstrated in Lab – 01.

QRC:

To extract the Parasitics, select “**Assura → Quantus**”, select “**Technology → gpk180**”, “**Output → Extracted View**” from the “**Setup**” option, select “**Extraction Type → RC**” and “**Ref Node → VSS**” from the “**Extraction**” and click on “OK” as demonstrated in Lab – 01.

The result can be checked from the Library Manager.

BACKANNOTATION:

Import the parasitics into the Test Schematic and re-run the simulation to check their impact by calculating the delay elements as demonstrated in Lab – 01.

APPENDIX – 1: CHANGING BACKGROUND COLOR IN VIRTUOSO SCHEMATIC EDITOR

To change the background color for the Virtuoso Schematic Editor, select “**Options → User Preferences**” from the Command Interpreter Window as shown in Figure – a.



Figure – a: Options → User Preferences

The “**User Preferences**” window pops up as shown in Figure – b.

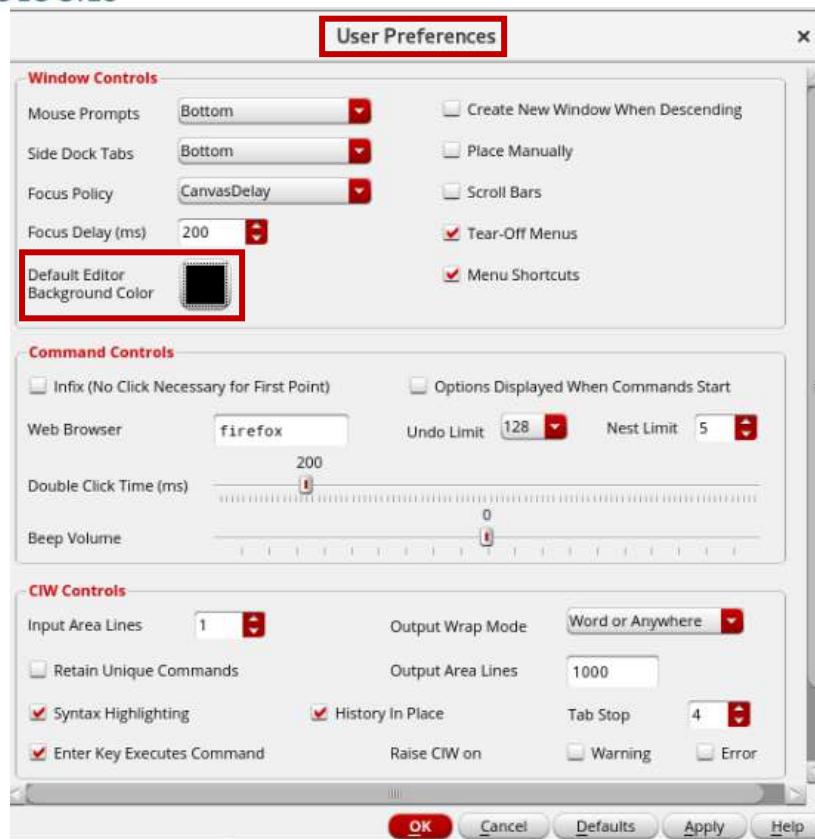


Figure – b: User Preferences window

Click on “Default Editor Background Color” as shown in Figure – b. The “Select Color” window pops up as shown in Figure – c.

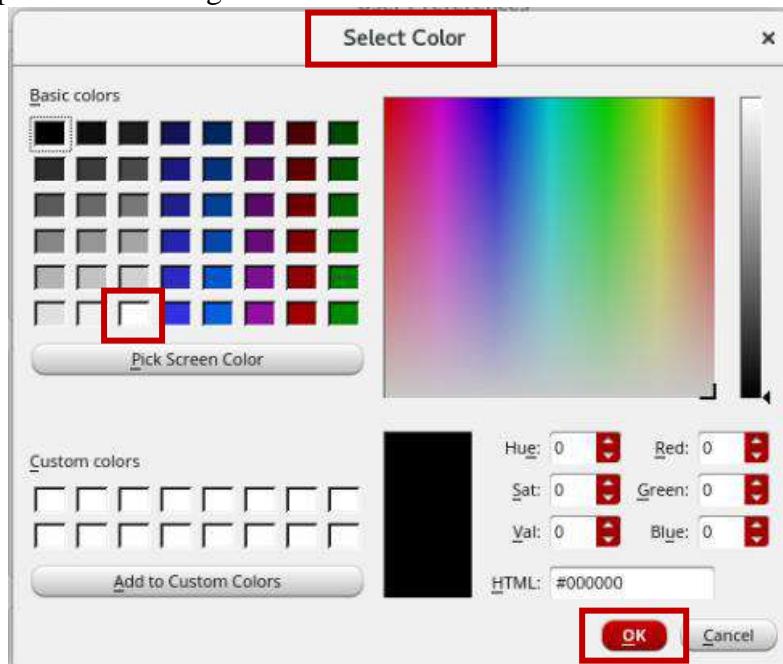


Figure – c: Select Color window

Select the Screen Color of interest and click on “OK” as shown in Figure – c.



Figure – d: Updated User Preferences window

The updated “User Preferences” window can be seen as shown in Figure – d. Click on “Apply” and click on “OK”.

The updated “Virtuoso Schematic Editor L Editing” window can be seen as shown in Figure – e.

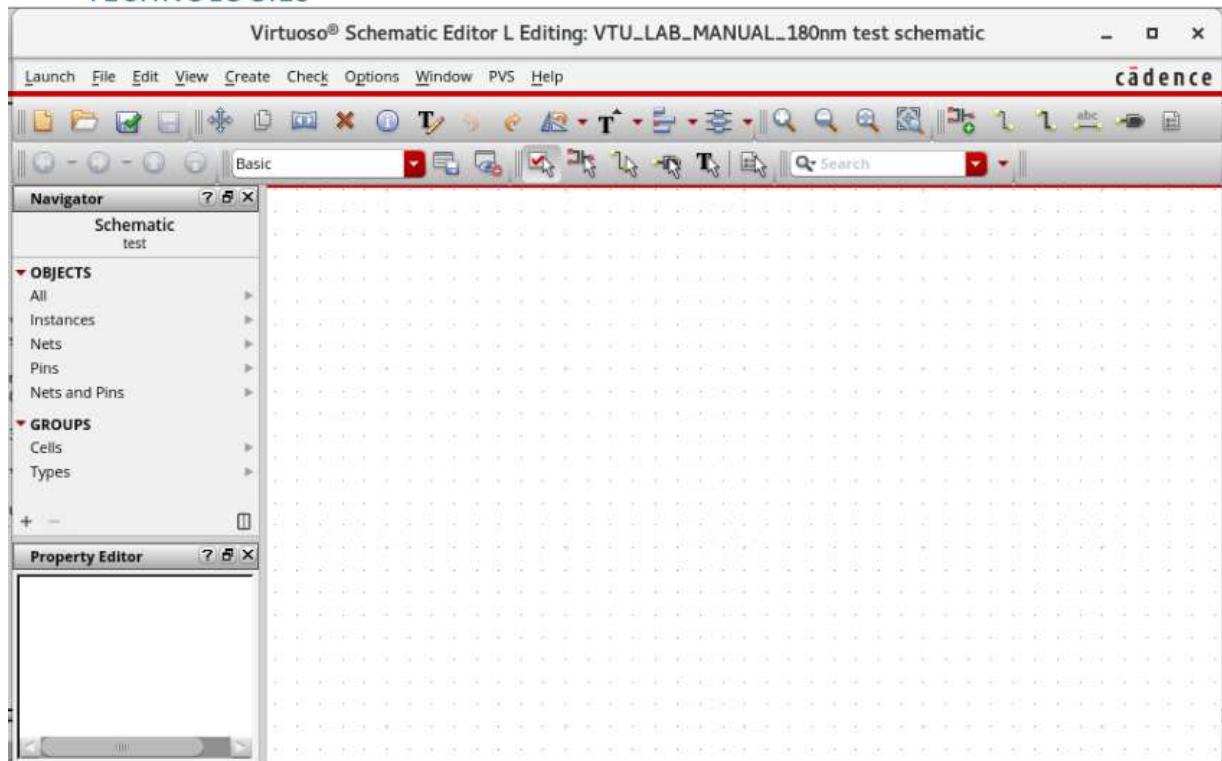


Figure – e: Updated Virtuoso Schematic Editor L Editing window



Support:

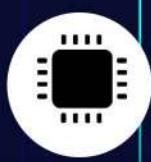
For queries, please drop an email to cadence.support@entuple.com

Training:

For Training requirements, please drop an email to training@entuple.com.

Nurturing Excellence in VLSI

Entuple Training Domains



VLSI



Mechanical



Antenna design



Internet of
Things

● Career Builder Programs

● Internships

● Short Term Programs