ENGR 3430 Miniproject 1 Report: USB-Powered LED Flasher

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1. Overview

The objective of this project was to design a USB-powered LED flasher with a nominal period of 1 s (within ±10%) using a two-layer PCB and only components from the provided parts list. The final design uses a **hysteretic oscillator** implemented with a **Schmitt trigger** and an RC feedback network. This topology was selected because it produces a stable rail-to-rail square wave whose period is analytically predictable and robust to component tolerances.

A dual op-amp package is used. One op-amp implements the hysteretic oscillator, while the second op-amp is used as a buffered mid-supply reference generator.

2. Circuit Explanation

The circuit is a **hysteretic oscillator** based on an noninverting Schmitt trigger. The RC network drives the inverting input of the op-amp, while the noninverting input is set by a resistive linear combiner of V_{ref} and the output voltage V_{out}. Positive feedback causes the output to saturate at one rail or the other, depending on whether the RC node voltage is above or below a threshold.

The output switches state when the inverting input voltage crosses the noninverting input voltage. Due to the positive feedback, this switching occurs at two distinct thresholds: an up-going threshold V_{up} and a down-going threshold V_{dn}.

The circuit is powered from the 5 V USB Type-A VBUS supply, which is regulated down to 3.3 V. This regulated voltage serves as the single-ended supply voltage V_{dd} for the op-amp circuitry.

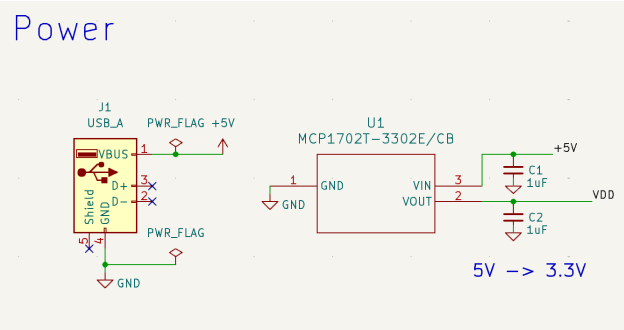

Figure 1: Power input stage showing the 5 V USB Type-A VBUS supply regulated to 3.3 V using a linear regulator. Input and output bypass capacitors (1 µF) are included to ensure regulator stability.

The Schmitt trigger requires a reference voltage V_{ref} at its noninverting input. To generate a stable reference, the second op-amp in the dual package is configured as a buffered voltage rail

splitter, producing $V_{\text{ref}} = \frac{1}{2}V_{\text{dd}}$. This value was chosen as such to center the switching thresholds symmetrically about mid-supply.

Derivation of V_{up} and V_{dn}

In the inverting Schmitt trigger configuration, the noninverting input voltage is set by a two-input resistive linear combiner consisting of V_{ref} and the output voltage V_{out}. This node voltage can be written as

$$V = \frac{G_1}{G_1 + G_2}V_{\text{ref}} + \frac{G_2}{G_1 + G_2}V_{\text{out}}, \tag{1}$$

where G_1 and G_2 are the conductances of the two resistors connected to V_{ref} and V_{out}, respectively.

Expressing this relation in terms of resistor values gives

$$V = \frac{R_2}{R_1 + R_2}V_{\text{ref}} + \frac{R_1}{R_1 + R_2}V_{\text{out}}. \tag{2}$$

The switching thresholds for the inverting input occur when the RC node voltage equals V. When the output is low ($V_{\text{out}} = 0$), the up-going transition threshold is obtained by substituting into Eq. (2):

$$V_{\text{up}} = \frac{R_2}{R_1 + R_2}V_{\text{ref}}. \tag{3}$$

When the output is high ($V_{\text{out}} = V_{\text{dd}}$), the down-going transition threshold becomes

$$V_{\text{dn}} = \frac{R_2}{R_1 + R_2}V_{\text{ref}} + \frac{R_1}{R_1 + R_2}V_{\text{dd}}. \tag{4}$$

In this design, the reference voltage is chosen as $V_{\text{ref}} = \frac{1}{2}V_{\text{dd}}$. Substituting this into Eqs. (3) and (4) yields

$$V_{\text{up}} = \frac{V_{\text{dd}}}{2}\left(\frac{R_2}{R_1 + R_2}\right), \tag{5}$$

$$V_{\text{dn}} = \frac{V_{\text{dd}}}{2}\left(\frac{2R_1 + R_2}{R_1 + R_2}\right). \tag{6}$$

With the additional choice $R_1 = R_2$, the thresholds simplify to

$$V_{\text{up}} = \frac{1}{4}V_{\text{dd}}, \qquad V_{\text{dn}} = \frac{3}{4}V_{\text{dd}}. \tag{7}$$

Under these conditions, the thresholds satisfy

$$V_{\text{dn}} = V_{\text{dd}} - V_{\text{up}}, \tag{8}$$

which results in equal high and low times in steady-state (i.e., $T_h = T_l$) after the initial transient. This symmetry produces a nominal duty cycle of approximately 50% while keeping the oscillation period primarily determined by the RC time constant.

Moreover, the hysteresis window is defined as the difference between the switching thresholds:

$$\Delta V_{\text{hyst}} \equiv V_{\text{dn}} - V_{\text{up}} = \frac{R_1}{R_1 + R_2}V_{\text{dd}}. \tag{9}$$

With the choice $R_1 = R_2$, the hysteresis window simplifies to

$$\Delta V_{\text{hyst}} = \frac{1}{2} V_{\text{dd}}. \tag{10}$$

Period derivation

Low interval (T_l). When the output transitions low ($V_{\text{out}} = 0$), the RC node starts at V_{dn} and exponentially decays toward 0 V:

$$V_n(t) = V_{\text{dn}} e^{-t/\tau}. \tag{11}$$

The next switching event occurs when $V_n(t)$ reaches the up-going threshold V_{up}, so

$$V_{\text{up}} = V_{\text{dn}} e^{-T_l/\tau} \quad \Rightarrow \quad T_l = \tau \ln\left(\frac{V_{\text{dn}}}{V_{\text{up}}}\right). \tag{12}$$

High interval (T_h). When the output transitions high ($V_{\text{out}} = V_{\text{dd}}$), the RC node starts at V_{up} and exponentially rises toward V_{dd}:

$$V_n(t) = V_{\text{dd}} - (V_{\text{dd}} - V_{\text{up}})\, e^{-t/\tau}. \tag{13}$$

The next switching event occurs when $V_n(t)$ reaches the down-going threshold V_{dn}, giving

$$V_{\text{dn}} = V_{\text{dd}} - (V_{\text{dd}} - V_{\text{up}})\, e^{-T_h/\tau} \quad \Rightarrow \quad T_h = \tau \ln\left(\frac{V_{\text{dd}} - V_{\text{up}}}{V_{\text{dd}} - V_{\text{dn}}}\right). \tag{14}$$

Total period. The oscillation period is $T = T_l + T_h$, so combining Eqs. (12) and (14) yields

$$T = \tau \ln\left(\frac{V_{\text{dn}}}{V_{\text{up}}}\right) + \tau \ln\left(\frac{V_{\text{dd}} - V_{\text{up}}}{V_{\text{dd}} - V_{\text{dn}}}\right) = \tau \ln\left(\frac{V_{\text{dn}}}{V_{\text{up}}} \cdot \frac{V_{\text{dd}} - V_{\text{up}}}{V_{\text{dd}} - V_{\text{dn}}}\right). \tag{15}$$

With the design choices $V_{\text{ref}} = \frac{1}{2} V_{\text{dd}}$ and $R_1 = R_2$, the switching thresholds become $V_{\text{up}} = \frac{1}{4} V_{\text{dd}}$ and $V_{\text{dn}} = \frac{3}{4} V_{\text{dd}}$, which also implies $V_{\text{dn}} = V_{\text{dd}} - V_{\text{up}}$ and therefore $T_h = T_l$. Substituting these values into Eq. (15) gives

$$T = \tau \ln\left(\frac{\frac{3}{4} V_{\text{dd}}}{\frac{1}{4} V_{\text{dd}}} \cdot \frac{\frac{3}{4} V_{\text{dd}}}{\frac{1}{4} V_{\text{dd}}}\right) \tag{16}$$

$$= \tau \ln(9) \tag{17}$$

$$= 2\tau \ln(3) \tag{18}$$

$$= 2RC \ln(3) \approx 0.455\,12\,\text{s}. \tag{19}$$

From this expression, the required RC time constant is

$$RC = \frac{T}{2 \ln(3)}. \tag{20}$$

To meet the 1 s period target using components from the provided bill of materials, the capacitor value was chosen as $C = 0.1\,\mu\text{F}$. This capacitor was selected because it has a tighter tolerance

(±5%) compared to other available options with ±10% tolerance, providing greater confidence in meeting the period specification under component variation.

Using $C = 0.1\,\mu\text{F}$, the required resistance is on the order of a few megaohms. Since no single resistor with the exact desired value was available in the parts list, the resistance was implemented using a series combination of resistors. Specifically, $3.01\,\text{M}\Omega$, $1\,\text{M}\Omega$, and $499\,\text{k}\Omega$ resistors were placed in series, yielding an effective resistance of approximately $4.51\,\text{M}\Omega$.

With these values, the resulting period is

$$T = 2RC\ln(3) \approx 2\ln(3)\,(4.51\,\text{M}\Omega)(0.1\,\mu\text{F}) \approx 0.99\,\text{s}, \tag{21}$$

which lies within the ±10% requirement around 1 s.

Lastly, the LED is driven directly by the output of the hysteretic oscillator. A series resistor of $10\,\text{k}\Omega$ is used to limit the LED current and ensure safe operation.

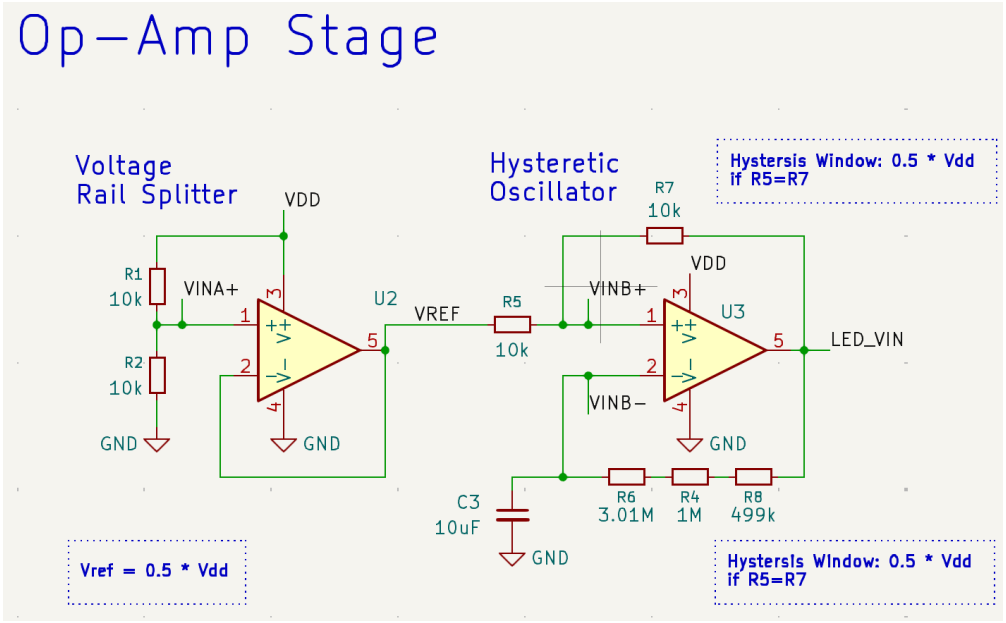

Figure 2: Op-amp stage showing the buffered mid-supply voltage rail splitter that generates V_{ref}, along with the hysteretic oscillator implemented using a Schmitt trigger and RC feedback network.

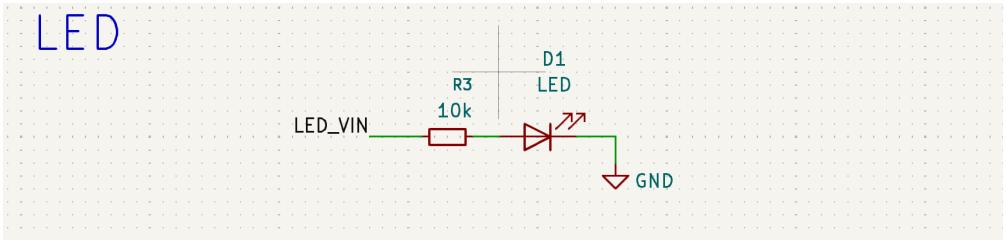

Figure 3: LED Output driven by series resistor.

3. LTspice Simulation Results

LTspice simulations were used to verify the analytical period derivation, confirm proper startup behavior, and evaluate robustness to component tolerances. All simulations were performed using the complete circuit schematic, including the Schmitt trigger, RC feedback network, and buffered reference voltage.

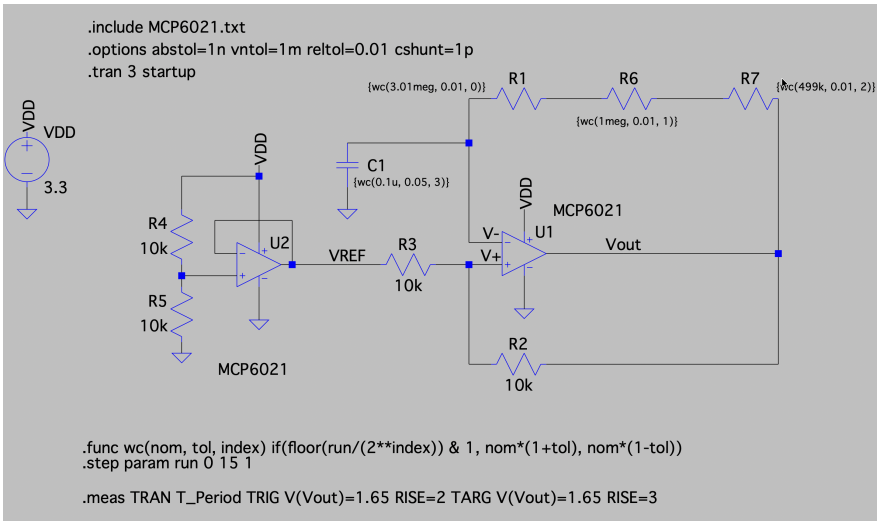

Figure 4: LTSpice Simulation Circuit Schematic

Nominal Transient Simulation

A transient simulation was first performed using the nominal component values ($R \approx 4.51\,\mathrm{M\Omega}$ and $C = 0.1\,\mu\mathrm{F}$). The output waveform exhibits clean rail-to-rail switching and stable oscillation after a brief startup transient. The measured oscillation period from the steady-state waveform agrees closely with the analytical prediction of $T = 2RC\ln(3) \approx 1.0\,\mathrm{s}$.

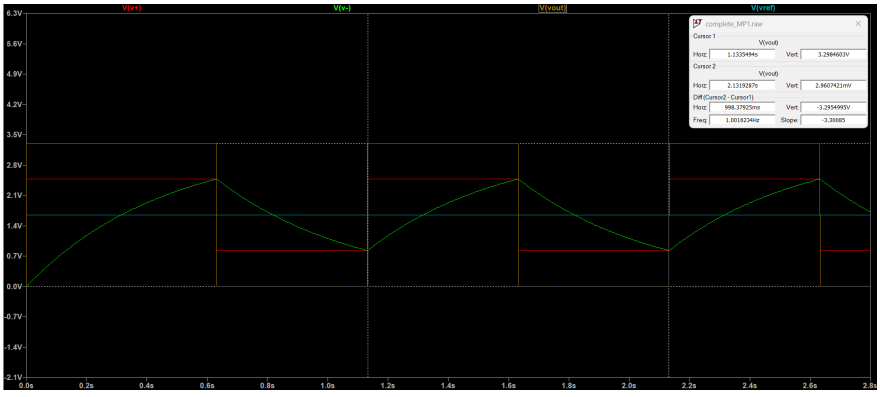

Figure 5: Nominal LTspice transient simulation showing the hysteretic oscillator operation. The RC node voltage exhibits exponential charge and discharge between the Schmitt trigger thresholds, while the output switches rail-to-rail at approximately 1 Hz.

Worst-Case Tolerance Analysis

To evaluate sensitivity to component tolerances, a worst-case analysis was performed by sweeping four components in the RC and hysteresis network across their tolerance extremes, resulting in $2^4 = 16$ corner cases. The fastest and slowest oscillation cases were identified and compared. All 16 simulations produced periods within the required $\pm 10\%$ range around 1 s, demonstrating that the design meets the specification under worst-case component variation.

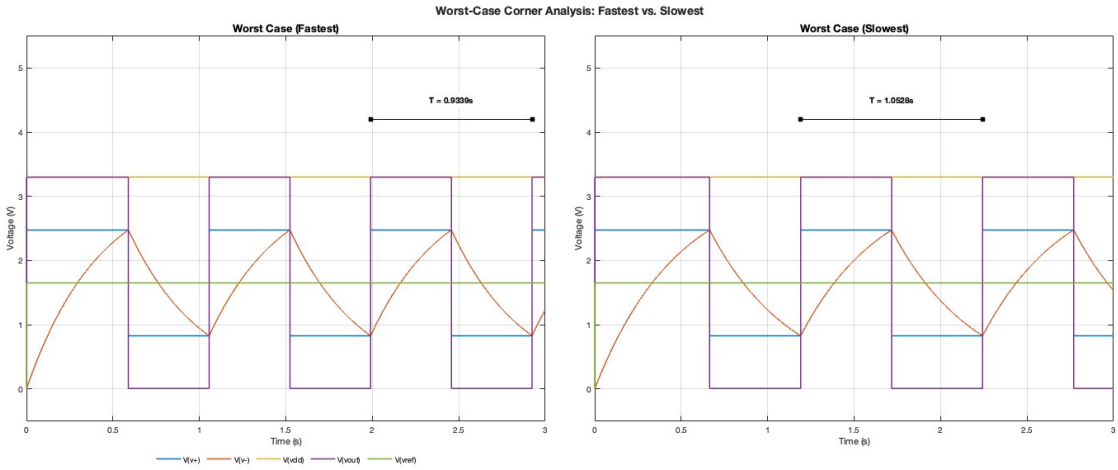

Figure 6: Worst-case corner analysis waveforms corresponding to the fastest and slowest oscillation periods observed across all tolerance combinations. The fastest case yields a period of 0.933 s, while the slowest case yields a period of 1.0528 s. Both cases remain within the $\pm 10\%$ requirement around the 1 s target.

Figure 7: Measured oscillation period for all 16 worst-case tolerance combinations. The shaded region indicates the acceptable $\pm 10\%$ range around the 1 s target. All simulated cases satisfy the period specification.

Monte Carlo Simulation

A Monte Carlo simulation with 500 runs was also performed in which component values were randomly varied within their specified tolerances. The resulting distribution of oscillation periods

shows a tight clustering around the nominal value, with no runs violating the ±10% period requirement. These results provide additional confidence that the oscillator period is robust to realistic component variation.

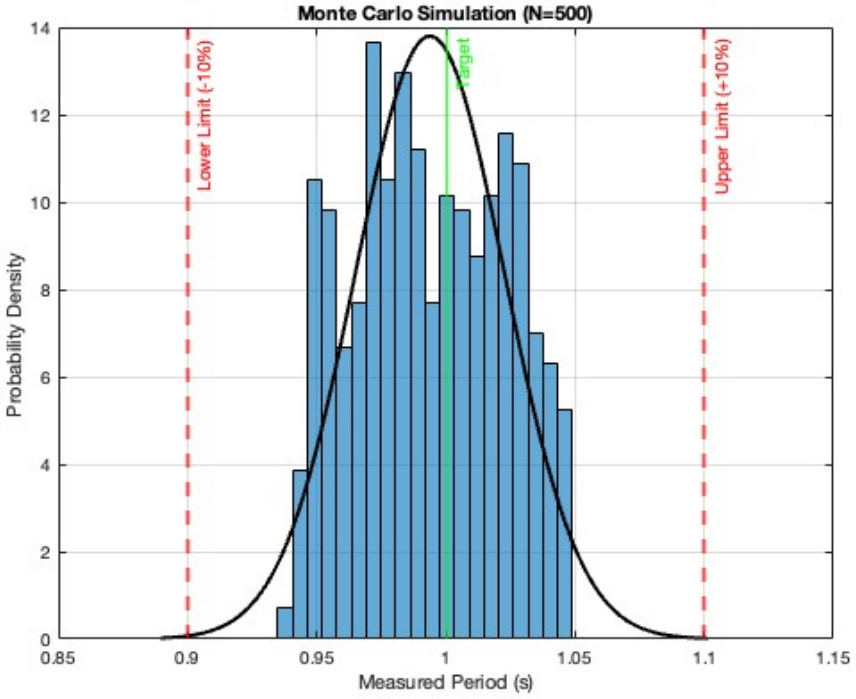

Figure 8: Monte Carlo simulation results for 500 runs with randomized component values within specified tolerances. The distribution of measured periods is centered near the nominal value, and no runs violate the ±10% period requirement.

3. PCB Layout

The PCB was designed as a two-layer board with all components placed on the top layer, in accordance with the project requirements. The layout prioritizes short signal paths for the RC network and Schmitt trigger and local bypass capacitors placed close to the op-amp supply pins. All trace width, spacing, and via dimensions meet the minimum manufacturing constraints specified for this assignment.

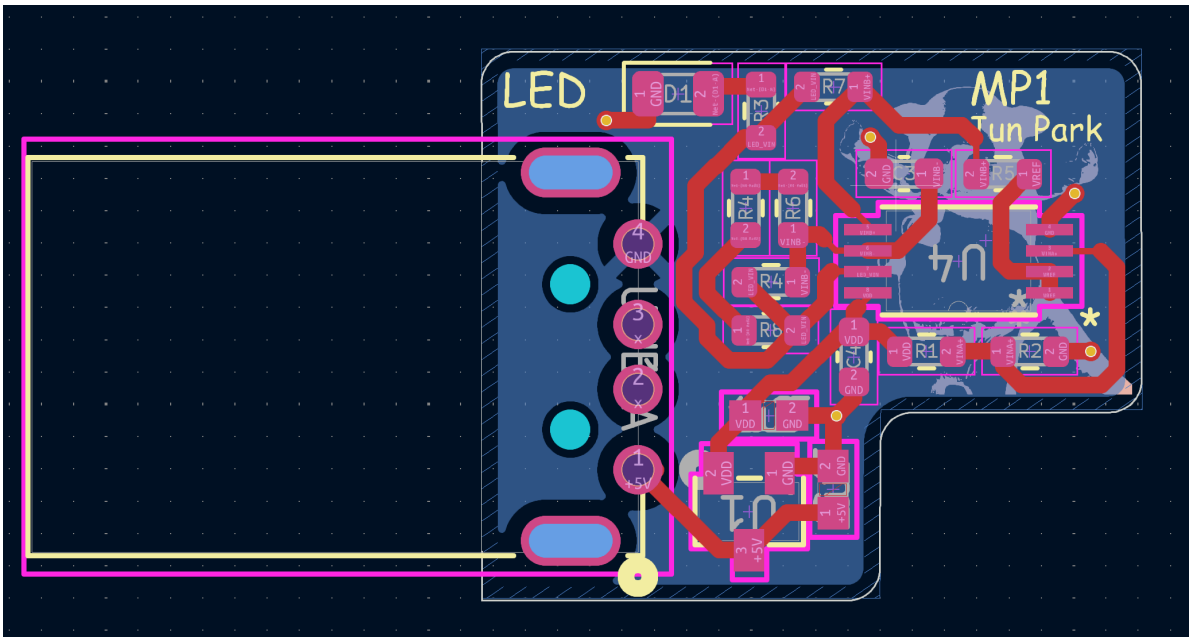

Figure 9: Top-layer PCB layout showing component placement and signal routing. All components are placed on the top layer, and the RC network is routed compactly near the op-amp to minimize parasitic effects.

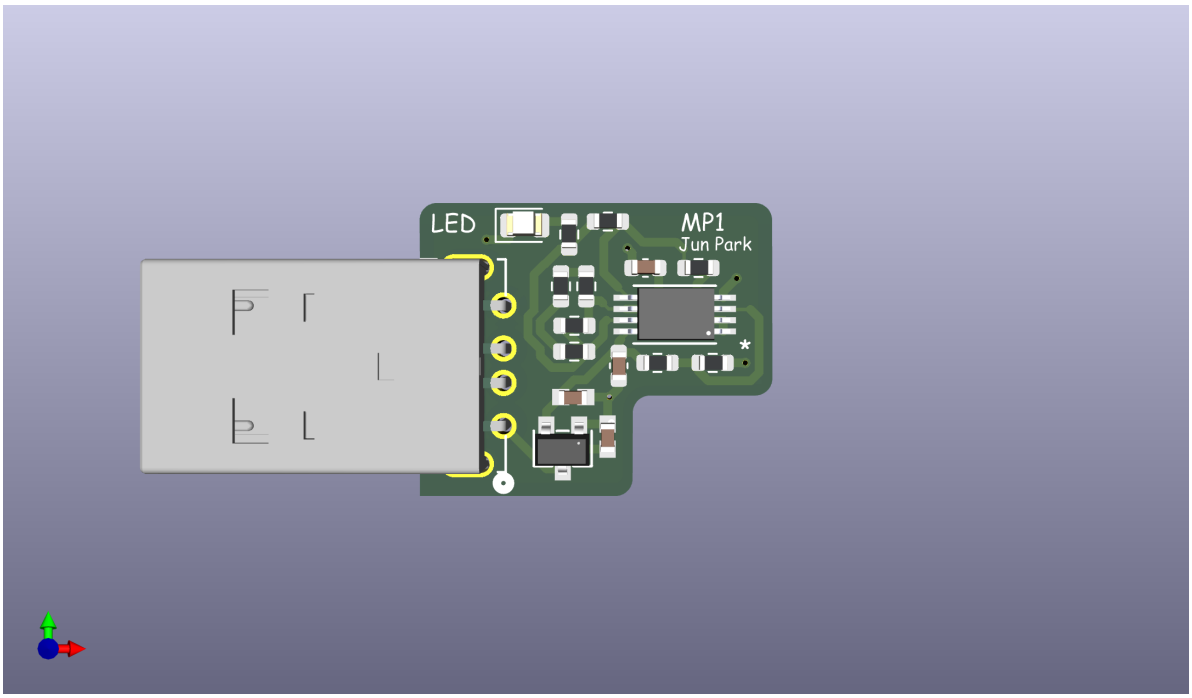

Figure 10: 3D rendering of the final PCB layout generated in KiCad, showing overall component placement and board form factor.