1. How to read this chapter

The contents of this chapter apply to all LPC29xx parts. Available ports depend on the pin configuration for each part.

Table 197. GPIO ports available

Part number	GPIO port 0	GPIO port 1	GPIO port 2	GPIO port 3	GPIO port 4	GPIO port 5	GPIO port 5/ USB
LPC2917/19/01	P0[31:0]	P1[31:0]	P2[27:0]	P3[15:0]	-	-	-
LPC2921/23/25	P0[31:0]	P1[27:0]	-	-	-	-	P5[19:18]
LPC2926/27/29	P0[31:0]	P1[27:0]	P2[27:0]	P3[15:0]	-	-	P5[19:18]
LPC2930	P0[31:0]	P1[27:0]	P2[27:0]	P3[15:0]	P4[23:0]	P5[15:0]	P5[19:16]
LPC2939	P0[31:0]	P1[27:0]	P2[27:0]	P3[15:0]	P4[23:0]	P5[15:0]	P5[19:16]

2. GPIO functional description

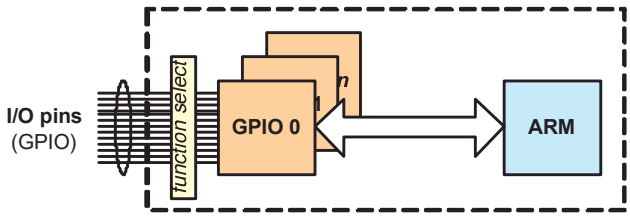

Fig 59. Schematic representation of the GPIO

Each General-Purpose I/O block GPIO provides control over up to 32 port pins. The data direction (in/out) and output level of each port pin can be programmed individually.

If a port pin is to be used it must first be routed to an I/O pin so that it is available externally. This part of the configuration is done via the SCU. See Section 6–3.1 for information on mapping of GPIO port pins to I/O pins. GPIO port pinning can be found in Ref. 31–1.

A number of points should be noted in regard to SCU mapping of GPIO pins:

- If an input port is not mapped through the SCU to an external I/O pin it is assigned a logical 0.
- If an output port is not mapped through the SCU to an external I/O pin it is left dangling; i.e. not connected.

The GPIO pins can also be used in an open-drain configuration. In this configuration, multiple devices can communicate on one signal line in any direction (e.g. bi-directionally).

The signal line is normally pulled up to a HIGH voltage level (logic 1) by an external resistor. Each of the devices connected to the signal line can either drive the signal line to a LOW voltage level (logic 0) or stay at high impedance (open-drain). If none of the devices drives the signal line to a LOW voltage level the signal line is pulled-up by the resistor (logic 1).

Devices in high-impedance can also read the value of the signal line to detect a logic 0 or logic 1. This allows communication in multiple directions.

The open-drain configuration is achieved by:

- Initially:
  - Configuring the pin direction as input (high impedance/open drain).
  - Setting the pin output to a LOW voltage level (logic 0).
- Configuring the pin direction as output to drive a LOW voltage level (logic 0).
- Configuring the pin direction as input to provide an open drain. In this case the other devices and external resistor determine the voltage level. The actual level (logic 0 or logic 1) can be read from the GPIO pin.

3. Register overview

Table 198. Register overview: GPIO (base address: 0xE004 A000 (GPIO0), 0xE004 B000 (GPIO1), 0xE004 C000 (GPIO2), 0xE004 D000 (GPIO3), 0xE004 E000 (GPIO4), 0xE004 F000 (GPIO5))

Name	Access	Address offset	Description	Reset value	Reference
PINS	R	0x0	Port input register	-	Table 16–199
OR	R/W	0x4	Port output register	0x0000 0000	Table 16–200
DR	R/W	0x8	Port direction register	0x0000 0000	Table 16–201

3.1 GPIO port input register

The port input register is used to reflect the synchronized input level on each I/O pin individually. In the case of writing to the port input register, the contents are written into the port output register.

Table 16–199 shows the bit assignment of the PINS register. Bits for for unavailable ports are reserved (see Table 16–197), do not modify, and read as logic 0.

Table 199. PINS register bit description (PINS0 to 5, addresses 0xE004 A000 (GPIO0), 0xE004 B000 (GPIO1), 0xE004 C000 (GPIO2), 0xE004 D000 (GPIO3), 0xE004 E000 (GPIO4), 0xE004 F000 (GPIO5))

Bit	Symbol	Access	Value	Description
31	PINS[31]	R/W	1	Pn[31] input pin is HIGH
			0	Pn[31] input pin is LOW
30:1	...	...	...	...
0	PINS[0]	R/W	1	Pn[0] input pin is HIGH
			0	Pn[0] input pin is LOW

3.2 GPIO port output register

The port output register is used to define the output level on each I/O pin individually if this pin has been configured as an output by the port direction register. If the port input register is written to the port output register is written to as well.

Table 16–200 shows the bit assignment of the OR register. Bits for for unavailable ports are reserved (see Table 16–197), do not modify, and read as logic 0.

Table 200. OR register bit description (OR0 to 5, addresses 0xE004 A004 (GPIO0), 0xE004 B004 (GPIO1), 0xE004 C004 (GPIO2), 0xE004 D004 (GPIO3), 0xE004 E004 (GPIO4), 0xE004 F004 (GPIO5))

** = reset value*

Bit	Symbol	Access	Value	Description
31	OR[31]	R/W	1	If configured as an output, pin Pn[31] is driven HIGH
			0*	If configured as an output, pin Pn[31] is driven LOW
30:1	...	...	...	...
0	OR[0]	R/W	1	If configured as an output, pin Pn[0] is driven HIGH
			0*	If configured as an output, pin Pn[0] is driven LOW

3.3 GPIO port direction register

The port direction register is used to individually control each I/O pin output-driver enable. If the port is configured as input, see Table 6–59 to configure the appropriate pad type.

Table 16–201 shows the bit assignment of the DR register. Bits for for unavailable ports are reserved (see Table 16–197), do not modify, and read as logic 0.

Table 201. DR register bit description (DR0 to 5, addresses 0xE004 A008 (GPIO0), 0xE004 B008 (GPIO1), 0xE004 C008 (GPIO2), 0xE004 D008 (GPIO3), 0xE004 E008 (GPIO4), 0xE004 F008 (GPIO5))

** = reset value*

Bit	Symbol	Access	Value	Description
31	DR[31]	R/W	1	Pin Pn[31] is configured as an output
			0*	Pin Pn[31] is configured as an input
30:1	...	...	...	...
0	DR[0]	R/W	1	Pin Pn[0] is configured as an output
			0*	Pin Pn[0] is configured as an input