Project: StreetRacer CPU Card

VERSION	REVISION	DATE	DESCRIPTION	NAME
0.1	A	07-06-2003	Initial Design Created	R. Bauer
0.2	A	07-18-2003	Preliminary Design	M. Daroy
0.3	A	07-31-2003	Updated based on Design Review (07-29-2003).	M. Daroy
0.4	A	08-01-2003	Changed J7 to SIP4 Header.	M. Daroy
0.5	A	08-06-2003	Reduced the FLASH Memory Option to just the INTEL Strata FLASH to avoid the difficulty of routing in PCB CAD Design. U7 and U8 (the entire AMD FLASH Memory Option page) was deleted.	M. Daroy
		08-21-2003	Released for PCB Fabrication.	M. Daroy
1.0	B	09-26-2003	Added pull-up resistors on the FPGA Configuration signals. Added pull-up resistor on the CF Socket Select signal. Added Delay Circuit on the FPGA VCCO inputs for Banks 0, 6 and 7 to implement proper FPGA Power-up Sequence.	M. Daroy
2.0	C	06-23-2004	Changed resistor values on R15 thru R20 and R89. Deleted C100 and C101.	M. Daroy
2.1	C	06-25-2004	Marked the DNI (Do Not Install) Parts for Assembly BOM generation. Added Mounting Hole connection to the Ground Plane.	M. Daroy

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NOTES

1. Components marked with a dashed and crossed box will not be installed during assembly.

2. Please refer to the Bill of Material (BOM) which provides all necessary component information for the final assembly.

3. The following parameters will apply to all components unless otherwise stated in the BOM or Schematic.

    Resistor: +/- 5% or better, 1/16 Watt, 0603

    Capacitor, non - polarized: Ceramic, +/- 20%, 0603

    Capacitor, polarized: Tantalum, +/- 20%

    Inductance: +/- 10%
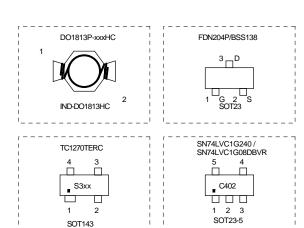
4. Bypass capacitors shall be distributed evenly amongst power pins of the IC power and GND pin.

5. Always observe layout guidelines and documentation from the component manufacturers

Schematic Statistics:

Parts:	00
Library Parts:	00
Nets:	00
Pins:	00

LAST REFERENCES USED

REF.	Last used	Not used
ANT	n/a	n/a
BR	n/a	n/a
BT	n/a	n/a
C	C140	C100,C101
CN	n/a	n/a
CON	n/a	n/a
D	n/a	n/a
F	n/a	n/a
FB	FB4	n/a
FL	n/a	n/a
J	J7	n/a
JP	JP1	n/a
K	n/a	n/a
L	L1	n/a
LED	n/a	n/a
M	n/a	n/a
P	n/a	n/a
PB	n/a	n/a
Q	Q6	n/a
R	R110	n/a
RN	RN7	n/a
SW	SW1	n/a
T	n/a	n/a
TP	TP6	n/a
U	U21	U7,U8
X	X1	n/a
XP	XP1	n/a
Y	Y2	n/a

DO1813P-xxxHC
IND-DO1813HC

FDN204P/BSS138
3 D
1 G 2 S
SOT23

TC1270TERC
4 3
S3xx
1 2
SOT143

SN74LVC1G240 / SN74LVC1G08DBVR
5 4
C402
1 2 3
SOT23-5

STREETRACER CPU CARD TITLE PAGE

DWN: Mario Daroy		
ENG: Mario Daroy		
REV: C	DWG. SIZE C	
DATE: Friday, June 25, 2004	TITLE	StreetRacer CPU Card
SHEET 1 of 10	DWG. No.	ST008-01-01B
Vytek Confidential and Proprietary	12670 High Bluff Drive, San Diego CA 92130-2013	

PXA255 ADDR/DATA/CONTROL

U1A — Intel PXA255 Processor
Address and Data Buses
GDPXA255A0400

[Sht 3,4,5,6,7,8,10] VCC3.3V

[Sht 4,5,8,10] XS_A[0..25]

XS_D[0..31] [Sht 4,5,8,10]

Resistor networks / values:
- RN1, RN2, RN3, RN4, RN5, RN6, RN7 — 22 Ohm
- R1 4.7K, R2 4.7K
- R3 1.5K
- R9 100K DNI, R11 100K DNI, R10 27.4 Ohm 1%, R12 27.4 Ohm 1%
- R13 100K, R14 100K
- R4 10K, R5 10K, R6 10K, R7 10K, R8 10K, R96 10K
- R15 43 Ohm, R16 43 Ohm
- R17 22 Ohm, R18 22 Ohm
- R19 43 Ohm, R20 43 Ohm

Address bus (XS_A0 … XS_A25) → A_0 … A_25

Data bus (XS_D0 … XS_D31) → D_0 … D_31

I2C: XS_I2C_SCL (SCL, D11), XS_I2C_SDA (SDA, A11) [Sht 9]

USB Ch: USB_DPU [Sht 3], USB_UDCP [Sht 7,9], USB_UDCN [Sht 7,9]; XS_USB_UDCP (UDCP, C12), XS_USB_UDCN (UDCN, B12)

IrDA Ch: XS_ST_TXD (IR_TXD_GPIO47, C15), XS_ST_RXD (IR_RXD_GPIO46, B15) [Sht 9]

BT Ch: XS_BT_RTS (BT_RTS_GPIO45, B14), XS_BT_CTS (BT_CTS_GPIO44, A15), XS_BT_TXD (BT_TXD_GPIO43, D13), XS_BT_RXD (BT_RXD_GPIO42, B13) [Sht 7]

SSP Ch: XS_SSP_EXTCLK (EXTCLK_GPIO27, B9), XS_SSP_SFRM (SFRM_C_GPIO24, E9), XS_SSP_SCLK (SCLK_C_GPIO23, D9), XS_SSP_TXD (TXD_C_GPIO25, D9), XS_SSP_RXD (RXD_C_GPIO26, A9) [Sht 8,9]

MMC: XS_MMC_CMD (MMCCMD, D14), XS_MMC_DAT (MMCDAT, B16), XS_CF_RESET (MMCCLK_GPIO6, H14), CF_CD1_N (MMCCS0_GPIO8, F14), CF_CD2_N (MMCCS1_GPIO9, F12) [Sht 10]

FF Ch: XS_FF_RI (FF_RI_GPIO38, R10), XS_FF_DCD (FF_DCD_GPIO36, A12), XS_FF_DSR (FF_DSR_GPIO37, B11), XS_FF_DTR (FF_DTR_GPIO40, F10), XS_FF_RTS (FF_RTS_GPIO41, F8), XS_FF_CTS (FF_CTS_GPIO35, A14), XS_FF_TXD (FF_TXD_GPIO39, E13), XS_FF_RXD (FF_RXD_GPIO34, A13) [Sht 8,9]

CARD Interface: XS_CI_POE_N (nPOE_GPIO48, P13), XS_CI_PWE_N (nPWE_GPIO49, T14), XS_CI_PIOR_N (nPIOR_GPIO50, T15), XS_CI_PIOW_N (nPIOW_GPIO51, R15), XS_CI_PCE_1_N (nPCE_1_GPIO52, P14), XS_CI_PCE_2_N (nPCE_2_GPIO53, R16), XS_CI_PSKTSEL (PSKTSEL_GPIO54, P16), XS_CI_PREG_N (nPREG_GPIO55, M13), XS_CI_WAIT_N (nPWAIT_GPIO56, N16), XS_CI_IOIS16_N (nIOIS16_GPIO57, M16) [Sht 8,10]

NSSP: XS_NSSP_RXD (NSSP_TXD_RXD_GPIO84, D16), XS_NSSP_TXD (NSSP_TXD_RXD_GPIO83, F15), XS_NSSP_FRAME (NSSP_FRAME_GPIO82, E16), XS_NSSP_CLK (NSSP_CLK_GPIO81, F16) [Sht 9]

Memory Control:
- nCS_0, XS_CS0_N (nCS_1_GPIO15 N8/T8) [Sht 5]
- XS_CS1_N (nCS_2_GPIO78, P9) [Sht 8]
- XS_CS2_N (nCS_3_GPIO79, T9) [Sht 8]
- XS_CS3_N (nCS_4_GPIO80, R13) [Sht 8]
- XS_CS4_N (nCS_5_GPIO33, T13) [Sht 8]
- XS_CS5_N [Sht 8]
- XS_DQM_0 (DQM_0, M8) [Sht 4,8]
- XS_DQM_1 (DQM_1, B1) [Sht 4,8]
- XS_DQM_2 (DQM_2, B2) [Sht 4,8]
- XS_DQM_3 (DQM_3, L7) [Sht 4,8]
- XS_SDCS0_N (nSDCS_0, F1), nSDCS_1 (G6), nSDCS_2 (G3), nSDCS_3 (F2) [Sht 4]
- XS_SDCKE_0 (SDCKE_0, E4), XS_SDCKE_1 (SDCKE_1, E3) → SDCKE_0 [Sht 8], SDCKE_1 [Sht 4]
- XS_SDCLK_0 (SDCLK_0, D2), XS_SDCLK_1 (SDCLK_1, F5), SDCLK_2 (D1) → SDCLK_0 [Sht 5,8], SDCLK_1 [Sht 4]
- XS_SDRAS_N (nSDRAS, E1), XS_SDCAS_N (nSDCAS, F3) → SDRAS_N [Sht 4], SDCAS_N [Sht 4,5]
- XS_OE_N (nOE, G5), XS_WE_N (nWE, G4) → XS_OE_N [Sht 5,8], XS_WE_N [Sht 4,5]
- XS_RD_WR_N (RD_nWR, D3), XS_RDY (RDY_GPIO18, C1) → XS_RD_WR_N [Sht 8], XS_RDY [Sht 5,8]
- XS_DREQ_0 (DREQ_0_GPIO20, N12), XS_DREQ_1 (DREQ_1_GPIO19, N14) → [Sht 8], [Sht 8]

AC97: XS_AC97_RST_N (nAC97_RESET, D10), XS_AC97_SYNC (SYNC_GPIO31, E11), XS_AC97_SDOUT (SDATA_OUT_GPIO30, A10), XS_AC97_SDIN0 (SDATA_IN0_GPIO29, E10), XS_AC97_BITCLK (BITCLK_GPIO28, C9), XS_AC97_SDIN1 (SDATA_IN1_GPIO32, A16) [Sht 8]

P.W.: XS_PWM0 (PWM_0_GPIO16, E12), XS_PWM1 (PWM_1_GPIO17, D12) [Sht 8]

VCC3.3V

VYTEK

PXA255 POWER/CLOCK/GPIO

U1B — Intel PXA255 Processor

NATIVE LCD CONNECTOR

PXA255 BOOT CONFIGURATION

BOOT FROM ...	Sel2	Sel1	Sel0	Rbs6	Rbs5	Rbs4	Rbs3	Rbs2	Rbs1
Async. 32bit ROM	L	L	L	100K	DNI	100K	DNI	100K	DNI
Async. 16bit ROM	L	L	H	100K	DNI	100K	DNI	DNI	100K
RESVD	L	H	L	100K	DNI	DNI	100K	100K	DNI
RESVD	L	H	H	100K	DNI	DNI	100K	DNI	100K
32/16bit Sync Mask ROM 64 or 32 Mbit each	H	L	L	DNI	100K	100K	DNI	100K	DNI
16bit Sync Mask ROM 64Mbit	H	L	H	DNI	100K	100K	DNI	DNI	100K
16bit Sync Mask ROMs 64Mbit, 64Mbit each	H	H	L	DNI	100K	DNI	100K	100K	DNI
16bit Sync Mask ROMs 32Mbit	H	H	H	DNI	100K	DNI	100K	DNI	100K

Layout:
Place capacitors next to Core — Capacitors for Core

Layout:
Place capacitors next to VDDX — Capacitors for VDDX

BOOT_SEL 0
BOOT_SEL 1
BOOT_SEL 2

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REV: C
DWG. SIZE: C
DATE: Friday, June 25, 2004
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SDRAM BANK0

SDRAM OPTIONS

MEMORY SIZE		SDRAM MODULES	Rsd1 Rsd3 Rsd5	Rsd2 Rsd4
16MB	64 Mbit x 2	MT48LC4M16A2TG-75	DNI	0.0 ohm
32MB	128 Mbit x 2	MT48LC8M16A2TG-75	DNI	0.0 ohm
64MB	256 Mbit x 2	MT48LC16M16A2TG-75	0.0 ohm	DNI
64MB	256 Mbit x 2	K4S561632C-TC/L75	0.0 ohm	DNI

VCC3.3V

[Sht 2,3,5,6,7,8,10] VCC3.3V

[Sht 2,5,8,10] XS_A[0..25]

XS_A[0..25]

XS_D[0..31] [Sht 2,5,8,10]

Rsd1 XS_A22 R29 0.0 Ohm SD_A12
Rsd2 XS_A22 R30 DNI
Rsd3 XS_A23 R98 0.0 Ohm SD_BA0
Rsd4 XS_A23 R99 DNI
Rsd5 XS_A24 R100 0.0 Ohm SD_BA1

U3 MT48LC16M16A2TG-75

Pin	Signal		Pin	Signal
23	A0	DQ0	2	XS_D0
24	A1	DQ1	4	XS_D1
25	A2	DQ2	5	XS_D2
26	A3	DQ3	7	XS_D3
29	A4	DQ4	8	XS_D4
30	A5	DQ5	10	XS_D5
31	A6	DQ6	11	XS_D6
32	A7	DQ7	13	XS_D7
33	A8	DQ8	42	XS_D8
34	A9	DQ9	44	XS_D9
22	A10	DQ10	45	XS_D10
35	A11	DQ11	47	XS_D11
36	A12	DQ12	48	XS_D12
40	NC	DQ13	50	XS_D13
20	BA0	DQ14	51	XS_D14
21	BA1	DQ15	53	XS_D15

XS_A10..XS_A21, SD_A12, SD_BA0, SD_BA1

XS_SDCAS_N 17 CAS
XS_SDRAS_N 18 RAS
XS_SDCS0_N 19 CS   VDD 1
XS_WE_N 16 WE   VDD 14
XS_DQM_1 39 DQMH   VDD 27
XS_DQM_0 15 DQML
XS_SDCLK_1 38 CLK
XS_SDCKE_1 37 CKE

28 VSS
41 VSS
54 VSS

6 VSSQ   VDDQ 3
12 VSSQ VDDQ 9
46 VSSQ VDDQ 43
52 VSSQ VDDQ 49

VCC3.3V

[Sht 2,8] XS_DQM_1
[Sht 2,8] XS_DQM_0

C25 0.01uF   C26 0.01uF   C27 0.01uF   C28 2700pF   C29 2700pF   C30 2700pF   C24 22uF, TANT

U4 MT48LC16M16A2TG-75

Pin	Signal		Pin	Signal
23	A0	DQ0	2	XS_D16
24	A1	DQ1	4	XS_D17
25	A2	DQ2	5	XS_D18
26	A3	DQ3	7	XS_D19
29	A4	DQ4	8	XS_D20
30	A5	DQ5	10	XS_D21
31	A6	DQ6	11	XS_D22
32	A7	DQ7	13	XS_D23
33	A8	DQ8	42	XS_D24
34	A9	DQ9	44	XS_D25
22	A10	DQ10	45	XS_D26
35	A11	DQ11	47	XS_D27
36	A12	DQ12	48	XS_D28
40	NC	DQ13	50	XS_D29
20	BA0	DQ14	51	XS_D30
21	BA1	DQ15	53	XS_D31

[Sht 2,5] SDCAS_N 17 CAS
[Sht 2] SDRAS_N 18 RAS
[Sht 2] XS_SDCS0_N 19 CS   VDD 1
[Sht 2,5] XS_WE_N 16 WE   VDD 14
[Sht 2,8] XS_DQM_3 39 DQMH   VDD 27
[Sht 2,8] XS_DQM_2 15 DQML
[Sht 2] SDCLK_1 38 CLK
[Sht 2] SDCKE_1 37 CKE

28 VSS
41 VSS
54 VSS

6 VSSQ   VDDQ 3
12 VSSQ VDDQ 9
46 VSSQ VDDQ 43
52 VSSQ VDDQ 49

VCC3.3V

C32 0.01uF   C33 0.01uF   C34 0.01uF   C35 2700pF   C36 2700pF   C37 2700pF   C31 22uF, TANT

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DWN: Mario Daroy
ENG: Mario Daroy
REV: C   DWG. SIZE C
DATE: Friday, June 25, 2004
SHEET 4 of 10   DWG. No. ST008-01-01B
TITLE StreetRacer CPU Card

VYTEK

Vytek Confidential and Proprietary   12670 High Bluff Drive, San Diego CA 92130-2013

FLASH MEMORY MODULE OPTIONS

MEMORY SIZE		FLASH MODULES
16MB	64 Mbit x 2	RC/E28F640J3A
32MB	128 Mbit x 2	RC/E28F128J3A
64MB	256 Mbit x 2	RC28F256K3C

FLASH MEMORY CONFIGURATION RESISTORS

Resistor	J3	K3
Rflsh1	0 ohm	DNI
Rflsh2	0 ohm	DNI
Rflsh3	DNI	0 ohm
Rflsh4	DNI	0 ohm
Rflsh5	10K	DNI
Rflsh6	10K	DNI
Rflsh7	DNI	0 ohm
Rflsh8	DNI	0 ohm
Rflsh9	DNI	10K
Rflsh10	DNI	0 ohm

Resistor	J3-Async	K3-Async	K3-Sync
Rflsh11	DNI	DNI	0 ohm
Rflsh12	DNI	DNI	0 ohm
Rflsh13	DNI	10K	DNI
Rflsh14	DNI	10K	DNI

Note: A0 input buffer is turned off if BYTE# is high.

POPULATE the FLASH MEMORY MODULES (either the BGA [RC28F] or TSOP [E28F]) only. See OPTION and Resistor Configuration Table.

For 16-bit FLASH MEMORY Configuration, populate ONLY the MODULE with the Lower Data Bits (D0 to D15) . Check PXA255 BOOT CONFIGURATION on page 3.

FLASH MEMORY

DWN: Mario Daroy
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REV: C
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VYTEK

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VCC3.3V

VCC3.3V

VCC3.3V   [Sht 2,3,4,5,7,8,10]

Power Monitor
TP1 Red Testpoint   TP2 Red Testpoint

[Sht 3] XS_PWR_EN

R46   100K

U9
1 RUN	PLL LPF 8
2 ITH	SYNC / MODE 7
3 VFB	VIN 6
4 GND	SW 5
LTC1878EMS8

XS_PWR_EN
ITH
VFB

C62 220pF

Mounting Holes

M1 .125	1	M4 .125	1
M2 .125		M5 .125	1
M3 .125	1		

X1   DNI

L1   6.8uH

VSW   VOUT1   **Vout1 = 0.8V (1 + RB/RA)**

C63 22uF, TANT

C64 20pF

R48 374K, 1%
(RB)

C65 47uF

C66 0.1uF

R47   0.10 Ohm   VCCCORE   VCCCORE [Sht 3]

500mA max.

1.5V CPU CORE VOLTAGE REGULATOR

Layout:
Please refer to suggested Layout on the Datasheet of LTC1878.

R49 392K, 1%
(RA)

Ground Test Points
TP3 Black Testpoint   TP4 Black Testpoint

Power Monitor
TP5 Red Testpoint   TP6 Red Testpoint

Q1 FDN304P

V3.3V_IN
+3.3 V DC
1600 mA min.
Ramp Time < 2 ms

[Sht 9,10] V3.3V_IN

FB1   3A, 0.012 DCR

VCC3.3V

U10
3 VIN	VOUT1 2
	VOUT2 1
	ADJ
LM1086CSX-ADJ

VOUT2   **Vout2 = 1.25V (1 + RD/RC)**

C70 0.1uF   C71 0.1uF   C67 10uF

C68 0.1uF

R50   0.10 Ohm   V1.8V

C69 10uF

R53 2.2K

1.8V FPGA CORE VOLTAGE REGULATOR

VCCINT [Sht 7]

500mA max.

VADJ   **(RC)**
R51 147 Ohm, 1%

R52 68.1 Ohm, 1%   **(RD)**

C72 47uF

J5   DNI
| 1 | |
| 2 | |
2X1 0.1"

VCC3.3V

Q2 FDN304P

C73 10uF

R54 22K

VCCFPGA [Sht 7]

Q4 FDN304P

VCCFPGA_B0 [Sht 7]

C138 10uF

R108 22K

Q5 FDN304P

VCCFPGA_B6 [Sht 7]

C139 10uF

R109 22K

Q6 FDN304P

VCCFPGA_B7 [Sht 7]

C140 10uF

R110 22K

Rev. B   V.1.0

[Sht 3] VCC_BANK0
[Sht 3] VCC_BANK6
[Sht 3] VCC_BANK7

MANUAL RESET

SW1
| 1 | 2 |
| 3 | 4 |
EVQ-PHP03T

MRESET

VCC3.3V

U11
| 4 VCC | RESET 2 |
| 3 MR | GND 1 |
TC1270TERC

Reset when VCC < 3.08V

uP RESET SUPERVISOR

HRESET

VCC3.3V
R55 100K

VCC3.3V
R56 100K

VCC3.3V
U12
SN74LVC1G240

RST_CPU_N   RST_CPU_N [Sht 3,7]

Reset Active Time > 250ms

VCC3.3V
U13
SN74LVC1G240

JTAG_RST_N   JTAG_RST_N [Sht 7]

POWER/RESET

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REV: C	DWG. SIZE C	
DATE: Friday, June 25, 2004	TITLE	StreetRacer CPU Card
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VYTEK

JTAG/TEST UART/FPGA POWER

BTUART — U14 MAX3225CAP

DEBUG UART — J1, 4X2 0.1"

USB TYPE B — J7, 4X1 0.1"

CPU JTAG PORT — J2, 10X2 0.1"

FPGA JTAG PORT — J3, 6X1 0.1"

U15B — XC2S400E-6FT256C

JTAG CONFIGURATION JUMPERS

Jumper	Separate	Chain
JP1 (1)	Install	DNI
JP1 (2)	DNI	Install
JP1 (3)	DNI	Install
JP1 (4)	DNI	Install
JP1 (5)	DNI	Install

FPGA PROGRAMMING MODE CONFIGURATION

Resistor	Slave Parallel	Slave Serial
Rfp1	DNI	10K
Rfp2	10K	DNI

Net labels (left side):
- [Sht 2,3,4,5,6,8,10] VCC3.3V
- [Sht 2] XS_BT_TXD
- [Sht 2] XS_BT_RXD
- [Sht 2] XS_BT_CTS
- [Sht 2] XS_BT_RTS
- [Sht 3] USB_DWAKE
- [Sht 2,9] USB_UDCP
- [Sht 2,9] USB_UDCN
- [Sht 6] JTAG_RST_N
- [Sht 3] XS_JTAG_TRST_N
- [Sht 3] XS_JTAG_TDI
- [Sht 3] XS_JTAG_TMS
- [Sht 3] XS_JTAG_TCK
- [Sht 3] XS_JTAG_TDO
- [Sht 3,6] RST_CPU_N
- [Sht 6] VCCFPGA
- [Sht 3] FPGA_PROG
- [Sht 3] FPGA_DONE
- [Sht 3] FPGA_CCLK
- [Sht 6] VCCFPGA_B0
- [Sht 6] VCCFPGA_B6
- [Sht 6] VCCFPGA_B7
- [Sht 6] VCCINT

Rev. B V.1.0 / Rev. C / V.2.0

SPARTAN IIE FPGA

XC2S400E-6FT256C

Rev. B V.1.0

R106 10K

VCC3.3V

VYTEK

DIMM168 CARD EDGE

XP1 — 168 DIMM CARD EDGE

Pin	Signal		Pin	Signal
1	VSS		85	EB_85
2	EB_2		86	EB_86
3	EB_3		87	EB_87
4	VDD		88	VSS
5	EB_5		89	EB_89
6	EB_6		90	EB_90
7	EB_7		91	VDD
8	VSS		92	EB_92
9	EB_9		93	EB_93
10	EB_10		94	EB_94
11	EB_11		95	VSS
12	VSS		96	EB_96
13	EB_GCK3_13		97	VCC_BANK0
14	VSS		98	EB_98
15	EB_15		99	VSS
16	VCC_BANK7		100	EB_100
17	EB_17		101	EB_101
18	EB_18		102	VDD
19	VSS		103	EB_103
20	EB_20		104	EB_104
21	EB_21		105	VSS
22	VDD		106	EB_106
23	EB_23		107	EB_107
24	EB_24		108	VDD
25	VSS		109	EB_109
26	EB_26		110	EB_110
27	EB_27		111	VSS
28	VDD		112	EB_112
29	EB_29		113	EB_113
30	EB_30		114	VDD
31	VSS		115	EB_115
32	EB_32		116	VSS
33	VDD		117	EB_117
34	EB_34		118	VSS
35	VSS		119	EB_119
36	EB_36		120	VDD
37	VDD		121	VCC_BANK7
38	EB_38		122	VSS
39	VDD		123	EB_123
40	EB_40		124	EB_124
41	EB_41		125	VDD
42	VSS		126	EB_126
43	EB_43		127	EB_127
44	EB_44		128	VSS
45	VSS		129	EB_129
46	EB_46		130	EB_130
47	EB_47		131	VDD
48	VDD		132	EB_132
49	EB_49		133	EB_133
50	EB_50		134	VSS
51	VSS		135	EB_135
52	EB_52		136	EB_136
53	VCC_BANK6		137	VCC_BANK6
54	EB_54		138	VSS
55	EB_55		139	EB_139
56	VSS		140	EB_140
57	EB_57		141	EB_141
58	EB_58		142	VDD
59	EB_59		143	EB_143
60	VDD		144	EB_144
61	EB_61		145	EB_145
62	EB_62		146	VSS
63	EB_63		147	EB_GCK1_147
64	VSS		148	RESET_OUT_N
65	XS_GPIO0		149	XS_GPIO1
66	XS_GPIO2		150	VDD
67	XS_GPIO3		151	XS_GPIO4
68	VSS		152	XS_ST_RXD
69	XS_ST_TXD		153	VSS
70	XS_I2C_SCL		154	XS_I2C_SDA
71	VSS		155	USB_UDCP
72	USB_UDCN		156	VDD
73	XS_NSSP_FRAME		157	XS_NSSP_CLK
74	VDD		158	XS_NSSP_RXD
75	XS_NSSP_TXD		159	VSS
76	EB_XS_SSP_TXD_76		160	EB_XS_SSP_RXD_160
77	VSS		161	EB_XS_SSP_SFRM_161
78	EB_XS_SSP_EXTCLK_78		162	EB_XS_SSP_SCLK_162
79	EB_XS_FF_RI_79		163	VDD
80	EB_XS_FF_DSR_80		164	EB_XS_FF_DCD_164
81	VDD		165	EB_XS_FF_DTR_165
82	EB_XS_FF_RTS_82		166	VSS
83	XS_FF_TXD		167	EB_XS_FF_CTS_167
84	VSS		168	XS_FF_RXD

Left net labels:
[Sht 8] FPGA-E7, FPGA-C7, FPGA-B6, FPGA-A5, FPGA-A7, FPGA-D6, FPGA-D5, FPGA-B4, FPGA-C8, FPGA-G2, FPGA-A4, FPGA-B3, FPGA-C2, FPGA-D2, FPGA-K1, FPGA-E3, FPGA-E2, FPGA-F4, FPGA-F2, FPGA-K2, FPGA-H1, FPGA-H4, FPGA-L2, FPGA-J1, FPGA-K3, FPGA-G5, FPGA-G4, FPGA-L3, FPGA-M1, FPGA-N1, FPGA-L5, FPGA-M4, FPGA-N3, FPGA-P2, FPGA-P4, FPGA-T4, FPGA-P5, FPGA-R5, FPGA-P6, FPGA-T6, FPGA-M6
[Sht 3] XS_GPIO0, XS_GPIO2, XS_GPIO3
[Sht 2] XS_ST_TXD, XS_I2C_SCL
[Sht 2,7] USB_UDCN
[Sht 2] XS_NSSP_FRAME, XS_NSSP_TXD
[Sht 2,8] XS_SSP_TXD, XS_SSP_EXTCLK, XS_FF_RI, XS_FF_DSR, XS_FF_RTS
[Sht 2] XS_FF_TXD

Right net labels:
V3.3V_IN [Sht 6,10]
VCC_BANK0 [Sht 6]
VCC_BANK6 [Sht 6]
VCC_BANK7 [Sht 6]
[Sht 8] FPGA-D8, FPGA-D7, FPGA-B7, FPGA-C6, FPGA-B5, FPGA-A6, FPGA-E6, FPGA-C5, FPGA-C4, FPGA-H3, FPGA-J3, FPGA-A3, FPGA-D3, FPGA-C1, FPGA-D1, FPGA-G1, FPGA-E4, FPGA-E1, FPGA-F3, FPGA-F1, FPGA-J2, FPGA-J4, FPGA-H2, FPGA-K4, FPGA-F5, FPGA-G3, FPGA-K5, FPGA-M2, FPGA-L1, FPGA-L4, FPGA-M3, FPGA-N2, FPGA-P1, FPGA-R4, FPGA-T3, FPGA-N5, FPGA-T5, FPGA-N6, FPGA-R6, FPGA-T8
RESET_OUT_N [Sht 3,5]
XS_GPIO1 [Sht 3]
XS_GPIO4 [Sht 3]
XS_ST_RXD [Sht 2]
XS_I2C_SDA [Sht 2]
USB_UDCP [Sht 2,7]
XS_NSSP_CLK [Sht 2]
XS_NSSP_RXD [Sht 2]
XS_SSP_RXD [Sht 2,8]
XS_SSP_SFRM [Sht 2,8]
XS_SSP_SCLK [Sht 2,8]
XS_FF_DCD [Sht 2,8]
XS_FF_DTR [Sht 2,8]
XS_FF_CTS [Sht 2,8]
XS_FF_RXD [Sht 2]

VCC_BANK7, VCC_BANK0, VCC_BANK6

COMPACT FLASH SLOT

Compact Flash Type II Socket

U16 — 16_Bit Buffer/Line Driver — IDT74LVC162244APF

U17 — IDT74LVC162245APF

U18 — 74LVC1G08DBVR

U19 — IDT74LVC2244APG

J4 — CF_TYPE_II — FCI 62453-022

Rev. B V.1.0 R107 10K

NOTE:
DIR H = A -> B
DIR L = A <- B

FB2 3A, 0.012 DCR

VCC3.3V
VCC_CF

[Sht 2,3,4,5,6,7,8] VCC3.3V
[Sht 2,4,5,8] XS_A[0..25]
[Sht 2,8] XS_CI_PWE_N
[Sht 2,4,5,8] XS_D[0..31]
[Sht 2,8] XS_CI_PSKTSEL
[Sht 2,8] XS_CI_PCE_1_N
[Sht 2,8] XS_CI_PCE_2_N
[Sht 2,8] XS_CI_POE_N
[Sht 2,8] XS_CI_PIOR_N
[Sht 2,8] XS_CI_PIOW_N
[Sht 2,8] XS_CI_PREG_N
[Sht 2] XS_CF_RESET
[Sht 6,9] V3.3V_IN

XS_CI_WAIT_N   [Sht 2,8]
XS_CI_IOIS16_N [Sht 2,6]
CF_READY   [Sht 3]
CF_CD2_N   [Sht 2]
CF_CD1_N   [Sht 2]

R74 100K CF_CD2_N
R75 100K CF_CD1_N
R76 100K
R77 DNI
R78 DNI
R79 DNI
R80 100K
R81 1.0K
R82 DNI
R83 100K
R84 DNI
R85 100K
R86 100K

Capacitors: C111 0.01uF, C112 0.01uF, C113 0.01uF, C114 0.01uF, C115 0.01uF, C116 0.01uF, C117 0.01uF, C118 0.01uF, C119 0.01uF, C120 0.01uF, C121 0.01uF, C122 0.01uF, C123 0.01uF, C124 0.01uF, C125 0.01uF, C126 0.01uF, C127 0.01uF