


Project: **StreetRacer Test Board**

SHEET	DESCRIPTION
1	Title Page
2	CPU CARD INTERFACE
3	DIGITAL AUDIO BUFFERS
4	ETHERNET (DM9000)
5	ETHERNET (LAN91C111)
6	LOGIC ANALYZER INTERFACE
7	SERIAL, SWITCH and LEDS
8	SLINK and IR
9	DIGITAL AUDIO INPUT
10	DIGITAL AUDIO OUTPUT
11	POWER

- NOTES
1. Components marked with a dashed and crossed box will not be installed during assembly.



2. Please refer to the Bill of Material (BOM) which provides all necessary component information for the final assembly.

3. The following parameters will apply to all components unless otherwise stated in the BOM or Schematic.

Resistor: +/- 5% or better, 1/16 Watt, 0603

Capacitor, non - polarized: Ceramic, +/- 20%, 0603

Capacitor, polarized: Tantalum, +/- 20%

Inductance: +/- 10%

4. Bypass capacitors shall be distributed evenly amongst power pins of the IC power and GND pin.

5. Always observe layout guidelines and documentation from the component manufacturers

Schematic Statistics:

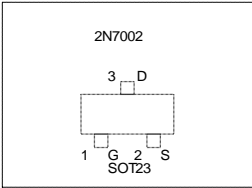
Parts: 00

Library Parts: 00

Nets: 00

Pins: 00

LAST REFERENCES USED		
REF.	Last used	Not used
R	R87	n/a
R N	n/a	n/a
C	C144	n/a
D	D7	n/a
U	U26	n/a
Y	Y2	n/a
FB	FB16	n/a
J	J17	n/a
JP	n/a	n/a
P	P1	n/a
K	n/a	n/a
L	L9	n/a
Q	Q9	n/a
SW	SW1	n/a
OPT	OPT8	n/a
TP	TP12	n/a
BT	n/a	n/a
LED	n/a	n/a
F	n/a	n/a
XJP	n/a	n/a
CN	n/a	n/a
CON	n/a	n/a
M	n/a	n/a
PB	n/a	n/a
BR	n/a	n/a
ANT	n/a	n/a
FL	n/a	n/a



VERSION	REVISION	DATE	DESCRIPTION	NAME
0.1	A	08-11-2003	Initial Design Created	S. Street
0.2	A	08-20-2003	Preliminary Design	M. Daroy
0.3	A	08-22-2003	Added Power and Ground Test Posts. Changed D2 to GREEN LED (550-1307). Added R87.	M. Daroy
0.4	A	09-04-2003	Correction on PULSE Ethernet Jack Pinout.	M. Daroy

STREETRACER TEST BOARD

DWN: Mario Daroy

ENG: Mario Daroy

REV: A

DWG. SIZE C


DATE: Thursday, September 04, 2003

SHEET 1 of 11

TITLE STREETRACER TEST BOARD

DWG. No. ST08-01-02A

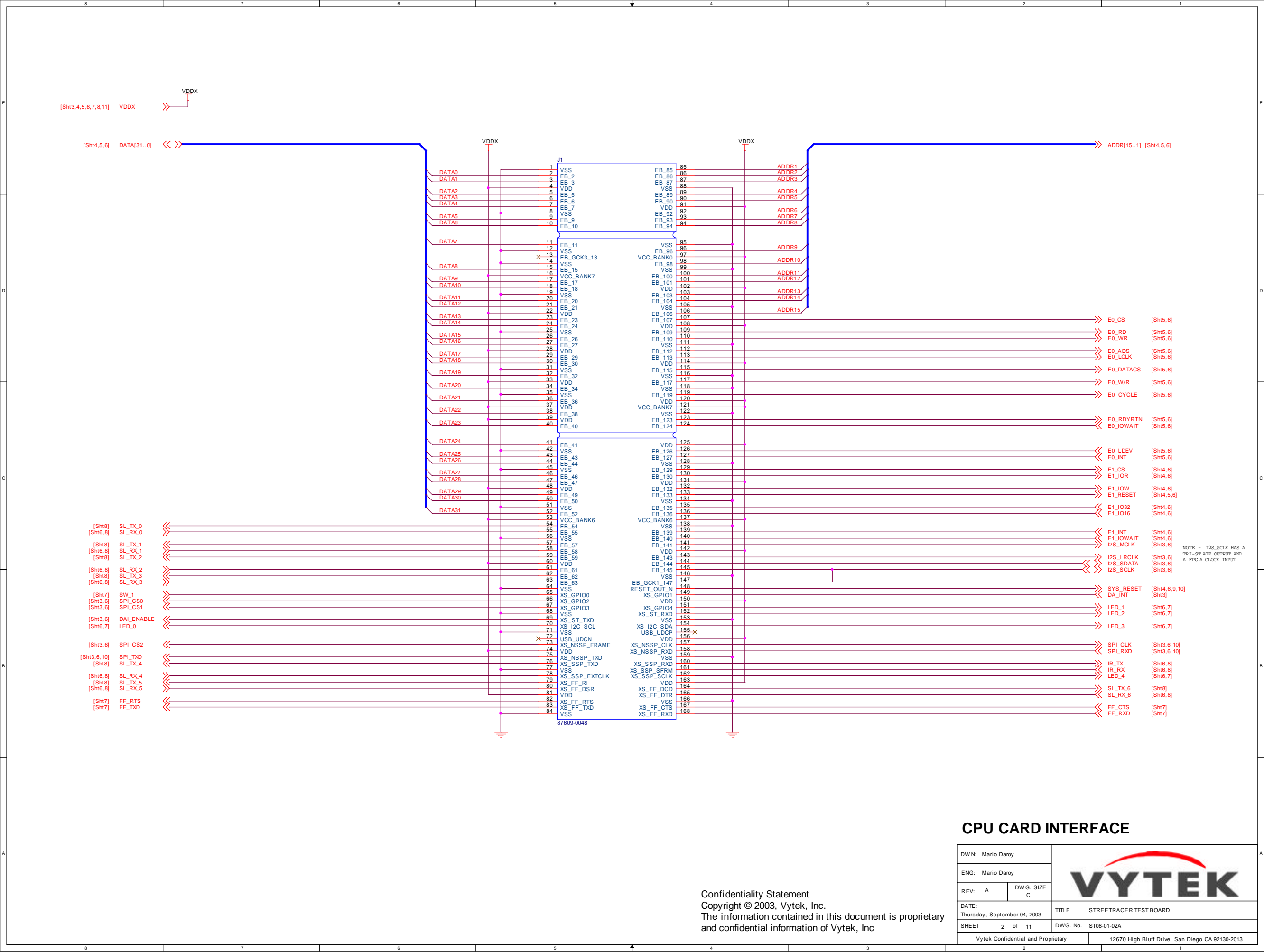
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1

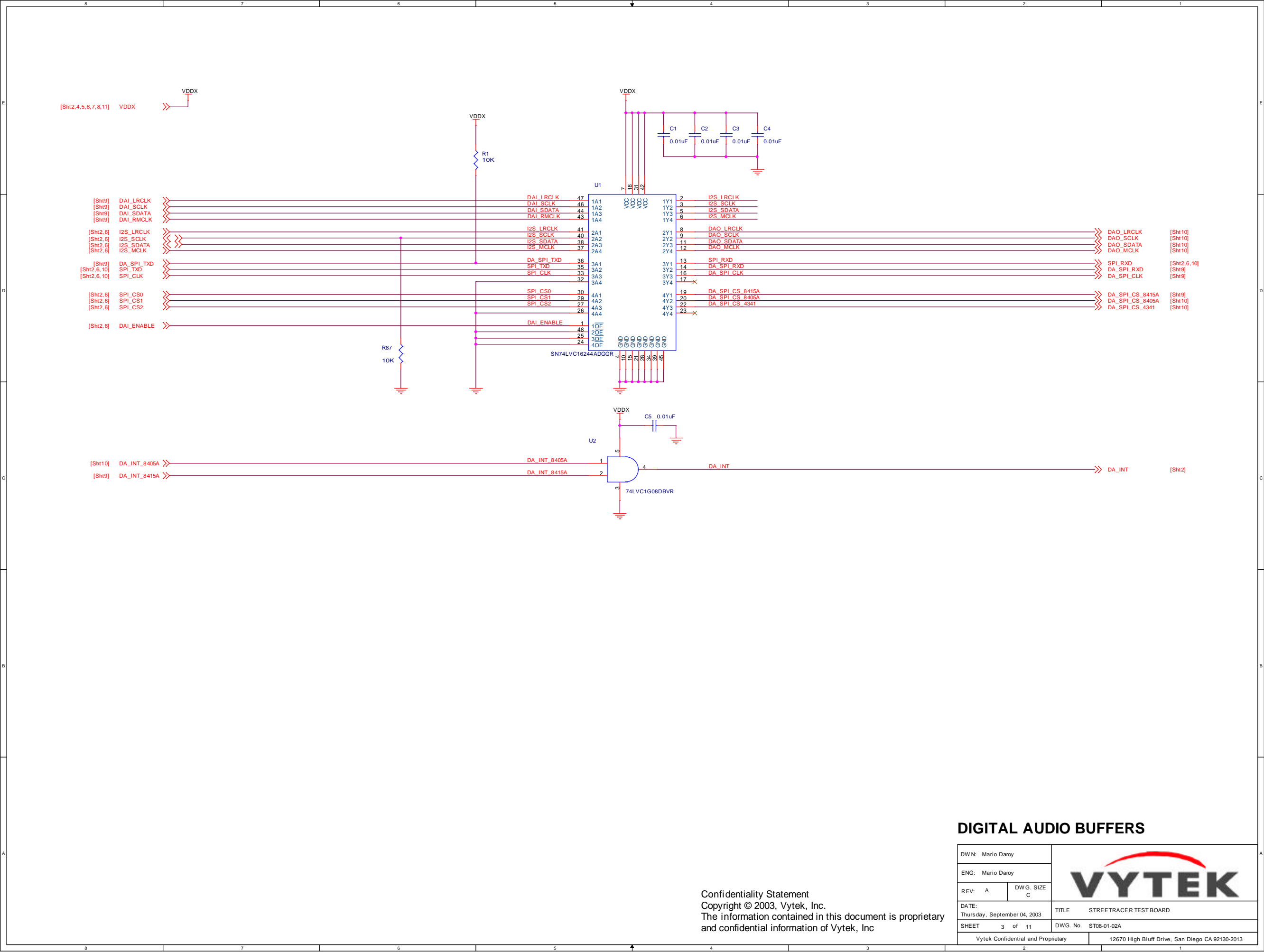
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CPU CARD INTERFACE

DWN: Mario Daroy			
ENG: Mario Daroy			
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DATE: Thursday, September 04, 2003			TITLE STREETRACER TEST BOARD
SHEET 2 of 11			DWG. No. ST08-01-02A
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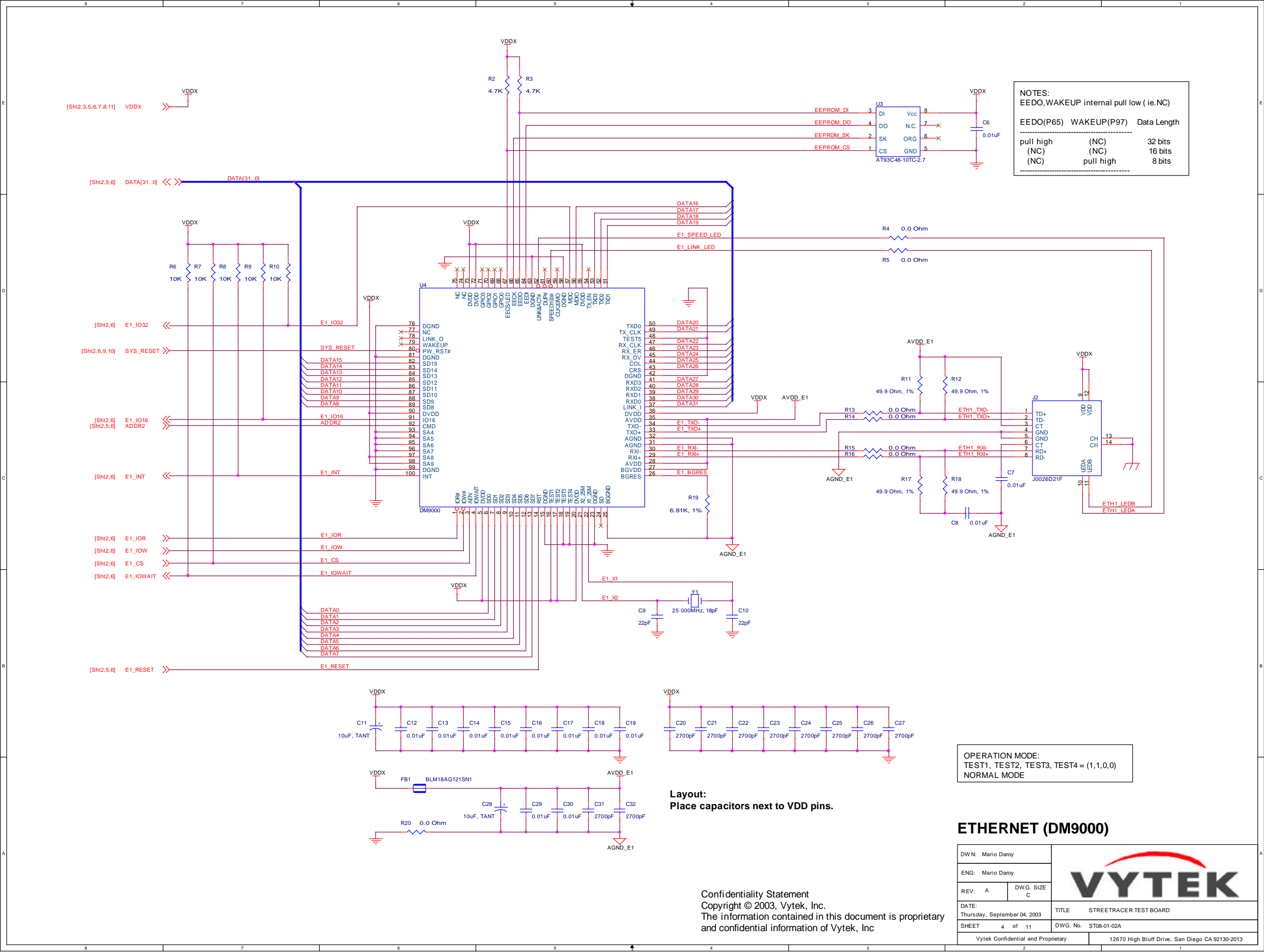
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DIGITAL AUDIO BUFFERS

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ENG: Mario Daroy		
REV: A	DWG. SIZE C	
DATE: Thursday, September 04, 2003		
SHEET 3 of 11		TITLE STREETRACER TEST BOARD
		DWG. No. ST08-01-02A
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NOTES:  
EEDO, WAKEUP internal pull low ( ie.NC)

EEDO(P65)	WAKEUP(P97)	Data Length
pull high	(NC)	32 bits
(NC)	(NC)	16 bits
(NC)	pull high	8 bits

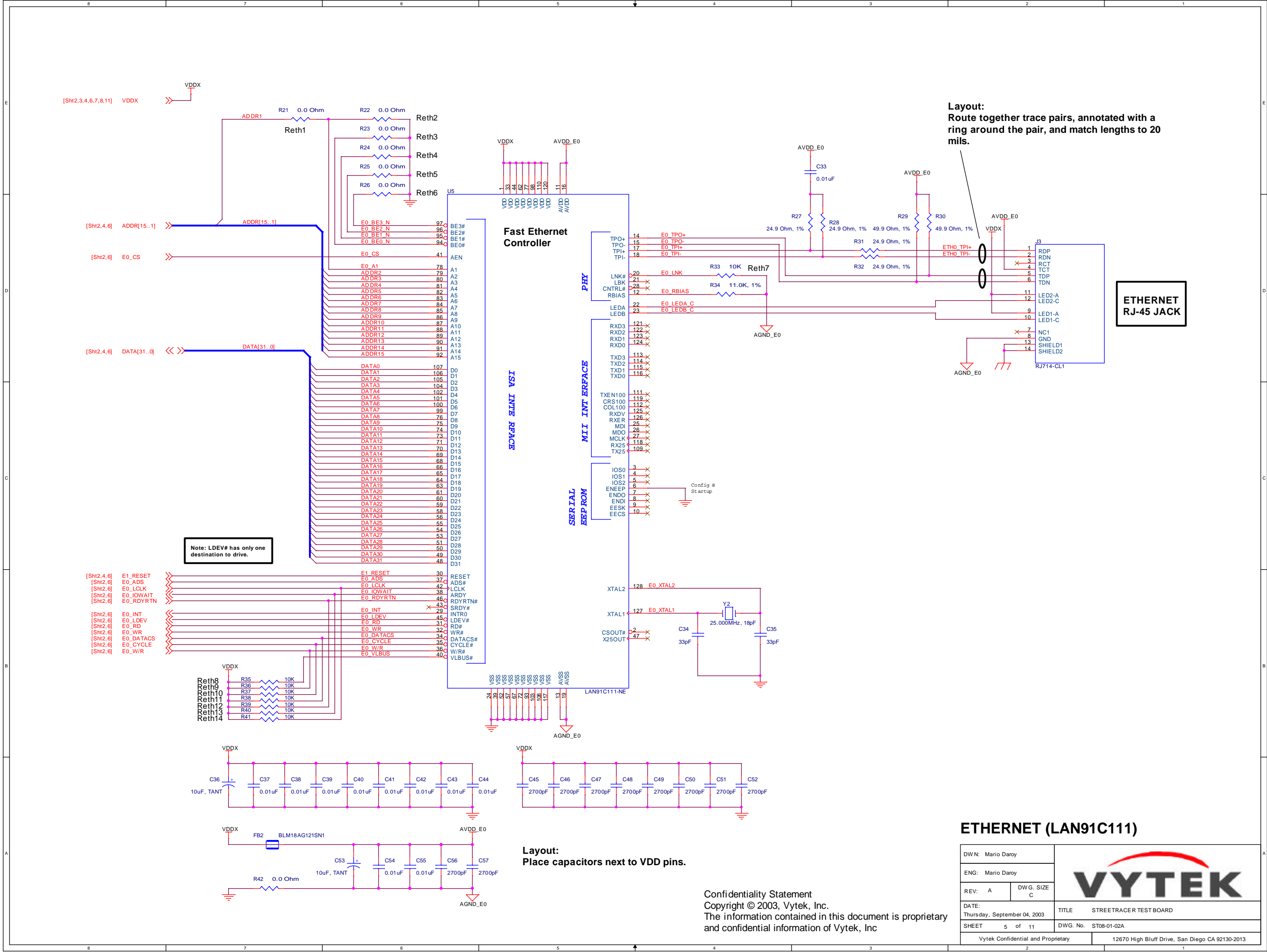
OPERATION MODE:  
TEST1, TEST2, TEST3, TEST4 = (1,1,0,0)  
NORMAL MODE

ETHERNET (DM9000)


DWN: Mario Daroy		
ENG: Mario Daroy		
REV: A	DWG. SIZE C	
DATE: Thursday, September 04, 2003		
SHEET 4 of 11		TITLE STREETRACER TEST BOARD
DWG. No. ST08-01-02A		
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Layout:  
Place capacitors next to VDD pins.

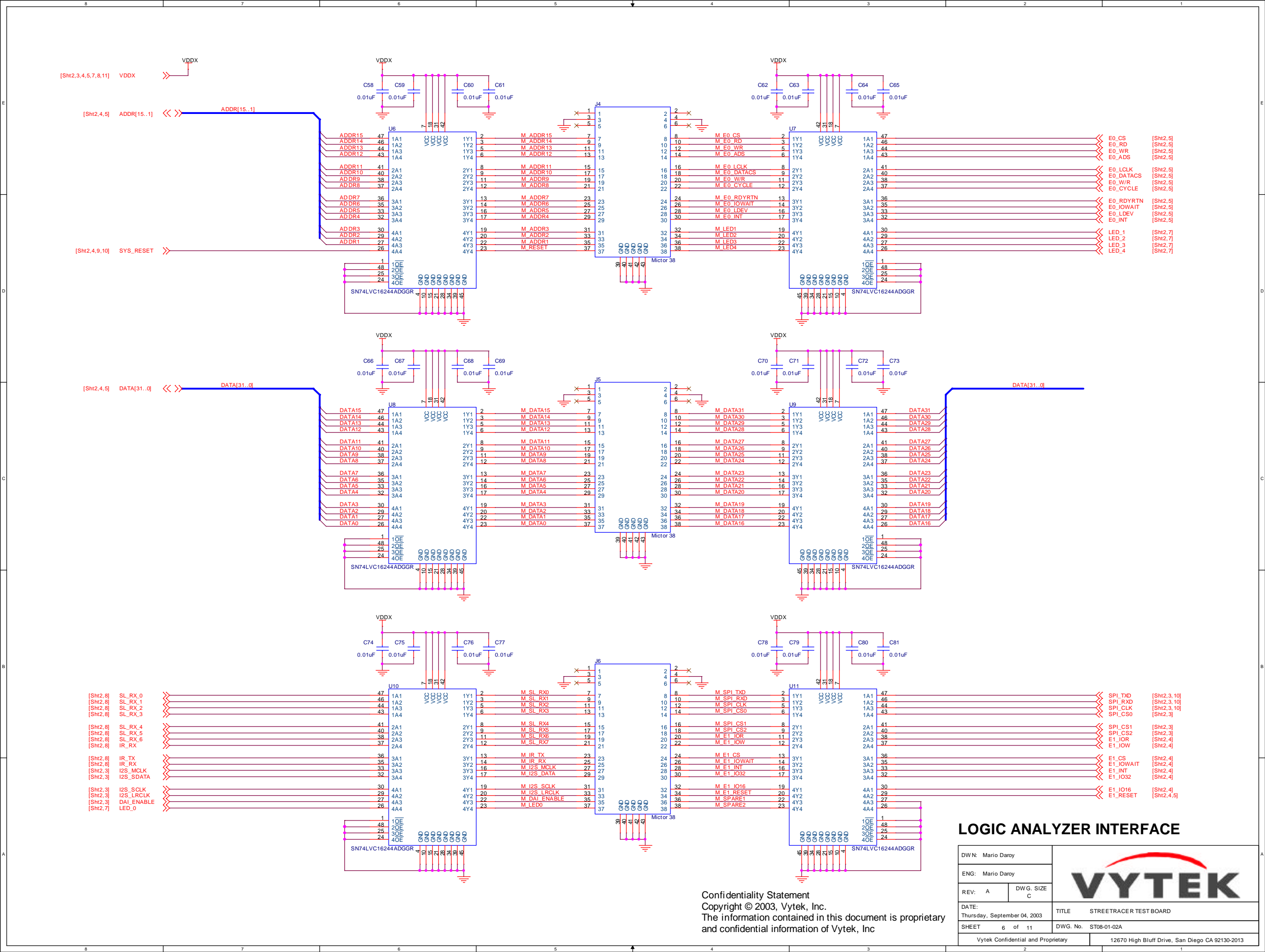
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ETHERNET (LAN91C111)


DWN: Mario Daroy			
ENG: Mario Daroy			
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SHEET 5 of 11			DWG. No. ST08-01-02A
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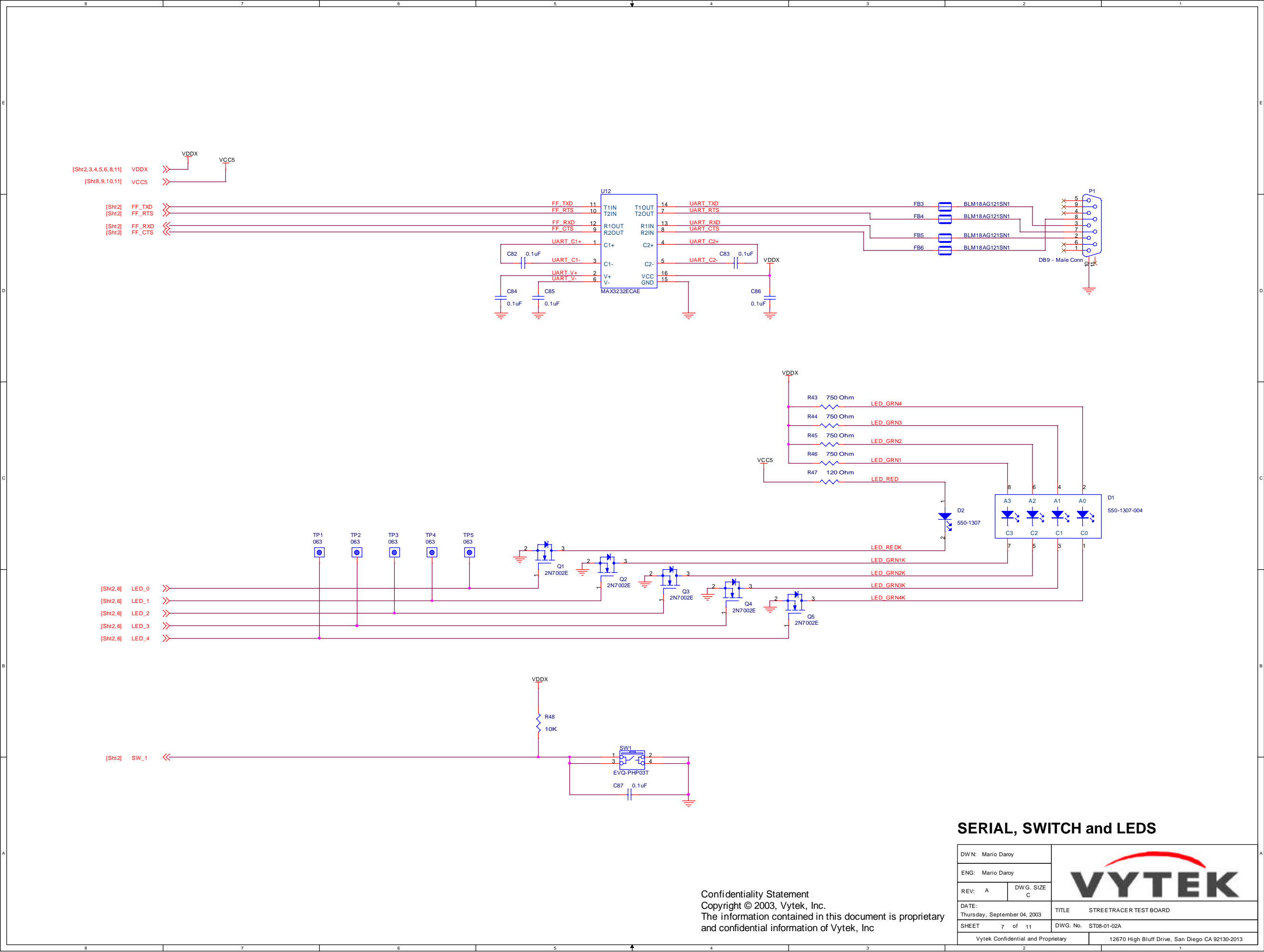
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LOGIC ANALYZER INTERFACE

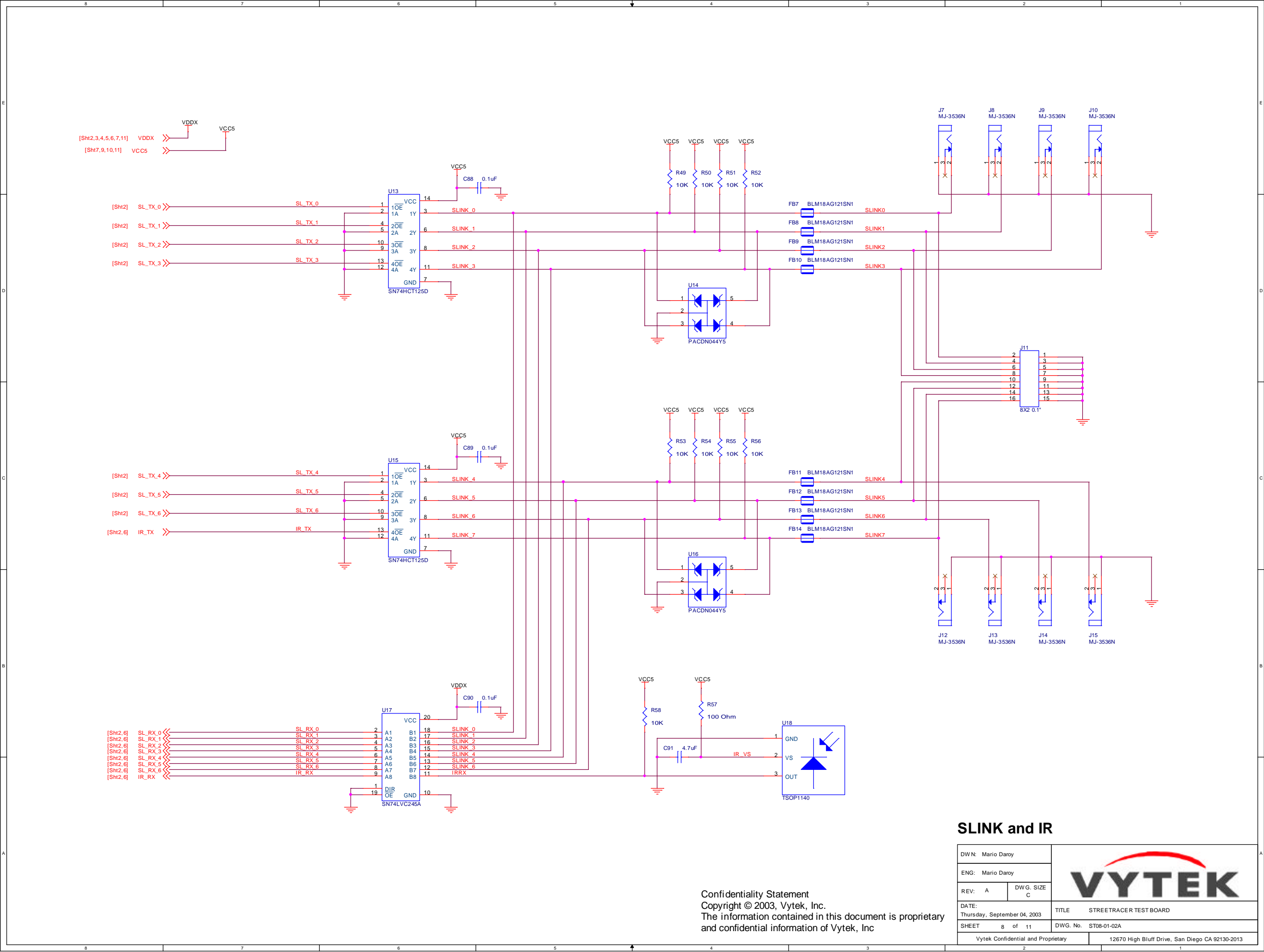
DWN: Mario Daroy			
ENG: Mario Daroy			
REV: A	DWG. SIZE C		
DATE: Thursday, September 04, 2003			TITLE STREETRACER TEST BOARD
SHEET 6 of 11			DWG. No. ST08-01-02A
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SERIAL, SWITCH and LEDS

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ENG: Mario Daroy		
REV: A	DWG. SIZE C	
DATE: Thursday, September 04, 2003		
SHEET 7 of 11		TITLE STREETRACER TEST BOARD
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SLINK and IR

DWN: Mario Daroy		
ENG: Mario Daroy		
REV: A	DWG. SIZE C	
DATE: Thursday, September 04, 2003		
SHEET 8 of 11		
TITLE STREETRACER TEST BOARD		
DWG. No. ST08-01-02A		
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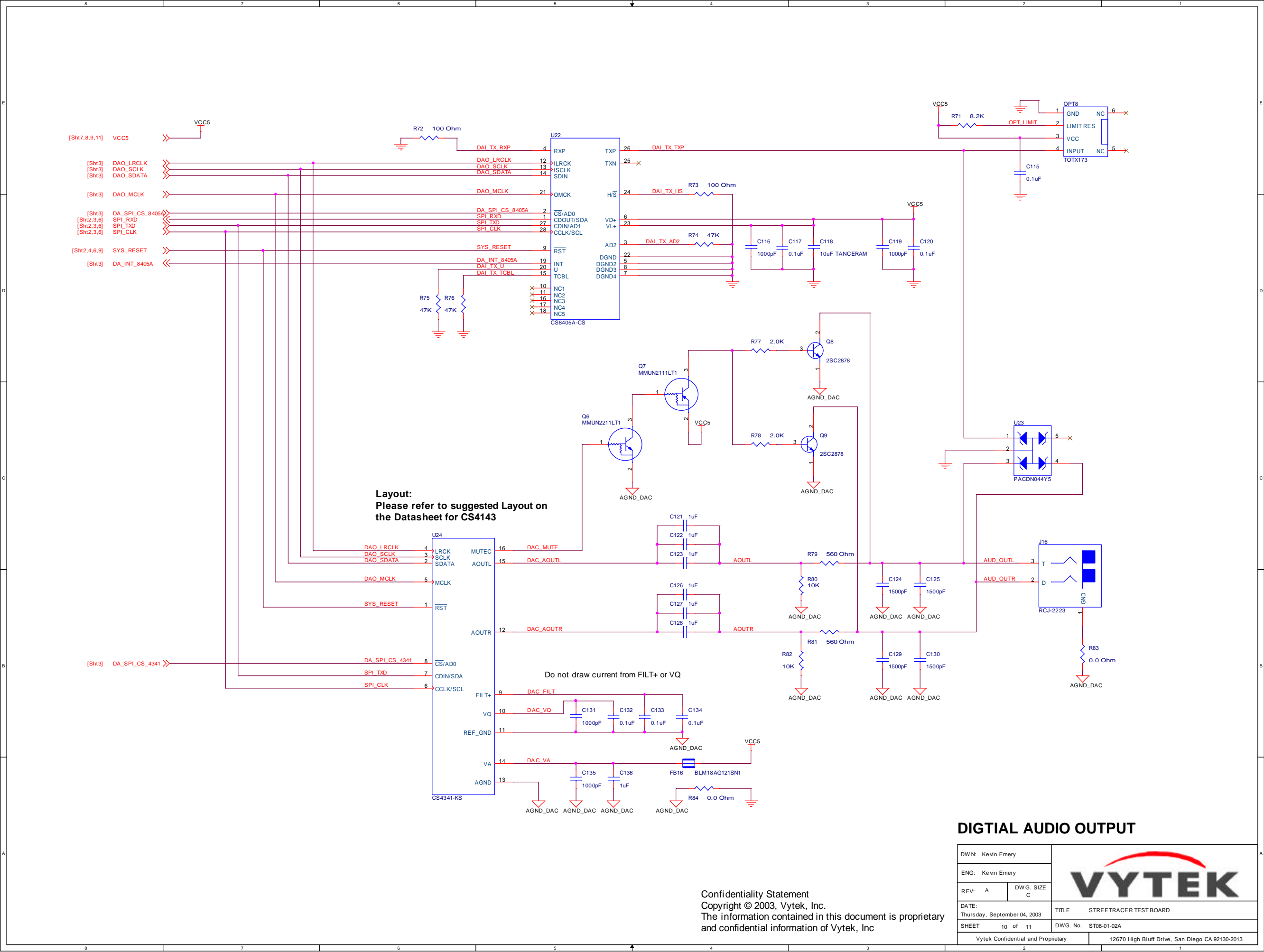
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DWN: Kevin Emery		
ENG: Kevin Emery		
REV: A	DWG. SIZE C	
DATE: Thursday, September 04, 2003		
SHEET 9 of 11		TITLE STREETTRACER TEST BOARD  DWG. No. ST08-01-02A
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Layout:  
Please refer to suggested Layout on  
the Datasheet for CS4143


Do not draw current from FILT+ or VQ

DIGITAL AUDIO OUTPUT

DWN: Kevin Emery			
ENG: Kevin Emery			
REV: A	DWG. SIZE C		
DATE: Thursday, September 04, 2003			TITLE STREETRACER TEST BOARD
SHEET 10 of 11			DWG. No. ST08-01-02A
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M1  
MTG125F

DWN: Kevin Emery		
ENG: Kevin Emery		
REV: A	DWG. SIZE C	
DATE: Thursday, September 04, 2003		
SHEET 11 of 11		TITLE STREETTRACER TEST BOARD
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