Batch: A1	**Roll No.: 16010120015**
Experiment / assignment / tutorial No. (9)	
Grade: AA / AB / BB / BC / CC / CD /DD	
Signature of the Staff In-charge with date	

TITLE: Study of RISC and CISC Architecture

AIM: Understanding RISC and CISC Architecture

Expected OUTCOME of Experiment:
CO 3 - Understand the Central processing unit with addressing modes and working of control unit

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Books/ Journals/ Websites referred:

1. Carl Hamacher, Zvonko Vranesic and Safwat Zaky, "Computer Organization", Fifth Edition, TataMcGraw-Hill.
2. William Stallings, "Computer Organization and Architecture: Designing for Performance", Eighth Edition, Pearson.
3. Dr. M. Usha, T. S. Srikanth, "Computer System Architecture and Organization", First Edition, Wiley-India.

Pre Lab/ Prior Concepts:

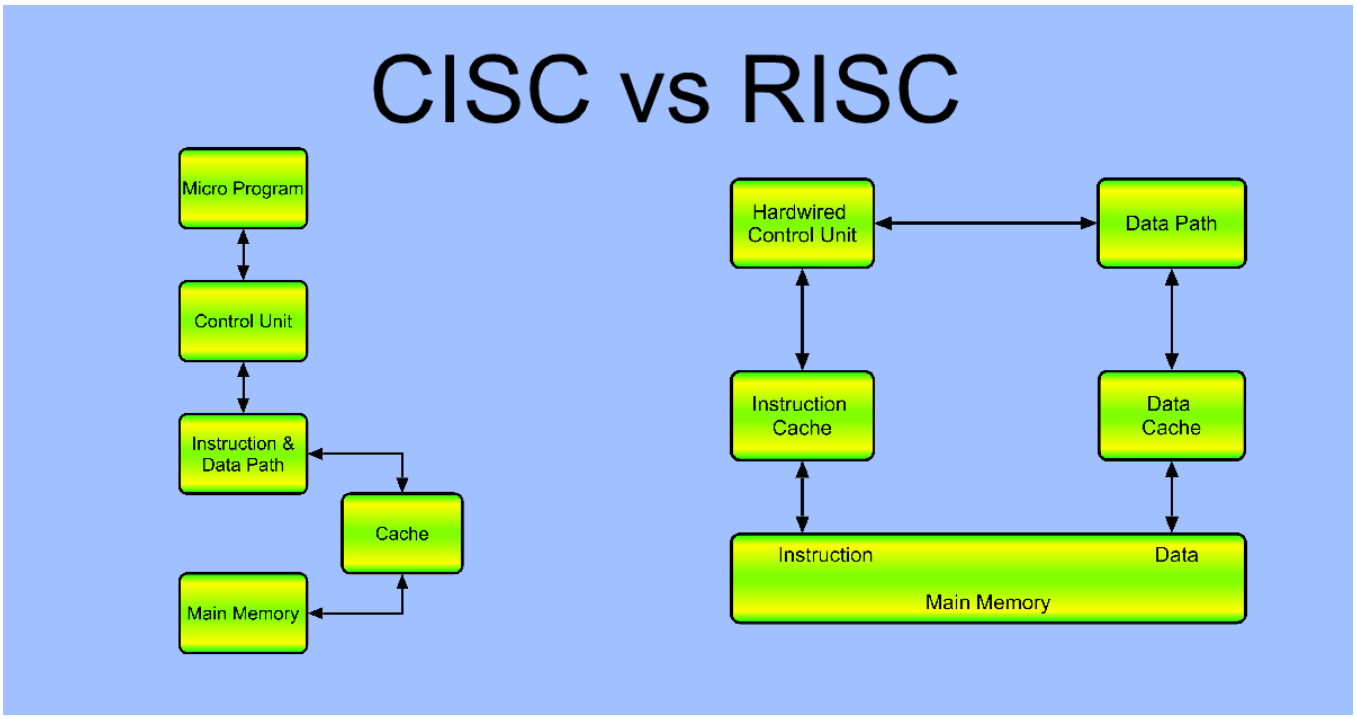
Reduced Set Instruction Set Architecture (RISC)

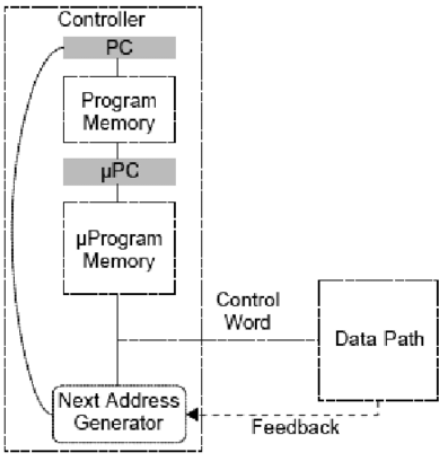
The main idea behind is to make hardware simpler by using an instruction set composed of a few basic steps for loading, evaluating and storing operations just like a load command will load data, store command will store the data.

Complex Instruction Set Architecture (CISC)

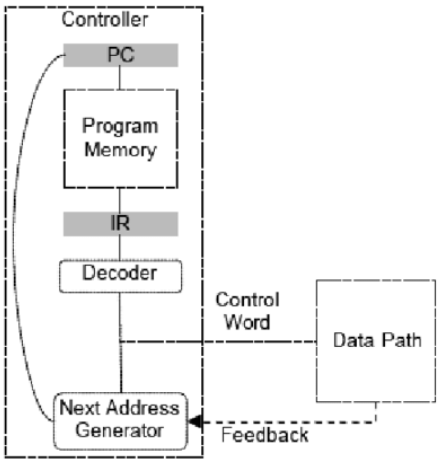
The main idea is that a single instruction will do all loading, evaluating and storing operations just like a multiplication command will do stuff like loading data, evaluating

and storing it, hence it's complex. Both approaches try to increase the CPU performance.





CISC
Complex Instructions Possible
1 Instruction = n µ-Instructions



RISC
Simple Instructions
No µ-programming
RISC PM = N x CISC PM

RISC Architecture

Definition:

RISC or Reduced Instruction Set Computer is a type of microprocessor architecture that utilizes a small, highly-optimized set of instructions, rather than a more specialized set of instructions often found in other types of architectures. It is a dramatic departure from historical architectures.

- RISC processor is implemented using the hardwired control unit. The hardwired control unit produces control signals which regulate the working of processors hardware. RISC architecture emphasizes on using the registers rather than memory.
- This is because the registers are the 'fastest' available memory source. The registers are physically small and are placed on the same chip where the ALU and the control unit are placed on the processor. The RISC instructions operate on the operands present in processor's registers.

Brief explanation of each component:

Hardwired Control Unit: RISC processor is implemented using the hardwired control unit. The hardwired control unit produces control signals which regulate the working of processors hardware
Instruction Cache: Instruction Cache is a temporary storage for the instructions
Data Path: Elements that process data and addresses in the CPU
Data Cache: Data Cache is a temporary storage for data

RISC Processor Instruction Set Examples with explanation: (Any 2)

- The Load instruction loads the operand present in memory to the processor register: Load R2, A
  The load instruction above will load the operand present at memory location A to the processor register R2
- The Store instruction stores the operand back to the memory. Generally, the Store instruction is used to store the intermediate result or the final result in the memory: Store R2, A
  The Store instruction above will store the content in register R2 into the A memory location

CISC Architecture

Definition:

Stands for Complex Instruction Set Computing**.** This is a type of microprocessor design. The CISC architecture contains a large set of computer instructions that range from very simple to very complex and specialized.

- MUL loads two values from the memory into separate registers in CISC.
- CISC uses minimum possible instructions by implementing hardware and executes operations.
- Instruction Set Architecture is a medium to permit communication between the programmer and the hardware. Data execution part, copying of data, deleting or editing is the user commands used in the microprocessor and with this microprocessor the Instruction set architecture is operated.

Brief Explanation of each component:

Micro Program Control Unit: Micro program control unit uses a series of microinstructions of the microprogram stored in the "control memory" of the microprogram control unit and generate the control signals.
Control Unit: The control units access the control signals produced by the microprogram control unit & operate the functioning of processors hardware.
Instruction and Data Path: Instruction and data path fetches the opcode and operands of the instructions from the memory.
Cache and Main Memory: Cache and main memory is the location where the program instructions and operands are stored.

CISC Processor Instruction Set Examples with explanation: (Any 2)

- Like RISC uses Load/Store for accessing the memory operands, CISC has Move instruction to access memory operands. It can move an immediate operand, to a memory location or a register: Move A, B || Move R1, R2 Transfer the data from one memory location to another || transfer of data from one register to another.
- To add two data stored in memory locations or registers, ADD instruction is used. It adds two values and stores in the memory of the first memory location/register named: ADD A, B
  It adds values stored in A and B and then stores the output in A thus overwriting the data in A.

Post Lab Descriptive Questions

Write a tabular comparative analysis of RISC v/s CISC

CISC	RISC
Instructions can take several clock cycles.	Single-cycle instructions.
More efficient use of RAM the RISC.	Heavy use of RAM. (Can cause bottlenecks if RAM is limited).
Complex and variable length instructions.	Simple, standardized instructions.
Large number of instructions.	Small number of fixed-length instructions.
Compound addressing modes.	Limited addressing modes.
Emphasis on hardware.	Emphasis on software
Less registers	More registers.
Pipelining is difficult.	Pipelining is easy.

Conclusion: RISC and CISC Architecture was studied in detail.

Date: 21.10.2021 **Signature of faculty in-charge**