# Digital Circuits

Lab Session 1 on Combinational Logic

(Group 3 – Team 5)

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# 1. Introduction:

The goal of this laboratory session is to design, implement, and test a combinational logic circuit for a smart home environment. This circuit acts as a room controller, enabling both automated and manual management of lighting and blinds according to predefined scenarios. The exercise involves working with Small-Scale Integration (SSI) Integrated Circuits (ICs) and Field Programmable Gate Arrays (FPGAs), providing hands-on experience with real-world digital circuit design and verification.

Critical activities include creating a truth table and Boolean logic for the room controller, simulating and verifying the design using the "Digital" software, and converting the design into VHDL code for FPGA implementation. The circuit operates in four distinct scenarios: "Standard," "Lunchtime," "Nighttime," and "Emergency," each with unique behavioral requirements. Additionally, the lab offers practical experience with hardware configurations, such as using NAND-only circuits and FPGA synthesis, focusing on essential skills in digital electronics.

This report aims to document the approach, findings, and lessons learned from this laboratory session.

# 2. Laboratory preparation overview:

**Lab preparation summary:**

The lab preparation was focused on designing and validating the combinational logic for the smart home room controller, as detailed in the lab description. Several key steps were involved in this preparation:

1. **Truth Table and Boolean logic**
   A detailed truth table was created to outline the input-output relationships for all possible input variable combinations (fig 1 and fig 2):

   - **SC [1:0]**: Scene inputs representing the different scenarios—Standard (00), Lunchtime (01), Nighttime (10), and Emergency (11).
   - **LIT**: Light switch input for manual control of lighting.
   - **BS**: Blind switch input for manual operation of blinds.
   - **LS:** Light sensor input indicating the level of solar radiation.
   - Output variables:
   - **B**: Blind control (0 = down/closed, 1 = up/open).
   - **L**: Light control (0 = off, 1 = on).

2. **Circuit Design**
   The initial circuit design was built using fundamental logic gates (AND, OR, NOT). A second design was developed utilizing only NAND gates to simplify the circuit and ensure its universality in construction. Both designs were methodically created and tested using the "Digital" software**:**

- Design 1: Used OR, AND, and NOT gates to represent the logic (fig 3).
- Design 2: Converted into a NAND-only configuration for hardware implementation.

3. **Simulation**
   The designs were simulated using the "Digital" software to ensure logical correctness. The simulation results verified that both configurations performed as expected and met the specified behaviors for all scenes:

   - Standard: Manual control only.
   - Lunchtime: Automatic blind closure based on the light sensor.
   - Nighttime: Manual light control, with blinds always closed.
   - Emergency: Lights turned on and blinds opened, overriding all other inputs.

4. **VHDL Code**
   The verified circuit design was exported to VHDL for FPGA implementation. The code was organized with descriptive signal names, following best practices for readability and compatibility with hardware synthesis. Both the general logic and the NAND-only configurations were developed for implementation.

5. **Test Plan and Testbench**
   A structured test plan was developed, containing test cases for each scene and condition, resulting in a total of 16 tests (fig 4). Unique identifiers (e.g., R1.1, R2.1) were assigned to each test case to ensure traceability. Additionally, a corresponding testbench was created to automate the simulation, covering all functional scenarios derived from the truth table.

# 3. Setup description:

The laboratory setup included the following components and tools for implementing and testing the room controller logic:

1. **Hardware components:**
   - **FPGA Board**: The final VHDL design was implemented and tested on an FPGA.
   - **7400 NAND ICs**: Used to build the combinational logic circuit with NAND gates only.
   - **Evaluation Board**: Provided the platform for wiring and testing the 7400 NAND circuit.
   - **Switches and LEDs**: Represented input signals (SC1, SC2, LS, LIT, BS) and output signals (L, B).
   - **Function Generator**: Generated square wave signals to test the circuit with different input conditions.
   - **Oscilloscope**: Used to analyze signal behavior and measure propagation delay in the circuit.

2. **Software tools:**
    - Digital Program: Used to simulate the initial circuit designs and generate VHDL code.
    - EDA Playground: Set up to validate VHDL code and execute testbenches.
    - Vivado: Used for synthesizing, implementing, and generating the bitstream for the FPGA.

3. **Circuit connection:**
    - Inputs (SC1, SC2, LS, LIT, BS) and outputs (L, B) were connected using switches and LEDs.
    - Proper orientation and grounding of components were ensured to guarantee reliable circuit operation.
    - The power supply was maintained at Vcc = 3.3V and GND = 0V to prevent any damage to the components.

4. **Testing and verification:**
    - Manual Testing: Inputs were manually toggled using switches to observe the corresponding LED outputs.
    - Automated Testing: Testbenches were used in simulation environments to validate the functional behavior of the circuit.
    - Propagation Delay Measurement: The oscilloscope was used to measure delays at specific points in the circuit using signals from the function generator.

# 4. Task preparation:

## 4.1 **Task 1:** Implementation of lamp control Using NAND Gates

**Objective:**

The objective of this task was to construct the lamp control section of the room controller logic using only NAND gates on the IC Evaluation Board. This task focused on understanding the implementation of logic gates and verifying the functional behavior through manual input testing**.**

**Method:**

1. **Circuit construction:**
    - The lamp control logic was implemented using only NAND gates. The schematic was simulated using the "Digital" program, as shown in Fig 5 below.

- Inputs were assigned to represent the light switch (LIT), and the light output (L) was connected to an LED.
- The circuit was assembled on the IC Evaluation Board, ensuring the proper orientation of the 7400 IC and careful wiring of the inputs and outputs (fig 7).
- The power supply was set to 3.3V, and all connections were verified before powering on.

2. **Verification:**
   - The input switch (LIT) was toggled to simulate various scenarios.
   - The LED indicator for the light output (L) was monitored to verify the functionality of the circuit.

3. **Outcomes:**
   - The circuit was implemented correctly and operated as expected:
     - The LED turned ON when the light switch (LIT) was activated.
     - The LED turned OFF when the light switch (LIT) was deactivated.
   - The observed behavior matched the truth table created during the lab preparation phase.

## 4.2 **Task 2:** Measurement of propagation Delays

### Task 2.1:

**objective:**

The goal of this task was to check the signal of the function generator using the oscilloscope. The settings on the function generator were at $V_{pp}$ of 3.3V with an offset of +3.3V, note the plateau of the rectangular wave.

### **Task 2.2:** Measurement of propagation Delay for the Lamp Control Circuit

**Objective:**

The goal of this task was to measure the propagation delay of the lamp control circuit, which was built using NAND gates. The propagation delay represents the time it takes for a change in the input signal (light switch) to affect the output signal (light control).

**Method:**

1. **Circuit construction:**
   - The lamp control circuit from Task 1 was kept and connected to the oscilloscope.

- The function generator provided a square wave signal as input to simulate the toggling of the light switch (LIT).
- The oscilloscope was configured to monitor:
    - **Channel 1**: Input signal from the function generator.
    - **Channel 2**: Output signal from the circuit (light control).
- The function generator settings were:
    - **Waveform**: Square wave.
    - **Amplitude**: 3.3 V peak-to-peak.
    - **Offset**: 1.650 V.
    - **Frequency**: 10k Hz.

**2. Collection of data:**

- The oscilloscope recorded both the input and output waveforms.
- The time interval (Δt) between the rising edge of the input signal and the corresponding rising edge of the output signal was calculated.

**3. Outcomes:**

- The propagation delay of the lamp control circuit was calculated based on the oscilloscope reading.
- Measured Delay: $\Delta t = 31.300$ ns.
- A screenshot of the oscilloscope display offers a visual representation of the input and output waveforms, clearly illustrating the measured propagation delay (fig 8).

## **Task 2.3:** Measurement of propagation delay for a single NAND gate

**Objective:**
The goal of this task was to measure the propagation delay of a single 2-input NAND gate configured as a NOT gate. This measurement offers insight into the fundamental delay characteristics of a single NAND gate.

**Method:**

**Circuit construction:**

- A single 2-input NAND gate was configured as a NOT gate by connecting both inputs together.
- The input signal to the NAND gate was supplied by the function generator.

- The oscilloscope was connected, and the signal parameters and channel settings remained the same as in Task 2.1.
- The oscilloscope recorded and measured the time difference between the rising edge of the input signal and the corresponding falling edge of the output signal (fig 9).

**Outcomes:**

Measured delay: $\Delta t$=10.760 ns.

**Comparison of Findings:**

The propagation delays observed in Task 2.2 (lamp control circuit) and Task 2.3 (single NAND gate) are summarized below:

Propagation delay for the lamp control circuit: 31.300 ns
Propagation delay for a single NAND gate: 10.760 ns

**Discussion**

**Difference in Delays:**

1. The propagation delay of the lamp control circuit is greater because it is composed of multiple NAND gates arranged in series. Each gate contributes its own delay to the total circuit delay.
2. The delay of the individual NAND gate serves as a reference, indicating the minimal delay introduced by a single gate.

**Insights:**

The chaining of several gates in the lamp control circuit leads to compounded delays, which is why the measured delay for the circuit is nearly twice as large as that of a single NAND gate. These observations underline the importance of minimizing the gate count in high-speed circuit designs to decrease the overall propagation delay.

## 4.3 **Task 3:** FPGA implementation of the room controller

**Objective:**

The goal of this task was to implement the room controller logic on an FPGA and verify its functionality. This process involved transferring the VHDL code developed in the preparatory tasks to the FPGA, setting up the inputs and outputs, and testing the design's performance.

**Method:**

1. **FPGA setup:**
   The FPGA board was connected and powered on (fig 10). The VHDL code was synthesized and implemented using Vivado, with the pin constraints file edited to ensure proper hardware mapping.

2. **Design flow:**

- **Synthesis**: The VHDL design was synthesized to ensure logical correctness.
- **Implementation**: The synthesized design was implemented to map the logic to the FPGA hardware.
- **Bitstream Generation**: The final design was compiled into a bitstream and uploaded to the FPGA.

**3. Testing:**

Input switches on the I/O board were toggled to simulate all the scenarios outlined in the preparatory test plan. LEDs on the I/O board displayed the output signals (L for light and B for blinds), verifying the functionality of the room controller.

**Outcomes:**

**1. FPGA functionality:**

The design performed as expected for all tested scenarios, with the outputs matching the truth table and simulation results prepared earlier.

**2. Insights from Schematic and Hardware:**

The generated FPGA schematic (Figure 12) confirmed the correct mapping of inputs to logic gates and outputs. The hardware implementation was stable, and all input-output relationships were consistent with the designed logic.

# 5. Conclusion:

This laboratory session effectively demonstrated the design, implementation, and testing of a combinational logic circuit for a smart home room controller. The tasks, combining theoretical concepts with hands-on application, highlighted crucial skills in digital circuit design and analysis.

**1. Desing and preparation:**

The initial tasks included developing truth tables, designing logic circuits, and translating them into VHDL code. These designs were verified through simulations to confirm their correctness for all predefined scenarios: "Standard," "Lunchtime," "Nighttime," and "Emergency." A detailed test plan was created and executed to ensure the functionality was accurate.

**2. Implementation of lamp control circuit (Task 1):**

The lamp control logic was constructed using only NAND gates and manually verified on the evaluation board. The circuit correctly toggled the light output based on the input switch, perfectly matching the truth table and logical design.

**3. Measurement of propagation delays (Task 2):**

The propagation delay of both the lamp control circuit and a single NAND gate was measured using an oscilloscope. The results highlighted the influence of gate count on the total circuit delay, emphasizing the importance of optimization strategies for high-speed designs.

**4. FPGA Implementation (Task 3):**

The room controller logic was successfully implemented on an FPGA. The synthesized VHDL design, tested with switches and LEDs, performed correctly for all test cases. The hardware results aligned with the simulations and the truth table, showcasing the robustness of the design and the accurate mapping of input and output signals.

This lab experience offered a thorough understanding of designing combinational logic circuits, verifying their behavior, and implementing them on hardware platforms. Each task progressively built on the previous one, leading to a fully functional and validated smart home room controller.

# 6. Figures:

**Fig 1: Truth Table:**

| SC[1:0] | LIT | BS | LS | L | B | Scene | Notes |
|---|---|---|---|---|---|---|---|
| 00 | 0 | 0 | 0 | 0 | 0 | Standard | Manual control only |
| 00 | 0 | 1 | 0 | 0 | 1 | Standard | Manual control only |
| 00 | 1 | 0 | 0 | 1 | 0 | Standard | Manual control only |
| 00 | 1 | 1 | 0 | 1 | 1 | Standard | Manual control only |
| 00 | 0 | 0 | 1 | 0 | 0 | Standard | Light sensor ignored |
| 00 | 0 | 1 | 1 | 0 | 1 | Standard | Light sensor ignored |
| 00 | 1 | 0 | 1 | 1 | 0 | Standard | Light sensor ignored |
| 00 | 1 | 1 | 1 | 1 | 1 | Standard | Light sensor ignored |
| 01 | X | X | 0 | 0 | 1 | Lunch | Manual override disabled |
| 01 | X | X | 1 | 0 | 0 | Lunch | Close blinds when bright |
| 10 | 0 | X | X | 0 | 0 | Night | Blinds always closed |
| 10 | 1 | X | X | 1 | 0 | Night | Manual light control |
| 11 | X | X | X | 1 | 1 | Emergency | Light always on, blind always open |

X = Don’t care situation (1 or 0)

**Fig 2: Boolean equations:**

$$B = (BS \wedge \overline{SC1} \wedge \overline{SC2}) \vee (\overline{LS} \wedge SC2) \vee (SC1 \wedge SC2)$$

$$L = (LIT \wedge \overline{SC2}) \vee (SC1 \wedge SC2)$$

**Fig 3: The circuit using AND, OR, and NOT Gate:**

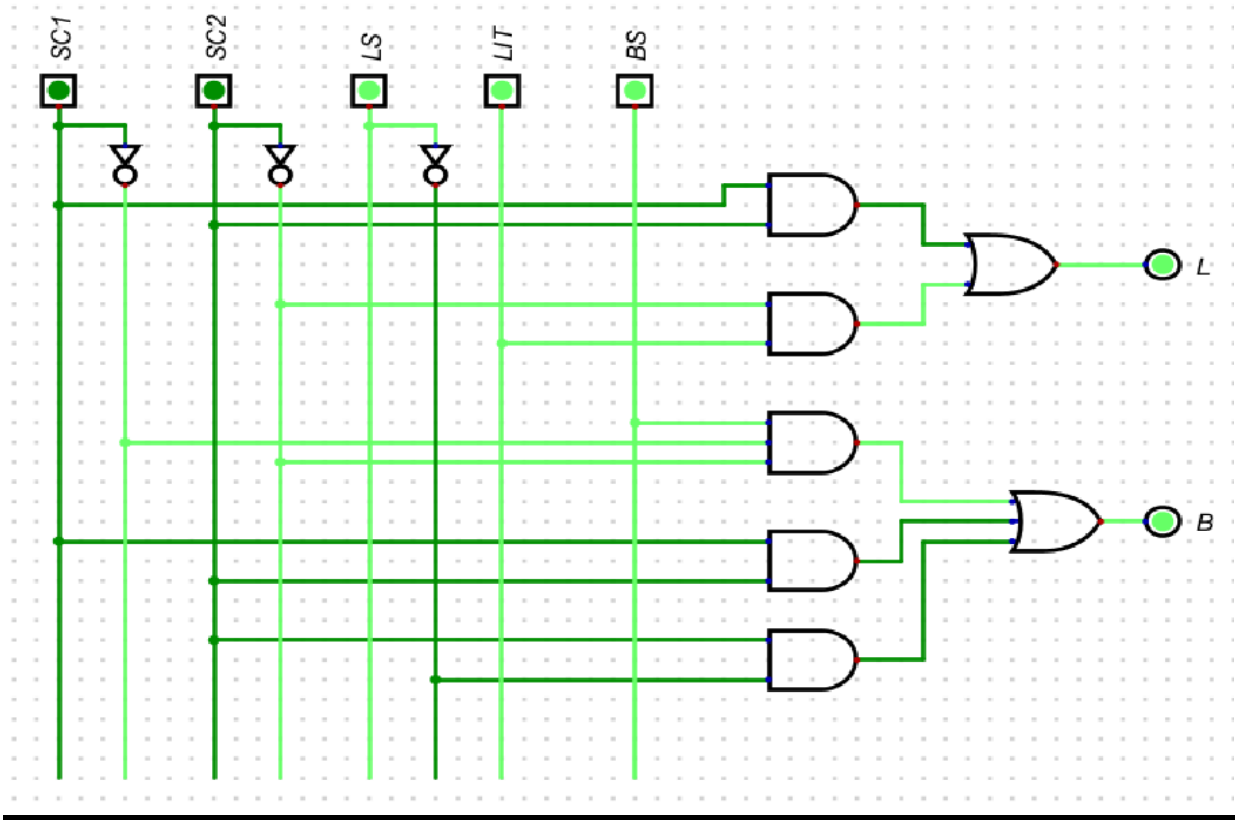



**Fig 4: Test table containing test plans and testbenches:**

| Req ID | Test Description | Stimuli | Expected Response | Coded in Testbench (Line No Range) | Digital Simulation Check | Testbench Simulation Check | 7400 Circuit Check | FPGA Check |
|---|---|---|---|---|---|---|---|---|
| R1.1 | Standard scene, all inputs inactive. | SC1=0,SC2=0, LS=0,LIT=0,BS=0 | L=0,B=0 | 47-51 | ok | ok | ok | ok |
| R1.2 | Standard scene, light switch active. | SC1=0,SC2=0, LS=0,LIT=1,BS=0 | L=1,B=0 | 53-57 | ok | ok | ok | ok |
| R1.3 | Standard scene, blind switch active. | SC1=SC2=0, LS=0,IT=1,BS=0 | L=0,B=1 | 59-63 | ok | ok | ok | ok |
| R1.4 | Standard scene, light and blind switches active. | SC1=SC2=0, LS=0,IT=1,BS=1 | L=1,B=1 | 65-69 | ok | ok | ok | ok |
| R2.1 | Lunchtime scene, light sensor & light switch active. | SC1=0,SC2=1, LS=1,LIT=1,BS=0 | L=0,B=0 | 72-76 | ok | ok | ok | ok |
| R2.2 | Lunchtime scene, all inputs inactive. | SC1=0,SC2=1, LS=0,LIT=0,BS=0 | L=0,B=0 | 78-82 | ok | ok | ok | ok |
| R2.3 | Lunchtime scene, all inputs active. | SC1=0,SC2=1, LS=1,LIT=1,BS=1 | L=0,B=1 | 84-88 | ok | ok | ok | ok |
| R2.4 | Lunchtime scene, light sensor & light switch active. | SC1=0,SC2=1, LS=1,LIT=1,BS=0 | L=0,B=0 | 90-94 | ok | ok | ok | ok |
| R3.1 | Nighttime scene, light switch active. | SC1=1,SC2=0, LS=0,LIT=1,BS=0 | L=1,B=0 | 97-101 | ok | ok | ok | ok |
| R3.2 | Nighttime scene, light & blind switches inactive. | SC1=1,SC2=0, LS=0,LIT=0,BS=0 | L=0,B=0 | 103-107 | ok | ok | ok | ok |
| R3.3 | Nighttime scene, light blind switches active. | SC1=1,SC2=0, LS=0,LIT=1,BS=1 | L=1,B=0 | 109-113 | ok | ok | ok | ok |
| R3.4 | Nighttime scene, light sensor active. | SC1=1,SC2=0, LS=1,LIT=0,BS=0 | L=0,B=0 | 115-119 | ok | ok | ok | ok |
| R4.1 | Emergency scene, all inputs inactive. | SC1=SC2=1, LS=0,LIT=0,BS=0 | L=1,B=1 | 122-126 | ok | ok | ok | ok |
| R4.2 | Emergency scene, all inputs active. | SC1=SC2=1, LS=1,LIT=1,BS=1 | L=1,B=1 | 128-132 | ok | ok | ok | ok |
| R4.3 | Emergency scene, light sensor active. | SC1=SC2=1, LS=1,LIT=0,BS=0 | L=1,B=1 | 134-138 | ok | ok | ok | ok |
| R4.4 | Emergency scene, all switches and sensor active. | SC1=SC2=1, LS=1,LIT=1,BS=1 | L=1,B=1 | 140-144 | ok | ok | ok | ok |

**Fig 5: The NAND only circuit:**

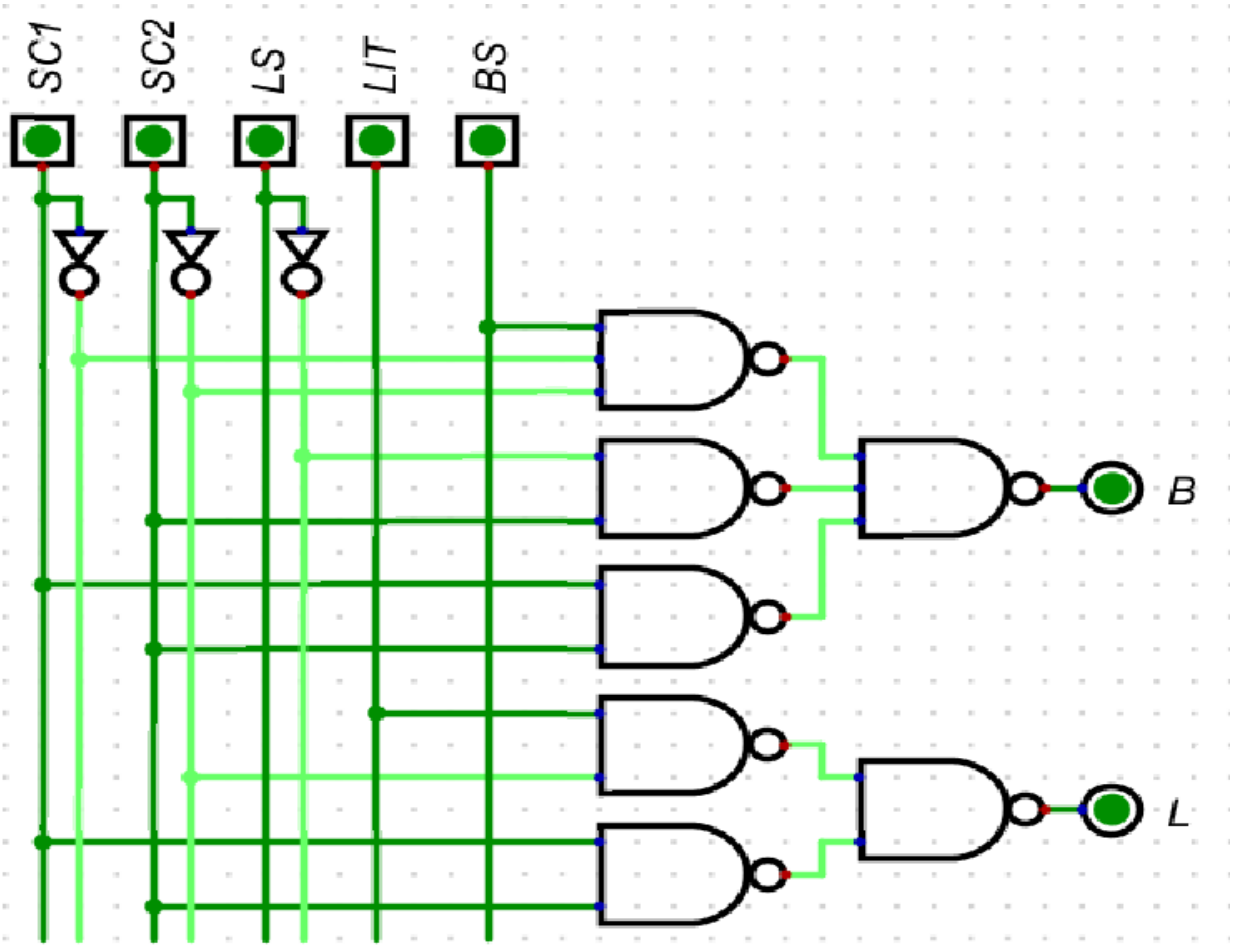



**Fig 6: Circuit with only light switch:**

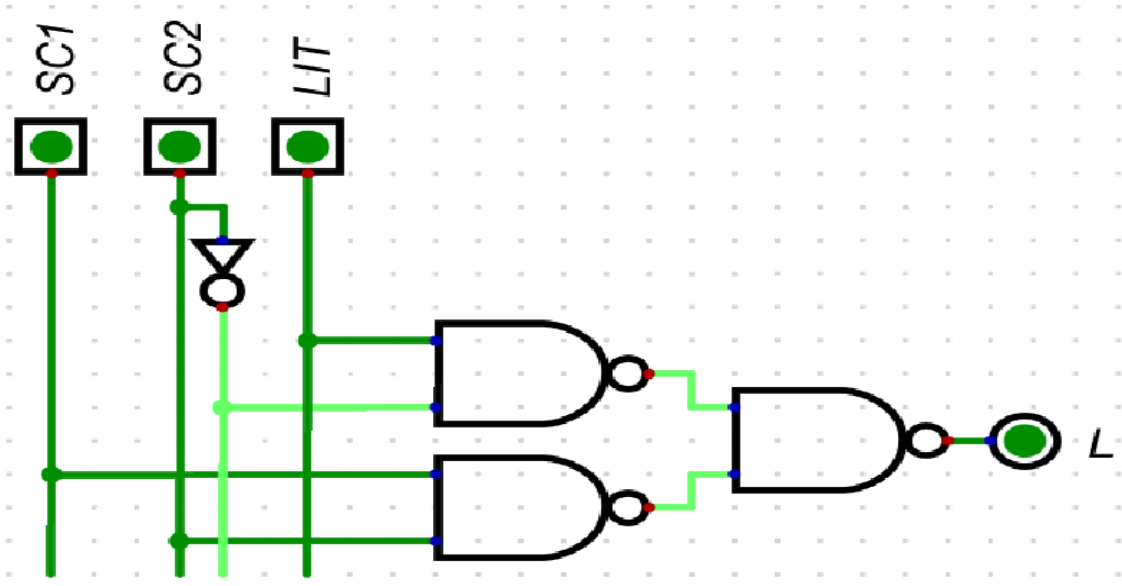


**Fig 7: Implementation of lamp control circuit on IC evaluation board:**

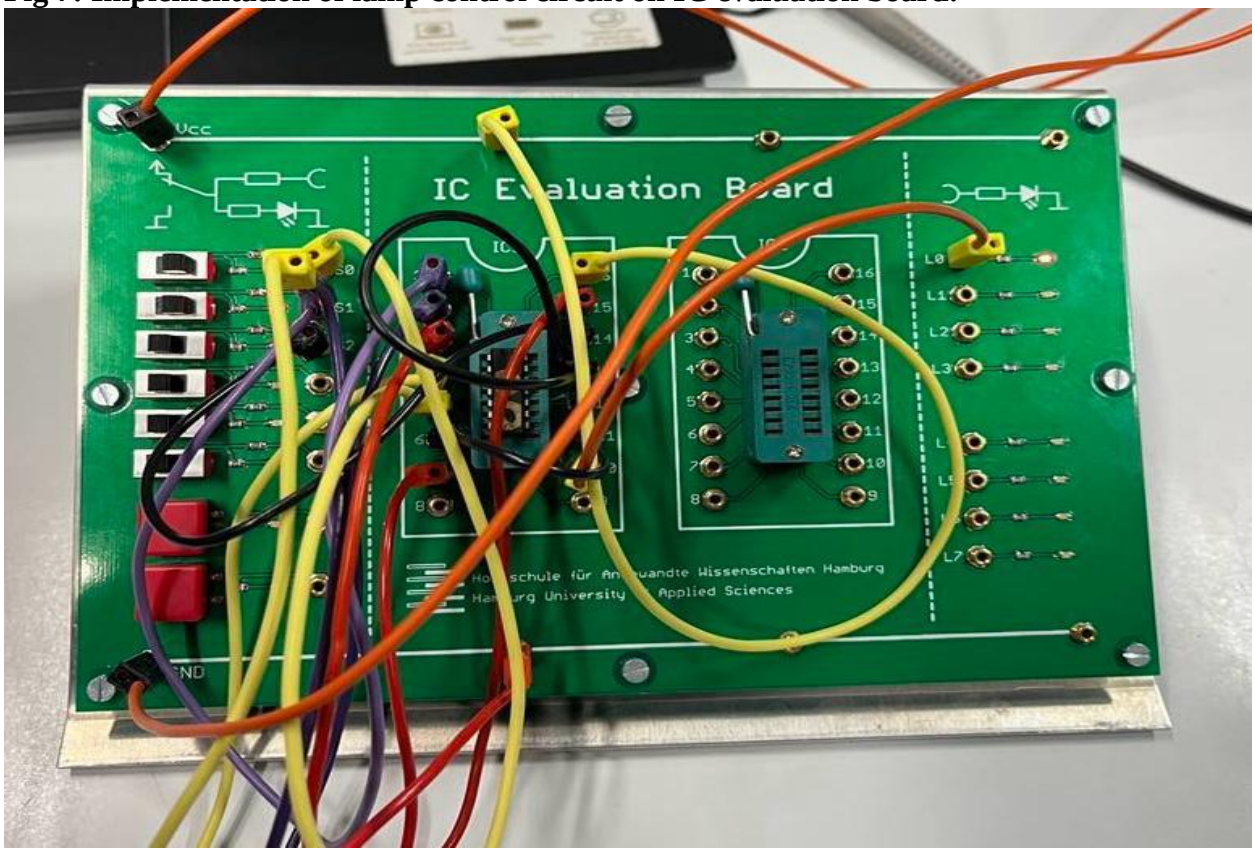



**Fig 8: Measuring propagation delay of lamp control circuit:**

**Fig 9: Measuring propagation delay of a single NAND gate:**

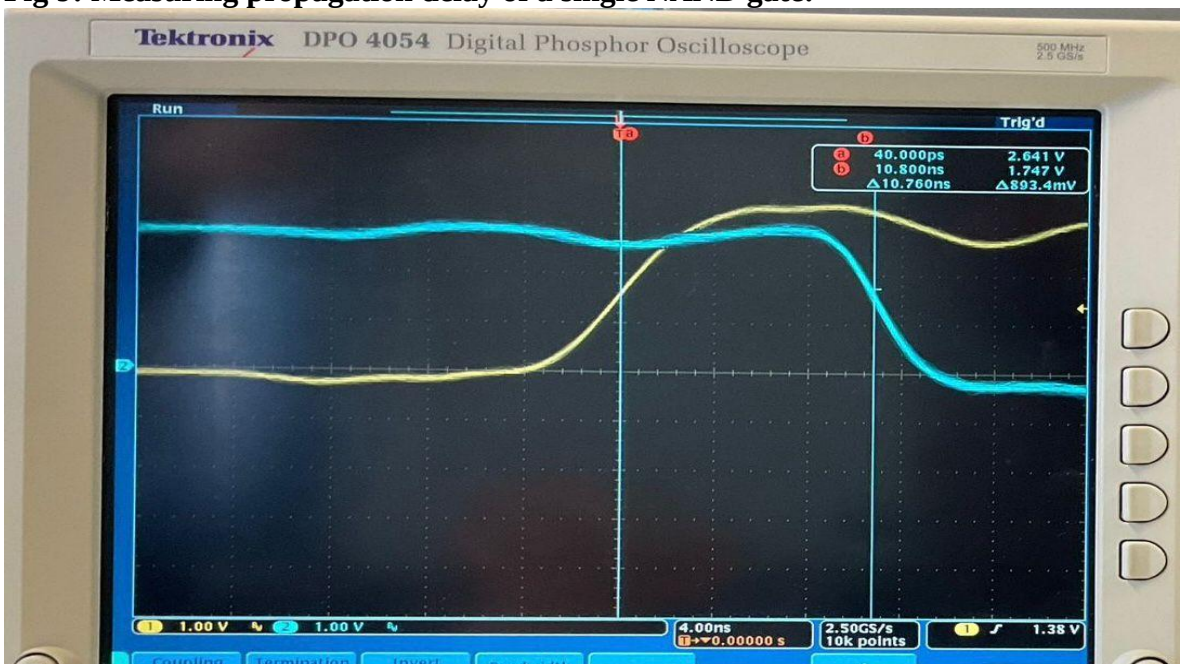
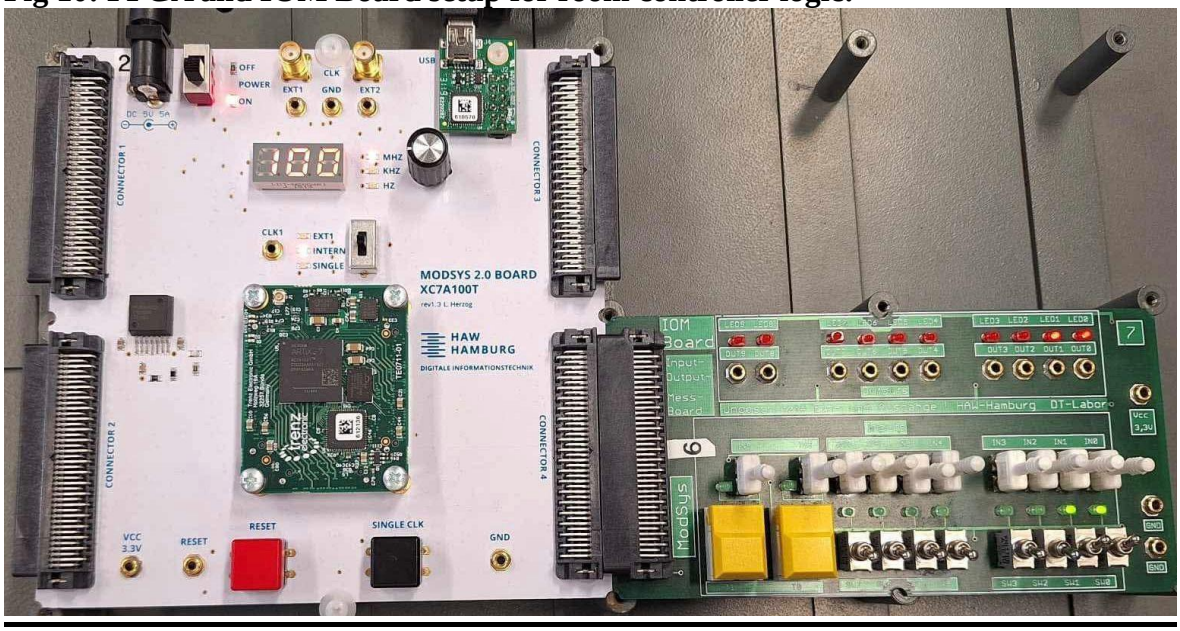



**Fig 10: FPGA and IOM Board setup for room controller logic:**



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**[4] H. Neemann, *Digital Circuit Design Tool*, Germany, 2024.**