Simon's algorithm in the NISQ cloud

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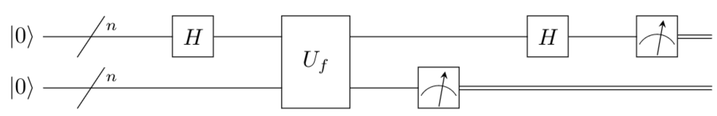
Abstract

Simon's algorithm demonstrates genuine quantum advantage, however, it assumes access to noise-free qubits. We use Simon's algorithm to benchmark the error rates of devices currently available in the "quantum cloud." Our main result is a comparison between the platforms made available by IBM and IonQ. This highlights the importance of understanding device architectures when transpiling quantum algorithms onto hardware. For instance, we show that two-qubit operations between distant superconducting qubits should be avoided.

Background

Simon's problem:

- Input: a black-box oracle function U_f which operates on bitstrings of size n.
  - U_f is two-to-one with a "secret string" s that relates input pairs.
- Objective: Determine s where the only allowable action is to make queries to U_f.
- Classical runtime is exponential in n. Quantum runtime is linear in n.



Simon's Algorithm: [1]

1. Initialize two quantum registers of size n in the $|0\rangle$ state.
2. Apply two Hadamard transformations and U_f to the registers as depicted above.
   - This creates a superposition in the first register over all size n bitstrings that are orthogonal to s.
3. Measure the registers to obtain a single size n bitstring that is orthogonal to s.

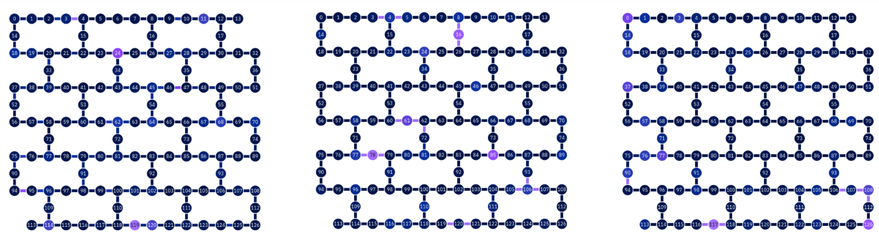
By iterating steps 1-3 to form a set of $n-1$ linearly independent bitstrings we can solve for s.

The Quantum Cloud

Several large corporations as well as smaller start-up companies have made their NISQ devices available for cloud access. For our study, we had access to IBM's superconducting platform and IonQ's trapped ion devices.

Superconducting qubits – IBM:

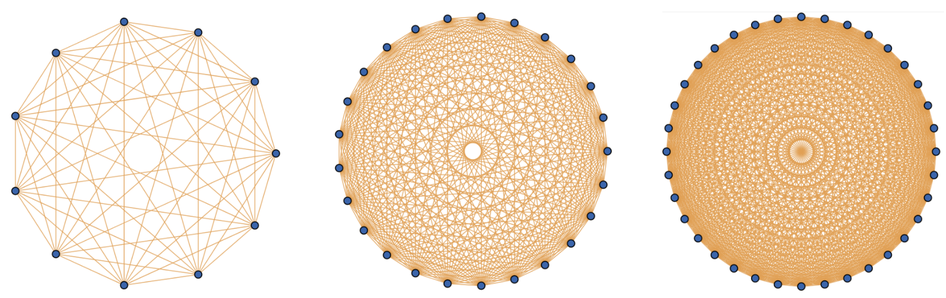
- Quantum processors made of superconducting transmon qubits.
- Physically located in dilution refrigerators at the Thomas J. Watson Research Center.
- Largest existing processor has 1,121 qubits.
- Chip topology limited to pairwise connections between qubits.
- We used the 127-qubit Brisbane, Osaka, and Kyoto (all instances of the Eagle chip design below).
- Noisy simulator models provided by IBM for these devices.



(a) IBM Brisbane (b) IBM Osaka (c) IBM Kyoto

Ion traps – IonQ:

- Quantum processors made of trapped ions.
- Physically located here in College Park.
- Largest existing processor has 36 qubits.
- Chip topology allows for all-to-all qubit connectivity.
- We used the 11-qubit Harmony, 25-qubit Aria, and 36-qubit Forte.
- Noisy simulator models provided by IonQ for Harmony and Aria.



(a) IonQ Harmony (b) IonQ Aria 1 (c) IonQ Forte 1

Methods & Results

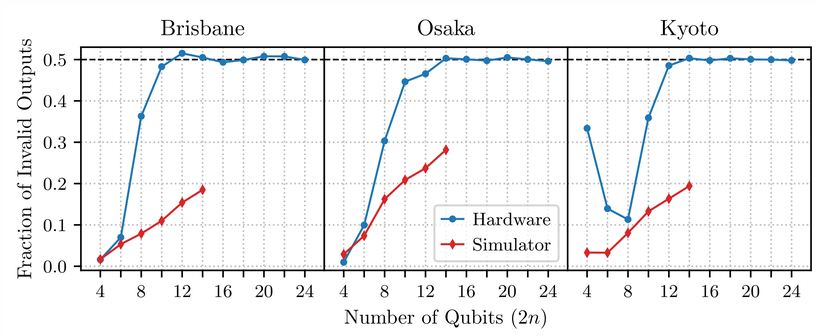
Methods:

Our objective was to determine the frequency with which Simon's algorithm failed on NISQ technology. To this end, we ran Simon's algorithm on the devices and simulator listed previously using the following process:

1. We initialized a variable n to iterate over the values 2—12.
2. For each n, we defined a two-to-one function using the string of n 1s as the secret string s.
   - This represents the most complex oracle in terms of the number of two-qubit gates required.
3. We prepared an implementation of Simon's algorithm to classify this function.
4. We repeated the implementation for 8192 shots.
5. We counted the fraction of shots that produced a final result *not* orthogonal to s—the *algorithmic error*.
   - These shots indicate presence of hardware noise which resulted in a failure of the implementation.
6. We averaged the algorithmic error of each device over many repetitions of steps 1-5, and plotted the results.

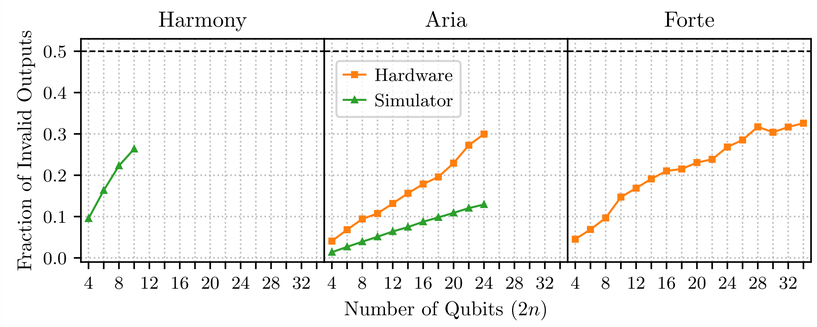
IBM Results:

- IBM simulators predict a roughly linear scaling in algorithmic error as a function of n.
- IBM devices experience a nonlinear jump in algorithmic error at $2n = 8$ (or $2n = 10$ for Kyoto).
  - This increase in error on hardware coincides with the addition of swap gates into the algorithm.
  - These swap operations may introduce correlated errors not captured in the simulators' noise model.
- The observed 50% algorithmic error for $2n \geq 12$ demonstrates a failure of the algorithm.



IonQ Results:

- IonQ simulators predict a roughly linear scaling in algorithmic error as a function of n.
- IonQ devices demonstrate a roughly linear scaling in algorithmic error as a function of n.
- On Aria, there is a roughly constant factor of 2 difference between the simulator and hardware results.
- The observed 30% algorithmic error for $2n \geq 24$ will likely nullify quantum advantage.



In sum, we find that the algorithmic error of Simon's algorithm on NISQ devices scales at least linearly, and all devices show irrecoverable error for intermediate-scale problems ($2n = 24$).

Physical Parameters of the NISQ Devices

Parameter	Brisbane	Osaka	Kyoto	Forte	Aria 1	Harmony
Manufacturer	IBM	IBM	IBM	IonQ	IonQ	IonQ
T1 Time	213.12 μs	297.17 μs	215.43 μs	100 s	100 s	10000 s
T2 Time	145.97 μs	127.23 μs	109.44 μs	1 s	1 s	0.2 s
2-Qubit Gate Speed	660 ns	660 ns	660 ns	970 μs	600 μs	200 μs
1-Qubit Gate Error (%)	0.03	0.03	0.03	0.09	0.06	0.67
2-Qubit Gate Error (%)	0.74	0.93	0.92	0.74	8.57	3.07
Average Readout Error (%)	1.32	2.18	1.48	0.5	0.52	0.42
Topology	Eagle r3	Eagle r3	Eagle r3	all-to-all	all-to-all	all-to-all

Notes:

- IBM reports median values; IonQ reports average values.
- IBM native gate set: ECR, ID, RZ, SX, and X.
- IonQ native gate set: MS, GPI, and GPI2 (Forte includes ZZ).

References

[1] D. R. Simon, On the power of quantum computation, SIAM Journal on Computing 26 (5) (1997) 1474–1483. arXiv: https://doi.org/10.1137/S0097539796298637, doi:10.1137/S0097539796298637.