

# Analysis and Modeling of InGaZnO Thin Film Transistor Common-Gate Amplifier

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**Abstract**—In this work, an InGaZnO (IGZO) thin film transistor (TFT) common-gate amplifier and a TFT small signal model are demonstrated. The fabricated amplifier achieves a DC gain of nearly 2 and 3dB bandwidth of roughly 30kHz. The model integrates the intrinsic parasitic capacitances of the amplifier and accurately predicts the experimentally measured frequency response when the measurement apparatus parasitics are considered.

**Index Terms**—Indium Gallium Zinc Oxide, thin film transistors, high speed analog integrated circuits

## I. INTRODUCTION

Amorphous thin film transistors are simple to fabricate and can be constructed on flexible substrates, making them a great platform for inexpensive wearable or embedded systems. InGaZnO (IGZO) is a popular material for thin film transistors due to its relatively high mobility and ease of fabrication [1]. Monolithic integration of analog and digital systems in IGZO could provide a solution for embedded/wearable computing and sensing, but in order to enable the design of analog circuits in a new material system, engineers need accurate models that quantitatively predict the behavior of their circuits across all frequencies. Typically, this is done with a small signal model of the transistor: a local linear approximation of the transistor around some operating point that includes an intrinsic transconductance and output resistance as well as parasitic capacitance and resistance. An accurate small signal model for a single transistor amplifier would capture virtually all of the parameters needed to model the behavior of complex, multi-transistor circuits.

To benchmark the accuracy of the small signal model, a common gate amplifier is fabricated in a three mask IGZO top gate process. The DC current-voltage characteristics of the process are measured to extract the DC small signal parameters of the amplifier core, while the small signal capacitances are estimated based on device geometry and materials. The small signal parameters are de-embedded from the IGZO parasitic sheet resistance, following a procedure similar to [2]. The model is then compared with the experimentally measured frequency response of the common-gate amplifier.

## II. BACKGROUND

### A. Common Gate Amplifier

The common gate amplifier configuration is often used in CMOS radio-frequency (RF) applications due to its real input impedance and ability to operate near its transit frequency  $f_T$  [3]. While there's no gate-drain overlap capacitance  $C_{gd}$  in the top-gate thin film transistor process used in this work (and thus

the degradation in bandwidth typically observed in a common source amplifier due to the Miller effect would be negligible), a common gate amplifier was chosen over the common source configuration to minimize overlap with the projects of other students. A circuit schematic of the common gate configuration is shown in Fig. 1:

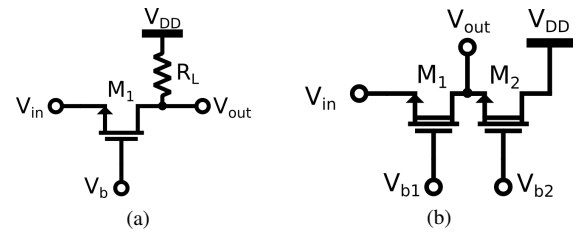


Fig. 1. Canonical common gate amplifier configuration with resistive load and common gate amplifier with active load.  $V_{b1}$  and  $V_{b2}$  are DC bias voltages that can be changed to alter the operating point of the amplifier.

### B. Thin-Film-Transistor Small Signal Model

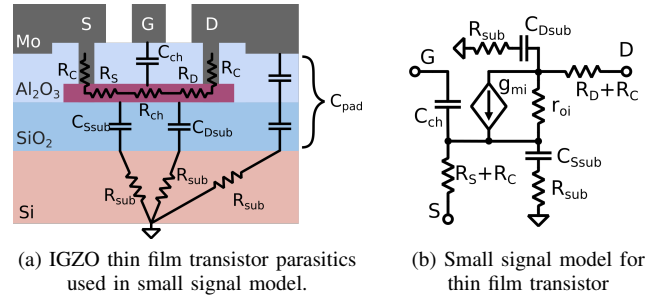


Fig. 2. IGZO thin film transistor small signal model and transistor cross section depicting origin of parasitics.

Unlike in traditional MOSFETs, thin film transistors typically have large contact resistance and depending on their geometry, little to no overlap capacitance [2]. In order to accurately model this effect, a new small signal model needs to be used which accounts for elevated contact resistance. Fig. 2a shows the various parasitic resistances and capacitances present in the top gate IGZO transistors. The Si substrate resistance  $R_{sub}$  is calculated assuming a resistivity of  $100\Omega\text{cm}$ , which assumes that the substrate has been lightly doped with Boron (roughly  $10^{14}/\text{cm}^3$  [4]). The capacitances  $C_{Ssub}$  and  $C_{Dsub}$  are lumped capacitances to model the distributed capacitance between the bottom of the IGZO transistor channel and the substrate.  $R_C$ ,  $R_S$ , and  $R_D$  model the IGZO-Mo contact

resistance and IGZO source/drain extension sheet resistance (respectively). The parasitics are combined to form the small signal model shown in Fig. 2b.

Since the contact and sheet resistance affect the measured IV characteristics, the intrinsic transconductance  $g_{mi}$  and output resistance  $r_{oi}$  must be de-embedded from the measured extrinsic transconductance  $g_m$  and output resistance  $r_o$ . The intrinsic small signal parameters can be de-embedded by following a similar procedure to [2], without making the simplifying assumption that  $R_S = R_D$ :

$$g_m = \frac{\partial I_D}{\partial V_{GS}}, \quad r_o = \frac{\partial V_{DS}}{\partial I_D} \quad (1)$$

$$r_{oi} = r_o - R_D - (1 + g_m r_o) R_S \quad (2)$$

$$g_{mi} = g_m \frac{r_o}{r_{oi}} \quad (3)$$

Fig. 3 shows a complete small signal model of the amplifier:

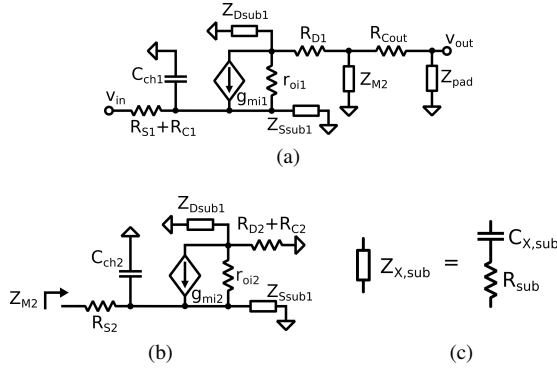


Fig. 3. Small signal model of amplifier. Fig. 3a shows the small signal model of the main amplifier.  $Z_{Dsub1}$  and  $Z_{Ssub1}$  are lumped capacitances to model the capacitance between the IGZO channel and the silicon substrate.  $Z_{pad,sub}$  is the capacitance between the output metal pad and the silicon substrate. Fig. 3b shows the small signal model for the load transistor  $M_2$  input impedance ( $Z_{M2}$ ) as seen by the drain of the amplifier transistor  $M_1$ .

### III. DEVICE FABRICATION

The common gate amplifier was fabricated with two transistors that share an IGZO mesa as shown in Fig. 4 and 5. Both transistors have a  $5\mu\text{m}$  channel with  $2\mu\text{m}$  ungated source/drain extensions. The active transistor  $M_1$  is  $80\mu\text{m}$  wide and the load transistor  $M_2$  is  $30\mu\text{m}$  wide. Fig. 4 shows the steps of the fabrication process. The devices were fabricated on a 6" p-type silicon wafer (Fig. 4a). Plasma-enhanced chemical vapor deposition was used to deposit 420nm of  $\text{SiO}_2$  on the wafer surface for electrical isolation from the substrate (Fig. 4b). Then, 8nm of IGZO was RF sputtered at 100W with flowrates of 20sccm Ar and 1sccm  $\text{O}_2$  at 1mtorr (Fig. 4c). AZ3312 photoresist and AZ726 developer were used for photolithography of the IGZO. The exposed IGZO was etched with 1:9  $\text{HCl}:\text{H}_2\text{O}$  for 10s to form the transistor channel (Fig. 4d). To form the gate oxide and IGZO passivation, 30nm of  $\text{Al}_2\text{O}_3$  was deposited with atomic layer deposition (Fig. 4e). The oxide vias were patterned with 10um AZ10XT photoresist and AZ435 developer. After a 7min spin-rinse

with the developer, the remaining AZ10XT and  $\text{Al}_2\text{O}_3$  were etched in a bath of AZ435 for an additional 20min (Fig. 4f). Next, 30nm of Mo was sputtered at 100W with 15sccm Ar at 2mtorr (Fig. 4g). Finally, the Mo was patterned with 1um thick AZ3312 photoresist and AZ726 developer. The exposed Mo was peroxide etched to form the metal contacts for the gate, drain, and source of the transistor (Fig. 4h).

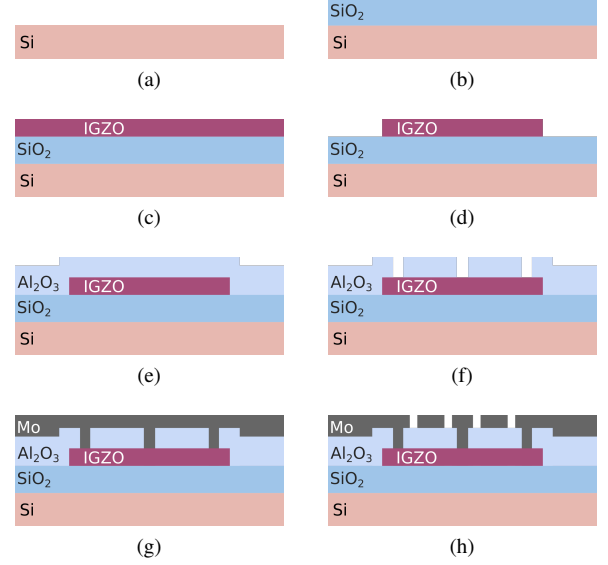


Fig. 4. Fabrication process of a pair of top-gate IGZO thin film transistors with a shared source/drain. Three masks are used (steps 4d, 4f, and 4h). This geometry can be configured as any of the single transistor amplifiers (common gate, common source, common drain). The common gate configuration is achieved by connecting the Mo pads (from left to right) to  $v_{in}$ ,  $V_{b1}$ ,  $v_{out}$ ,  $V_{b2}$ , and  $V_{DD}$ .

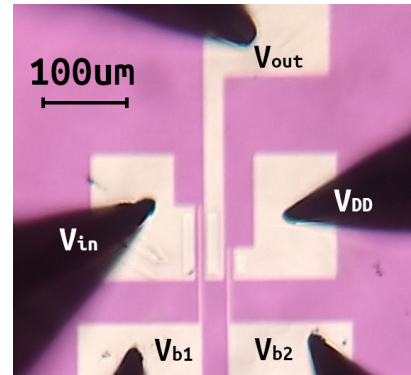


Fig. 5. Optical micrograph of fabricated common gate amplifier in probe station.

### IV. DEVICE CHARACTERIZATION AND TESTING

#### A. DC Characteristics of IGZO Process

A Keysight B1500A semiconductor device analyzer was used to measure the DC current-voltage characteristics of the individual  $80\mu\text{m}/5\mu\text{m}$  and  $30\mu\text{m}/5\mu\text{m}$  transistors as shown in Fig. 6a. The semiconductor analyzer was also used to measure the contact and sheet resistance of the IGZO film using a

series of two-point measurements on IGZO resistors of various dimensions.

### B. DC Gain and Bandwidth of Common Gate Amplifier

The common gate amplifier is configured as shown in Fig. 1b with the  $80\mu\text{m}/5\mu\text{m}$  transistor ( $M_1$ ) used as the amplifying transistor and the  $30\mu\text{m}/5\mu\text{m}$  transistor ( $M_2$ ) as an active load. The differential DC gain  $\Delta V_{out}/\Delta V_{in}$  was measured with the semiconductor device analyzer across a wide range of bias points to determine the optimal point for maximum gain.

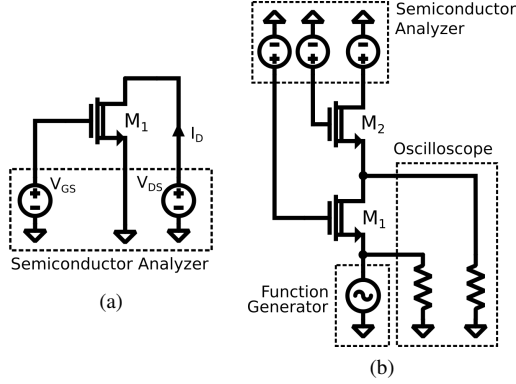


Fig. 6. Experimental setups for measuring the IV characteristics of a single transistor (Fig. 6a) and the frequency response of the common gate amplifier (Fig. 6b)

Fig. 6b shows a setup schematic for measurement of the amplifier's frequency response. The frequency response of the common gate amplifier was measured with a Keysight DSOX2014A oscilloscope and a Keysight 33520A 80MHz function generator. The function generator was set to produce a sinusoidal tone with a  $200\text{mV}_{pp}$  output swing connected to the input terminal of the amplifier. The oscilloscope was used to measure the function generator output as well as the output of the amplifier. The amplitude ratio and relative phase of the input and output signals were measured for frequencies from 500Hz to 1MHz. The DC biases  $V_{b1}$ ,  $V_{b2}$ , and  $V_{DD}$  were set with the source-measurement units of the semiconductor analyzer in standby mode.

## V. RESULTS

The sheet and contact resistances  $R_S$ ,  $R_D$ , and  $R_C$  used in the small signal model (Fig. 2b) were extracted from Fig. 7a. The slope of the resistance vs. IGZO rectangle aspect ratio gives the sheet resistance in  $\Omega/\square$  and the y-intercept is twice the contact resistance between the Mo and IGZO. The bulk resistivity and contact resistance were estimated to be  $\rho \approx 0.06\Omega\cdot\text{cm}$  (good agreement with literature [5]) and  $\rho_C \approx 0.022\Omega\cdot\text{cm}^2$ .

Fig. 8 shows the measured IV characteristics of the  $80\mu\text{m}/5\mu\text{m}$  and  $30\mu\text{m}/5\mu\text{m}$  devices. Both demonstrate an  $I_{on}/I_{off}$  ratio of about  $10^5$  and some amount of finite output resistance. The current density (normalized to the transistor width) for the same bias point was substantially lower for the  $30\mu\text{m}$  device than the  $80\mu\text{m}$  device. This is most likely due to

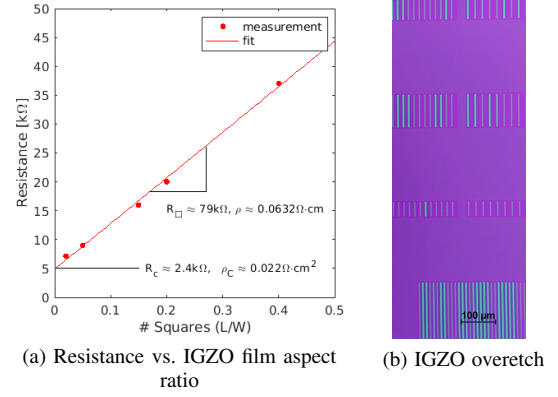


Fig. 7. Resistance of the IGZO film and properties of the IGZO-Mo interface. Fig. 7a shows the results of two-point resistance measurements of 8nm thick IGZO films of varying aspect ratios. The Mo-IGZO contact area was  $900\mu\text{m}^2$ . Fig. 7b is a contrast-enhanced optical micrograph of resistance test structures after etching of  $\text{Al}_2\text{O}_3$  vias. Some of the IGZO has been overetched. This resulted in many non-ohmic contacts (measurements not shown).

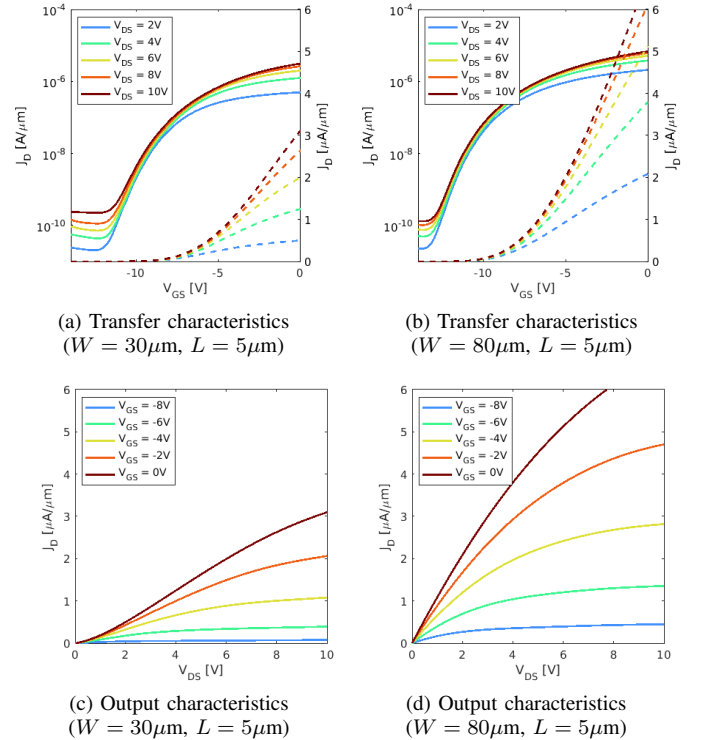


Fig. 8. Transfer and output characteristics of  $80\mu\text{m}/5\mu\text{m}$  and  $30\mu\text{m}/5\mu\text{m}$  transistors used in the amplifier. This data was measured after weeks of testing the transistor pair in different amplifier configurations.

the higher resistance of the  $2\mu\text{m}$  source/drain extensions for the  $30\mu\text{m}$  wide device. The extrinsic small signal parameters  $g_m$  and  $r_o$  were extracted from the full set of IV data and equation 3 was used to de-embed the intrinsic parameters  $g_{mi}$  and  $r_{oi}$ . The product  $g_{mi}r_{oi}$  is plotted for each transistor in Fig. 9.  $g_{mi}r_{oi}$  is the intrinsic gain of a transistor, and is the maximum possible DC voltage gain of a single transistor amplifier constructed with an ideal source and load.

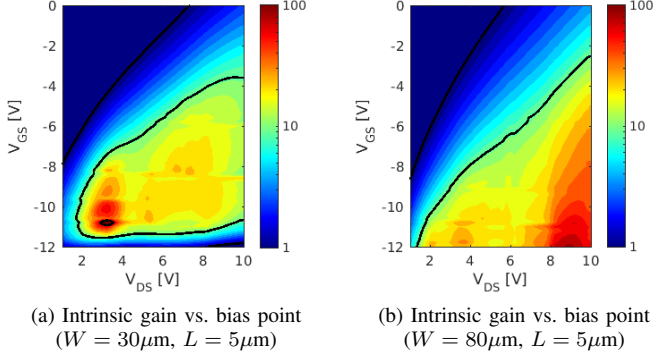


Fig. 9. Intrinsic gain  $g_{mi}r_{oi}$  for the two transistors used in the amplifier.

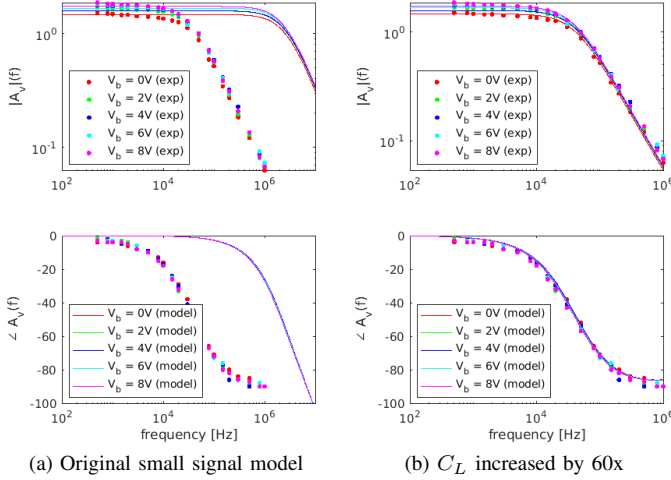


Fig. 10. Comparison of small signal model with experimental data. Points show experimental data and solid lines show the small signal model.

## VI. DISCUSSION

### A. Small Signal Model Agreement With Experiment

Fig. 10 shows that the small signal model correctly predicts the low frequency ( $<1\text{kHz}$ ) gain of the amplifier quite well for the different bias points. However, in Fig. 10a, the model overestimates the cutoff frequency of the amplifier by about 60x. The dominant capacitance is the amplifier output node capacitance between the Mo pad and the Si substrate, and is approximately 1.7pF. The capacitance between the IGZO channel and silicon substrate, while included in the small signal model for completeness sake, did not have a noticeable effect on the first two poles of the amplifier transfer function. The only capacitances not accounted for in the model are the fringing capacitance between the metal contacts and the capacitance of the measurement equipment. This fringing capacitance should be orders of magnitude lower than any of the other capacitances, and can be neglected. However, due to the construction of the triaxial cables used with the semiconductor analyzer SMUs, they can have relatively high capacitance (as much as 90-380pF/m of cable depending on how the central guard shield is terminated in the triax-coax adapter) [6]. A load

capacitance presented by the measurement equipment of just 60pF would explain the inaccuracy of the small signal model (Fig. 10b). Therefore, the cutoff frequency of the fabricated amplifier structure should be about 1.7-1.8MHz for the same bias points (based on Fig. 10a). If the large Mo pads used for measurement weren't included in the layout, i.e. in an integrated setting where the amplifier is driving some other onchip components, the cutoff frequency could be as high as 6MHz based on the other intrinsic capacitances in the device. In order to verify that the amplifier can actually function at such high frequencies, more experiments with specialized equipment, such as a network analyzer (which could calibrate out the cable capacitance), would need to be done.

### B. Proper Load Selection

As configured in Fig. 1b, the gain of this device as predicted by the small signal model is relatively poor compared to the device intrinsic gain. This is because the load is effectively in a common gate configuration, and thus presents a load impedance of:

$$Z_L(\omega = 0) = R_S + \frac{R_D + r_{oi}}{1 + g_{mi}r_{oi}} = \frac{1 + g_{m}r_o R_S + r_o}{1 + g_m(R_S + r_o)} \quad (4)$$

$$\approx R_S + \frac{1}{g_m} \quad (g_m r_o \gg g_m R_S, 1) \quad (5)$$

If the load transistor were diode connected with the gate and source shorted together, then its input impedance would be  $r_{o2}$ , and the DC gain would likely be closer to the maximum gain allowed by the transistor intrinsic gain  $g_{m1}(r_{o1}||r_{o2})$ . Based on the intrinsic gain  $g_{mi}r_{oi}$  in Fig. 9, this could be as high as 10, or even 20 for a similar level of bias current.

## VII. SUPPLEMENTAL INFORMATION AND MODEL CODE

Measured IV curves and Matlab code for the small signal model can be found at <https://github.com/reed-foster/common-gate-model>.

### ACKNOWLEDGMENT

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