Nicolas Reed

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Education

University of California, Berkeley GPA: 3.66/4.00
B.S. Electrical Engineering & Computer Sciences (EECS) *Expected May 2027*

Relevant coursework: Tapeout, Digital Design and Integrated Circuits (with ASIC Lab), Computer Architecture, Operating Systems, Signals and Circuits, Data Structures, Internet of Things, Foundations of Data Science

Experience

Apple Cupertino, CA
[Incoming] Hardware Engineering Intern *May 2026 – August 2026*

- Silicon Enginering Group: SoC Design Verification

Sandisk Milpitas, CA
Software Development Intern *May 2025 – August 2025*

- Reconciled CMDB and inventory data for 40,000+ virtual machines with Pandas, standardizing records, surfacing gaps, and producing migration plans for a cloud provider transition.
- Built an AI assistant with LlamaIndex and NLP to streamline license and contract workflows across 10,000 enterprise applications, improving compliance and reducing spend.

UC Berkeley SLICE Lab Berkeley, CA
Undergraduate Research Assistant - advised by Professor Sagar Karandikar *May 2025 – Present*

- Created a telemetry pipeline for Chipyard and FireSim on AWS S3, boosting debugging and reproducibility.
- Prepared a structured dataset of runs and metrics to enable LLM-driven regression triage and automated insights.

UC Berkeley Electrical Engineering & Computer Sciences (EECS) Berkeley, CA
Head Teaching Assistant *June 2024 – Present*

- Support 1,200+ students with C, RISC-V, and Python through office hours and an online forum.
- Ranked 1st among staff in helpfulness and teaching effectiveness.
- Host weekly lab sections for 50+ students, guiding programming exercises and problem-solving practice.
- Develop weekly homework and lab assignments, and maintain course infrastructure using GitHub and Docker.
- Answer 1,500+ student questions per semester to lead online forum engagement.

Micross Components - Silicon Turnkey Solutions Milpitas, CA
Engineering Intern *July 2023 – August 2023*

- Conducted mechanical and PCB testing on 1,000+ devices, translating results into actionable insights via Excel.
- Resolved a test issue by documenting compromised semiconductors and identifying the damage stage.

Projects

TSMC 16nm IoT SoC Tapeout - *Chisel, Chipyard, Hammer* 2026

- Contributed to a large-scale SoC tapeout with Apple mentorship, owning a block and driving signoff closure.

5-Stage Pipelined RISC-V CPU with I/D Caches - *Verilog* 2025

- Apple New Silicon Initiative Design Contest Winner: delivered best performance and area.
- Boosted throughput and frequency by refining hazard control and forwarding, reducing stall cycles.
- Achieved single-cycle read hits and two-cycle write hits and implemented optimized write-back logic.

Pintos Operating System - *C* 2025

- Extended core OS support for process control and system calls, handling invalid user memory safely.
- Added multithreading and synchronization primitives, enforcing priority scheduling to prevent inversion.
- Built UNIX-style file system features including caching, file growth, and subdirectories to improve I/O.

Scheme Interpreter - *Python* 2024

- Implemented an interpreter for a subset of Lisp (Scheme), supporting core expressions and syntax.
- Applied semantic and lexical analysis techniques that machines use to evaluate and execute code.

Technical Skills

Languages: Verilog, SystemVerilog, C, Python, RISC-V, Chisel, Scala, Java, x86. SQL, MATLAB
Tools & Frameworks: Git, Cadence Innovus, GDB, Valgrind, Pandas, NumPy, Docker, LTSpice