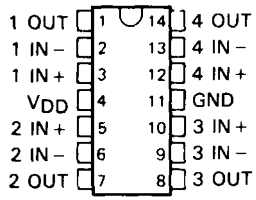
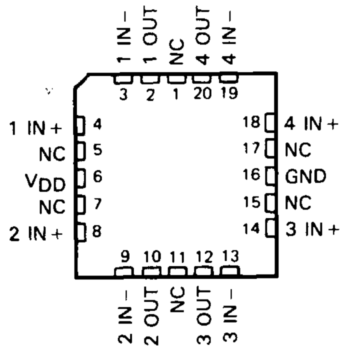
D3142, OCTOBER 1987—REVISED OCTOBER 1990

- **Trimmed Offset Voltage:**
  TLC27L9 . . . 900 µV Max at 25°C, V_{DD} = 5 V
- **Input Offset Voltage Drift . . . Typically 0.1 µV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  0°C to 70°C . . . 3 V to 16 V
  −40°C to 85°C . . . 4 V to 16 V
  −55°C to 125°C . . . 4 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)**
- **Ultra-Low Power . . . Typically 195 µW at 25°C, V_{DD} = 5 V**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up Immunity**

D, J, OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



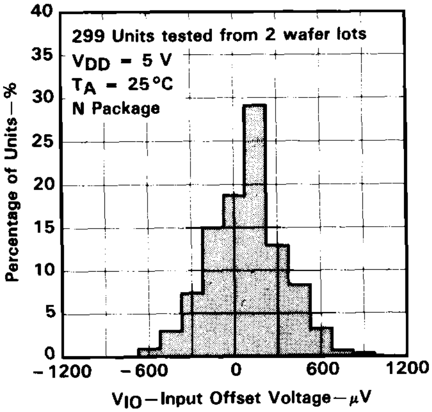
NC—No internal connection

AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE: SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	900 µV	TLC27L9CD	—	—	TLC27L9CN
	2 mV	TLC27L4BCD	—	—	TLC27L4BCN
	5 mV	TLC27L4ACD	—	—	TLC27L4ACN
	10 mV	TLC27L4CD	—	—	TLC27L4CN
−40°C to 85°C	900 µV	TLC27L9ID	—	—	TLC27L9IN
	2 mV	TLC27L4BID	—	—	TLC27L4BIN
	5 mV	TLC27L4AID	—	—	TLC27L4AIN
	10 mV	TLC27L4ID	—	—	TLC27L4IN
−55°C to 125°C	900 µV	TLC27L9MD	TLC27L9MFK	TLC27L9MJ	TLC27L9MN
	10 mV	TLC27L4MD	TLC27L4MFK	TLC27L4MJ	TLC27L4MN

The D package is available in tape and reel. Add R suffix to the device type, (e.g., TLC27L9CDR).

DISTRIBUTION OF TLC27L9
INPUT OFFSET VOLTAGE



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description

The TLC27L4 and TLC27L9 quad operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, extremely low power, and high gain.

These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and low power consumption make these cost-effective devices ideal for high gain, low frequency, low power applications. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27L4 (10 mV) to the high-precision TLC27L9 (900 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27L4 and TLC27L9. The devices also exhibit low voltage single-supply operation and ultra-low power comsumption, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

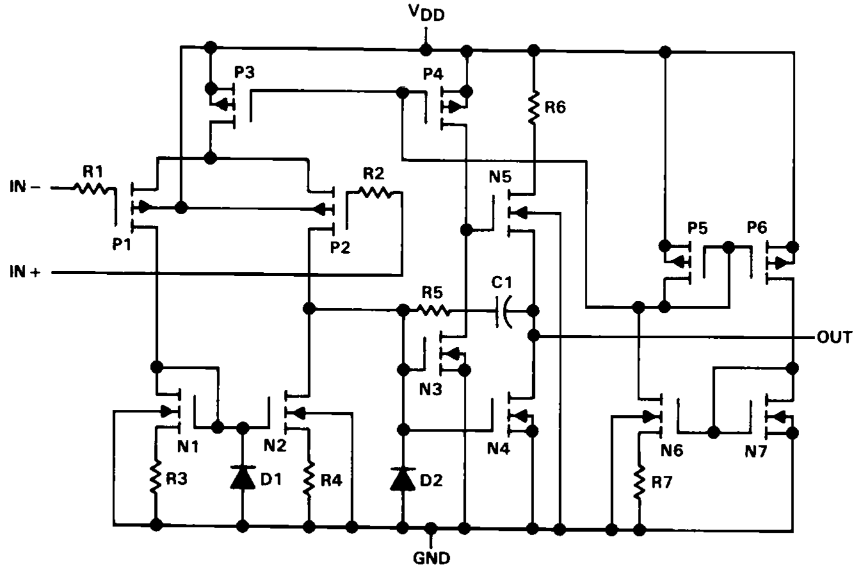
A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up.

The TLC27L4 and TLC27L9 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices, as exposure to ESD may result in the degradation of the device parametric performance.

C-suffix devices are characterized for operation from 0°C to 70°C. I-suffix devices are characterized for operation from −40°C to 85°C. M-suffix devices are characterized for operation from −55°C to 125°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . 18 V
Differential input voltage (see Note 2) . . . . $\pm V_{DD}$
Input voltage range, V_I (any input) . . . . -0.3 V to V_{DD}
Input current, I_I . . . . ± 5 mA
Output current, I_O (each output) . . . . ± 30 mA
Total current into V_{DD} terminal . . . . 45 mA
Total current out of ground terminal . . . . 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . Unlimited
Continuous total dissipation . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: C-suffix . . . . 0°C to 70°C
I-suffix . . . . -40°C to 85°C
M-suffix . . . . -55°C to 125°C
Storage temperature range . . . . -65°C to 150°C
Case temperature for 60 seconds: FK package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N package . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	

recommended operating conditions

		C-SUFFIX			I-SUFFIX			M-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		3		16	4		16	4		16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 5$ V	-0.2		3.5	-0.2		3.5	0		3.5	V
	$V_{DD} = 10$ V	-0.2		8.5	-0.2		8.5	0		8.5	
Operating free-air temperature, T_A		0		70	-40		85	-55		125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	mV
		TLC27L4AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		0.9	5	mV
					Full range			6.5	mV
		TLC27L4BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		240	2000	μV
					Full range			3000	μV
		TLC27L9C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		200	900	μV
					Full range			1500	μV
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					70°C		7	300	pA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					70°C		40	600	pA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	3.2	4.1		V
					0°C	3	4.1		V
					70°C	3	4.2		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	mV
					70°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 1 MΩ	25°C	50	520		V/mV
					0°C	50	680		V/mV
					70°C	50	380		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	94		dB
					0°C	60	95		dB
					70°C	60	95		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					0°C	60	97		dB
					70°C	60	98		dB
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		40	68	μA
					0°C		48	84	μA
					70°C		31	56	μA

†Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27L4AC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	
				Full range			6.5	
		TLC27L4BC	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		260	2000	μV
				Full range			3000	
		TLC27L9C	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		210	1200	
				Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	8	8.9		V
				0°C	7.8	8.9		
				70°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				0°C		0	50	
				70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 1 MΩ	25°C	50	870		V/mV
				0°C	50	1020		
				70°C	50	660		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	97		dB
				0°C	60	97		
				70°C	60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				0°C	60	97		
				70°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		57	92	μA
				0°C		72	132	
				70°C		44	80	

†Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			13	mV
		TLC27L4AI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.9	5	mV
				Full range			7	mV
		TLC27L4BI	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		240	2000	μV
				Full range			3500	μV
		TLC27L9I	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		200	900	μV
				Full range			2000	μV
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.1		pA
				85°C		24	1000	pA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V, V_{IC} = 2.5 V	25°C		0.6		pA
				85°C		200	2000	pA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		V
				−40°C	3	4.1		V
				85°C	3	4.2		V
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−40°C		0	50	mV
				85°C		0	50	mV
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V, R_L = 1 MΩ	25°C	50	480		V/mV
				−40°C	50	900		V/mV
				85°C	50	330		V/mV
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	94		dB
				−40°C	60	95		dB
				85°C	60	95		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				−40°C	60	97		dB
				85°C	60	98		dB
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, V_{IC} = 2.5 V, No load	25°C		39	68	μA
				−40°C		62	108	μA
				85°C		29	52	μA

†Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			13	
		TLC27L4AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		0.9	5	
					Full range			7	
		TLC27L4BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		260	2000	μV
					Full range			3500	
		TLC27L9I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		210	1200	
					Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					85°C		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	8	8.9		V
					−40°C	7.8	8.9		
					85°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	25°C	50	800		V/mV
					−40°C	50	1550		
					85°C	50	585		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	97		dB
					−40°C	60	97		
					85°C	60	98		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−40°C	60	97		
					85°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		57	92	μA
					−40°C		98	172	
					85°C		40	72	

†Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L9M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 1 MΩ	25°C		200	900	µV
					Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		1.4		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 4	−0.3 to 4.2		V
					Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	3.2	4.1		V
					−55°C	3	4.1		
					125°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 1 MΩ	25°C	50	480		V/mV
					−55°C	25	950		
					125°C	25	200		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	94		dB
					−55°C	60	95		
					125°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−55°C	60	97		
					125°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		39	68	µA
					−55°C		69	120	
					125°C		27	48	

†Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10	mV
				Full range			12	
		TLC27L9M	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		210	1200	μV
				Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 125°C		1.4		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.1		pA
				125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V, V_{IC} = 5 V	25°C		0.7		pA
				125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	0 to 9	−0.3 to 9.2		V
				Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	8	8.9		V
				−55°C	7.8	8.8		
				125°C	7.8	9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50	mV
				−55°C		0	50	
				125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V, R_L = 1 MΩ	25°C	50	800		V/mV
				−55°C	25	1750		
				125°C	25	380		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min	25°C	65	97		dB
				−55°C	60	97		
				125°C	60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		dB
				−55°C	60	97		
				125°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, V_{IC} = 5 V, No load	25°C		57	92	μA
				−55°C		111	192	
				125°C		35	60	

†Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				0°C		0.04		
				70°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.03		
				0°C		0.03		
				70°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				0°C		6		
				70°C		4.5		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				0°C		100		
				70°C		65		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				0°C		36°		
				70°C		30°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				0°C		0.05		
				70°C		0.04		
			V_{IPP} = 5.5 V	25°C		0.04		
				0°C		0.05		
				70°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				0°C		1.3		
				70°C		0.9		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				0°C		125		
				70°C		90		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				0°C		40°		
				70°C		34°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				−40°C		0.04		
				85°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.03		
				−40°C		0.04		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				−40°C		7		
				85°C		4		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				−40°C		130		
				85°C		55		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				−40°C		38°		
				85°C		28°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				−40°C		0.06		
				85°C		0.03		
			V_{IPP} = 5.5 V	25°C		0.04		
				−40°C		0.05		
				85°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				−40°C		1.4		
				85°C		0.8		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				−40°C		155		
				85°C		80		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				−40°C		42°		
				85°C		32°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				−55°C		0.04		
				125°C		0.02		
			V_{IPP} = 2.5 V	25°C		0.03		
				−55°C		0.04		
				125°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				−55°C		8		
				125°C		3		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				−55°C		140		
				125°C		45		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				−55°C		39°		
				125°C		25°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				−55°C		0.06		
				125°C		0.03		
			V_{IPP} = 5.5 V	25°C		0.04		
				−55°C		0.06		
				125°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				−55°C		1.5		
				125°C		0.7		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				−55°C		165		
				125°C		70		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				−55°C		43°		
				125°C		29°		

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC27L4 and TLC27L9 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.

FIGURE 1. UNITY-GAIN AMPLIFIER

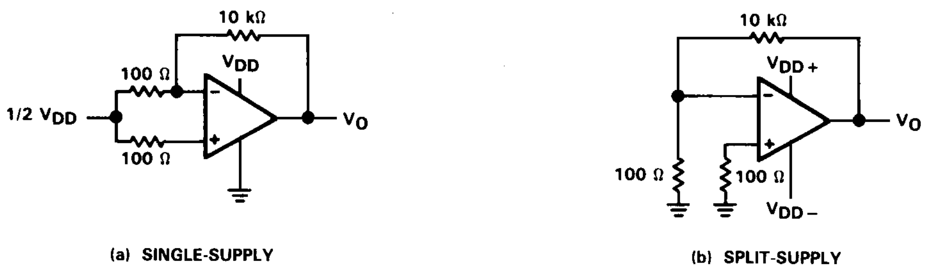


FIGURE 2. NOISE TEST CIRCUIT

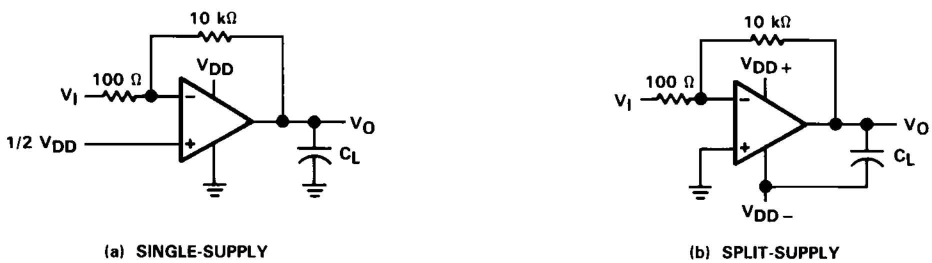


FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

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PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC27L4 and TLC27L9 op amps, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the ''open-socket'' leakage readings from the readings obtained with a device in the test socket.

One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an ''open-socket'' reading is not feasible using this method.

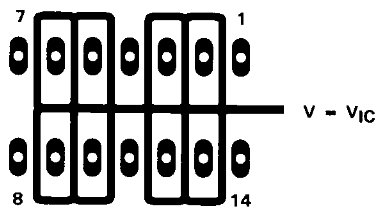


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS (J AND N DUAL-IN-LINE-PACKAGE)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

input offset voltage temperature coefficient

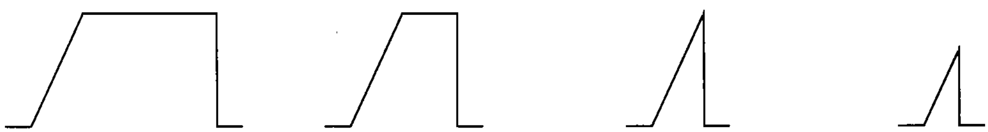
Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

PARAMETER MEASUREMENT INFORMATION

full-power response

Full-power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for ''significant'' distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



(a) f = 100 Hz (b) B_{OM} > f > 100 Hz (c) f = B_{OM} (d) f > B_{OM}

FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

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TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC27L4
INPUT OFFSET VOLTAGE

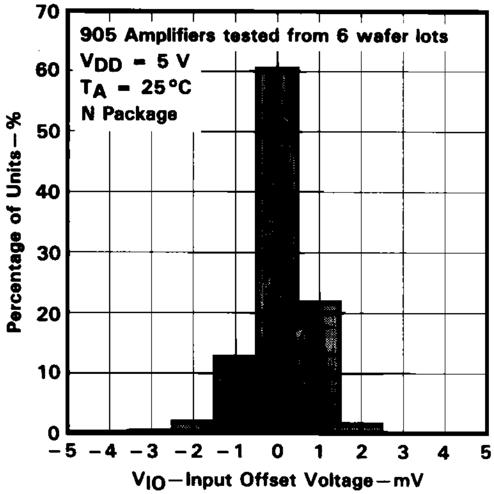

FIGURE 6

DISTRIBUTION OF TLC27L4
INPUT OFFSET VOLTAGE

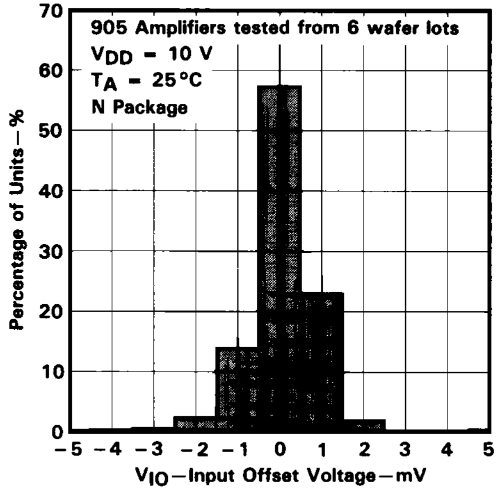

FIGURE 7

DISTRIBUTION OF TLC27L4 AND TLC27L9
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

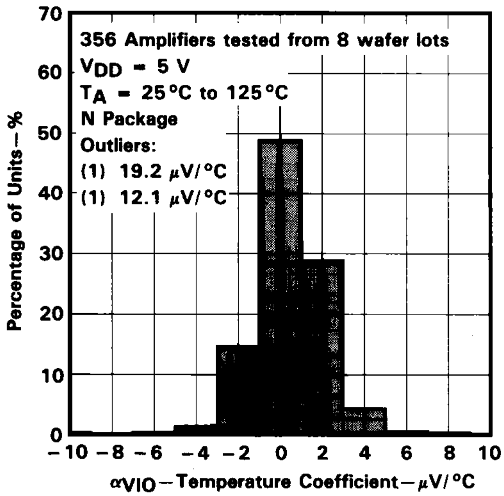

FIGURE 8

DISTRIBUTION OF TLC27L4 AND TLC27L9
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

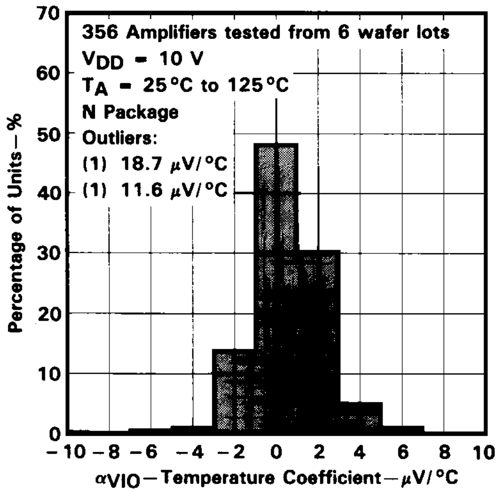

FIGURE 9

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

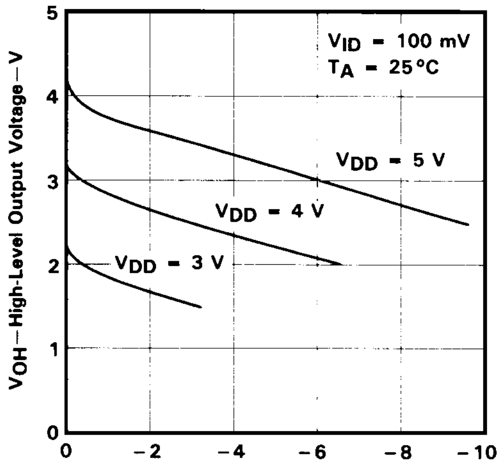

FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

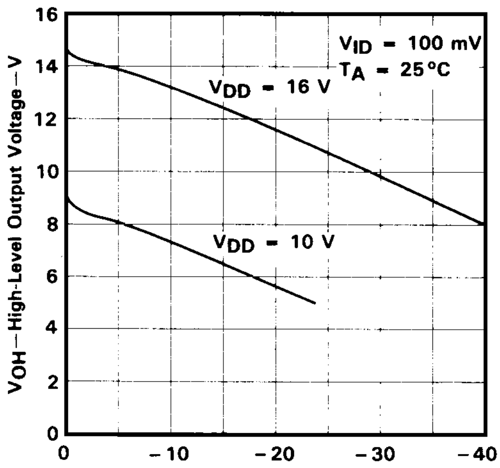

FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

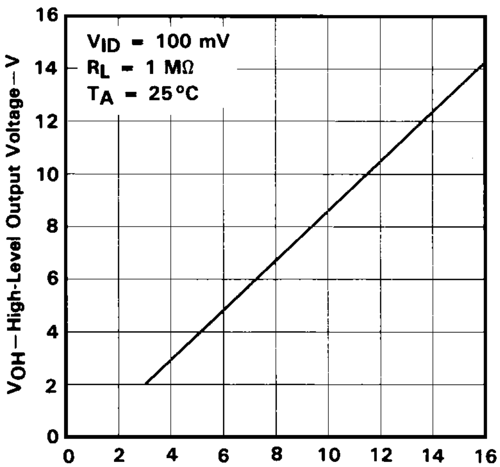

FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

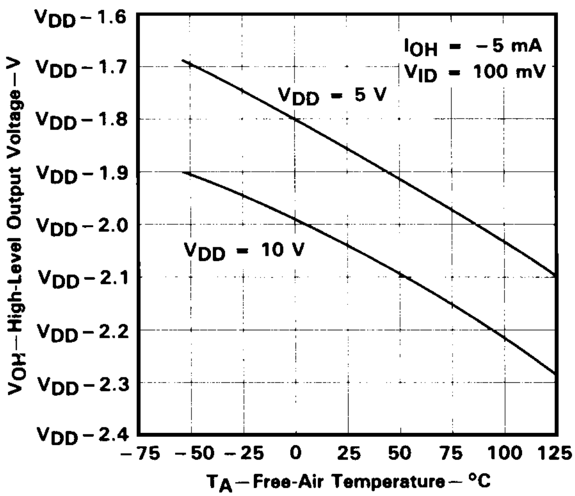

FIGURE 13

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

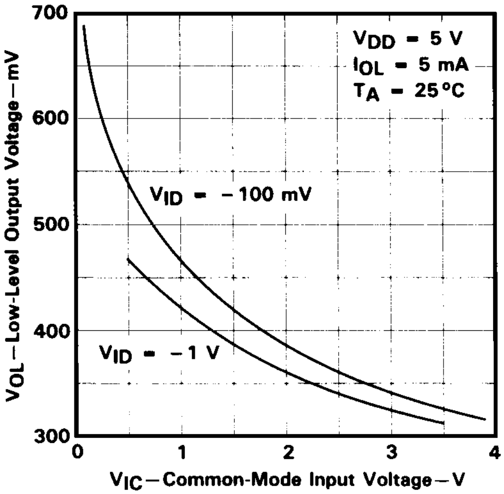

FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

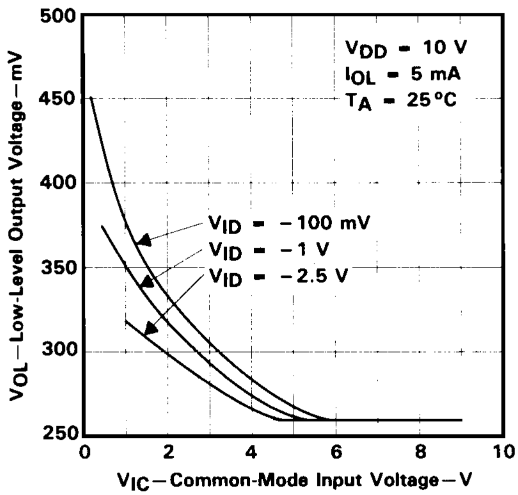

FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

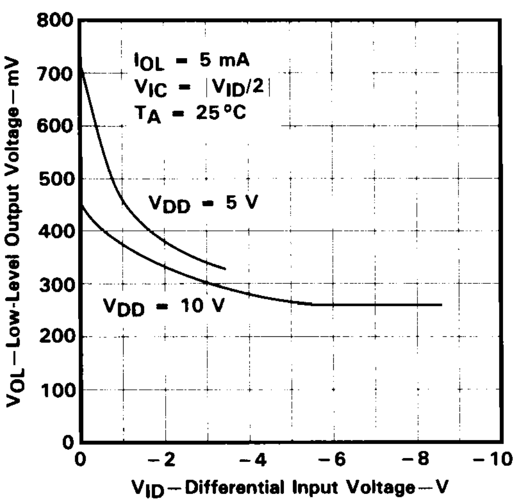

FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

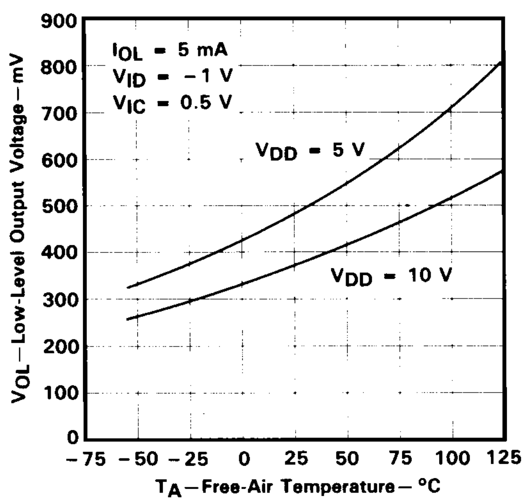

FIGURE 17

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

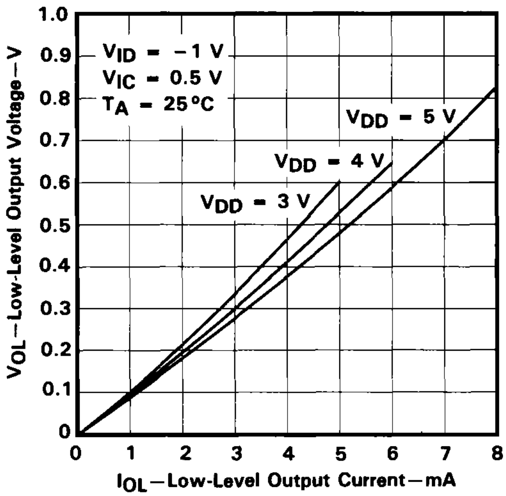

FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

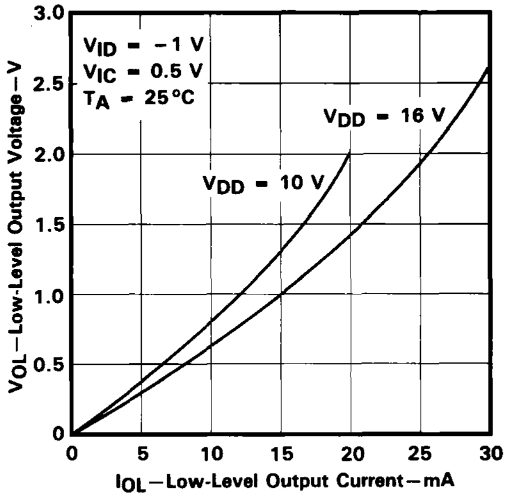

FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

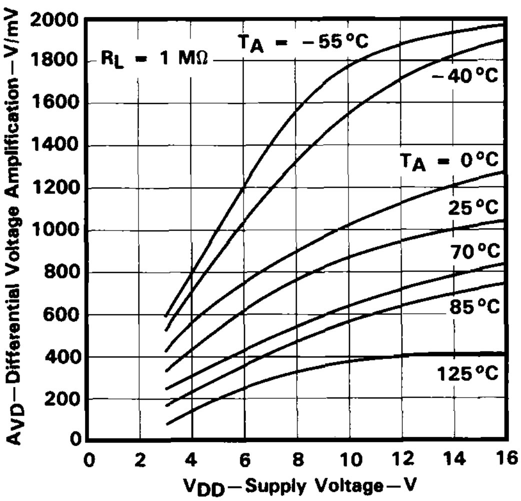

FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

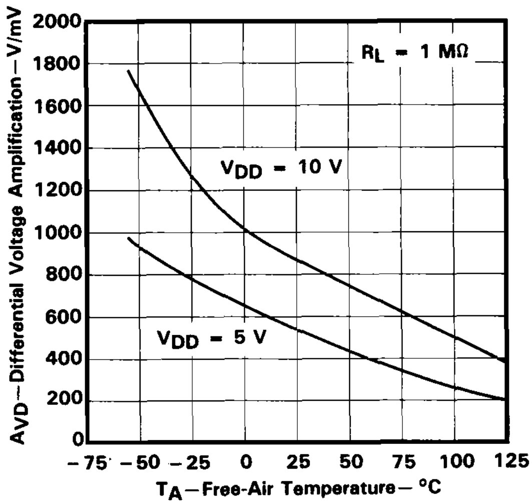

FIGURE 21

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

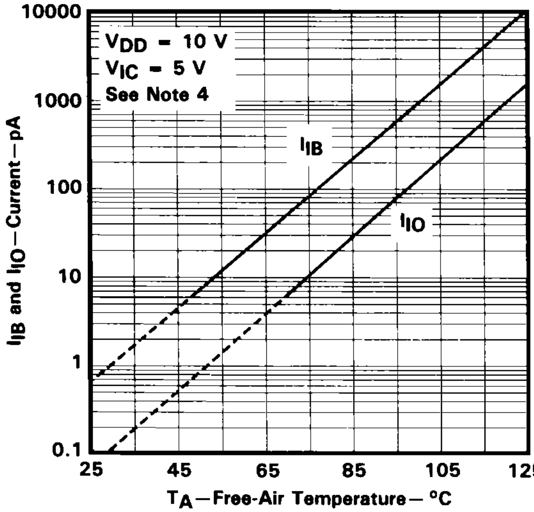

FIGURE 22

COMMON-MODE
INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

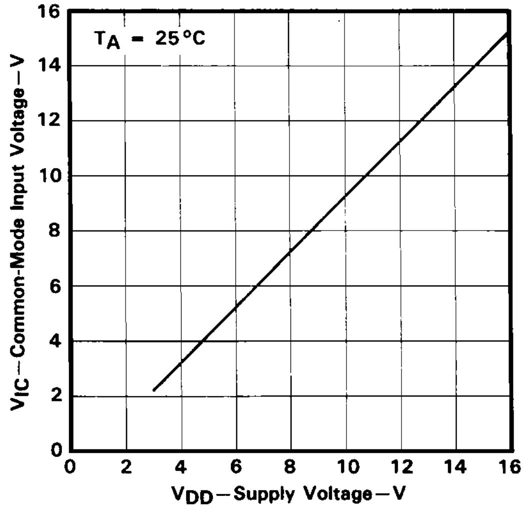

FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

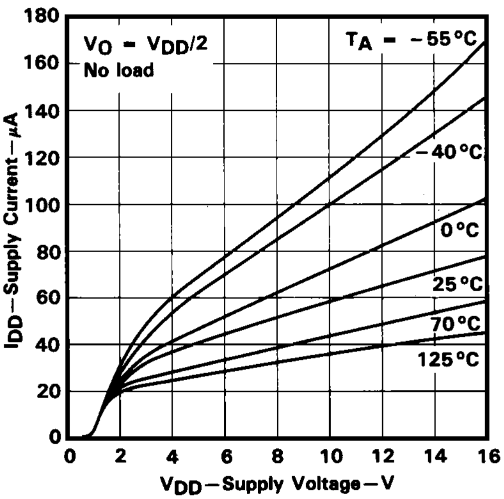

FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

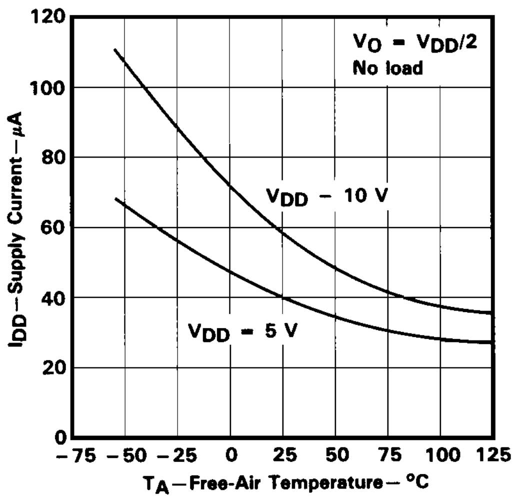

FIGURE 25

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

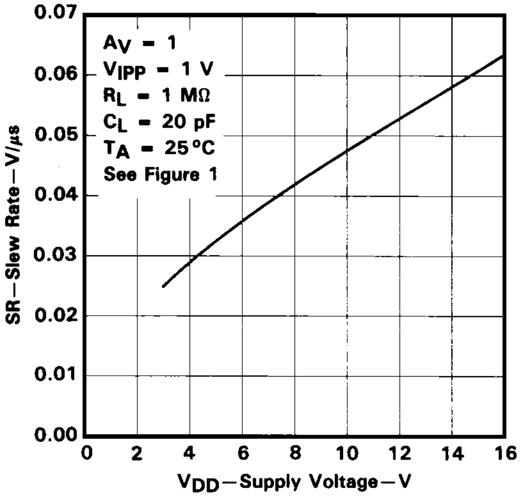

FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

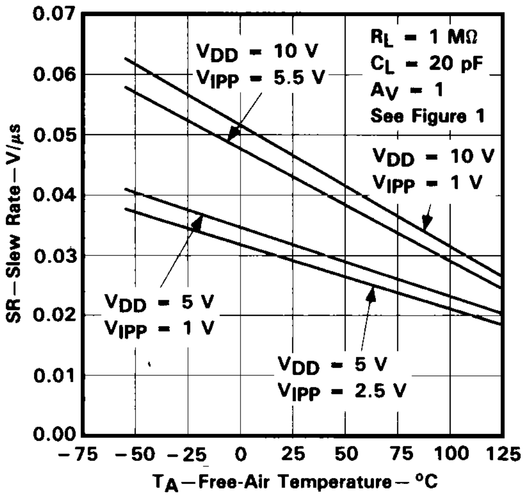

FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

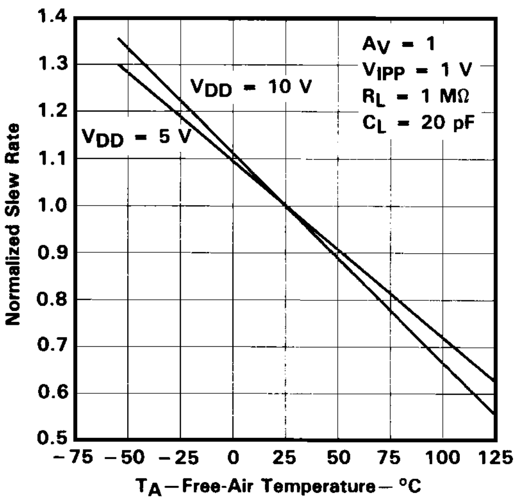

FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

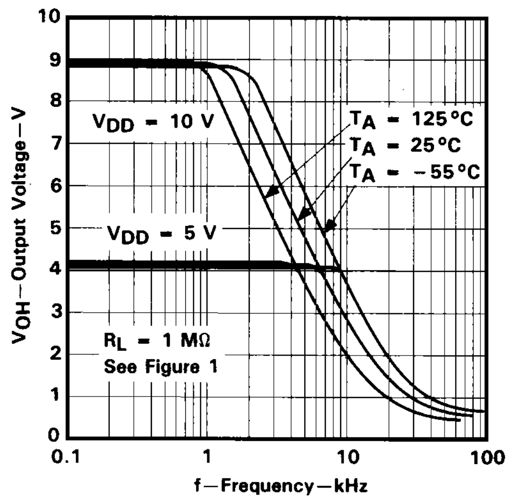

FIGURE 29

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

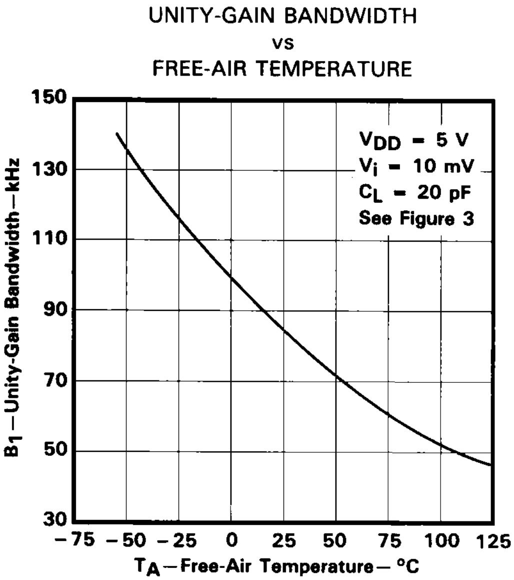


FIGURE 30

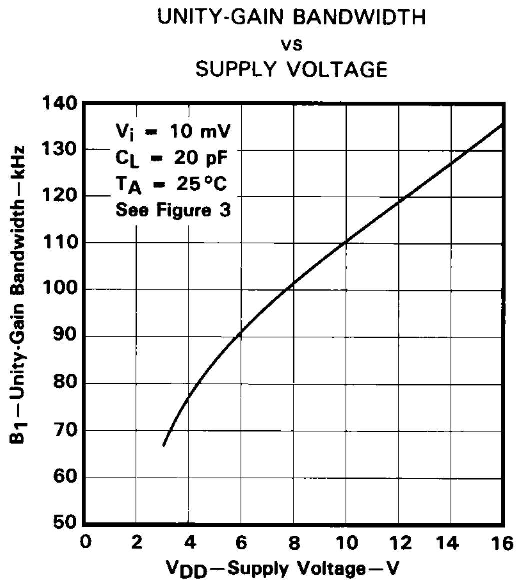


FIGURE 31

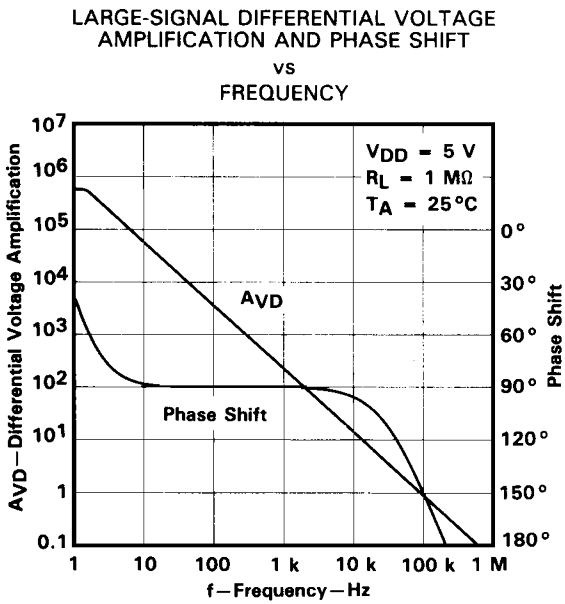


FIGURE 32

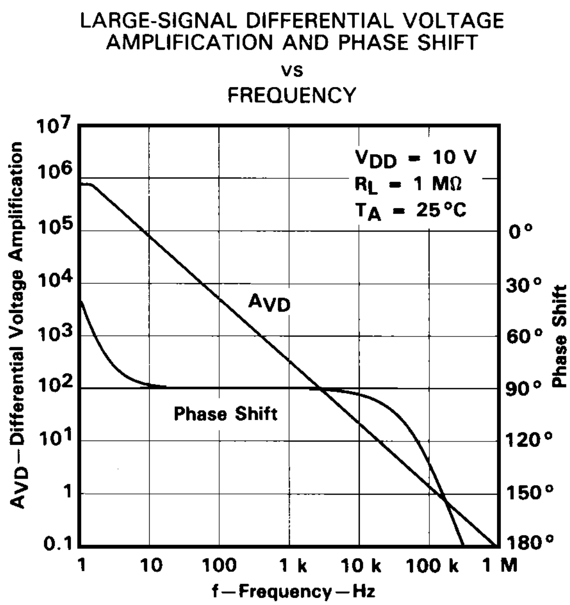


FIGURE 33

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

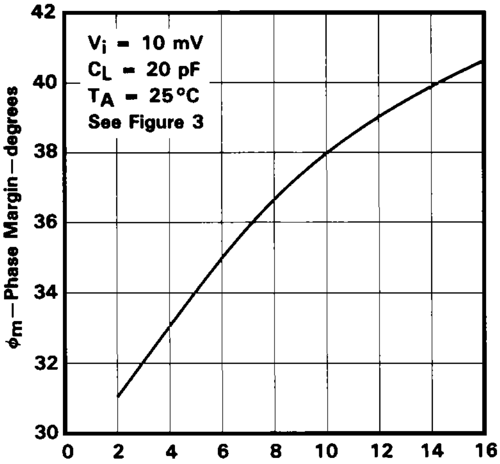


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

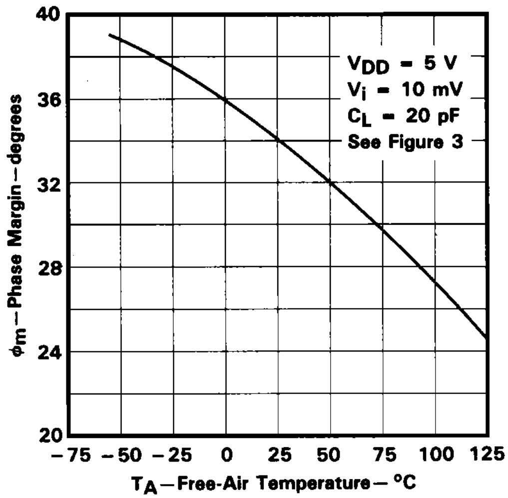


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

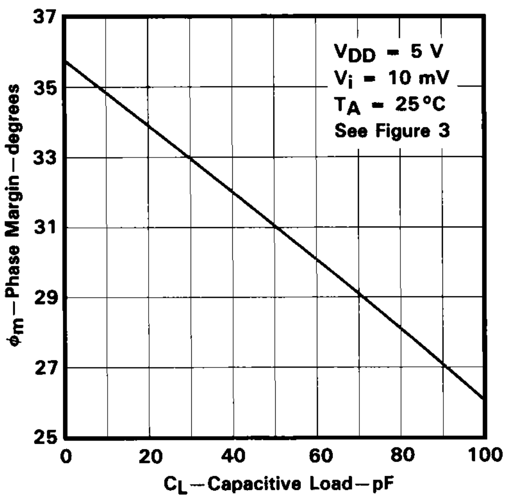


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

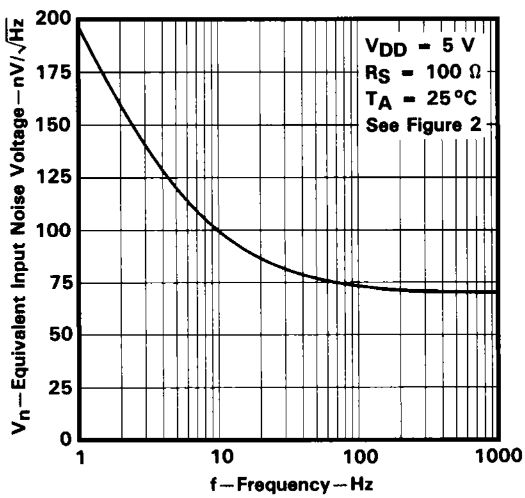


FIGURE 37

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

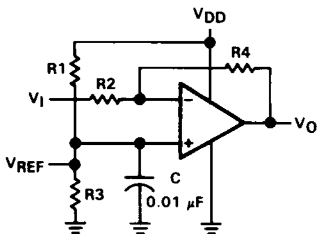
single-supply operation

While the TLC27L4 and TLC27L9 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC27L4 and TLC27L9 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27L4 and TLC27L9 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

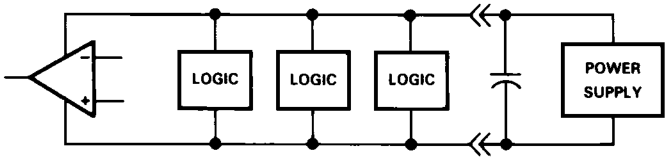
1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



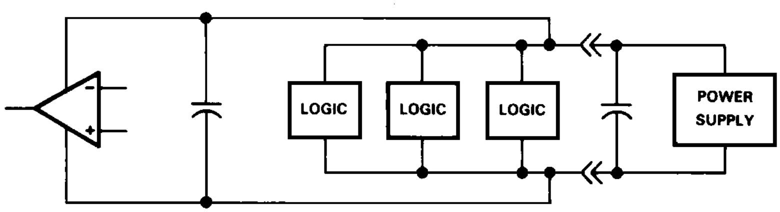
$$V_{REF} = V_{DD}\frac{R3}{R1 + R3}$$

$$V_O = \left(V_{REF} - V_I\right)\frac{R4}{R2} + V_{REF}$$

FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE



(a) COMMON SUPPLY RAILS



(b) SEPARATE BYPASSED SUPPLY RAILS (PREFERRED)

FIGURE 39. COMMON VS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC27L4 and TLC27L9 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25°C$ and at $V_{DD} - 1.5$ V at all other temperatures.

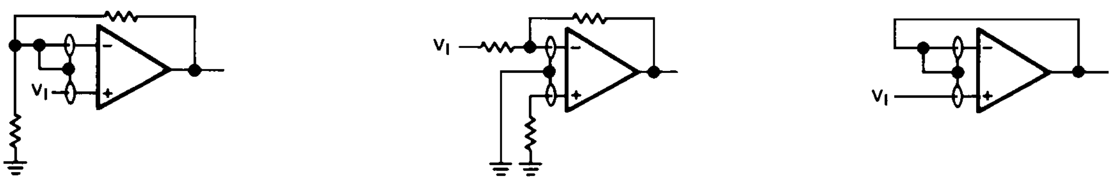
The use of the polysilicon-gate process and the careful input circuit design gives the TLC27L4 and TLC27L9 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27L4 and TLC27L9 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27L4 and TLC27L9 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

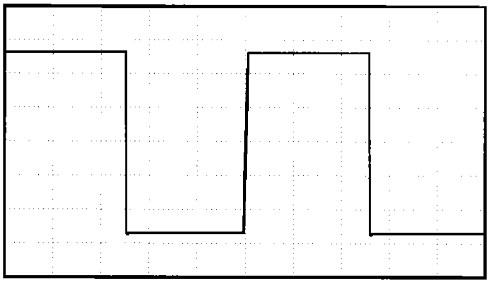
FIGURE 40. GUARD-RING SCHEMES

output characteristics

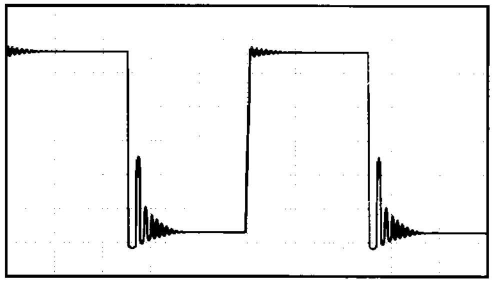
The output stage of the TLC27L4 and TLC27L9 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC27L4 and TLC27L9 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance will alleviate the problem.

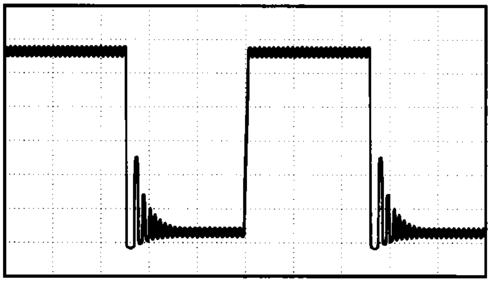
TYPICAL APPLICATION DATA



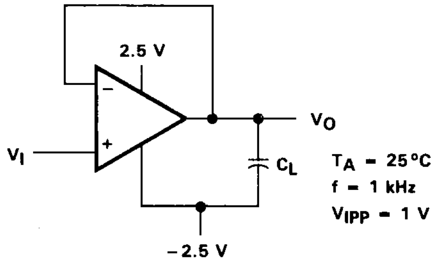
(a) C_L = 20 pF, R_L = NO LOAD



(b) C_L = 260 pF, R_L = NO LOAD



(c) C_L = 310 pF, R_L = NO LOAD



(d) TEST CIRCUIT

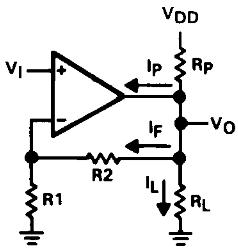
FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC27L4 and TLC27L9 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

TYPICAL APPLICATION DATA



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the op amp (typically 500 μA)

FIGURE 42. RESISTIVE PULLUP TO INCREASE V_{OH}

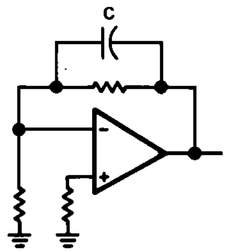


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

electrostatic discharge protection

The TLC27L4 and TLC27L9 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices, as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC27L4 and TLC27L9 inputs and outputs were designed to withstand − 100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

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TYPICAL APPLICATION DATA

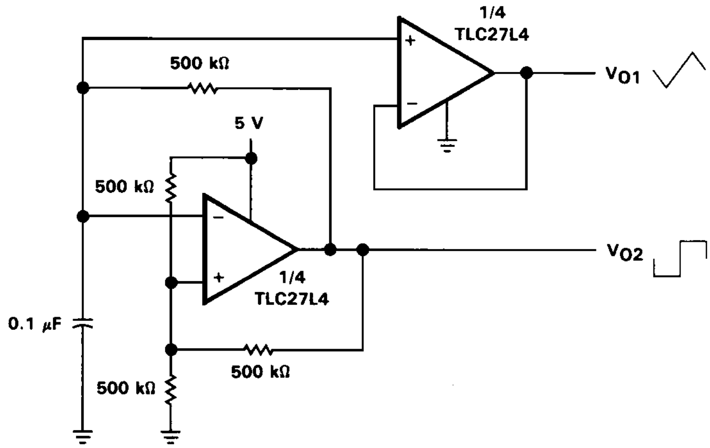
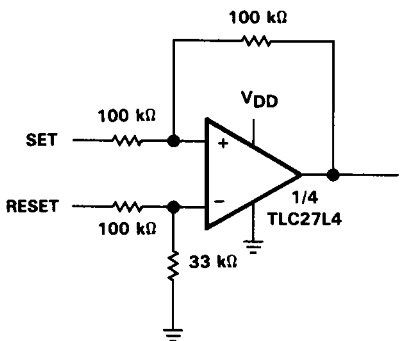


FIGURE 44. MULTIVIBRATOR

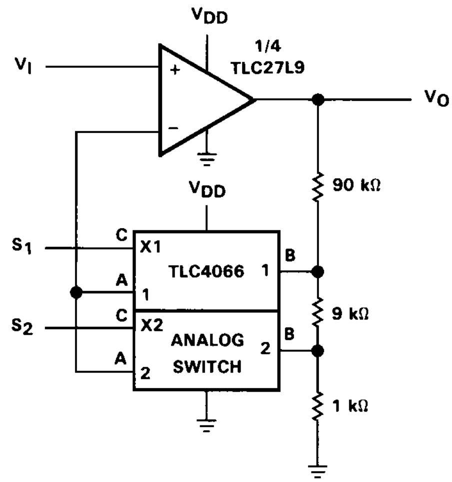


NOTE: V_{DD} = 5 V to 16 V

FIGURE 45. SET/RESET FLIP-FLOP

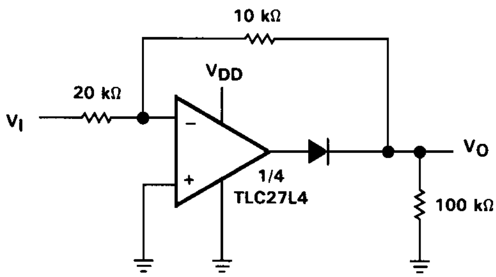
TYPICAL APPLICATION DATA

SELECT:	S_1	S_2
A_V	10	100



NOTE: V_{DD} = 5 V to 12 V

FIGURE 46. AMPLIFIER WITH DIGITAL GAIN SELECTION



NOTE: V_{DD} = 5 V to 16 V

FIGURE 47. FULL-WAVE RECTIFIER

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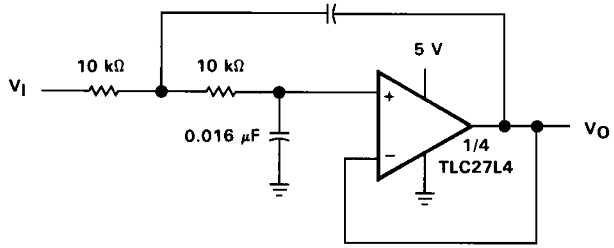
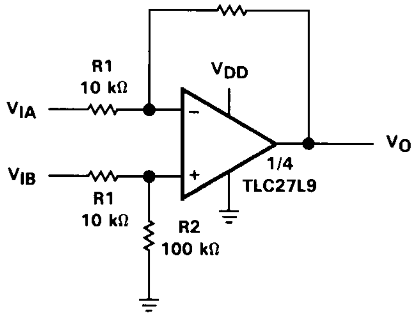
TYPICAL APPLICATION DATA



NOTE: Normalized to F_C = 1 kHz and R_L = 10 kΩ

FIGURE 48. TWO-POLE LOW-PASS BUTTERWORTH FILTER



NOTES: V_{DD} = 5 V to 16 V

$$V_O = \frac{R2}{R1}(V_{IB} - V_{IA})$$

FIGURE 49. DIFFERENCE AMPLIFIER