CPE301 – Fall 2019

Design Assignment 2B

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Directory: <https://github.com/reedjacobp/submission_da>

Submit the following for all Labs:

1. In the document, for each task submit the modified or included code (only) with highlights and justifications of the modifications. Also, include the comments.
2. Use the previously create a Github repository with a random name (no CPE/301, Lastname, Firstname). Place all labs under the root folder ESD301/DA, sub-folder named LABXX, with one document and one video link file for each lab, place modified asm/c files named as LabXX-TYY.asm/c.
3. If multiple asm/c files or other libraries are used, create a folder LabXX-TYY and place these files inside the folder.
4. The folder should have a) Word document (see template), b) source code file(s) and other include files, c) text file with youtube video links (see template).

1. **COMPONENTS LIST AND CONNECTION BLOCK DIAGRAM w/ PINS**

ATmega328PB Xplained Mini

1. **INITIAL/MODIFIED/DEVELOPED CODE OF TASK 1/A**

;

; DA2B.asm

;

; Created: 10/5/2019 6:03:29 PM

; Author : jreed

;

.ORG 0x00

JMP MAIN

.ORG 0x02

JMP TASK2

MAIN:

LDI R20, HIGH(RAMEND) ; initialize the stack

OUT SPH, R20

LDI R20, LOW(RAMEND)

OUT SPL, R20

LDI R20, 0x02 ; trigger interrupt on falling edge

STS EICRA, R20

SBI DDRB, 3 ; make DDRB3 output

SBI PORTB, 3 ; make PORTB3 high

SBI PORTD, 2 ; INT0

CBI DDRC, 3 ; make DDRC3 input

SBI PORTC,3 ; make PORTC3 high

LDI R20, 1<<INT0

OUT EIMSK, R20

SEI ; enable interrupt

START:

CBI PORTB, 3 ; turn on PB5/D1

; 250 ms delay loop

LDI R18, 21

LDI R19, 75

LDI R20, 191

DELAY1: DEC R20

BRNE DELAY1

DEC R19

BRNE DELAY1

DEC R18

BRNE DELAY1

NOP

SBI PORTB, 3 ; turn off PB5/D1

; 375 ms delay loop

LDI R18, 31

LDI R19, 113

LDI R20, 31

DELAY2: DEC R20

BRNE DELAY2

DEC R19

BRNE DELAY2

DEC R18

BRNE DELAY2

NOP

JMP START ; if switch is not pressed, go back to the beginning of code

TASK2:

IN R21, PORTB

LDI R22, (1<<2)

EOR R21, R22

OUT PORTB, R21

; 1.333 sec delay

LDI R18, 109

LDI R19, 51

LDI R20, 106

DELAY3: DEC R20

BRNE DELAY3

DEC R19

BRNE DELAY3

DEC r18

BRNE DELAY3

RETI ; return from interrupt

/\*

\* DA2B\_C.c

\*

\* Created: 10/5/2019 11:46:55 PM

\* Author : jreed

\*/

#define *F\_CPU* 16000000UL

#include <avr/io.h>

#include <avr/interrupt.h>

#include <util/delay.h>

int main(void)

{

DDRB = (1<<3); // set PORTB.3 for output

PORTB = (1<<3); // set LED low

PORTD = (1<<2); //pull-up activated

EIMSK = (1<<INT0); // enable external interrupt 0

EICRA = 0x2; // make INT0 falling edge triggered

sei (); // enable interrupts

while (1)

{

*\_delay\_ms*(250); // delay for 40% DC

PORTB &= ~(1<<3); // set LED on

*\_delay\_ms*(375); // delay for remaining 60%

PORTB |= (1<<3); // set LED off

}

}

ISR (INT0\_vect) { // ISR for external interrupt INT0

PORTB &= ~(1<<3); // turns on PORTB.3 (LED)

*\_delay\_ms*(1333); // delay for 1.33 sec

}

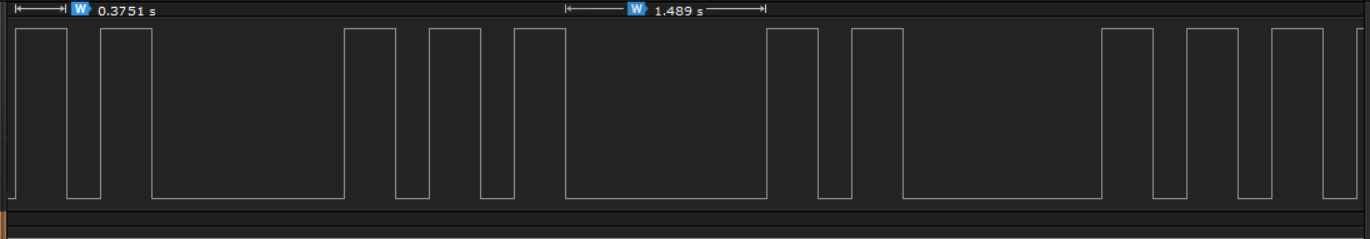
1. **DEVELOPED MODIFIED CODE OF TASK 2/A from TASK 1/A**

N/A

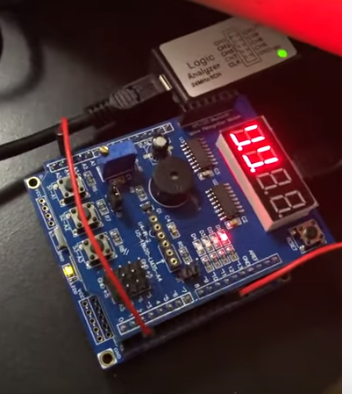
1. **SCHEMATICS**

Use fritzing.org

1. **SCREENSHOTS OF EACH TASK OUTPUT (ATMEL STUDIO OUTPUT)**



1. **SCREENSHOT OF EACH DEMO (BOARD SETUP)**



1. **VIDEO LINKS OF EACH DEMO**

https://youtu.be/FIsp94b3r-k

1. **GITHUB LINK OF THIS DA**

<https://github.com/reedjacobp/submission_da/tree/master/DesignAssignments/DA2B>

**Student Academic Misconduct Policy**

<http://studentconduct.unlv.edu/misconduct/policy.html>

“This assignment submission is my own, original work”.

NAME OF THE STUDENT