Joshua Reed

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October 27, 2016

3065 SW 178th Ave.
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Objective

To obtain a full time design or test engineering position which requires creativity and encourages self advancement. An ideal position might include low level programming, scripting for productivity and hardware or system design or test.

Education

Oregon State University — Corvallis, OR
B.Sc. Electrical and Computer Engineering — *2012 - Graduating: June, 2017*

- **GPA 3.5**
- **Focus in Computer Engineering and Digital Design**
- Key Courses Include:
  - Digital Logic Design
  - Assembly Language
  - Algorithms
  - Microcontroller System Design
  - Operating Systems
  - VLSI and VLSI System Design
  - Computer Architecture

Skills

- **HDL:** VHDL, Verilog, Modelsim and ActiveHDL Simulators and Altera Quartus II Design Software
- **System Design:** Microcontrollers, FPGAs and Basic Communication Protocols
- **Development & Productivity Tools:** Microsoft Office Suite, Vim, Latex and Git
- **Software Design:** Object Oriented Programming, Linux System Interaction, Regular Expressions, C and Python
- **Hardware Design:** Discrete Logic Design, Transistor Layout Basics, Circuit Design, PCB Layout and Power Supply Concepts

Internship and Work Experience

Mentor Graphics — Wilsonville, OR
Technical Marketing Engineer Intern — *July, 2016 - Current*

Role: As a Technical Marketing Engineer Intern I participated in team meetings and gave occasional presentations. My primary focus was a regression testing program that converted arbitrary graphs to usable input for Mentor's Calibre tools. Mostly written in Python, this project parsed graph files, generated SVRF and TVF scripts and managed process control of external programs. Designed for use in a Linux environment, I gained experience interacting with Linux development tools and the operating system itself.

Oregon State University — Corvallis, OR
Digital Design Lab TA — *March, 2014 - January, 2015 & September, 2015 - July 2016*

Role: As a teaching assistant I worked directly with instructor Matt Shuman to help guide the lab portion of the course. On occasion I developed and lead class lectures, managed lab grading and built lab study material. One of the larger projects I developed for the course was an FPGA voltmeter which required implementation of a SPI communications protocol.

Garmin AT Salem, OR
Design Engineer Intern *March - September, 2015*

Role: As a Design Engineer Intern at Garmin AT I interacted with a team of four and my team lead on a daily basis. Primarily I worked to redesign a portion of an aerial receiver's HDL that targeted an Altera FPGA. The main goal of this redesign was to reduce logic utilization. I achieved a reduction of 60% while also implementing VHDL 2008 constructs to develop cleaner, more extensible code. Other projects included parsing CSV Oscilloscope readings of USB communications, generating a top down compilation order for a large VHDL project using Python and developing a discrete logic circuit to multiplex LCD display data. During this internship I gained experience with a larger VHDL project, circuit design and layout, power supply design, Visual Basic, Python and Batch scripting and electronics lab tool usage.

Riverstone Residential Portland, OR
Maintenance Supervisor *July, 2009 - September, 2012*

Role: As a Maintenance Supervisor at Riverstone Residential I managed a team of three people toward the goal of maintaining over 350 homes located within a 10 mile radius. My responsibilities included: ordering supplies, scheduling of both vendors and employees, maintenance repair requests and resident communication. While in this position I developed skills in problem solving, communication, time management and leadership.

Project and Extracurricular Experience

VLSI System Design

I worked with instructor Roger Traylor to integrate FPGAs into OSU's VLSI System Design course. This included preparing and delivering two demonstrative lectures, building course assignments and exploring design options. During this process, I designed a blinking led pll demo and a sine wave generator which utilized the FPGA's on chip rom.

Senior Design High Field Pulse Magnet

Our project met or exceeded initial requirements. I helped achieve this goal by designing a voltmeter and voltage warning indicator. For the final prototype I successfully designed and utilized a PCB.

More Power Amplifier Design

I implemented a bridged amplifier design to improve upon a USB powered discrete transistor amplifier. To do this I added a unity gain stage to one half of the amplifier, inverting the phase of the original signal.

References

Marshal Barrett (541) 908-6761 – MarshalBarrett@gmail.com
Senior Design Engineer *Garmin AT*

Chris Schulte (503) 391-3303 – Chris.Schulte@garmin.com
Staff Engineer *Garmin AT*

Matthew Shuman (541) 737-1072 – ShumanM@oregonstate.edu
Instructor *Oregon State University*

Roger Traylor (541) 737-2975 – Traylor@eecs.oregonstate.edu
Senior Instructor *Oregon State University*

Lisa Shoop (503) 998-4266 – *Please Call*
Regional Manager *Riverstone Residential*