Joshua Reed

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Education

B.Sc. Electrical and Computer Engineering — Graduation: June, 2017
Oregon State Universitry — Current GPA: 3.45

Skills

- **Software Design:** Object Oriented Programming, Linux System, Interaction, Regular Expressions, C and Python
- **Development and Productivity Tools** Microsoft Office Suite, Vim, LaTeXand Git
- **HDL** VHDL, Verilog, Modelsim and ActiveHDL Simulators and Altera Quartus II Design Software
- **System Design** Microcontrollers, FPGAs, Basic Communication Protocols
- **Hardware Design** Discrete Logic Design, Transistor Layout Basics,
- Circuit Design, PCB Layout and Power Supply Concepts

Internship and Work Experience

Mentor Graphics — Wilsonville, OR
Technical Marketing Engineer Intern — *July - September, 2016*

Role: As a Technical Marketing Engineer Intern I participated in team meetings and gave occasional presentations. My primary focus was a regression testing program that converted arbitrary graphs in node neighbor format to usable input for Mentor's Calibre tools. Before this project, corner case tests were tediously hand drawn and black box random testing was infeasible. This program facilitates these tests and allows Mentor to reproduce customer test cases without proprietary customer data. As a result, Mentor's tools are more robust and easier to develop.

Oregon State University — Corvallis, OR
Digital Design Teaching Assistant — *September, 2015 - July, 2016*

Role: As a Digital Design Teaching Assistant I worked directly with instructor Matt Shuman to help guide the lab portion of the course. On occasion I developed and lead lectures, managed lab grading, and built lab study material. One of the larger projects I developed for the course was an FPGA voltmeter which included a SPI module written in System Verilog.

Garmin AT — Salem, OR
Design Engineer Intern — *March - September, 2015*

Role: As a Design Engineer Intern at Garmin AT I interacted with a team of four and my team lead on a daily basis. Primarily I worked to redesign a portion of an aerial receiver's HDL that targeted an Altera FPGA. The main goal of this redesign was to reduce logic utilization. I achieved a reduction of 60% while also implementing VHDL 2008 constructs to develop cleaner, more extensible code. Other projects included parsing CSV Oscilloscope readings of USB communications, automating top down compilation order of VHDL projects using Python, and developing a circuit to multiplex LCD display data. During this internship I gained experience with a large VHDL project, circuit design and layout, power supply design, Visual Basic, Python and Batch scripting, and electronics lab tool usage.

Project and Extracurricular Experience

VLSI System Design

I worked with instructor Roger Traylor to integrate FPGAs into OSU's VLSI System Design course. This included preparing and delivering two demonstrative lectures, building course assignments and exploring design options. During this process, I designed a blinking led pll demo and a sine wave generator which utilized the FPGA's on chip rom.

Senior Design High Field Pulse Magnet

Our project met or exceeded initial requirements. I helped achieve this goal by designing a voltmeter and voltage warning indicator. For the final prototype I successfully designed and utilized a PCB.

Increased Power Amplifier Design

I implemented a bridged amplifier design to improve upon a USB powered discrete transistor amplifier. To do this I added a unity gain stage to one half of the amplifier, inverting the phase of the original signal.