Joshua Reed

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236 NW 8Th St.
Corvallis, OR

Objective

To obtain a full time design, test, or otherwise general engineering position which requires creativity and encourages self advancement.

Education

Oregon State University   Corvallis, OR
B.Sc. Electrical and Computer Engineering   *2012 -* **Graduating: June, 2017**

- **GPA 3.5**
- **Focus in Computer Engineering and Digital Design** *Key Courses Include:*
    - Digital Logic Design
    - Assembly Language
    - Algorithms
    - Microcontroller System Design
    - Operating Systems
    - VLSI and VLSI System Design
    - Computer Architecture

Skills

- **HDL:** VHDL, Verilog, Modelsim and ActiveHDL Simulators and Altera Quartus II Design Software
- **System Design:** Microcontrollers, FPGAs and Basic Communication Protocols
- **Development & Productivity Tools:** Microsoft Office Suite, Vim, Latex and Git
- **Software Design:** Object Oriented Programming, Linux System Interaction, Parsing with Regular Expressions, C and Python
- **Hardware Design:** Discrete Logic Design, Transistor Layout Basics, Circuit Design, PCB Layout and Power Supply Concepts

Internship and Work Experience

Mentor Graphics   Wilsonville, OR
Technical Marketing Engineer Intern   *Summer, 2016 - Current*

Role: As a Technical Marketing Engineer Intern I participated in team meetings and gave occasional presentations. My primary focus was a regression testing program that converted arbitrary graphs to geometric edge-separator pairs for use as input to Mentor's Multi-Patterning tools. Mostly written in Python, this project parsed graph files, generated SVRF and TVF scripts and managed process control of external programs. Designed for use in a Linux environment, I gained experience interacting with Linux development tools and the operating system itself.

Garmin AT   Salem, OR
Design Engineer Intern   *Spring & Summer, 2015*

Role: As a Design Engineer Intern at Garmin AT I interacted with a team of four and my team lead on a daily basis. Primarily I worked to redesign a portion of an aerial receiver's HDL that targeted an Altera FPGA. The main goal of this redesign was to reduce logic utilization. I achieved a reduction of 60% while also implementing VHDL 2008 constructs to develop cleaner, more extensible code. Other projects included parsing CSV Oscilloscope readings of USB communications, generating a top down compilation order for a large VHDL project using Python and developing a discrete logic circuit to multiplex LCD display data. This internship was a period of major growth for me. I gained experience with a larger VHDL project, circuit design and layout, power supply design, Visual Basic, Python and Batch scripting and electronics lab tool usage.

Oregon State University Corvallis, OR
Digital Design Lab TA *Winter, 2015 - Current*

Role: As a teaching assistant I worked directly instructor Matt Shuman to help guide the lab portion of the course. On occasion I developed and lead class lectures, managed lab grading and built lab study material. One of the larger projects I developed for the course was an FPGA voltmeter which required implementation of a SPI communications protocol. I have also worked with Roger Traylor and lectured in his VLSI System Design course, though this was not an employment arrangement.

Riverstone Residential Portland, OR
Maintenance Supervisor *2009 - 2012*

Role: As a Maintenance Supervisor at Riverstone Residential I was entrusted with many responsibilities. I managed a team of three people toward the goal of maintaining over 350 homes located within a 20 mile radius. I developed skills in problem solving, communication, time management and leadership.

References

Marshal Barrett *Please Email* – MarshalBarrett@Gmail.Com
Senior Design Engineer *Garmin AT*

Chris Schulte (503) 391-3303 – Chris.Schulte@Garmin.Com
Staff Engineer *Garmin AT*

Matthew Shuman (541) 737-1072 – ShumanM@OregonState.Edu
Instructor *Oregon State University*

Roger Traylor (541) 737-2975 – Traylor@EECS.OregonState.Edu
Senior Instructor *Oregon State University*

Lisa Shoop (503) 998-4266 – *Please Call*
Regional Manager *Riverstone Residential*