

# Joshua Reed

ReedJosh@OregonState.edu  
(971) 275-5001

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236 NW 8th St.  
Corvallis, OR

## Objective

I'm looking for a three month plus internship starting mid June, 2016—with an implied job offer pending performance and graduation. I particularly want to work with FPGAs, VLSI, Microcontrollers, and work flow tools, but I'm always excited to try something new.

## Education

- **Oregon State University** Corvallis, OR  
*Senior Year –B.Sc. Electrical and Computer Engineering* 2012 - Now
  - GPA 3.5
  - Focus in Computer Engineering and Digital Design
    - \* Digital Logic Design ECE 271
    - \* Assembly Language ECE 375
    - \* Algorithms CS 325
    - \* Microcontroller System Design ECE 473
    - \* Operating Systems CS 311
    - \* Core ECE Courses
    - \* By End of Year: VLSI Design ECE 474 and Computer Architecture ECE 472

## Skills

- **HDL:** Strong with VHDL—Can use Verilog, Modelsim, ActiveHDL, Quartus, and script based automation.
- **Development:** Microcontroller System Design, OOP, Algorithms, and Operating System Interaction. Strongest in C/C++, and Python.
- **Circuit Design:** Discrete Logic Circuits, Power Supply Concepts, Amplifier Design Basics.
- Problem solving and debugging. Software tool development. Vim, L<sup>A</sup>T<sub>E</sub>X, git, bash, make, etc. . .

## Internship and Work Experience

- **Garmin AT** Salem, OR  
*Design Engineer Intern* Spring–Summer, 2015
  - **Exceeded Goals:** Completed all projects given with better than requested results (per midterm and final performance reviews).
  - **Motivated to Learn:** Learned VHDL 2008 standards and wrote function libraries.
- **Oregon State University** Corvallis, OR  
*Digital Design Lab TA* Winter–Fall 2015 & Current
  - **Mentor:** Learned through teaching.
  - **Communication:** Conveyed ideas in a way that will be understood.
- **Riverstone Residential** Portland, OR  
*Maintenance Manager* 2010-2013 & Summer 2014
  - **Leadership:** Managed a small team of people to maintain over 300 homes.
  - **Problem Solving:** Every day presented a new challenge to be solved in a timely manner.
  - **Resource Management:** Budgeted for supplies, services, and employees.

## Internship Projects

- **Message Reception Logic Reduction** VHDL, Python, TCL, .do  
*Reduce logic in the ADSB next-gen message reception transceiver FPGA*
  - **Management of Complexity:** Utilizing procedures, functions, and generics (VHDL), built abstraction layers facilitating a clean design.
  - **Logic Reduction:** Reduced FPGA logic utilization by %60.
  - **Testing:** Built automated test benches—Designed data generation Python scripts.
- **USB O-Scope Readout Parser** Python  
*Use Python to parse CSV Oscilloscope output to diagnose poor USB signals.*
  - **Demodulation:** Using a state machine design, parses data to data and diagnostics.
  - **Usability:** Output data to file with incremental numbering—Input from directory—Robust CLI.

- **Visualization:** Cut out dead space and plotted images of message transactions.

### HDL Auto Compilation

VHDL, Python, .do

*Parse VHDL with Python to generate a top down compilation order.*

- **Tool Integration:** Built .do scripts (like TCL) to integrate into Aldec Active HDL.
- **Robust:** Checks libraries and IP directories–Usable with VHDL 2008 standards and prior.
- **Simplicity:** Enter top file name in script once–Double click to run in future.

### Quad Screen Driver

PADs, Active HDL, VHDL

*Design a logical signal multiplexing circuit and supply power to the LED back light.*

- **On Time:** Two week turn around on a project with a lot of firsts for me.
- **Tool Usage:** Soldered many small parts by hand and used an O-Scope image to prove functionality.

### References

**Marshal Barrett**

*Senior Design Engineer*

*Please Email –* MarshalBarrett@Gmail.Com

*Garmin AT*

**Chris Schulte**

*New Product Concepts and Innovations Staff Engineer*

(503) 391-3303 – Chris.Schulte@Garmin.Com–

*Garmin AT*

**Matthew Shuman**

*Instructor*

(541) 737-1072 – ShumanM@OregonState.Edu

*Oregon State University*

**Roger Traylor**

*Senior Instructor*

(541) 737-2975 – Traylor@EECS.OregonState.Edu

*Oregon State University*

**Lisa Shoop**

*Regional Manager*

(503) 998-4266 – *Please Call*

*Riverstone Residential*