DECODER

Introduction

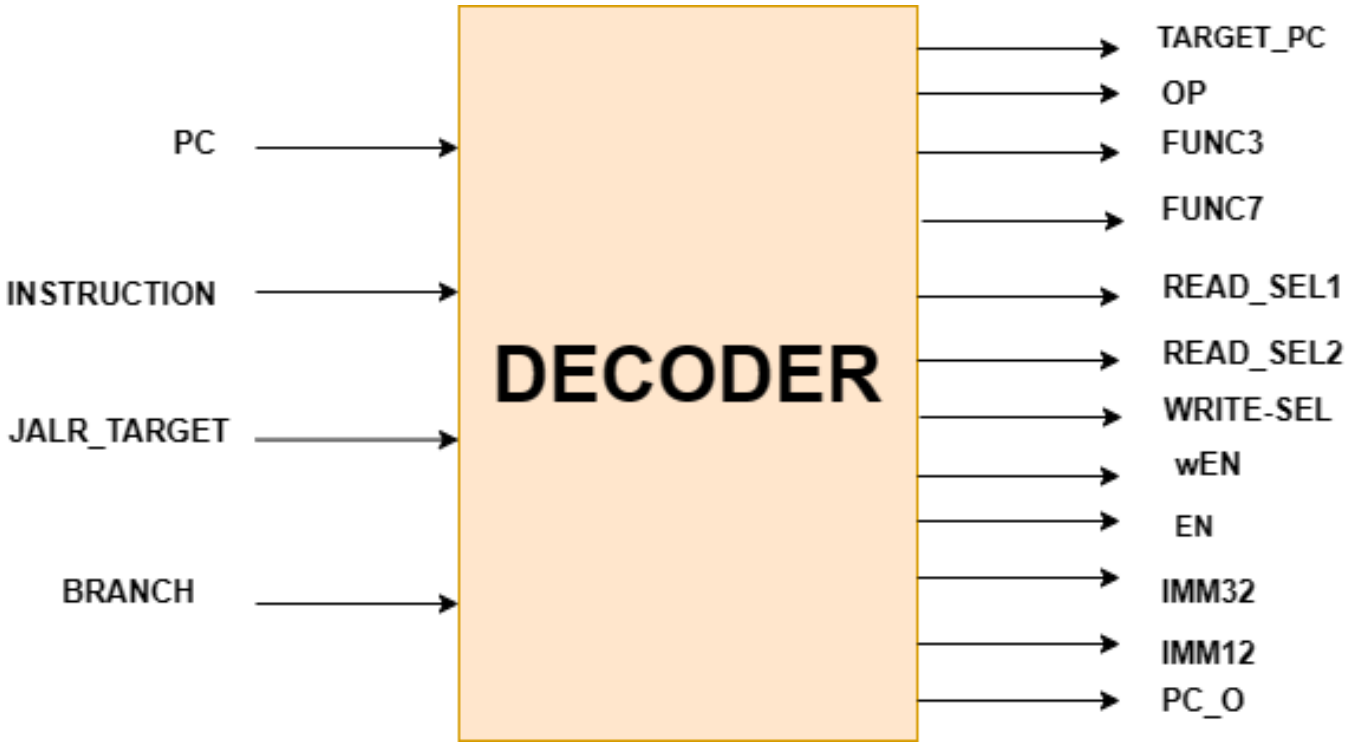
The decoder in zero-riscy is responsible for decoding the instruction fetched from the instruction memory and generating the control signals.

Problem Statement

- understanding the difference between ISA and their Types

Design and Implementation:

- Block Diagram



- **PC** : signal from fetch module have ADDRESS_BITS { ex : [ADDRESS_BITS-1:0] PC , ADDRESS_BITS = 16 }
- **JALR_TARGET:** signal from ALU , if the instructions JALR ALU send pc which will be fetched
- **BRANCH:** signal from ALU , if the instructions {beq , bne , blt , ...} ALU send signal high or low based on its true or not
- **INSTRUCTION :** The instructions 32 bit { ex : lw instruction 111111111100 01001 010 00110 **0000011** FFC4A303 }

- **TARGET_PC** : signal that have target PC calculations if the instruction is [branch , jal , jalr] ex: [ADDRESS_BITS-1:0] target pc .
- **OP** : first 7 bits of the instruction and it used to distinguish between difference Types { ex : LOAD 7'b**0000011**}
- **funct3 :** Bits of instruction [14:12]
- **funct7 :** Bits instruction [31:25]
- **READ_SEL1** : operand1 of the instruction { ex : x9 01001 }
- **READ_SEL2 :** operand2 of the instruction { ex : x6 00110 }
- **WRITE-SEL(RD) :** distention register to store the results in GPRs { ex : x5 }
- **wEN :** write Enable for GPRs
- **EN:** clk enable for GPR (for one clk)
- **IMM32** : it's output signal after sign extend {ex : 11111111111111111111111111111100 = -4 }
- **IMM12:** original 12 bit of the imm instruction
- **PC** : The same PC input signal

Note : IMM32 Calculated based on the type of the instruction

Table 7.5 ***ImmSrc*** **encoding.**

ImmSrc	ImmExt	Type	Description
00	{{20{*Instr*[31]}}, *Instr*[31:20]}	I	12-bit signed immediate
01	{{20{*Instr*[31]}}, *Instr*[31:25], *Instr*[11:7]}	S	12-bit signed immediate
10	{{20{*Instr*[31]}}, *Instr*[7], *Instr*[30:25], *Instr*[11:8], 1'b0}	B	13-bit signed immediate
11	{{12{*Instr*[31]}}, *Instr*[19:12], *Instr*[20], *Instr*[30:21], 1'b0}	J	21-bit signed immediate

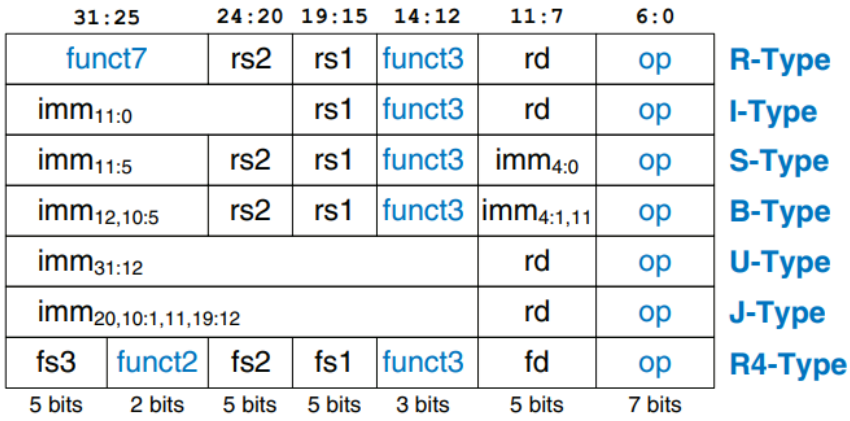


Figure B.1 RISC-V 32-bit instruction formats

Interfaces

Signals	Width	interface
PC	parametrized	Fetch module
INSTRUCTION	32 bit	Fetch module
OP	instruction[6:0]	Controller
TARGET_PC	parametrized	Fetch module
READ_SEL1	instruction[24:20]	GPRs
READ_SEL2	instruction[19:15]	GPRs
WRITE-SEL(RD)	instruction[11:7]	GPRs
wEN	1 bit	GPRs
IMM32	32 bit	Pipeline Register
funct3	instruction[14:12]	Pipeline Register OR Controller
funct7	instruction[31:25]	Pipeline Register OR Controller