challenge

Part 1 (OTA design)

→We want to design a digitally Controlled variable gain which has high gain and resistive feed back so we cannot use single stage as the gain will decrease when negative feed back is applied so we will use 2 stages and according this specs to achieve this gain, swing, UGF the best choice was “two stage miller OTA”

As dc level=1.2 then it is better to use input pair is NMOS type as

→$vicm\ min = vgsinput + vdstail$

→$vicm\ max = VDD - vdsmirror - vthinput$

→So, the OTA that will be designed is “two stage miller OTA with NMOS input pair”.

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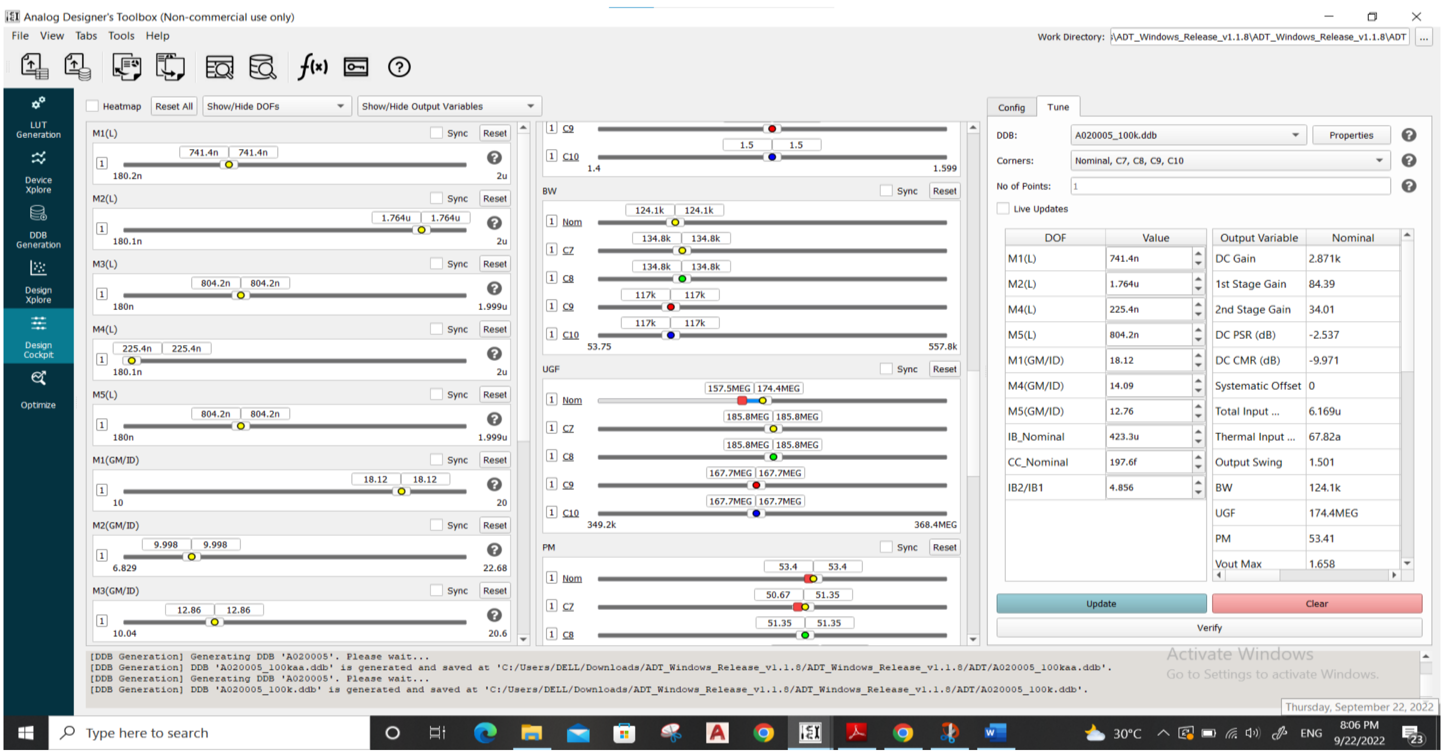
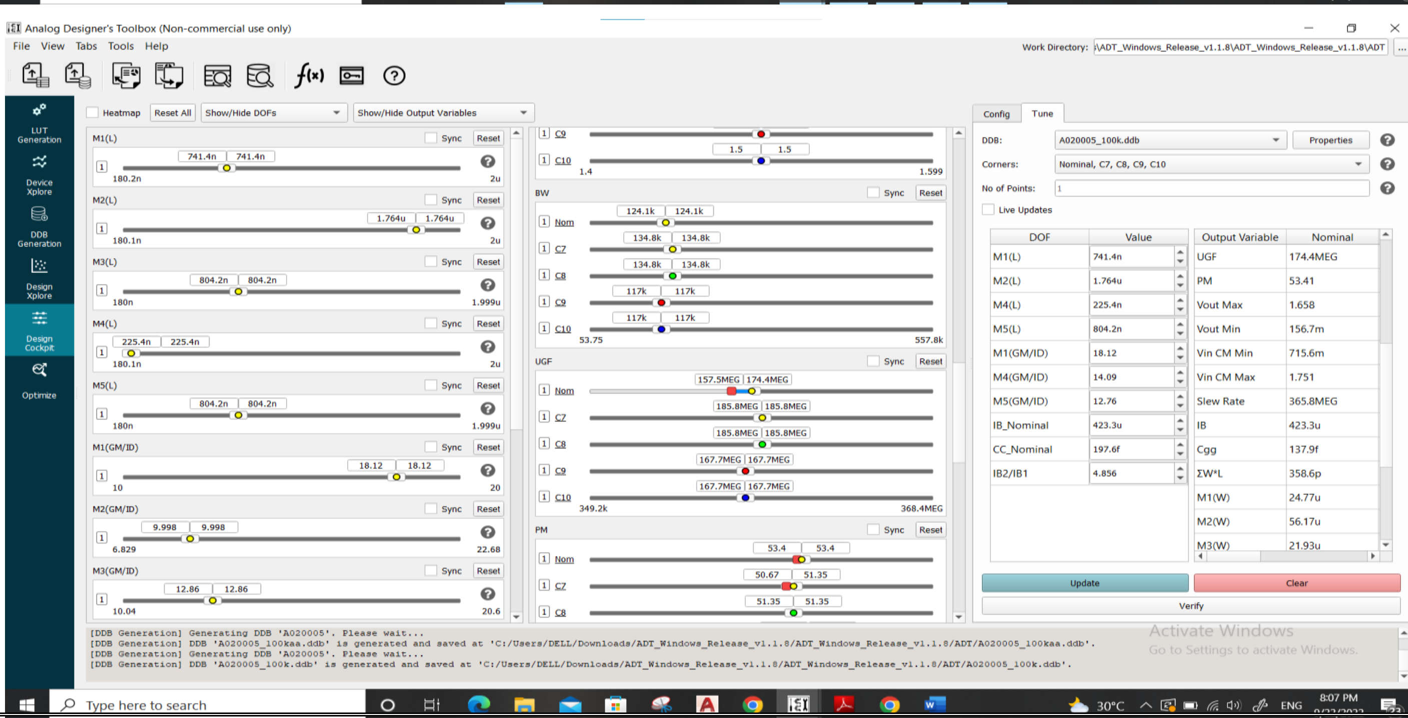
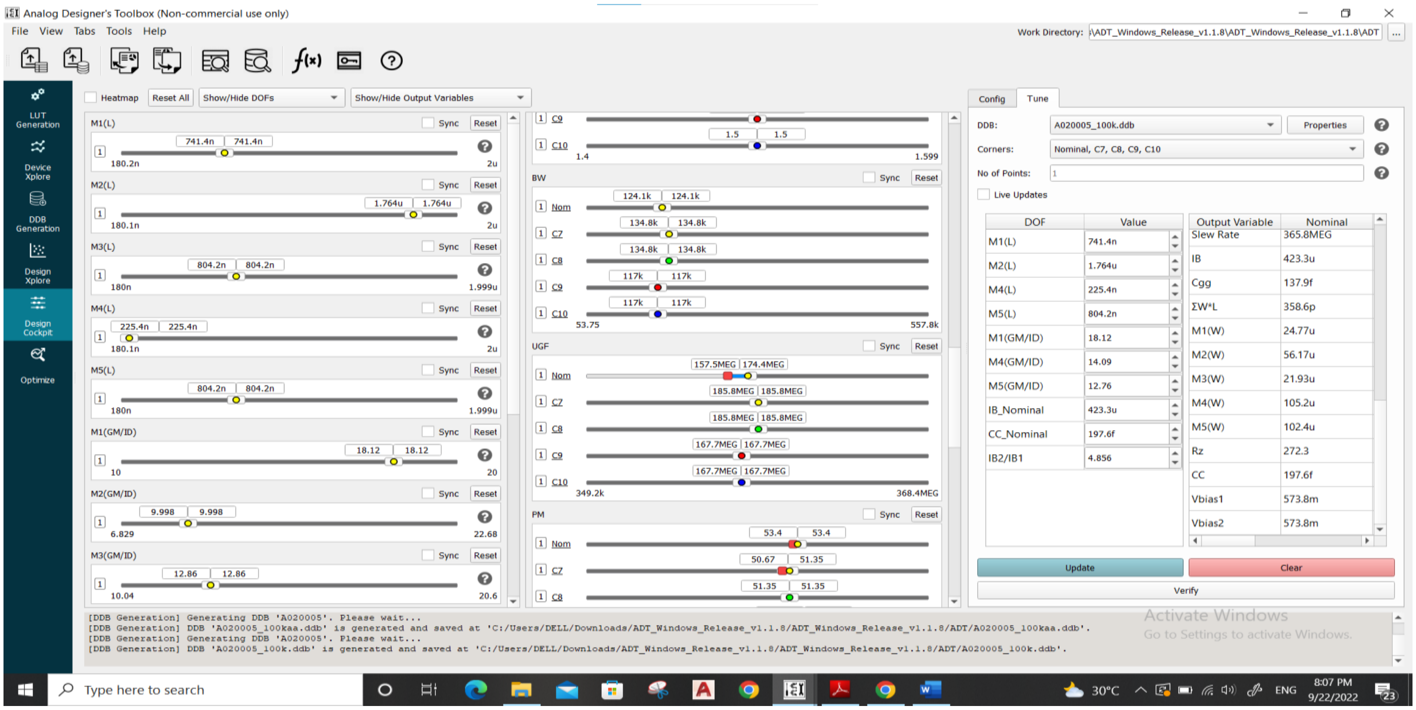
Part2(design strategy)

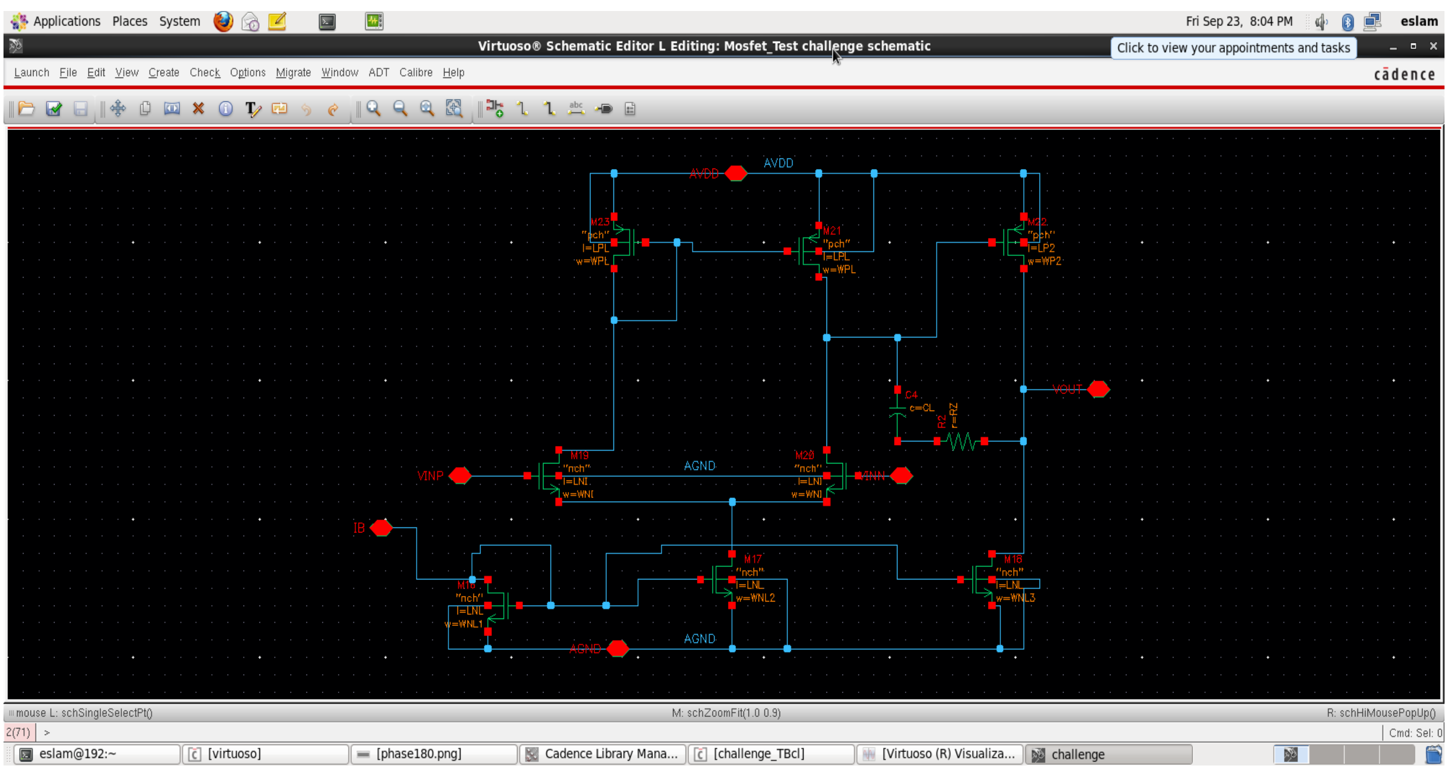
→I used ADT tool to achieve these specs and get sizing from it so I used ADT DDB generation and chose the design then using design cockpit to achieve these required specs as shown






Analog Designer's Toolbox (Non-commercial use only)
File View Tabs Tools Help
Work Directory:
LUT Generation
Device Xplore
DDB Generation
Design Xplore
Design Cockpit
Optimize
Heatmap
Reset All
Show/Hide DOFs
Show/Hide Output Variables
Config
Tune
DDB:
A020005_100k.ddb
Properties
Corners:
Nominal, C7, C8, C9, C10
No of Points:
Live Updates
DOF
Value
Output Variable
Nominal
Update
Clear
Verify
Type here to search

Schematic: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Virtuoso® Schematic Editor L Editing: Mosfet_Test challenge schematic
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mouse L: schSingleSelectPt()
M: schZoomFit(1.0 0.9)
R: schHiMousePopUp()

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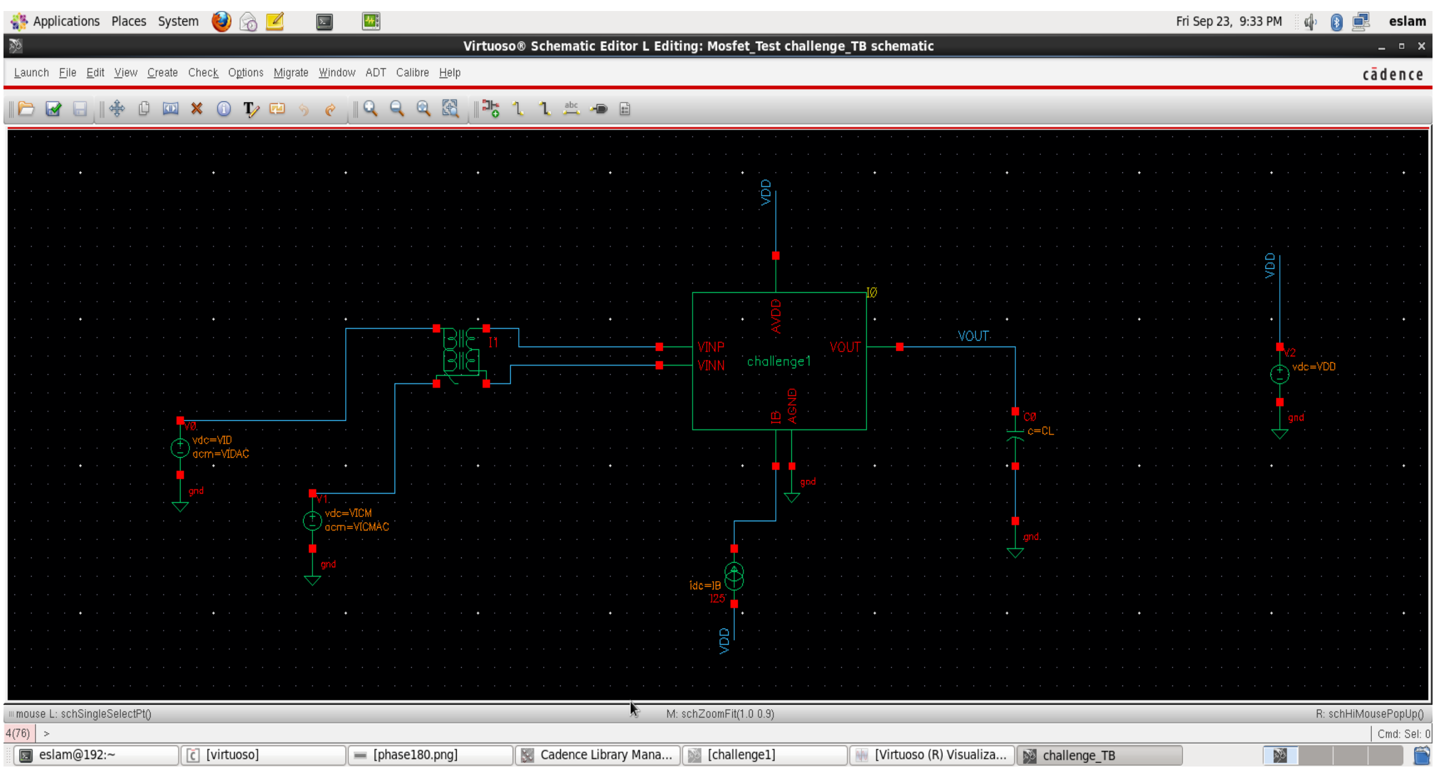
Device sizing:

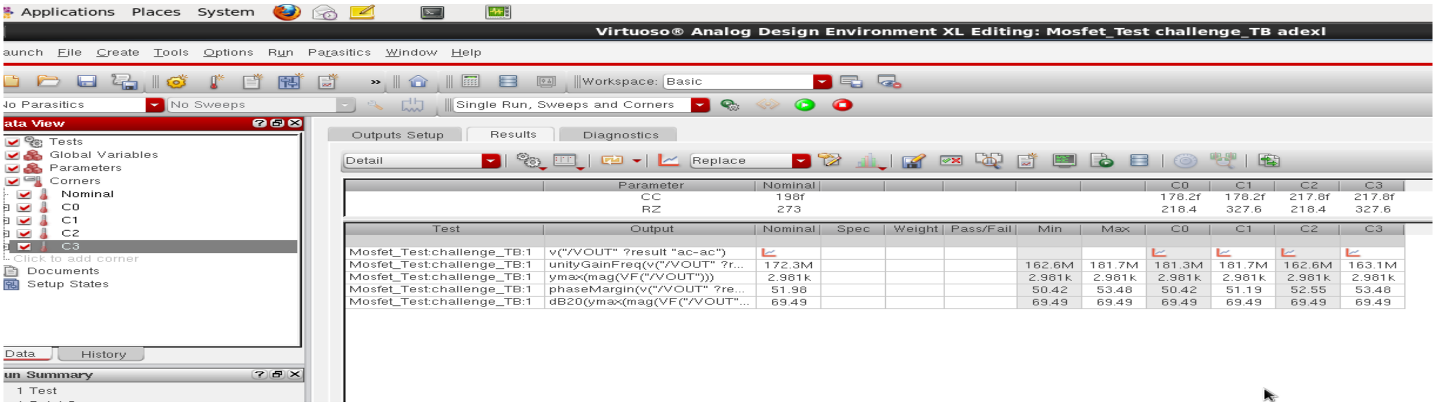
parameter	w	l	Gm/id
Inp pair	24.77u	741.4n	18.12
Mirror load	56.17u	1.76u	10.07
Inp 2nd stage	105.2u	225.4n	14.09
Tail cs	15.17u 21.93u 106.49u	804.2n	12.76

Part3(Open loop simulation)

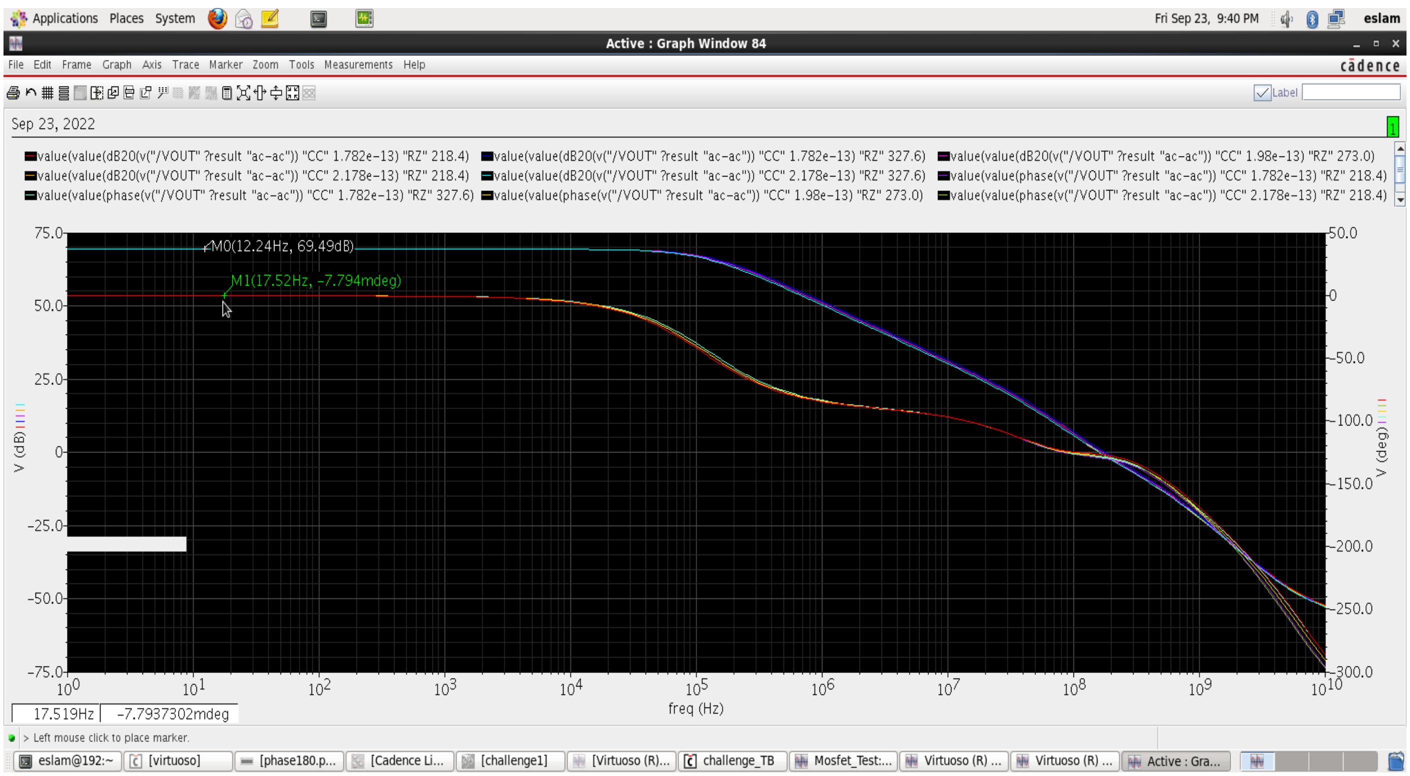
Open loop testbench schematic:



Open loop OTA specs:



open loop gain across all corners(magnitude &phase)



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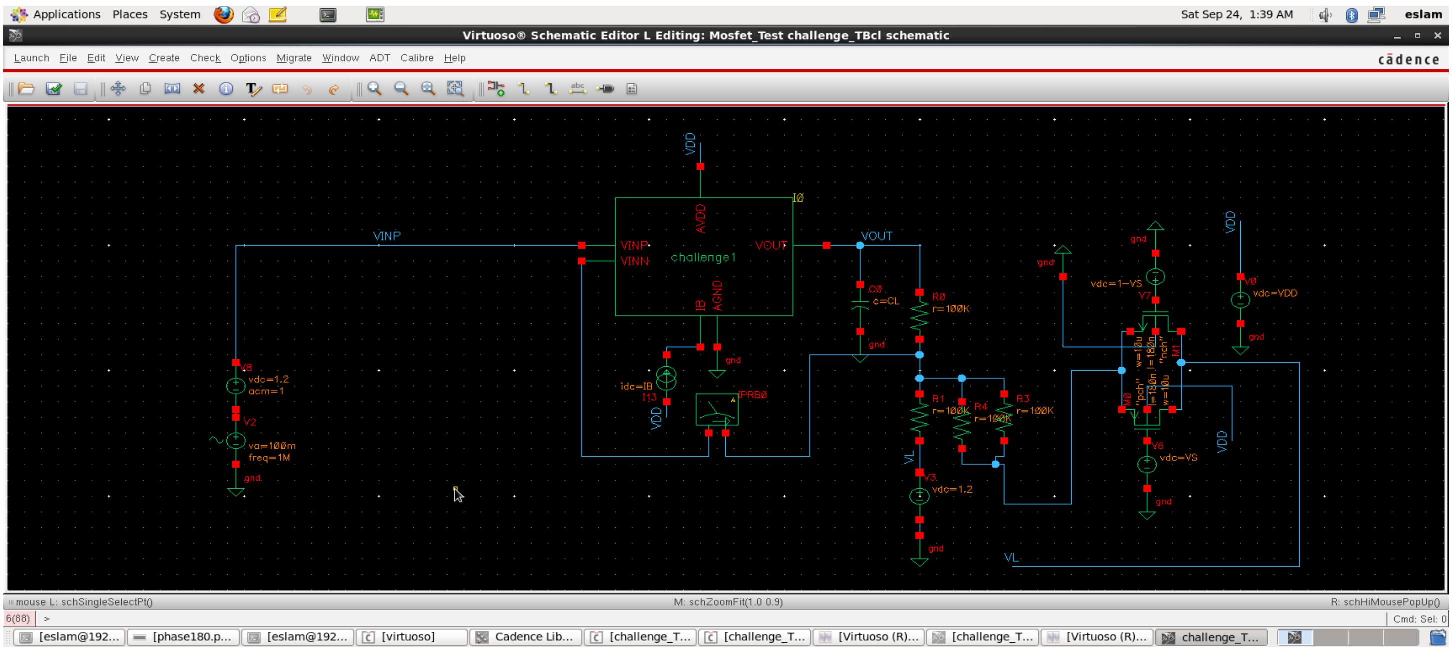
$$\rightarrow output\ swing = VDD - \frac{2}{\frac{gm}{id}} - \frac{2}{\frac{gm}{id}} = 1.8 - \frac{2}{12.76} - \frac{2}{14.09} = 1.5$$

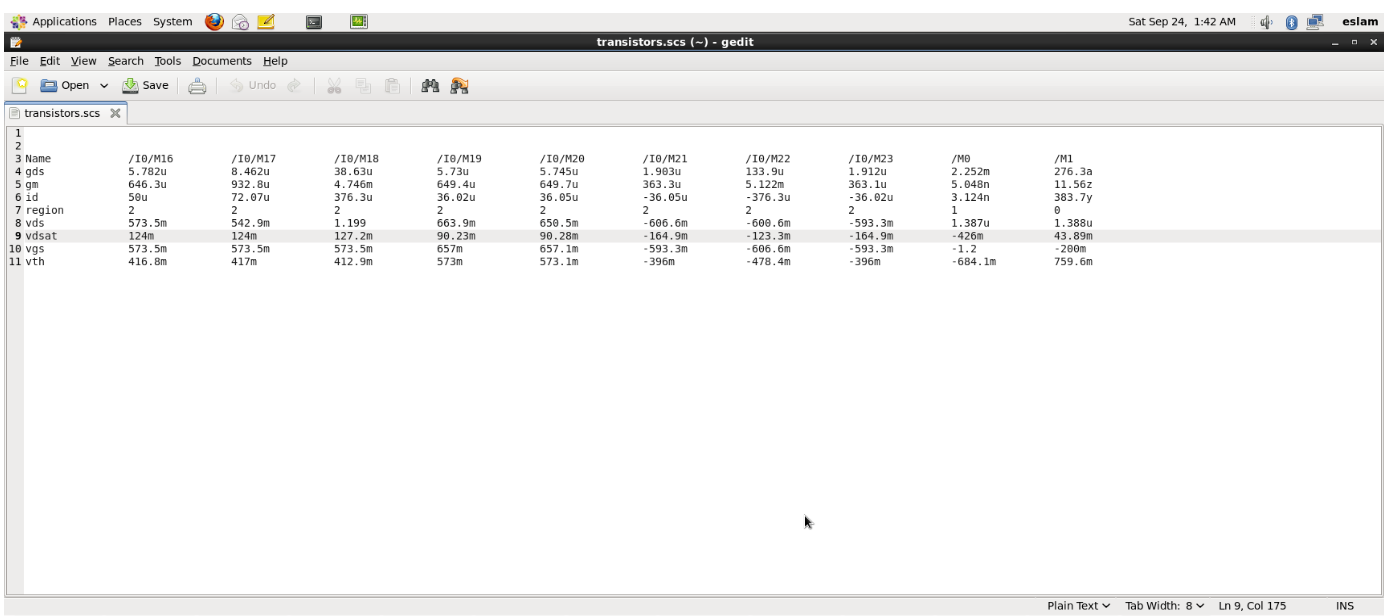
→op swing spec is satisfied.

Part4(closed loop simulation)

Closed loop testbench schematic:



Op point:



Name	/I0/M16	/I0/M17	/I0/M18	/I0/M19	/I0/M20	/I0/M21	/I0/M22	/I0/M23	/M0	/M1
gds	5.782u	8.462u	38.63u	5.73u	5.745u	1.903u	133.9u	1.912u	2.252m	276.3a
gm	646.3u	932.8u	4.746m	649.4u	649.7u	363.3u	5.122m	363.1u	5.048n	11.56z
id	50u	72.07u	376.3u	36.02u	36.05u	-36.05u	-376.3u	-36.02u	3.124n	383.7y
region	2	2	2	2	2	2	2	2	1	0
vds	573.5m	542.9m	1.199	663.9m	650.5m	-606.6m	-600.6m	-593.3m	1.387u	1.388u
vdsat	124m	124m	127.2m	90.23m	90.28m	-164.9m	-123.3m	-164.9m	-426m	43.89m
vgs	573.5m	573.5m	573.5m	657m	657.1m	-593.3m	-606.6m	-593.3m	-1.2	-200m
vth	416.8m	417m	412.9m	573m	573.1m	-396m	-478.4m	-396m	-684.1m	759.6m

→when I simulated closed loop I found that at 6 db gain the phase margin is very low so I found ringing in transient analysis and also I found that at some corners the PM is negative which means that circuit at this design sizing at some required corners is not stable so I redesigned the circuit by increasing Cc to be CL/2=250f as this decreasing UGF and increases PM as I want and makes the circuit stable at closed loop at all corners and also decreases peaking which disappeared at 1MHZ but this decreased UGF in open loop as I expected to improve PM but UGF spec was not satisfied at open loop at this value for Cc so I increased RZ to cancel the effect of feedforward zero which decreases UGF and decreases the second pole as it is in RHP so increasing RZ increases UGF and also improving PM which became satisfied in open loop and also makes closed loop PM greater then decreasing peaking as result and also guaranteed that circuit is stable at all corners.

So now, after changing Cc and RZ values I had new values for UGF and PM in open loop simulation and gain is same as expected so I will attach final values for open loop simulation:

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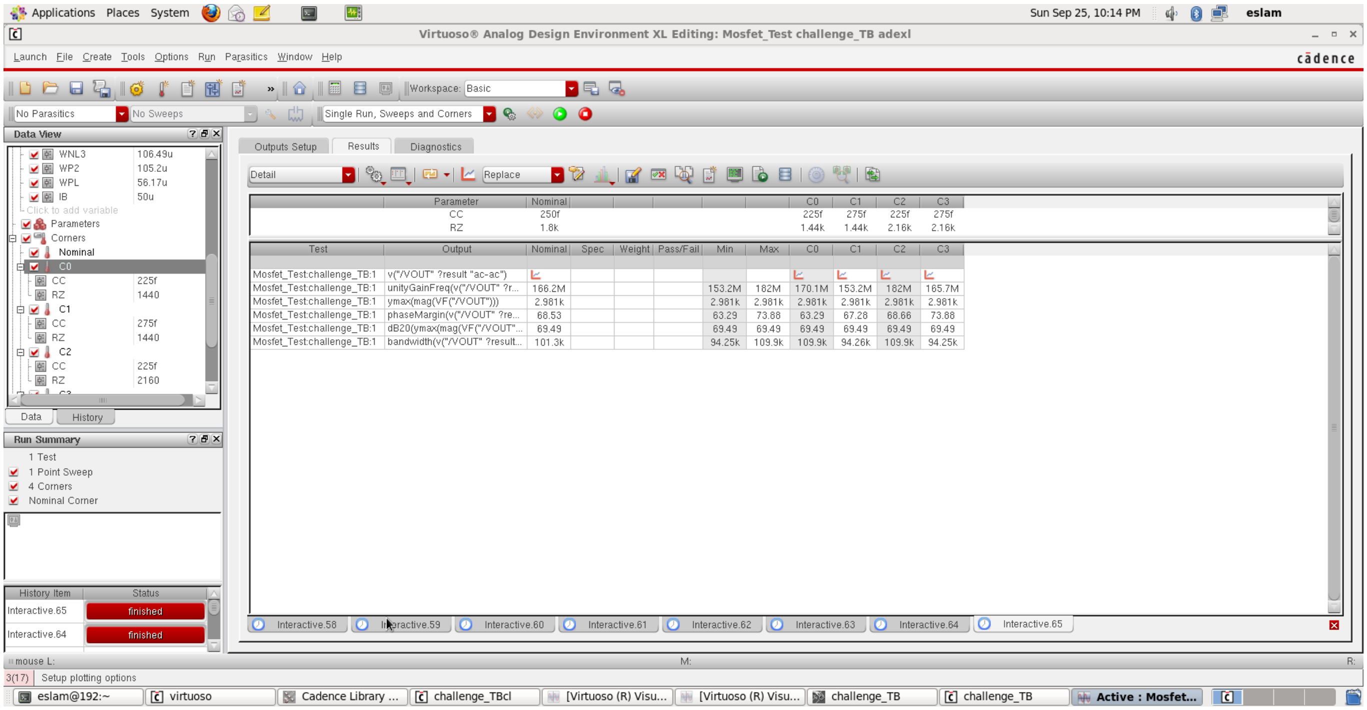
Open loop parameters after redesigning:



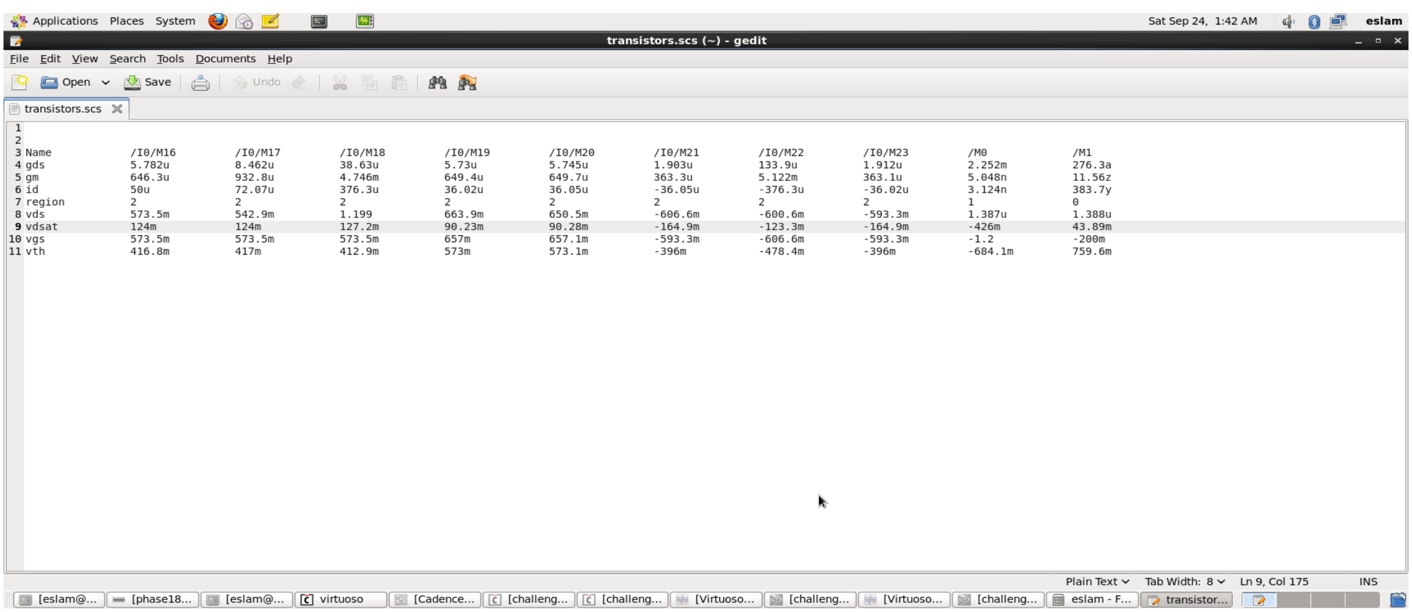
Virtuoso® Analog Design Environment XL Editing: Mosfet_Test challenge_TB adexl

Parameter	Nominal	C0	C1	C2	C3
CC	250f	225f	275f	225f	275f
RZ	1.8k	1.44k	1.44k	2.16k	2.16k

Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	C0	C1	C2	C3
Mosfet_Test:challenge_TB:1	v("/VOUT" ?result "ac-ac")										
Mosfet_Test:challenge_TB:1	unityGainFreq(v("/VOUT" ?r...	166.2M				153.2M	182M	170.1M	153.2M	182M	165.7M
Mosfet_Test:challenge_TB:1	ymax(mag(VF("/VOUT")))	2.981k				2.981k	2.981k	2.981k	2.981k	2.981k	2.981k
Mosfet_Test:challenge_TB:1	phaseMargin(v("/VOUT" ?re...	68.53				63.29	73.88	63.29	67.28	68.66	73.88
Mosfet_Test:challenge_TB:1	dB20(ymax(mag(VF("/VOUT"...	69.49				69.49	69.49	69.49	69.49	69.49	69.49
Mosfet_Test:challenge_TB:1	bandwidth(v("/VOUT" ?result...	101.3k				94.25k	109.9k	109.9k	94.26k	109.9k	94.25k

Satisfying specs at all corners.

Op point:



transistors.scs (~) - gedit

Name	/I0/M16	/I0/M17	/I0/M18	/I0/M19	/I0/M20	/I0/M21	/I0/M22	/I0/M23	/M0	/M1
gds	5.782u	8.462u	38.63u	5.73u	5.745u	1.903u	133.9u	1.912u	2.252m	276.3a
gm	646.3u	932.8u	4.746m	649.4u	649.7u	363.3u	5.122m	363.1u	5.048n	11.56z
id	50u	72.07u	376.3u	36.02u	36.05u	-36.05u	-376.3u	-36.02u	3.124n	383.7y
region	2	2	2	2	2	2	2	2	1	0
vds	573.5m	542.9m	1.199	663.9m	650.5m	-606.6m	-600.6m	-593.3m	1.387u	1.388u
vdsat	124m	124m	127.2m	90.23m	90.28m	-164.9m	-123.3m	-164.9m	-426m	43.89m
vgs	573.5m	573.5m	573.5m	657m	657.1m	-593.3m	-606.6m	-593.3m	-1.2	-200m
vth	416.8m	417m	412.9m	573m	573.1m	-396m	-478.4m	-396m	-684.1m	759.6m

M0,M1 are transmission gate transistors.

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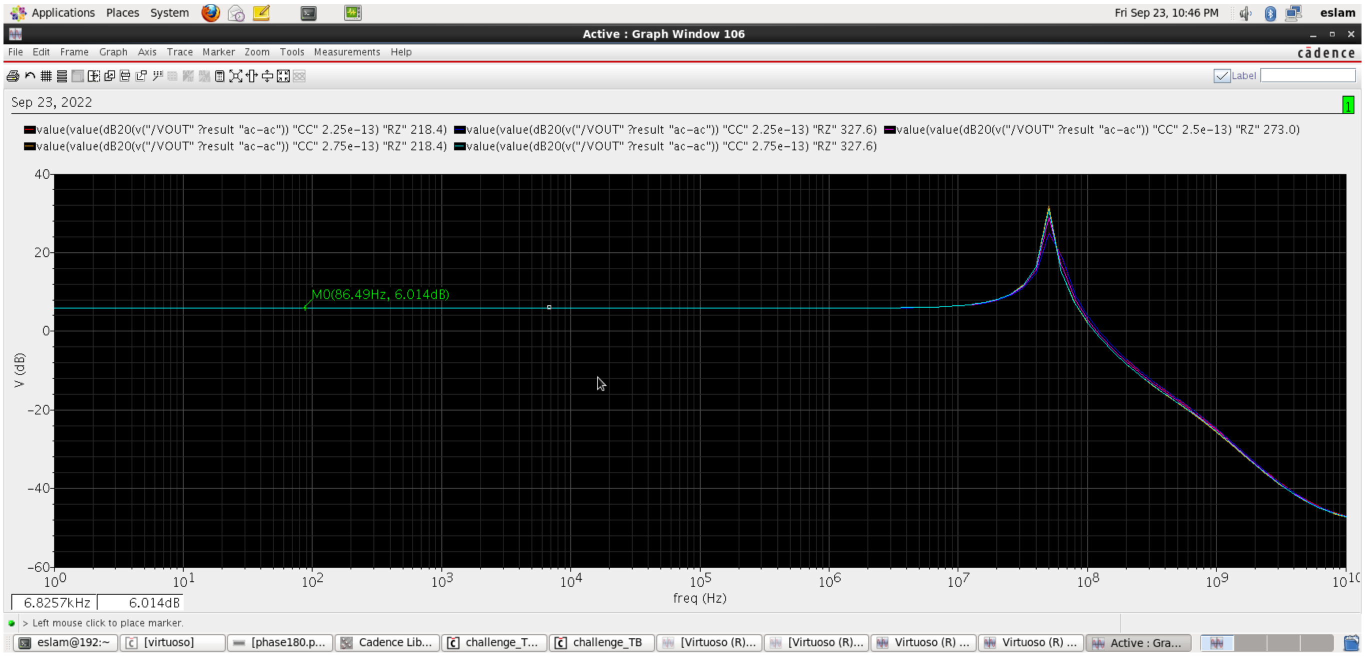
Closed loop at DO=0(6db):



There is some peaking due to zero effect which I tried to decrease this effect by RZ as I explained before and also I can decrease it by applying pole at this frequency to cancel the effect of this feedforward zero

UFG and PM across all corners:

Parameter	Nominal	C17	C18	C19	C20
Cc	250f	225f	225f	275f	275f
Rz	1.8k	1.44k	2.16k	1.44k	2.16k

Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	C17	C18	C19	C20
challenge:challengeswitch:1	dB20(VF("/VOUT"))										
challenge:challengeswitch:1	unityGainFreq(VF("/VOUT"))	125M				119.4M	135.3M	128.8M	135.3M	119.4M	123.5M
challenge:challengeswitch:1	phaseMargin(VF("/VOUT"))	60.89				55.86	66.26	55.86	61.69	59.05	66.26
challenge:challengeswitch:1	getData("/phaseMargin" ?res...	4.084				405.8m	7.738	405.8m	2.804	4.912	7.738
challenge:challengeswitch:1	bandwidth(VF("/VOUT") 3 "l...	104.3M				98.45M	111.9M	108.6M	111.9M	98.45M	100.7M

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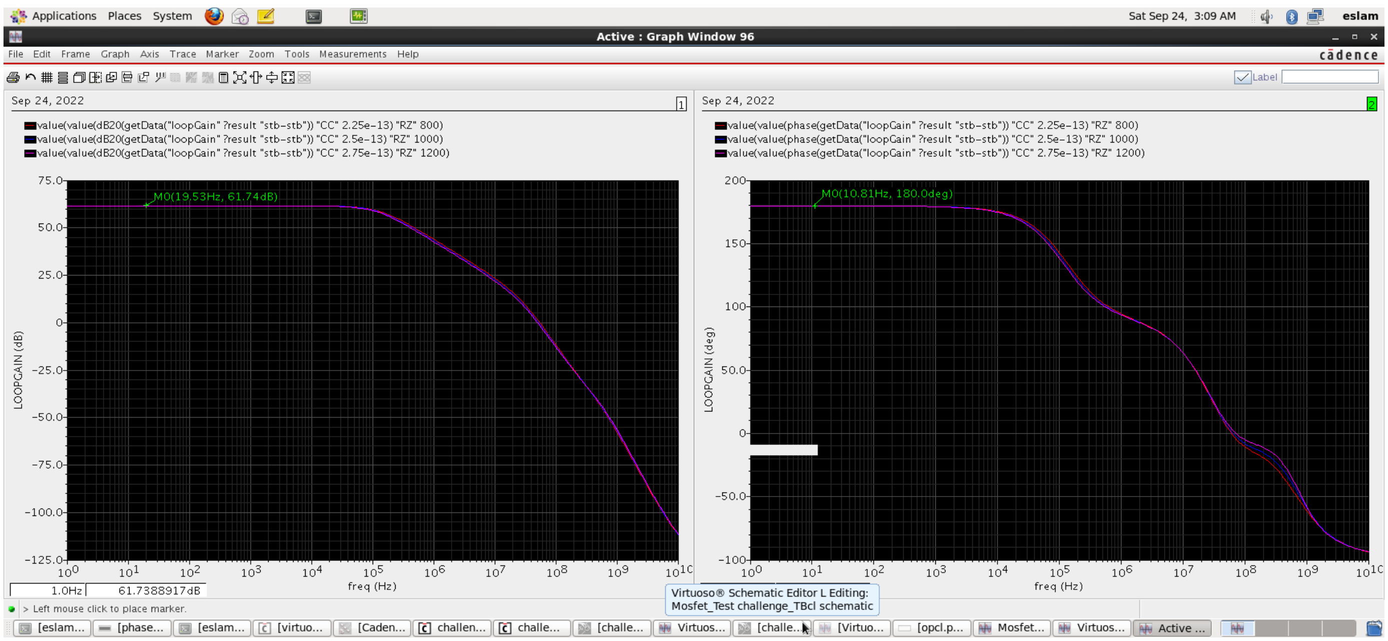
I also attached PM of loop gain by stb analysis at all corners and as shown the circuit is stable at all corners and also I can improve this PM more by adding pole at this frequency to cancel this effect of this feedforward zero.

<u>Loop gain simulation at all corners:</u>



→the value ≈60db as expected as open loop ≈2k and $\beta \approx \frac{1}{2}$

<u>transient simulation at all corners:</u>

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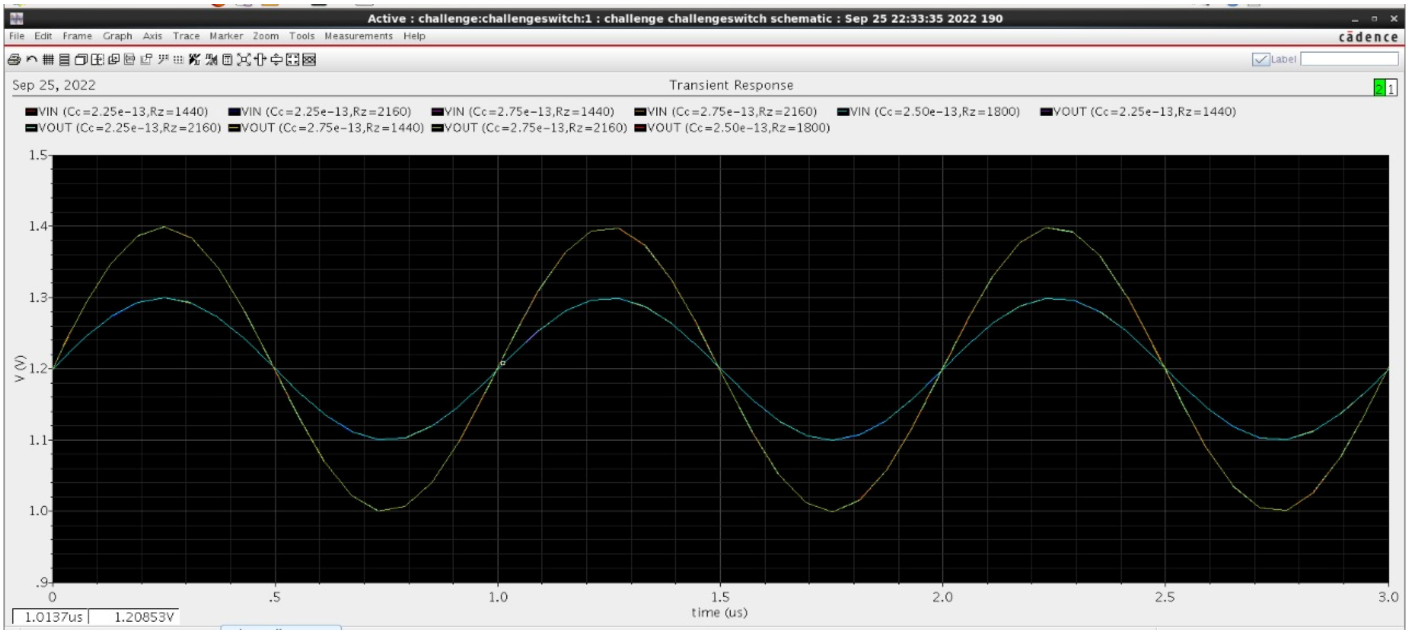
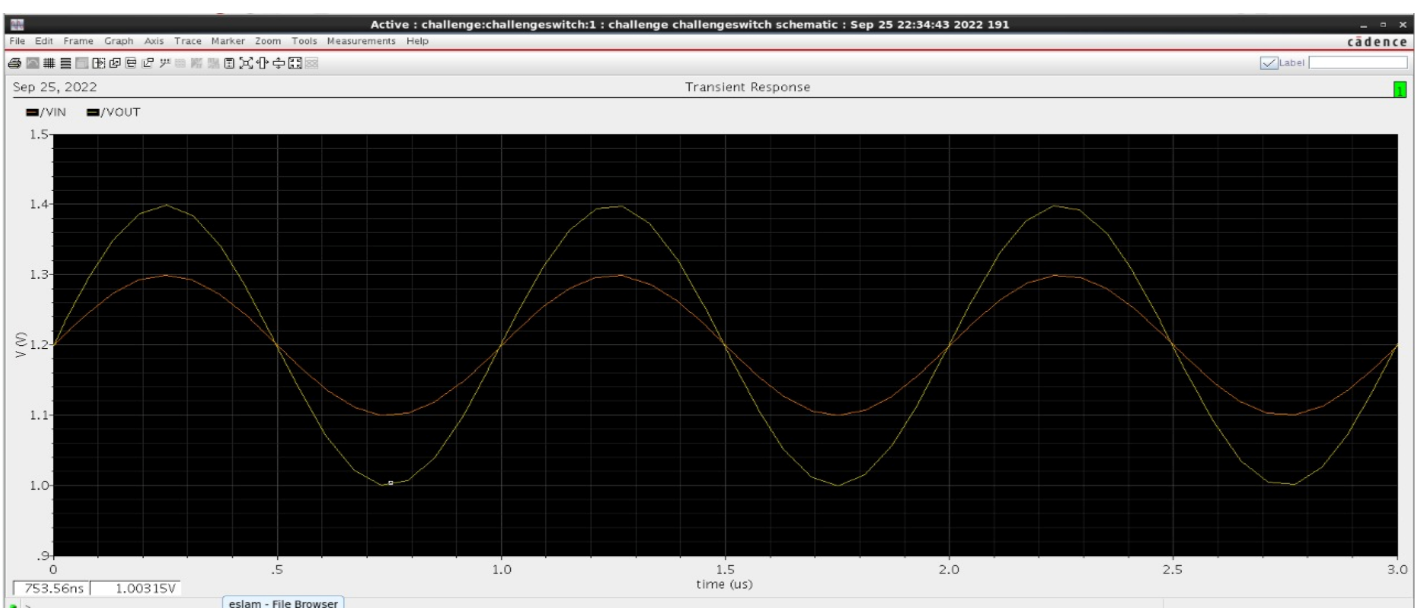


→as shown the circuit is stable at all corners and also no peaking occurs at this frequency as I tried to cancel zero effect before as I explained.

Transient simulation at nominal value:



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→the max value $=1.2+\left(100m*gain(2)\right)=1.4v$

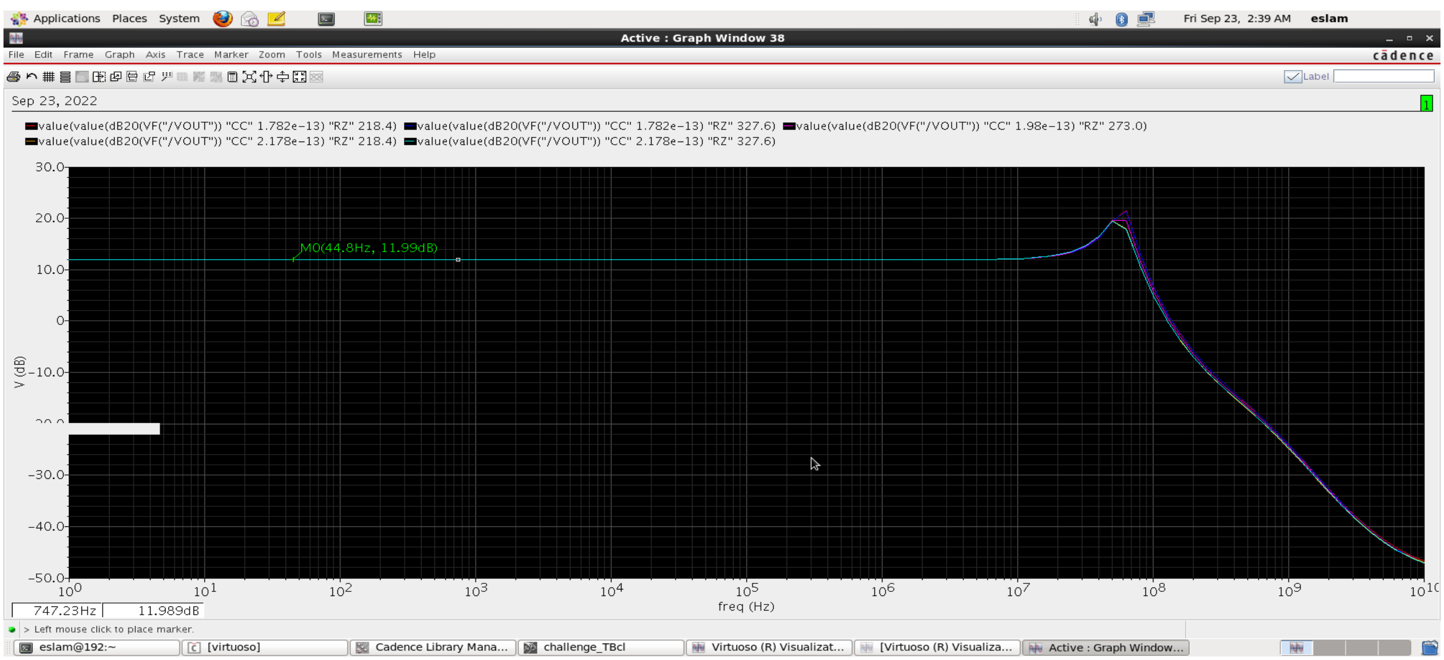
→the min value$=1.2-\left(100m*gain(2)\right)=1v$

As input is sinusoidal with 100mv amplitude.

→the output swing$=0.4v$

Test	Output	Nominal	Spec	Weight	Pass/Fail
challenge:challengeswitch:1	/VOUT				
challenge:challengeswitch:1	peakToPeak(v("/VOUT" ?res...	399.9m			
challenge:challengeswitch:1	/VIN				

<u>Closed loop at Do=1(12db):</u>



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There is some peaking due to zero effect which I tried to decrease this effect by RZ and Cc as I explained before and also I can decrease it by applying pole at this frequency to cancel the effect of this feedforward zero.

<u>UGF and PM across all corners:</u>

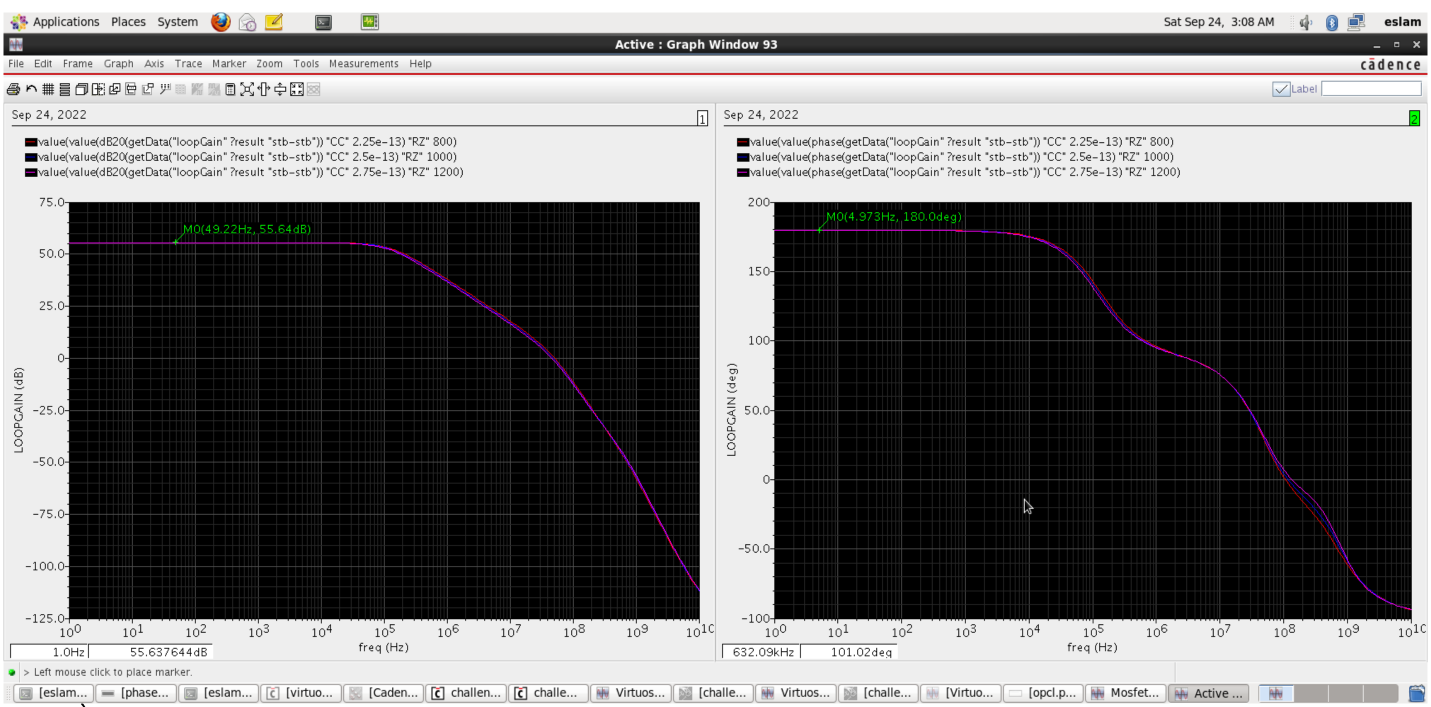
Detail | Replace

Parameter	Nominal	C17	C18	C19	C20
Cc	250f	225f	225f	275f	275f
Rz	1.8k	1.44k	2.16k	1.44k	2.16k

Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	C17	C18	C19	C20
challenge:challengeswitch:1	dB20(VF("/VOUT"))										
challenge:challengeswitch:1	unityGainFreq(VF("/VOUT"))	137.4M				126.4M	147.4M	141.4M	147.4M	126.4M	134.9M
challenge:challengeswitch:1	phaseMargin(VF("/VOUT"))	62.88				57.87	68.2	57.87	63.62	61.28	68.2
challenge:challengeswitch:1	getData("/phaseMargin" ?res...	23.03				19.36	26.6	19.36	21.34	24.32	26.6
challenge:challengeswitch:1	bandwidth(VF("/VOUT") 3 "l...	78.36M				75.64M	83.12M	81.53M	83.12M	75.64M	76.39M

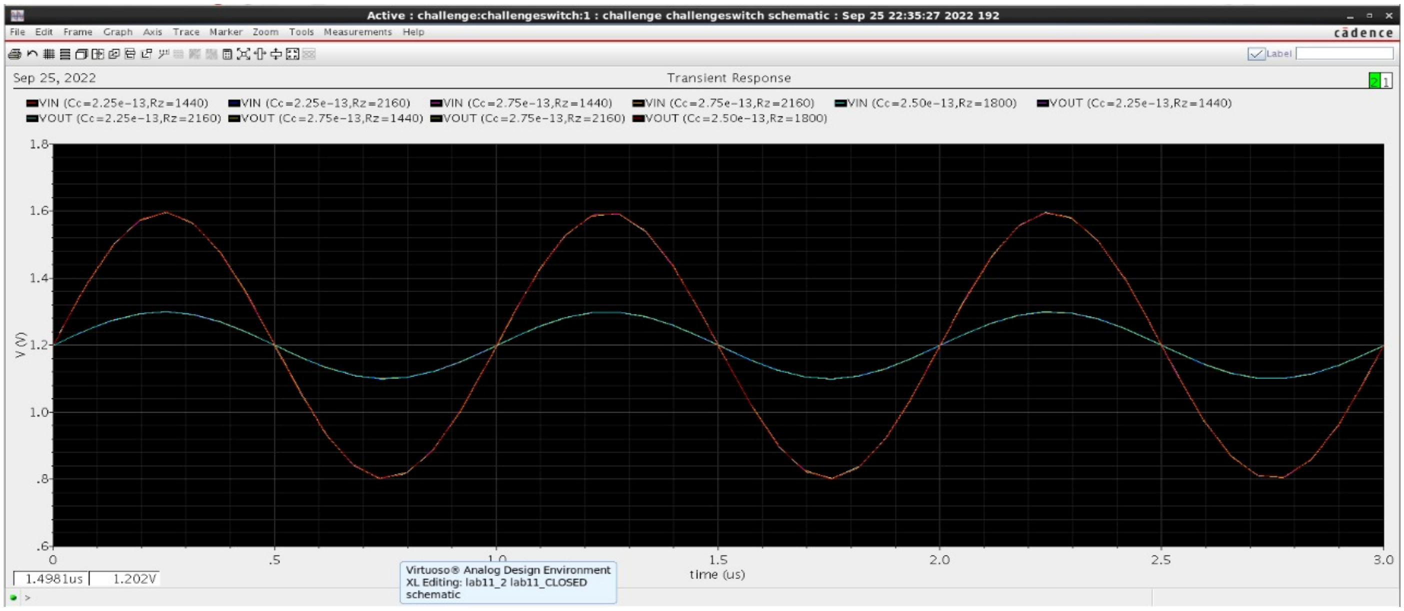
I also attached PM of loop gain at all corners and as shown the circuit is stable at all corners.

<u>Loop gain simulation:</u>



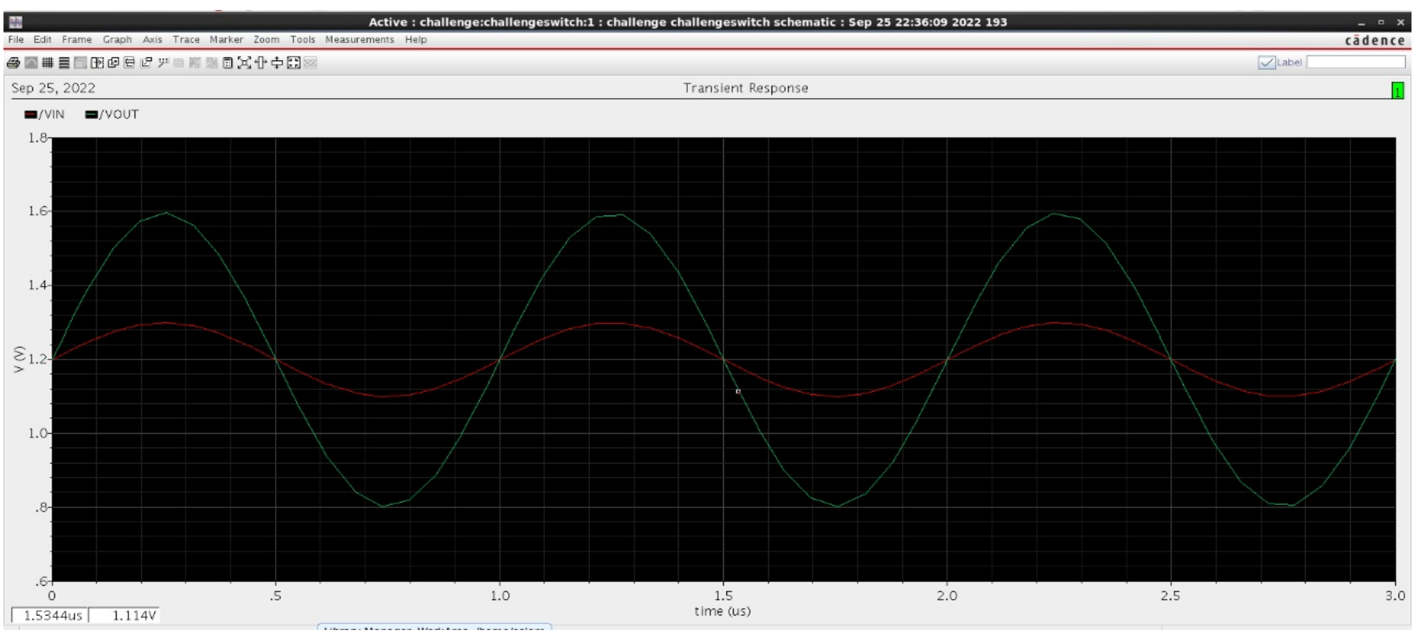
→ the value ≈54db as expected as open loop ≈2k and $\beta \approx \frac{1}{4}$

Transient simulation at all corners:



→as shown the circuit is stable at all corners

Transient simulation at nominal value:

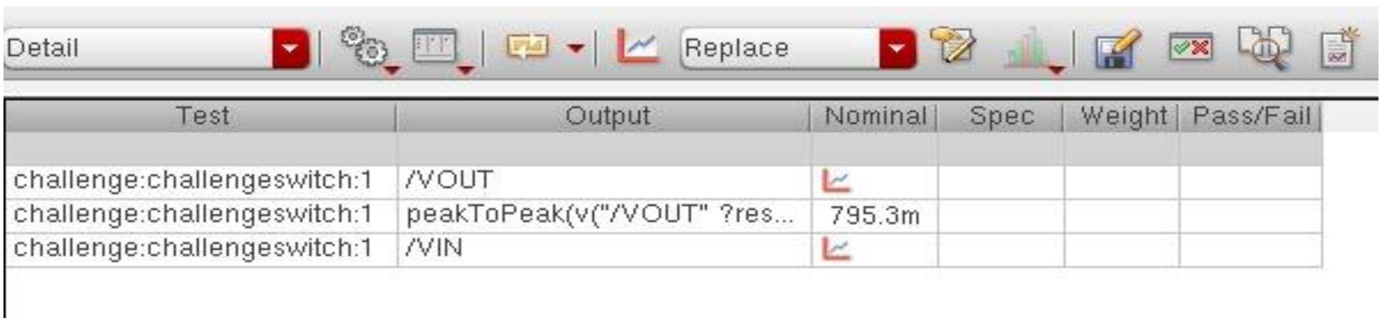


→the max value =1.2 $+ \left(100m * gain(4)\right) \approx 1.6v$

→the min value=1.2 $- \left(100m * gain(4)\right) \approx 0.8v$

As the input is sinusoidal with 100mv amplitude.

→the output swing $\approx 0.8v$



Test	Output	Nominal	Spec	Weight	Pass/Fail
challenge:challengeswitch:1	/VOUT				
challenge:challengeswitch:1	peakToPeak(v("/VOUT" ?res...	795.3m			
challenge:challengeswitch:1	/VIN				

<u>Comparing UGF and PM in closed loop and open loop :</u>

UGF: we can see that UGF decreases by decreasing gain so open loop has larger gain then at 12db has larger value than 6db.

PM: we can see that PM decreases as at feedback node the feedback resistance will create pole and this will be the first non-dominant pole so wp2 decreases so PM decreases than open loop state and also as at 12db rout of feedback node is smaller so wp2 will be larger so PM in 12db is better than PM at 6db but also they are smaller than open loop case state as I explained.

parameter	Open loop	D0=0(6db)	D0=1(12db)
UGF	166.2M	125M	137.4M
PM	68.35	60.89	62.88

So, decreasing feedback resistance is also solution to increase PM and get stability easily. But I only increased Rz as putting zero is LHP to get higher UFG and also higher phase and achieve stability and no peaking at all corners as shown and explained before but only I would like here to explain that decreasing feed back resistance was solution but we are forced to use specific value=100k.

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