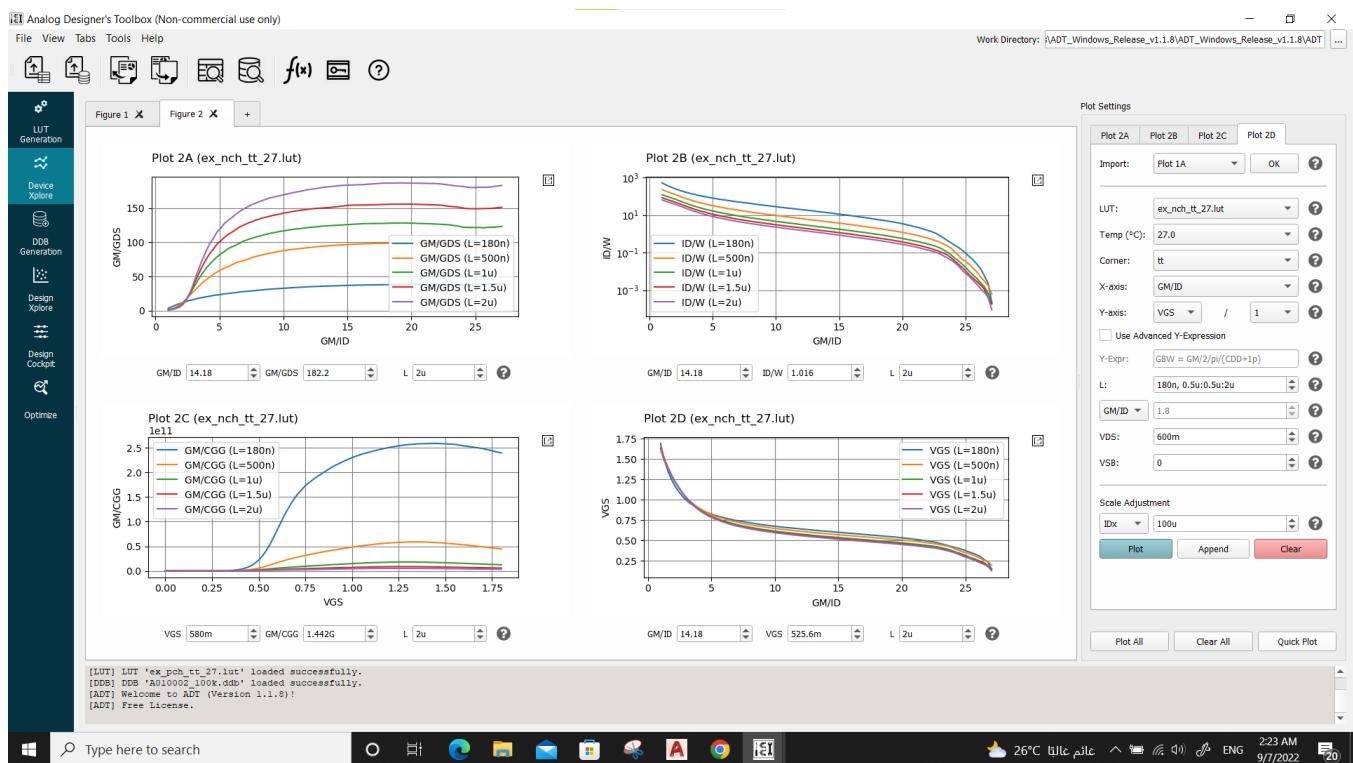


Lab 09

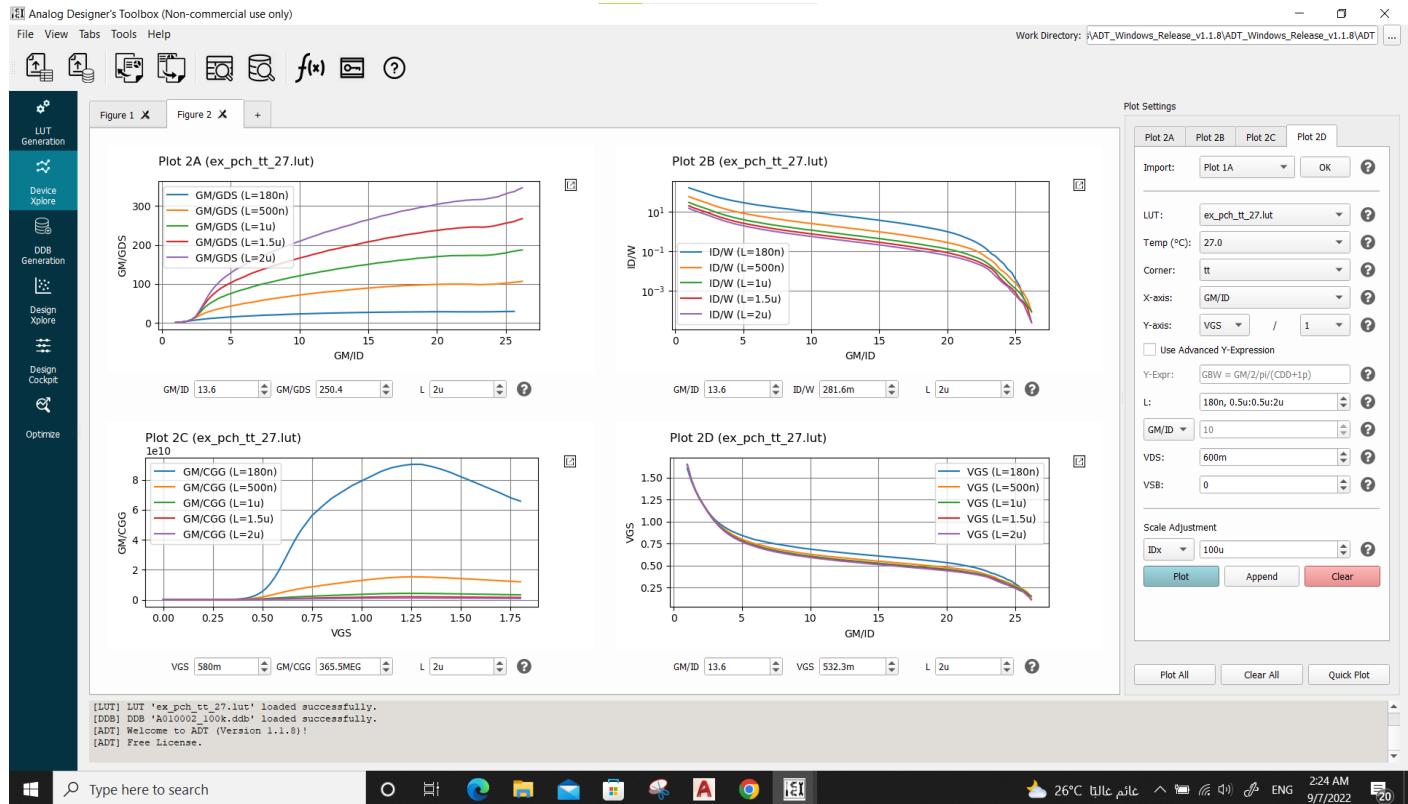
Part 1

Graphs from adt:

Nmos:



Pmos:



Part2

Design procedure:

$$\rightarrow \omega_{pcl} = GBW = \frac{1}{\tau} = 5MHz, GBW = \frac{gm1,2}{2\pi Cc},$$

$$gm1,2 = 78.5\mu s$$

$$\rightarrow IB1 = SR \times Cc = 12.5\mu A$$

$$\rightarrow \frac{gm1,2}{ID} = 12.56$$

$$\rightarrow IB2 = 60 - 12.5 = 47.5\mu A$$

$$\begin{aligned} \rightarrow Acl &= \frac{Aol}{1+\beta Aol} = \frac{Aol}{\beta Aol} \left(\frac{1}{1+\frac{1}{\beta Aol}} \right) = \frac{1}{\beta} \left(1 - \frac{1}{\beta Aol} \right) \\ &= 1 - \frac{1}{Aol} \quad \rightarrow \beta = 1 \end{aligned}$$

$$\rightarrow 0.0005 = \frac{1-Aol}{Aol}, Aol = 2000$$

\rightarrow first stage has larger gain as first stage for DC gain and second stage for max swing then first stage must have larger gain.

$$\rightarrow 2v^2 = 2000, v = \text{gain of second stage}$$

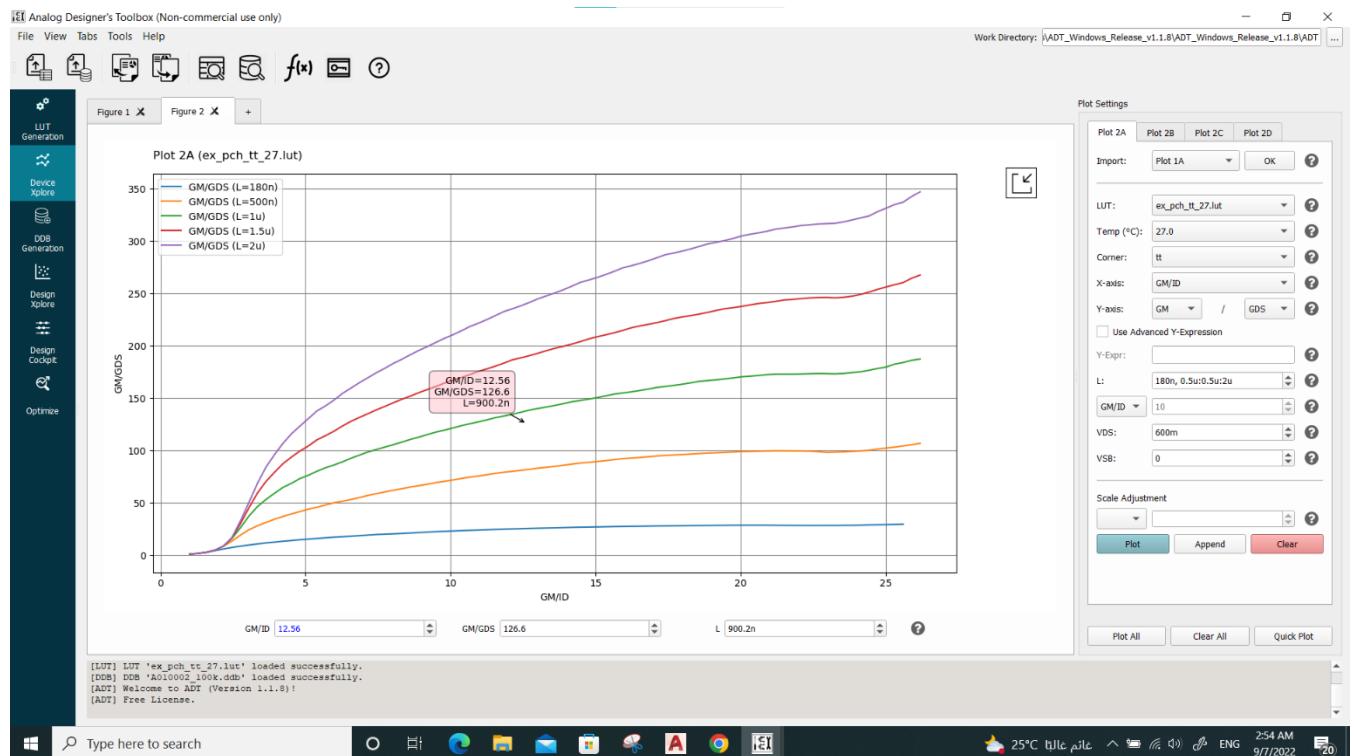
$$= 31.622 = 30db$$

→ gain of second stage = $63.244 = 36db$

→ gain = $\frac{gmro}{2} = 63.244, gds = 0.62\mu s$

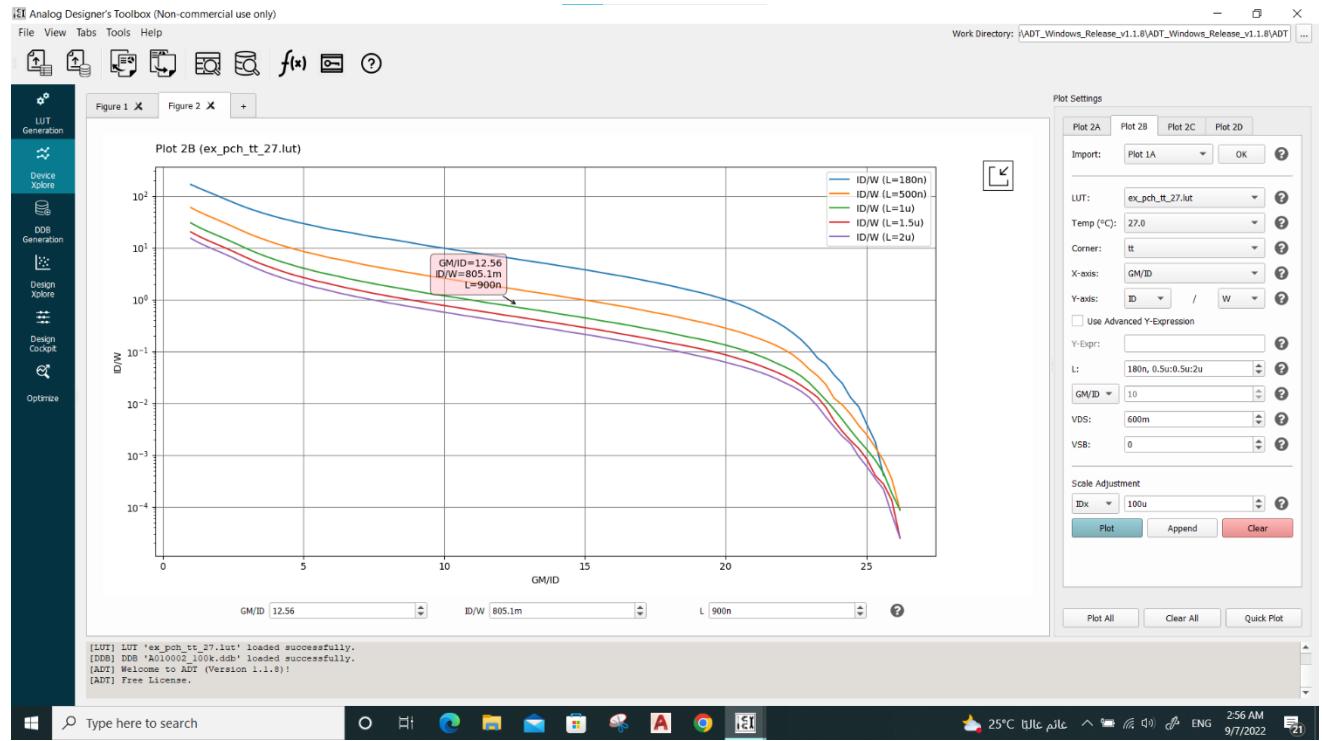
From adt charts get l and w for input pair:

L chart:



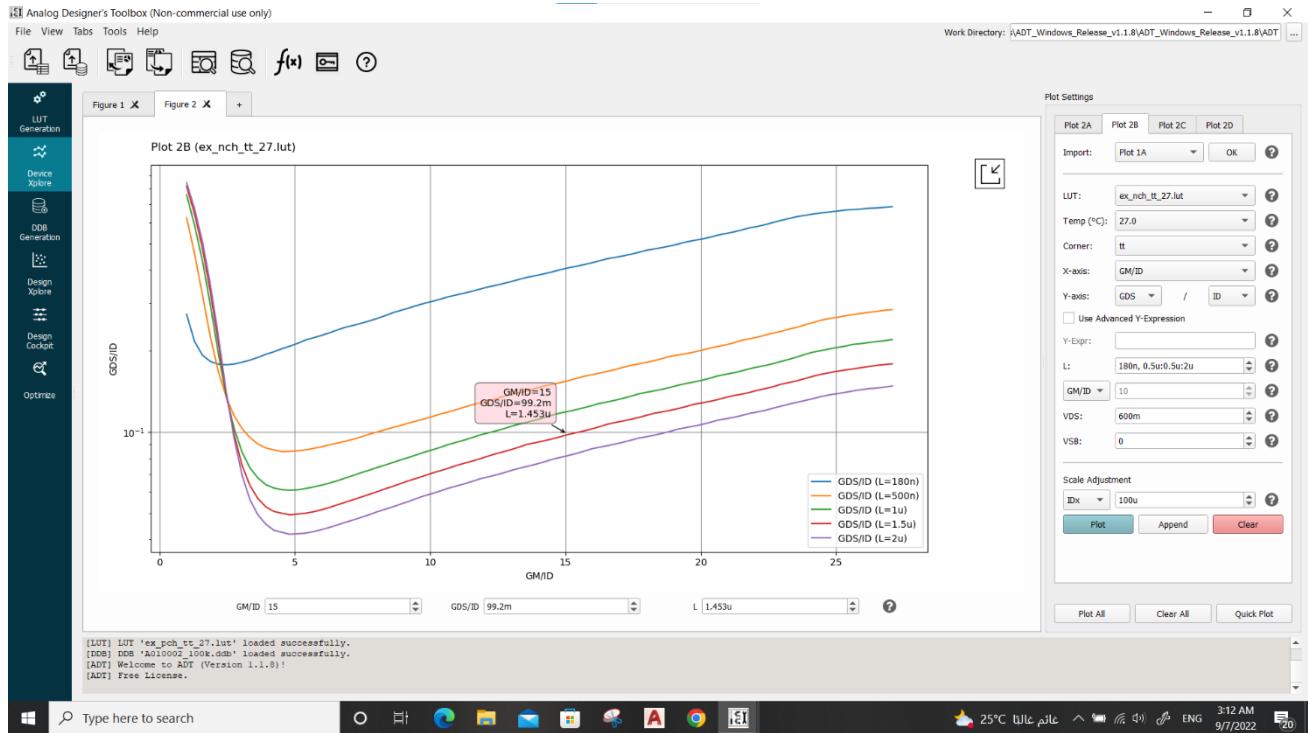
→ $l=900.2nm$

Id/w chart:



$$w = \frac{6.25}{805.1m} = 7.76\mu m$$

For active load charts:



L=1.453u for gm/id=15.

Id /w chart:



$$w = \frac{6.25}{1.202} = 5.19\mu m$$

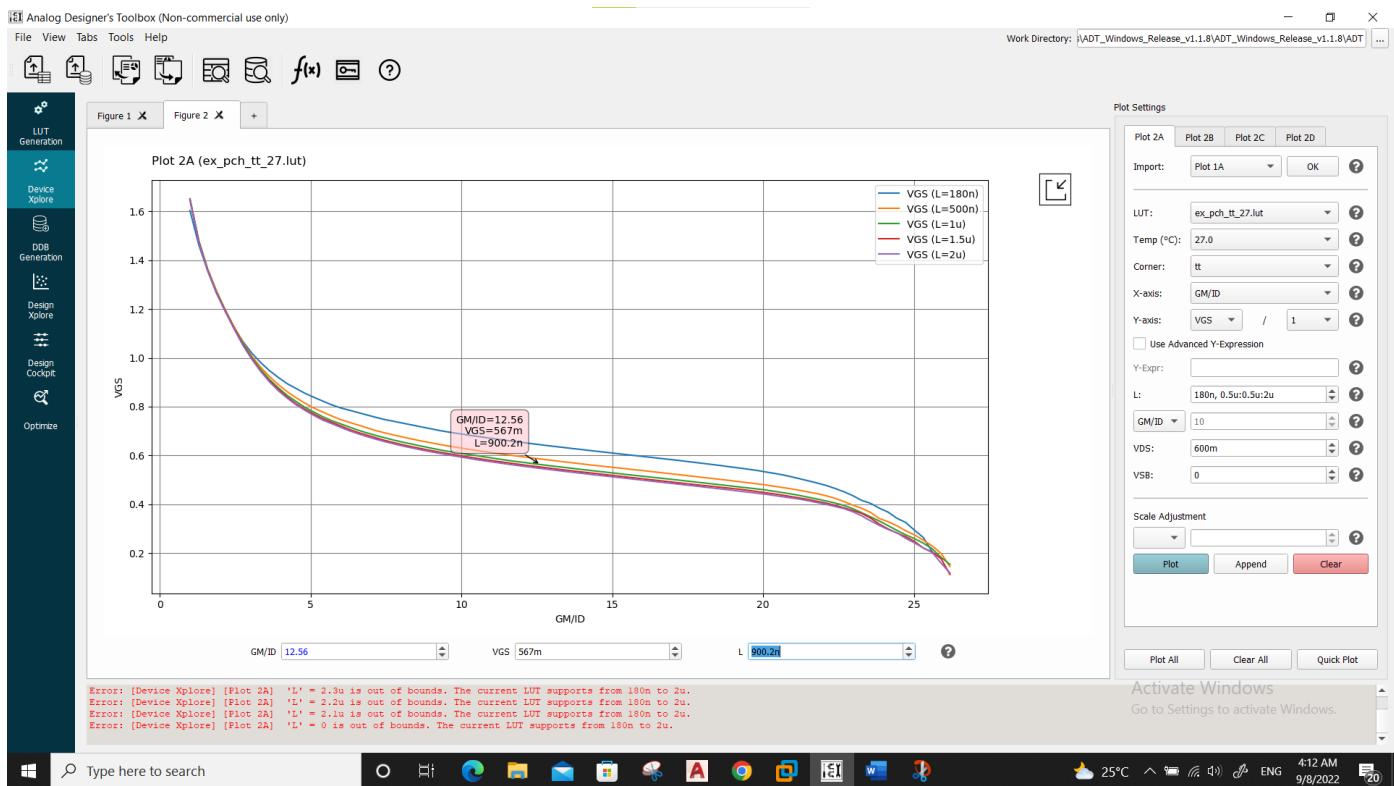
$$\rightarrow wp2 = 20MHz = \frac{gm}{2\pi cl}, gm = 628\mu s$$

$$\rightarrow \frac{gm}{id} = 13.22$$

$$\rightarrow v * < VDD - vi - vgs, v * max = 0.224v$$

$$\rightarrow \frac{gm}{id} = \frac{2}{v*} = 8.928$$

\rightarrow vgs of input pair from adt chart = 576mv

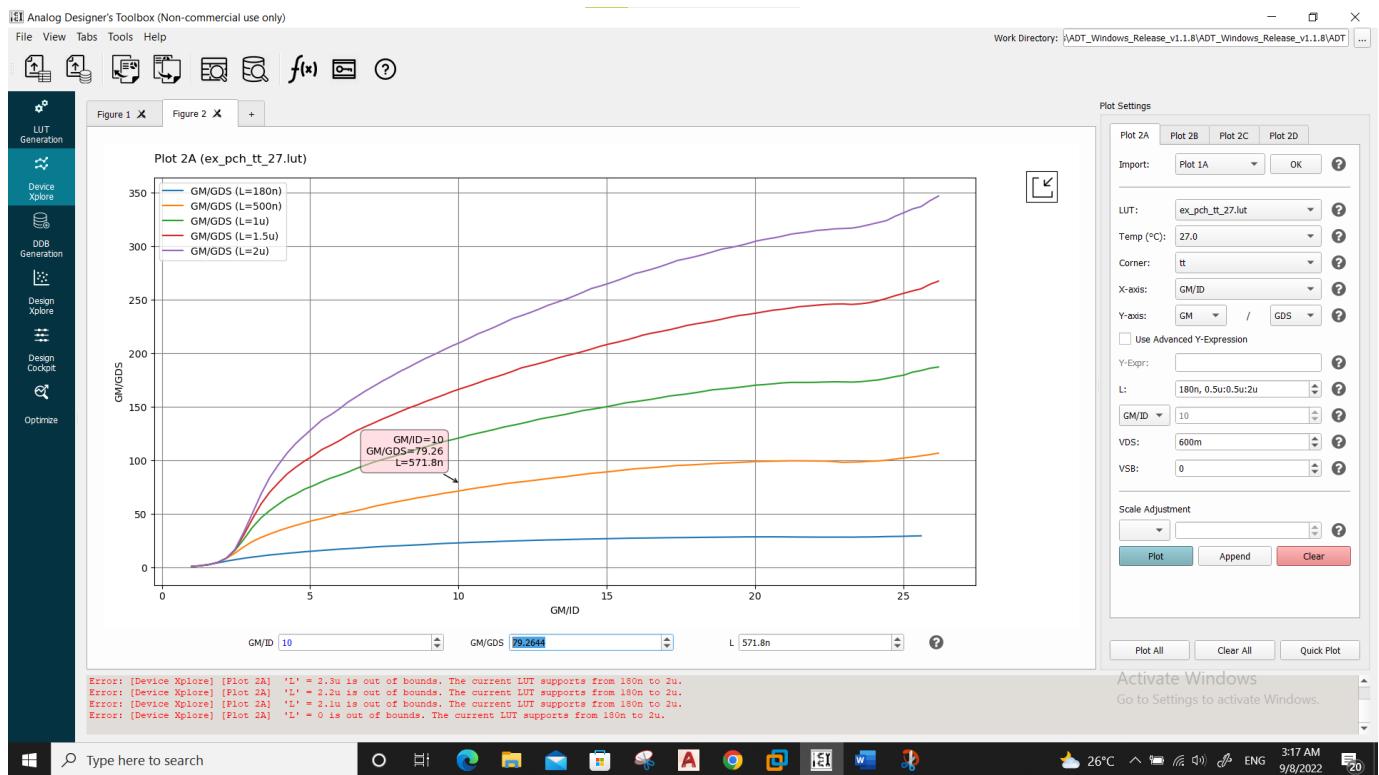


$$\rightarrow cmrr = \frac{Adif}{Acm} = 63.244 * 2r0 * gm,$$

$$gm = 62.5\mu s, gds \text{ of tail} = 1.577\mu s$$

\rightarrow now get l and w for tail cs of first stage:

L chart:



$$l=571.8nm$$

Id/w chart:



$$w = \frac{12.5}{2.203} = 5.67 \mu m$$

→ hint:

I used $gm/id = 10$ not 8 as we use moderate inversion

→ for second stage load has same I so same gm/gds
for same gm/id that I assumed to be 10

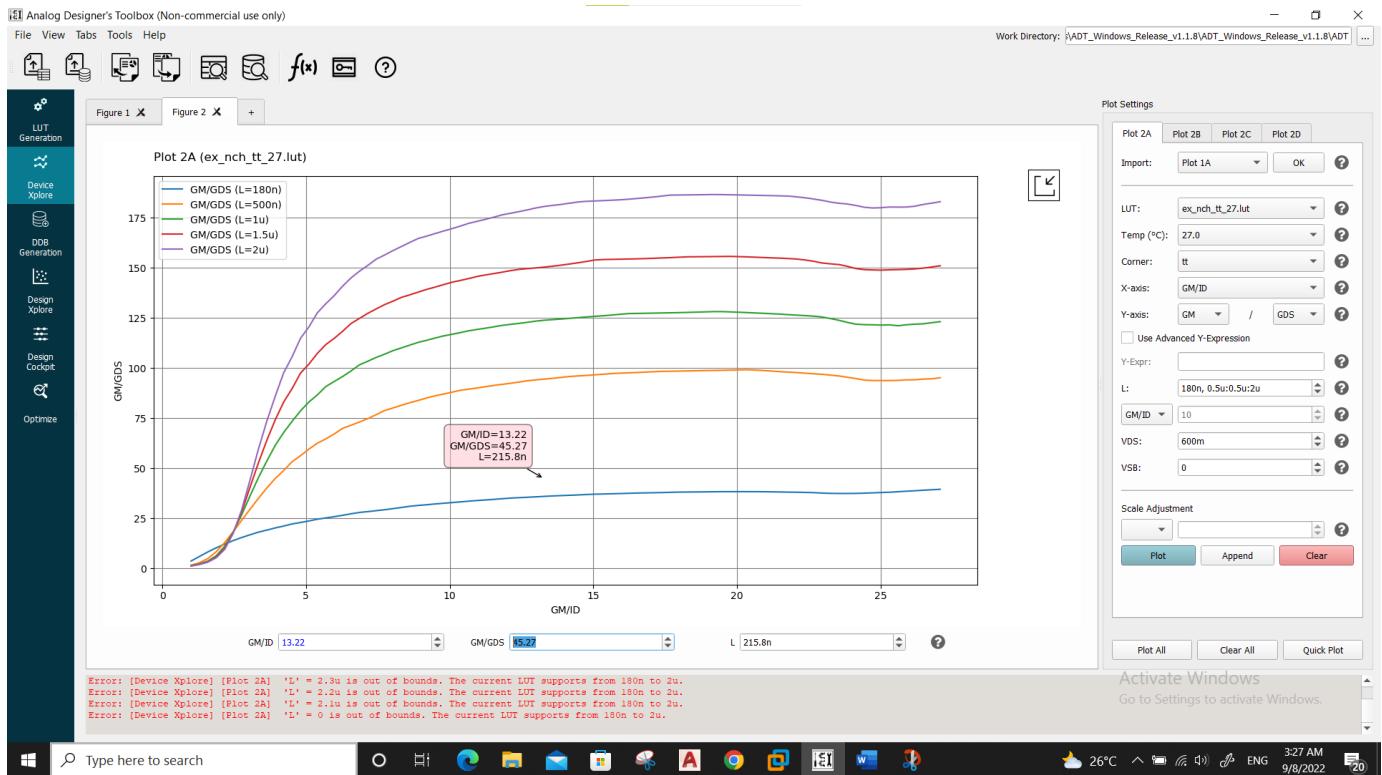
$$gm = 475\mu s, gds = 5.99\mu s$$

$$\rightarrow w = 5.67 * \frac{47.5}{12.5} = 21.546\mu m$$

→ gain = gm * ro1 parallel ro2 = 31.622

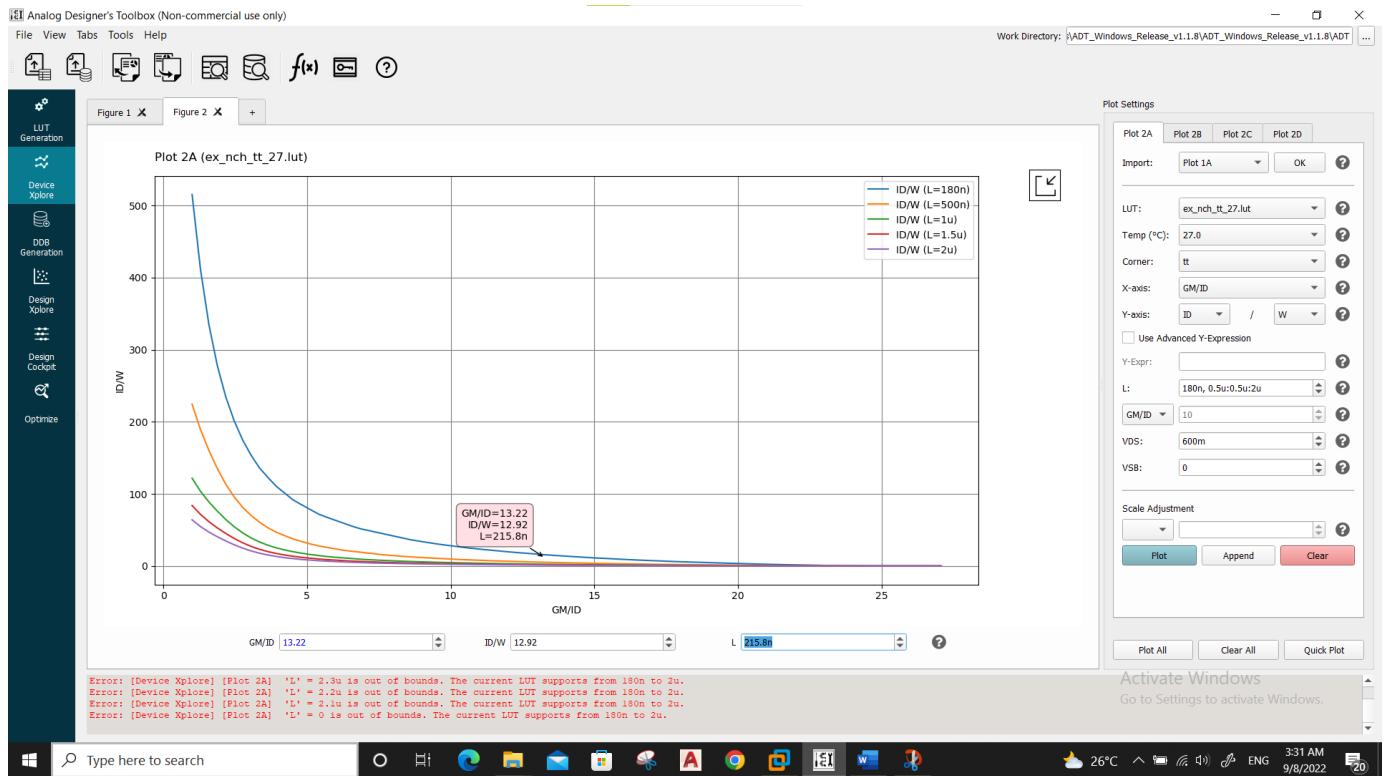
→ gds of input second stage = 13.87μs

Lchart:



$$l = 215.8n$$

Id/W chart:



$$w = \frac{47.5}{12.92} = 3.676\mu m$$

Vgs chart:



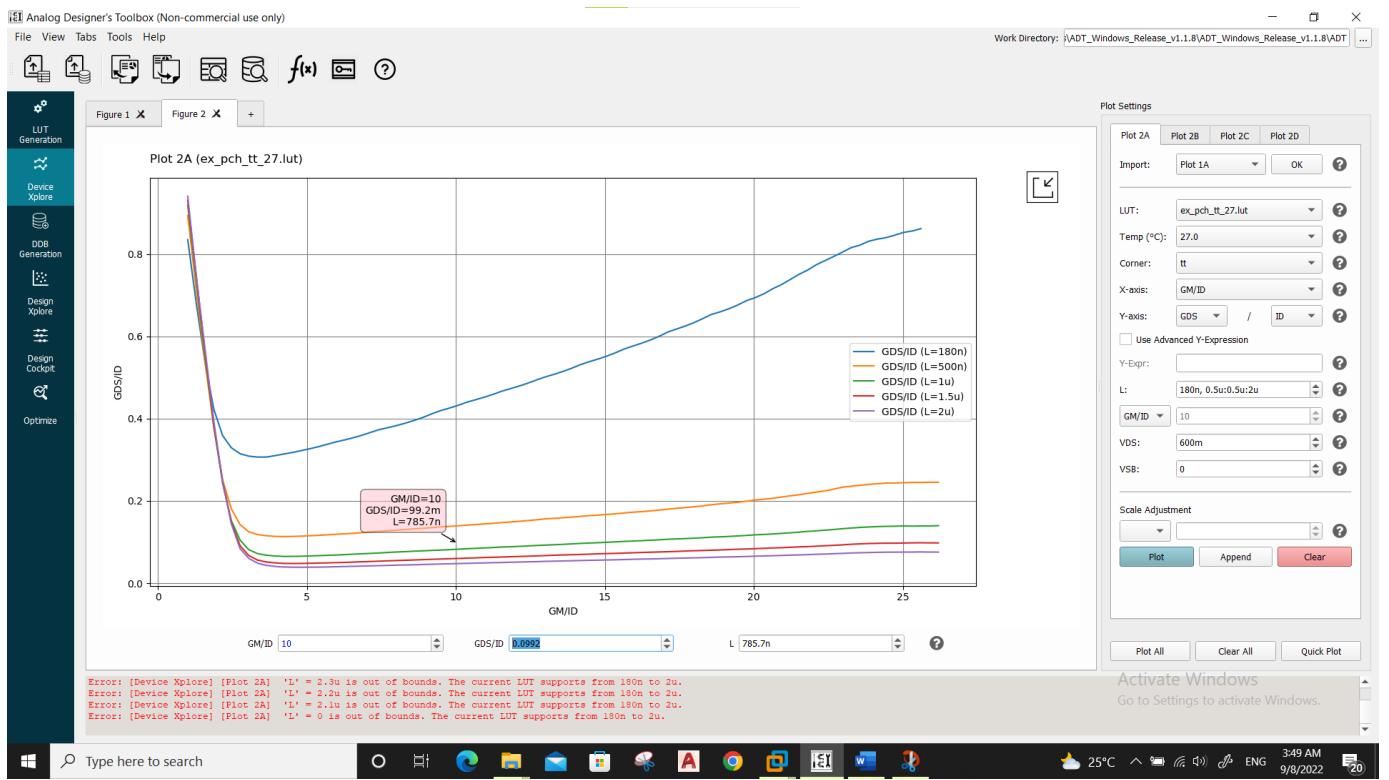
$$v_{gs} = 621.4 \text{ mV}$$

Check vgs for cative load:



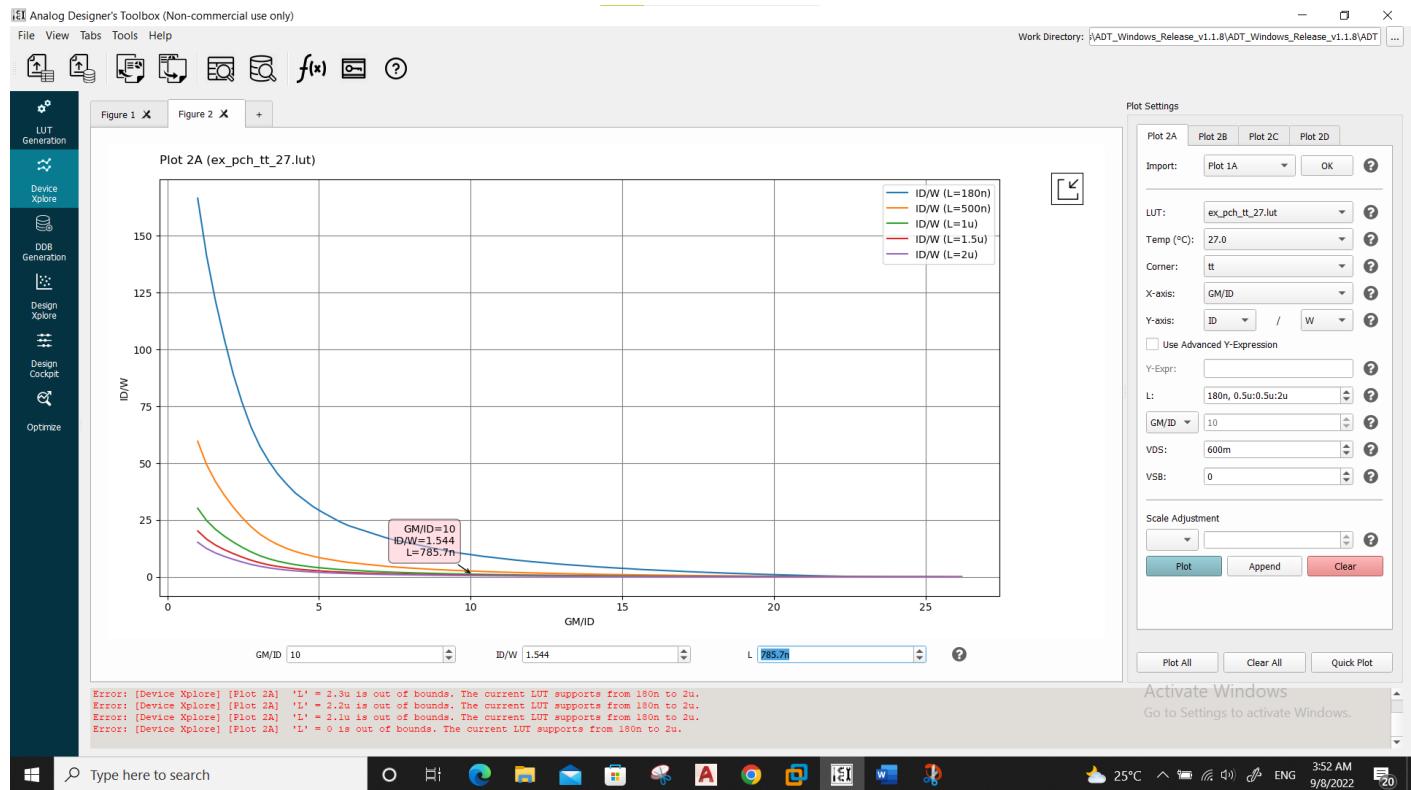
It is satisfied at gm/id less than 10 which can affect cmrr
so I will re iterate for gm/id =10

L chart:



$$l = 785.7\text{nm}$$

Id/w chart:



$$w = \frac{6.25}{1.544} = 4.047\mu m$$

Verification of output swing:

Max op = $VDD - v * OF$ op load of second stage =
 $1.8 - 0.2 = 1.6$

Min op = $v * of ip of second stage = \frac{2}{13.22} = 0.15$

→ op swing = $1.6 - 0.15 = 1.44$

→ op swing range is satisfied.

Verivication of cmir:

→ $v_{imax} = VDD - vgsip - v * cm = 1.033v$

→ $v_{inmin} = vgs of active load - vthip = 0.2064v$

→ cmir is satisfied.

→ $RZ = \frac{1}{g_{minput\ 2nd\ stage}} = \frac{1}{628\mu} = 1.59k\Omega$.

Cause of using nmos or pmos:

For first stage I used pmos as cmir its low value is near to ground and its high value is far away from VDD.

For second stage I used nmos as tail cs of first stage is pmos as input of first stage is pmos as I satisfied before so the mirroring current for the second stage is pmos so the input stage must be nmos.

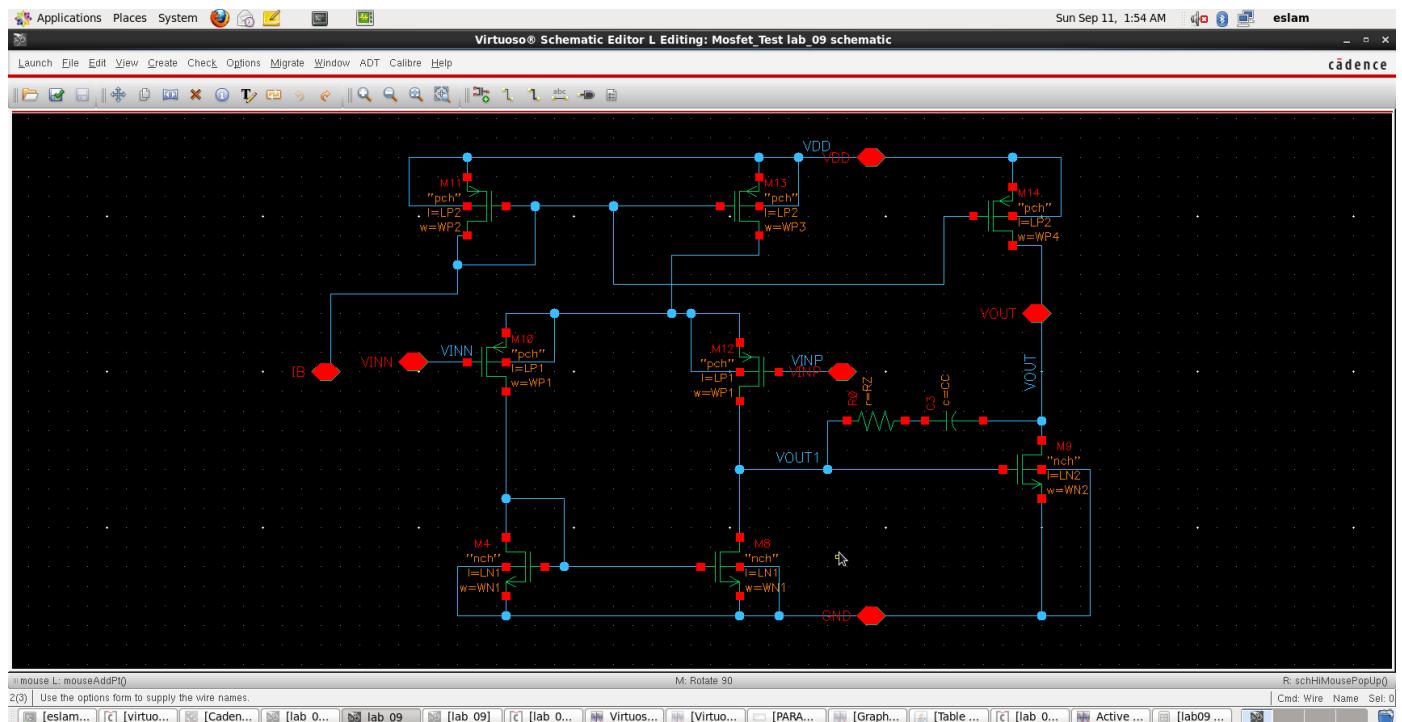
And as input of first stage is pmos and tail cs is pmos as result so active load will be nmos.

Table showing parameters calculated from charts:

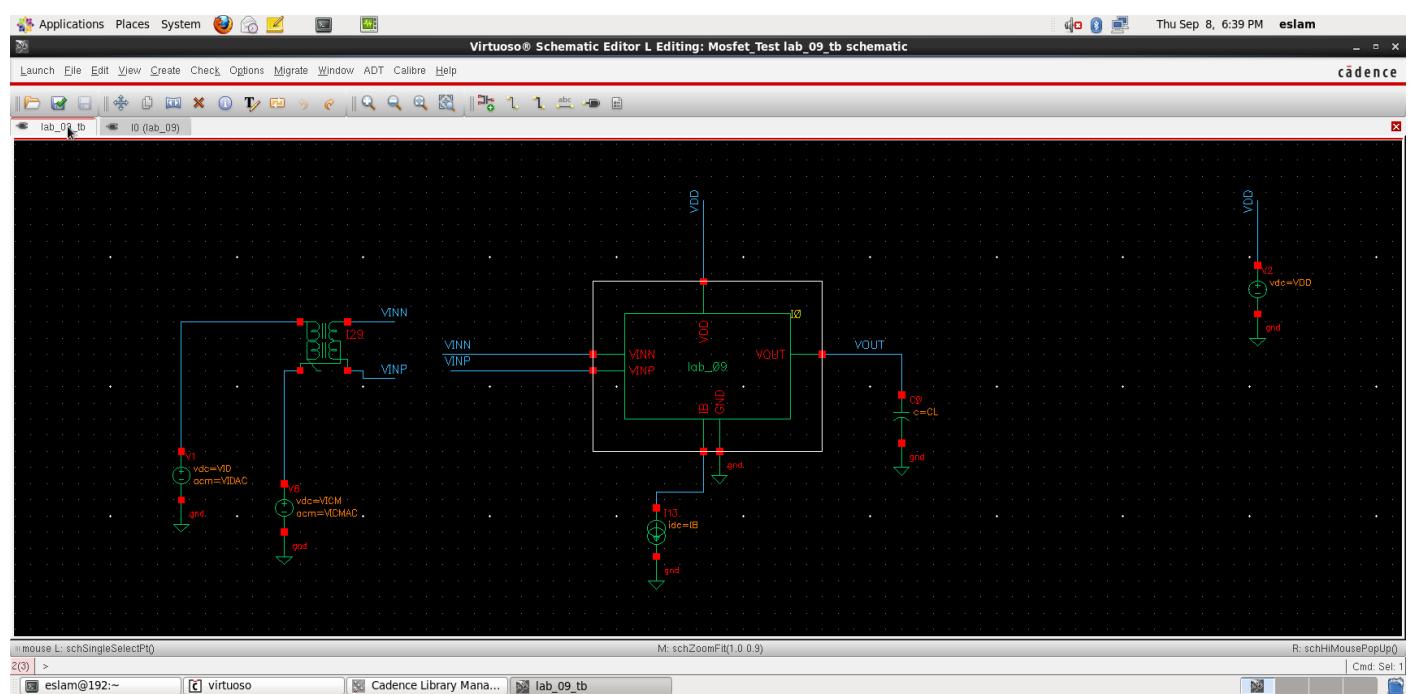
parameter	w	I	gm	id	Gm/id	vdsat	vov	V*
Input pair	7.76u	900.2n	78.5u	6.25u	12.56	132.2m	161m	159m
Active load	4.047u	785.7n	62.5u	6.25u	10	157.4m	206.4m	200m
2 nd input stage	4u	215.2n	627.6u	47.5u	13.22	115.4m	139.8m	151m
Tail cs	4.536u	571.8n	100u	10u	10	166.3m	195.3m	200m
	5.76u	571.8n	125u	12.5u	10	166.3m	195.3m	200m
	21.4u	571.8n	475u	47.5u	10	166.3m	195.3m	200m

Part3

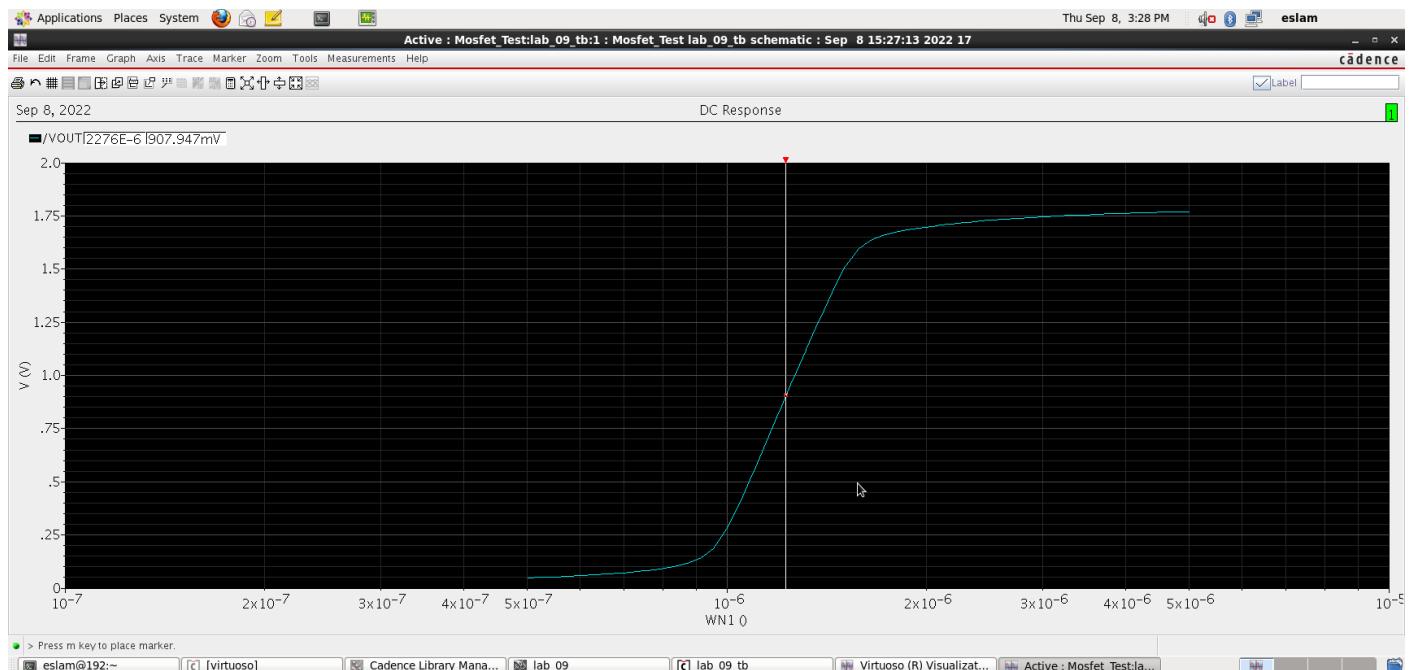
Schematic1(transistor level):



Schematic2(test bench):

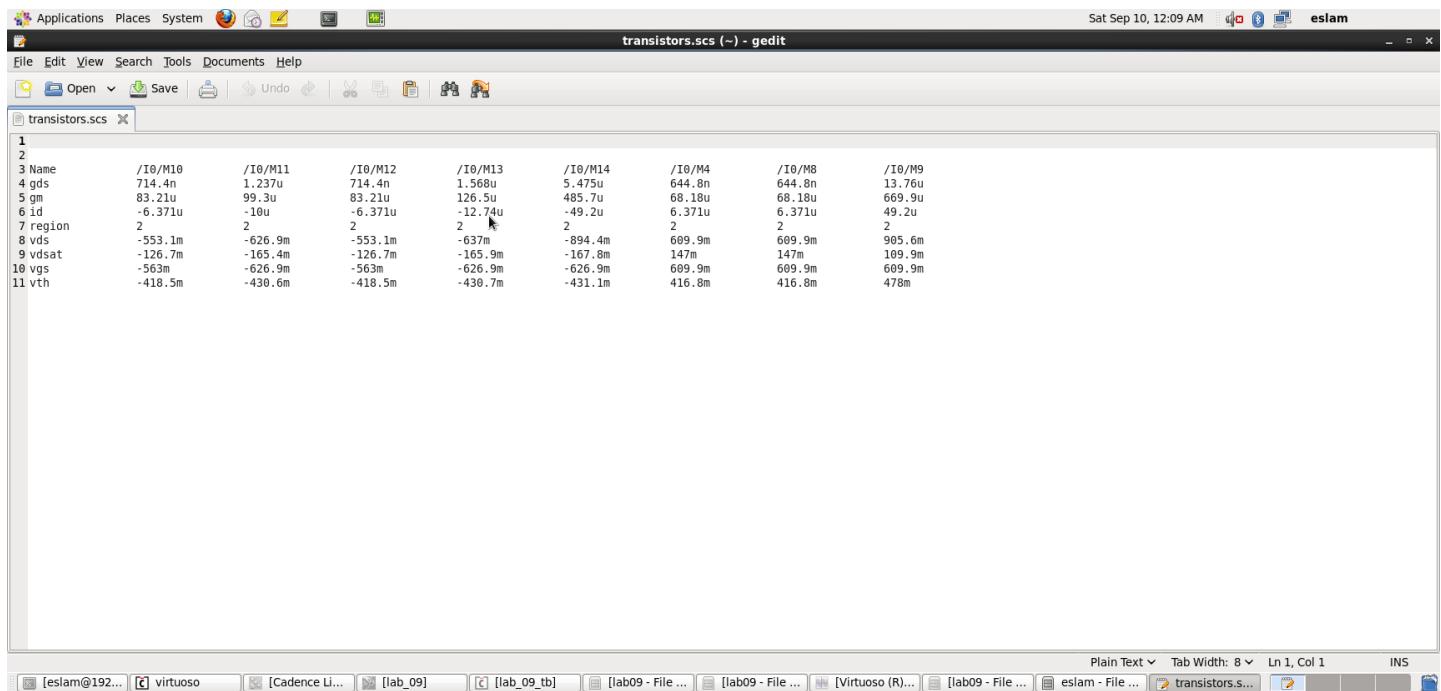


When I run op point I found that M14 is in triode and this is because the DC volt at op node is not defined as it is HIN so I swept W of active load vs vout and taking width at defined volt = VDD/2 :



$$w = 1.2276 \mu\text{m}$$

Op point of all transistors:



```
1
2
3 Name      /I0/M10    /I0/M11    /I0/M12    /I0/M13    /I0/M14    /I0/M4     /I0/M8     /I0/M9
4 gds       714.4n   1.237u   714.4n   1.568u   5.475u   644.8n   644.8n   13.76u
5 gm        83.21u   99.3u    83.21u   126.5u   495.7u   68.18u   68.18u   669.9u
6 id        -6.371u  -10u     -6.371u  -12.74u  -49.2u    6.371u   6.371u   49.2u
7 region    2          2          2          2          2          2          2          2
8 vds      -553.1m  -626.9m  -553.1m  -637m    -894.4m  609.9m   609.9m   985.6m
9 vdsat    -126.7m  -165.4m  -126.7m  -165.9m  -167.8m  147m     147m     109.9m
10 vgs     -563m    -626.9m  -563m    -626.9m  -626.9m  609.9m   609.9m   609.9m
11 vth     -418.5m  -430.6m  -418.5m  -430.7m  -431.1m  416.8m   416.8m   478m
```

→ yes, current and gm is equal in input pair as input is cm input so there is symmetry and half circuit principle is applied.

→ DC volt of first output stage = the volt at mirror node as input is cm so the circuit is symmetry, and half circuit principle is applied and vout follows the mirror node voltage = v_{gs} , 4 = 609.9mV

Check from simulation:



→the op node volt is not defined as it is HIN but for this DC analysis the op voltage = v_{ds} of M9 = 905,6mV

Check from simulation:

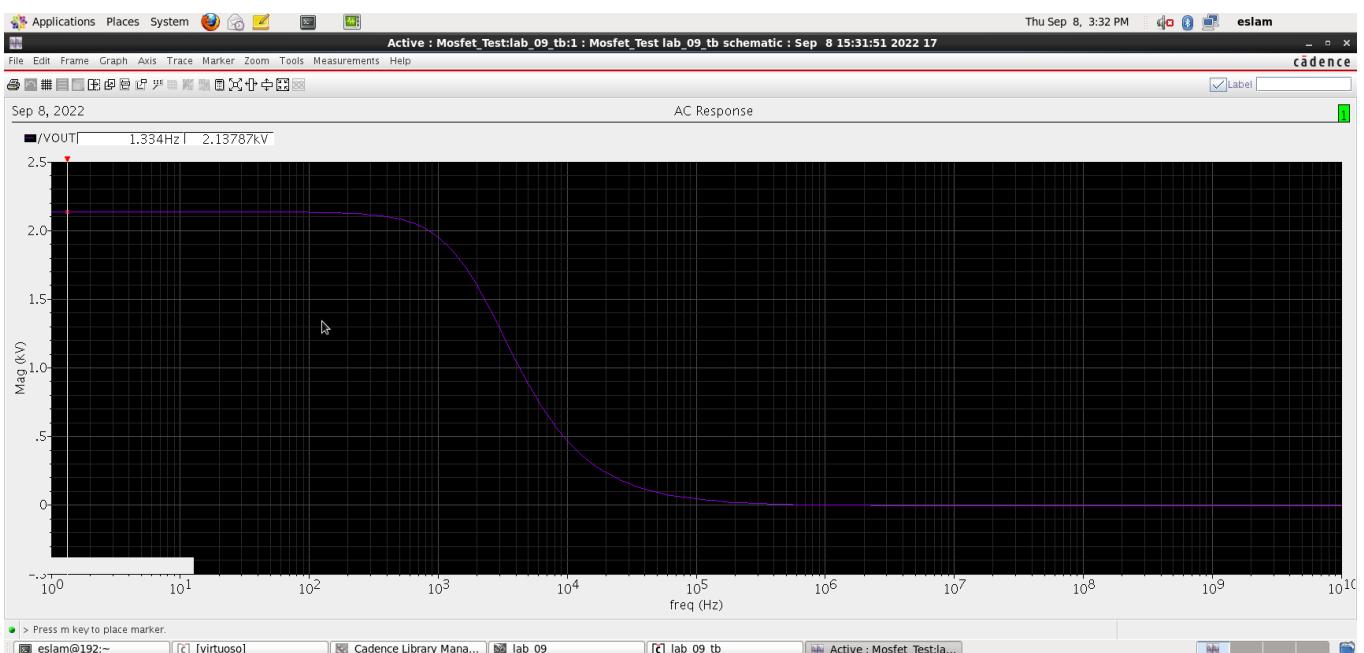
Table Window (XL)	
Line	Value
1.000	905.6E-3
10.00	905.6E-3

Diff small signal ccs:

Parameters:

Test	Output	Nominal	Spec	Weight	Pass/Fail
Mosfet_Test:lab_09_tb:1	unityGainFreq(v("/VOUT" ?r...)	4.949M			
Mosfet_Test:lab_09_tb:1	ymax(mag(v("/VOUT" ?result...)	2.122k			
Mosfet_Test:lab_09_tb:1	dB20(ymax(mag(v("/VOUT" ?...)	66.53			
Mosfet_Test:lab_09_tb:1	bandwidth(v("/VOUT" ?result...)	2.386k			
Mosfet_Test:lab_09_tb:1	gainBwProd(v("/VOUT" ?res...	5.074M			

differential Gain:



Hint: first I used dimensions that I calculated from ADT charts which gave me approximate values for parameters as shown in the following figure and then I plotted graphs and continued part3 but then I tried to improve my values of gain and GBW so I minimized the length of input pair from 900nm to 800nm which gave me more approximate values which I attached before in parameters label.

Test	Output	Nominal	Spec	Weight	Pass/Fail
Mosfet_Test:lab_09_tb:1	$\text{ymax}(\text{mag}(v("/VOUT" ?result...))$	2.138k			
Mosfet_Test:lab_09_tb:1	$\text{dB20}(\text{ymax}(\text{mag}(v("/VOUT" ?result...)))$	66.6			
Mosfet_Test:lab_09_tb:1	$\text{bandwidth}(v("/VOUT" ?result...))$	2.251k			
Mosfet_Test:lab_09_tb:1	$\text{unityGainFreq}(v("/VOUT" ?result...))$	4.743M			
Mosfet_Test:lab_09_tb:1	$\text{gainBwProd}(v("/VOUT" ?result...))$	4.823M			

Differential Gain in db:



Hand analysis:

→ gain =

$$gm10 * (ro12parallelro8) * gm9 \\ * (ro9parallel ro14) = 60.33 * 34.82 = 2.1k$$

→ gain in db = $20 \log 2100 = 66.44$

→ GBW = $\frac{gm of input pair}{2\pi c} = 5.2MHz$

→ UGF =

GBW as it is can be considered as a second order system with

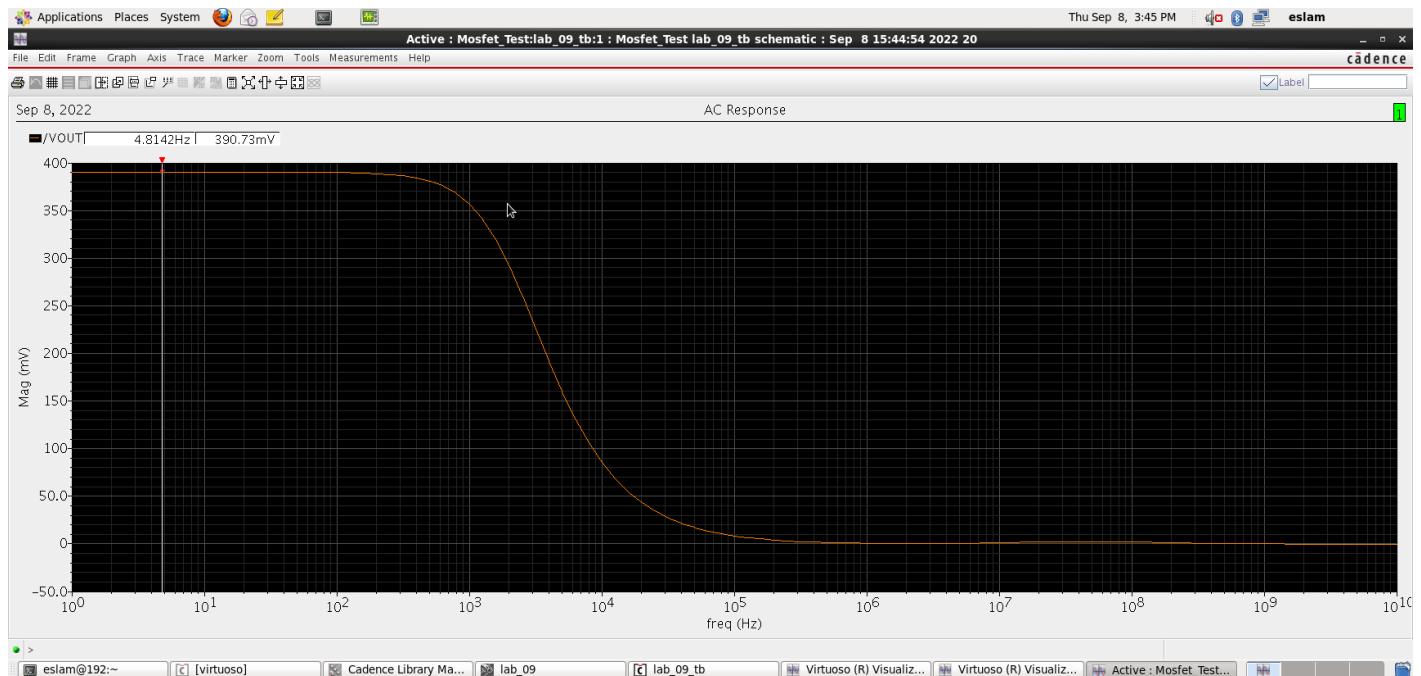
→ BW = $\frac{GBW}{DC gain} = 2.47kHz$

Comparison:

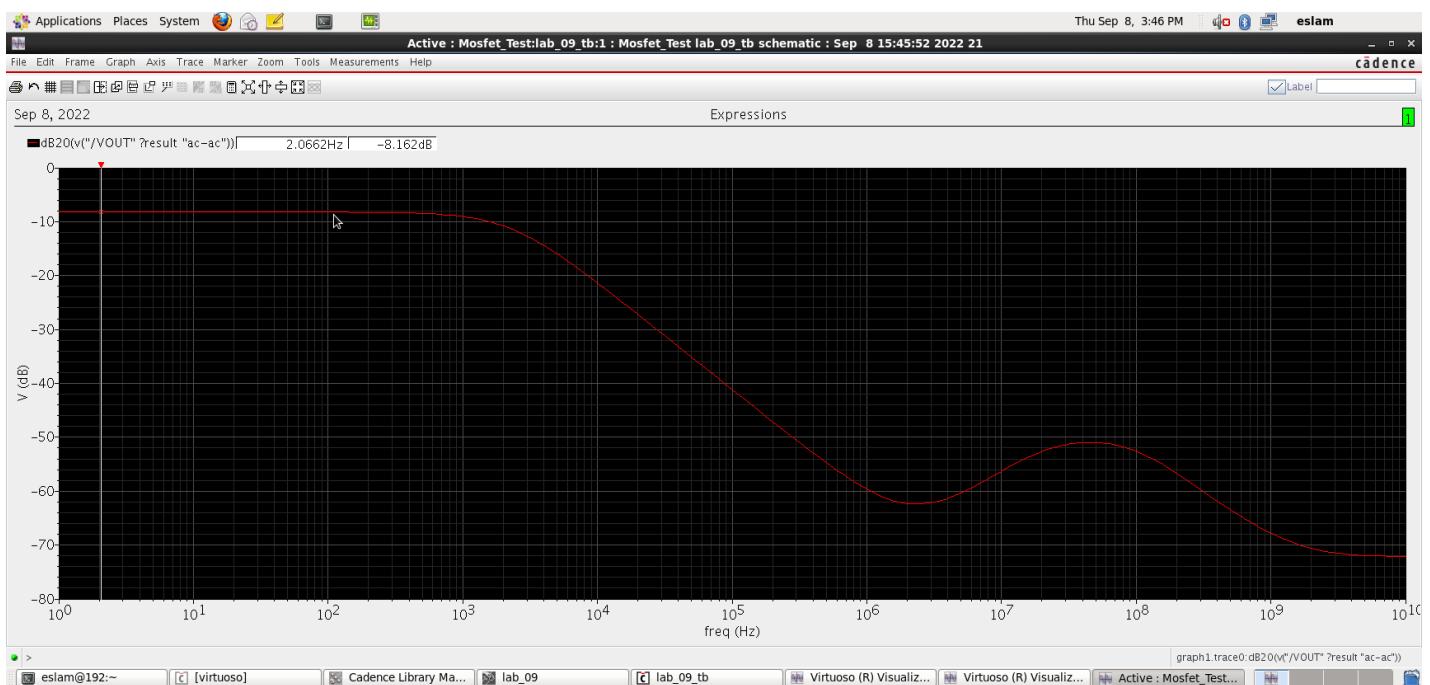
parameter	Hand analysis	simulation
DC gain	2.1k	2.122K
Gain in db	66.44	66.53
BW	2.47k	2.386K
GBW	5.2M	5.07M
UGF	5.2M	4.949M

Cm small signal ccs:

Cm gain:



Cm gain in db:



Hand analysis:

→ cm gain =

$$\frac{gm_{10}}{1 + 2 * gm_{10} * r_{013}} * \frac{1}{gm_4} * gm_9 * (r_{09\parallel} * r_{014}) = 400mV$$

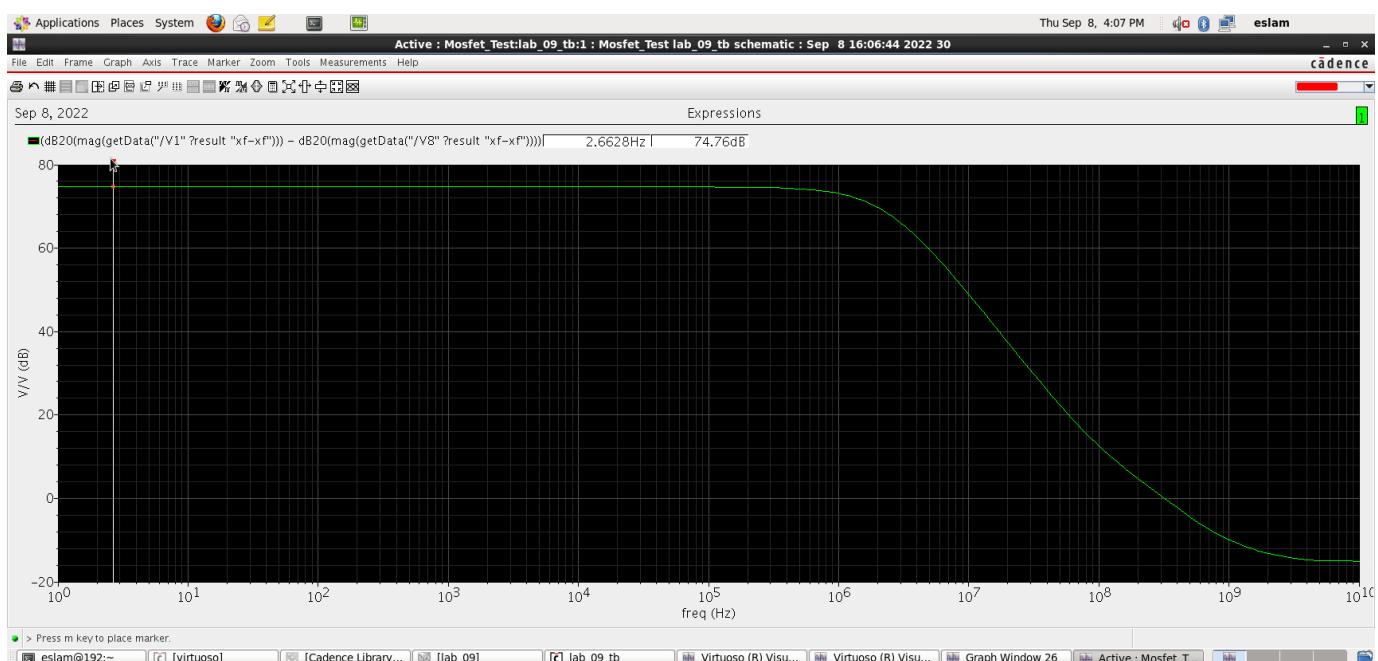
→ cm gain in db = $20 \log 400m = -7.95$

Comparison:

<u>parameter</u>	<u>Hand analysis</u>	<u>simulation</u>
Cm gain	<u>400m</u>	<u>390.7m</u>
Cm in db	<u>-7.95</u>	<u>-8.1</u>

CMRR:

CMRR in db:



Hand analysis:

$$\rightarrow CMRR = \frac{\text{differential gain}}{\text{cm gain}} = \frac{2.1k}{400m} = 5250$$

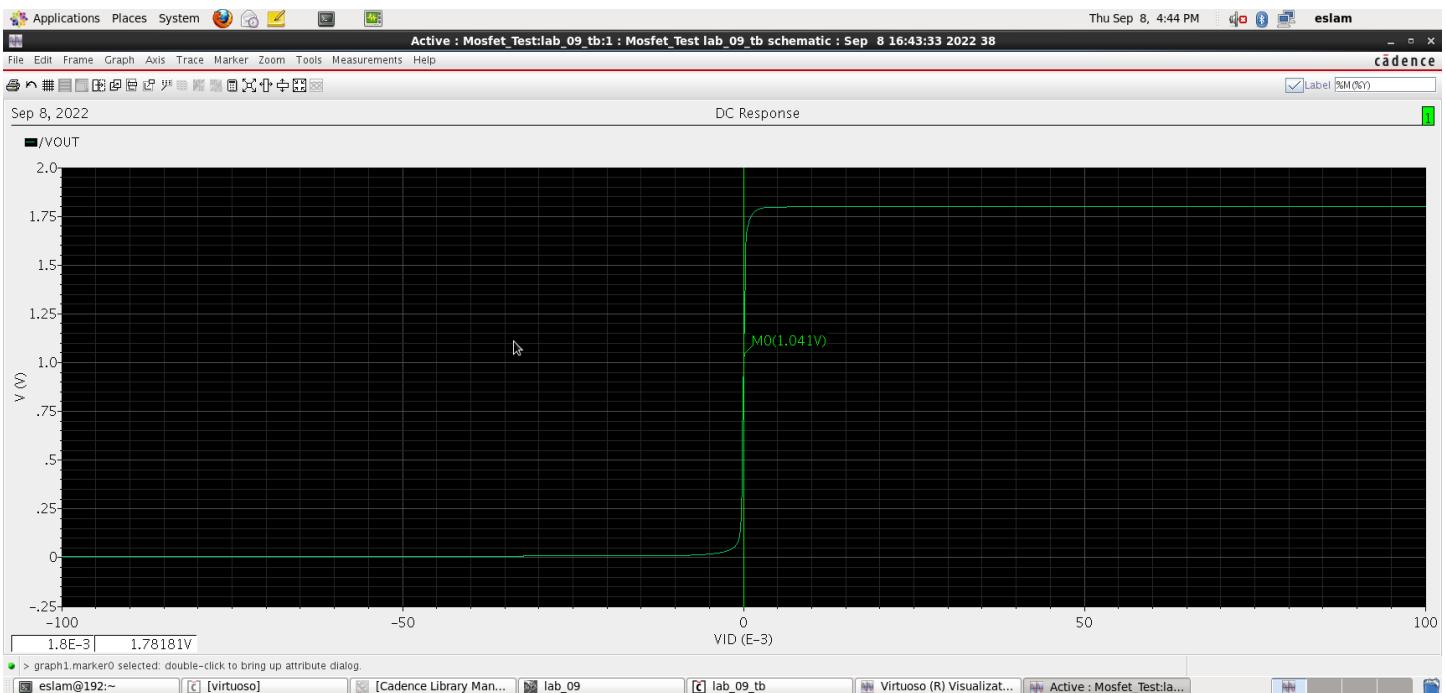
$$\rightarrow CMRR \text{ in db} = 20 \log 5250 = 74.4$$

Comparison:

parameter	Hand analysis	simulation
CMRR	5250	5470
CMRR in db	74.4	74.76

Diff large signal ccs:

Vout vs vid graph:



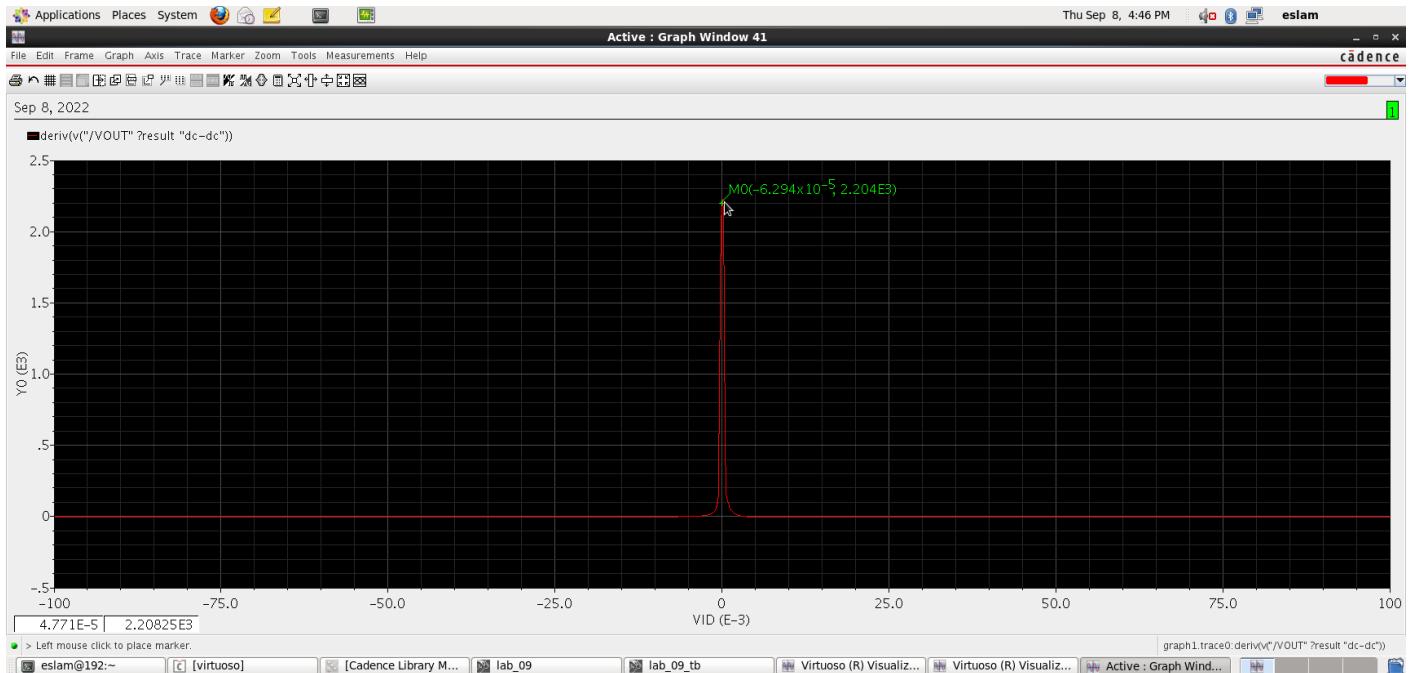
→ vout at vid=0=1.04v

Comparison:

DC OP(at vicm=0.6)	VID graph(at vicm=0.9)
0.9056v	1.041v

This is change with input cm as this node is ill defined node as it is HIN.

Derivative of Vout vs vid:



Comparison:

Avd	peak
2.13k	2.2k

The peak of derivative of vout vs vid approximately represents the differential gain.

Cm large signal ccs:

Region vs vicm graph:



Hand analysis:

$$\rightarrow v_{imax} = VDD - vgsip - v * cm = 1.033v$$

$$\rightarrow v_{inmin} = vgs of active load - vthip = 0.2064v$$

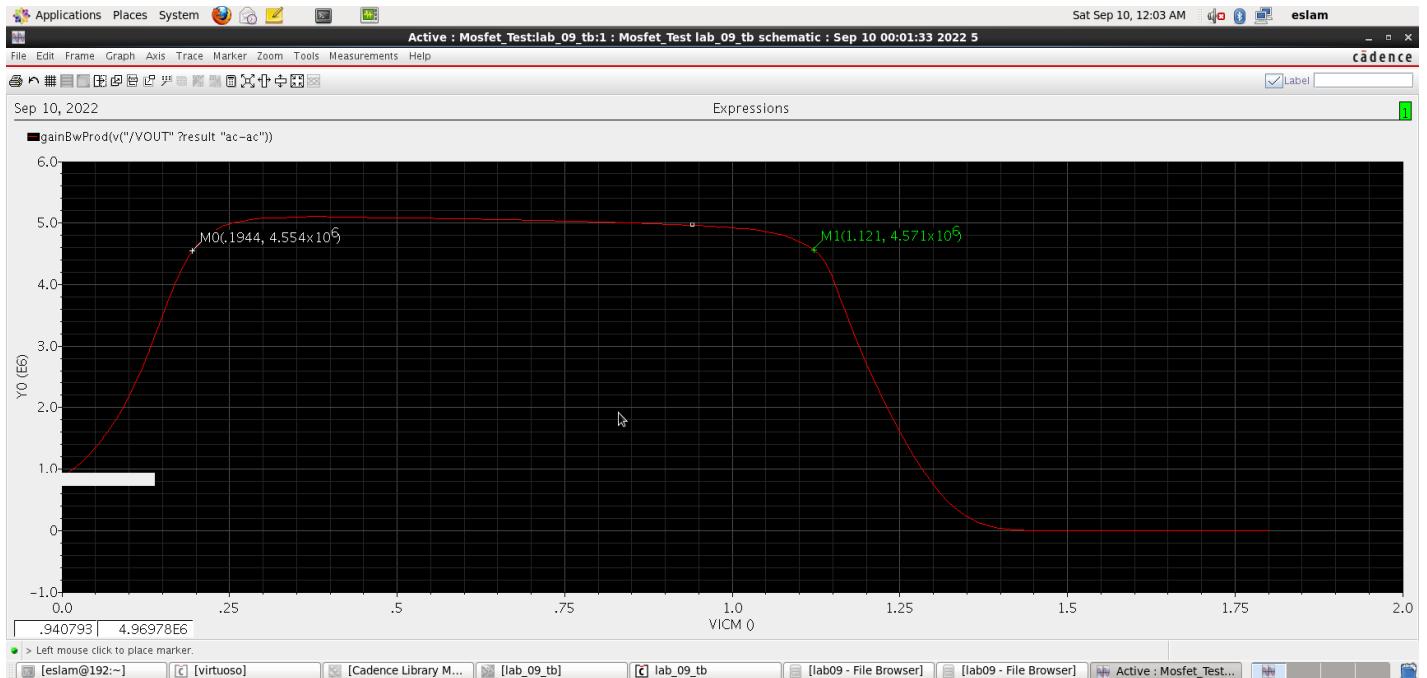
$$\rightarrow CMIR = 1.033 - 0.2064 = 0.8266$$

Comparison:

parameter	Hand analysis	graph
Vin max	1.033	1.068
Vin min	0.2064	0.1836
Range=max-min	0.8266	0.8844

CM large signal ccs(GBW vs VICM):

GBW vs vicm:

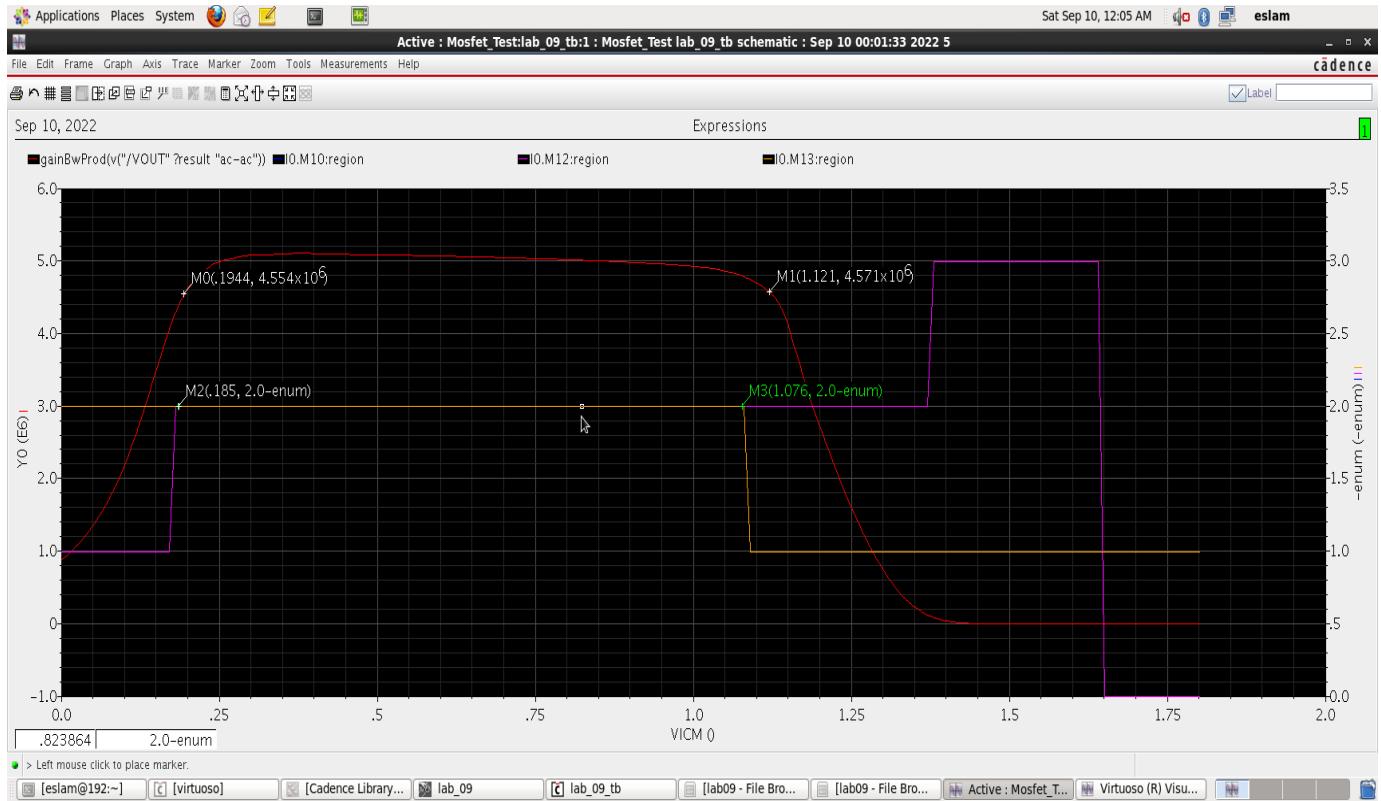


→ $\text{vicm max} = 1.121 \text{V}$

→ $\text{vicm min} = 0.1944 \text{V}$

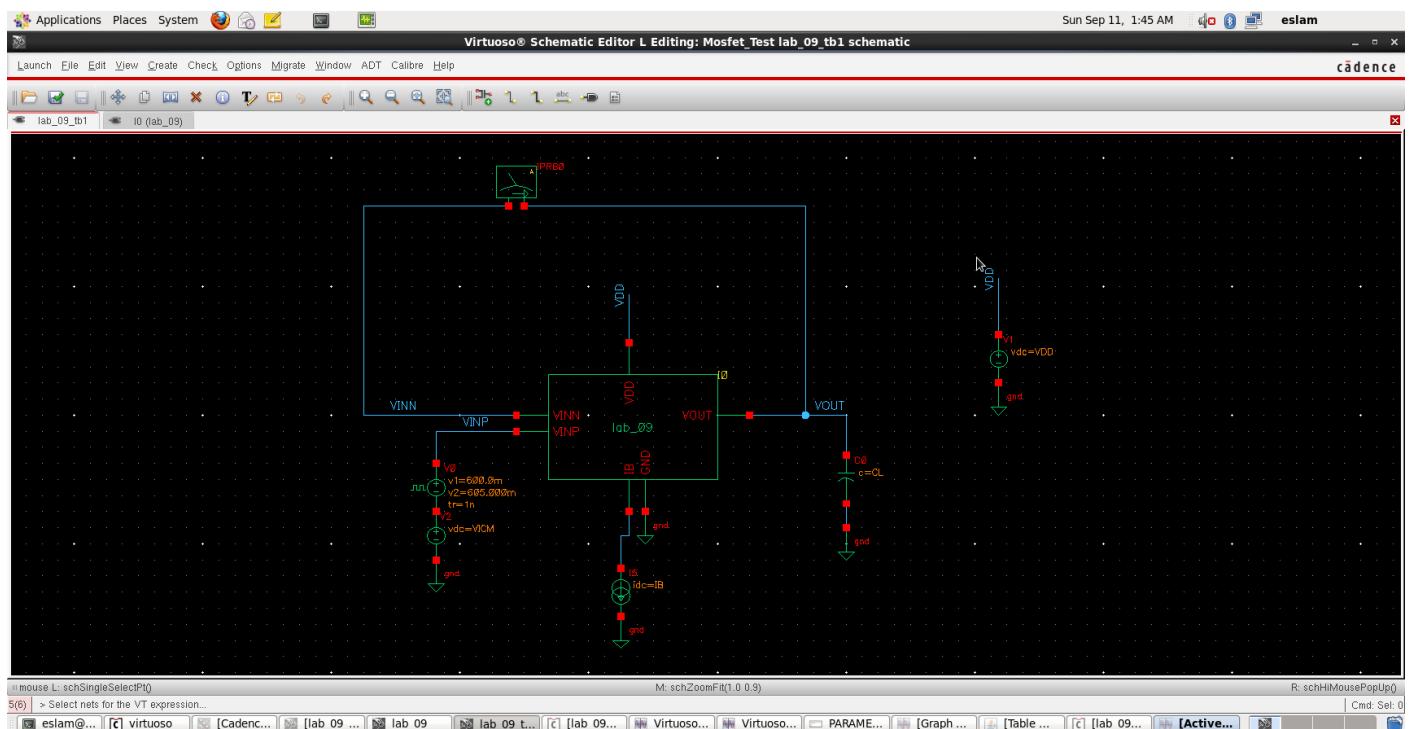
→ $\text{vicm range} = \text{max} - \text{min} = 0.9266$

Overlaid results graph:



Part4

Schematic (test bench):



→dc voltages at input terminals are approximately equal but they are not exactly equal as the open loop gain is finite.

Check from simulation:

Name (unk... ▾)	VDC("'/VINP")
1.000	600.0E-3
10.00	600.0E-3

Table Window (XL)		
File	View	Tools
Name (unk... ▾)	VDC("'/VINN")	
1.000	601.9E-3	

→no, it is not equal its value at open loop case as now it is closed loop with unity gain buffer so the output of the second stage is forced to be approximately equal the input = 600mv so this node became well defined node and there will be no symmetry in the circuit so the op point will change and output of first stage will not equal the mirror node as there is no symmetry as I explained but the output of first stage will only equal v_{gs} of input of second stage =618.8mv with no relation with current mirror node due to asymmetry.

Check from simulation:



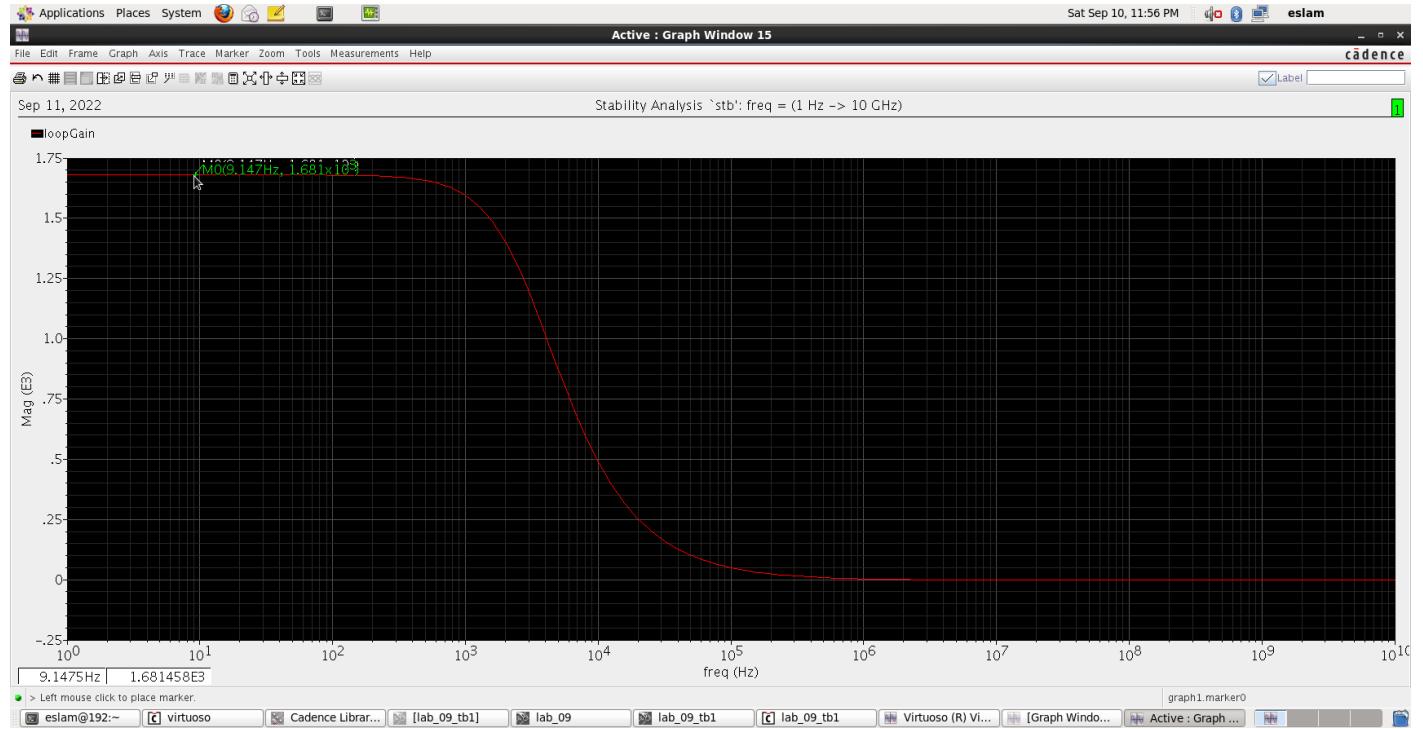
Op point:

	/I0/M10	/I0/M11	/I0/M12	/I0/M13	/I0/M14	/I0/M4	/I0/M8	/I0/M9
3 Name	689.7n	1.237u	720.9n	1.568u	5.27u	944.2n	929n	15.1u
4 gds	83.01u	99.3u	83.54u	126.5u	497.5u	106.4u	107.5u	678.6u
5 gm	-6.326u	-18u	-6.415u	-12.74u	-56.83u	6.326u	6.415u	50.83u
6 id	2	2	2	2	2	2	2	2
7 region	2	2	2	2	2	2	2	2
8 vds	-649.5m	-626.9m	-544.9m	-636.4m	-1.198	523.1m	618.8m	601.9m
9 vdsat	-125.8m	-165.4m	-127.2m	-165.9m	-167.8m	98.64m	91m	113.6m
10 vgs	-561.8m	-626.9m	-563.6m	-626.9m	-626.9m	523.1m	523.1m	618.8m
11 vth	-418.5m	-430.6m	-418.5m	-430.7m	-431.1m	418.1m	417.5m	480.6m

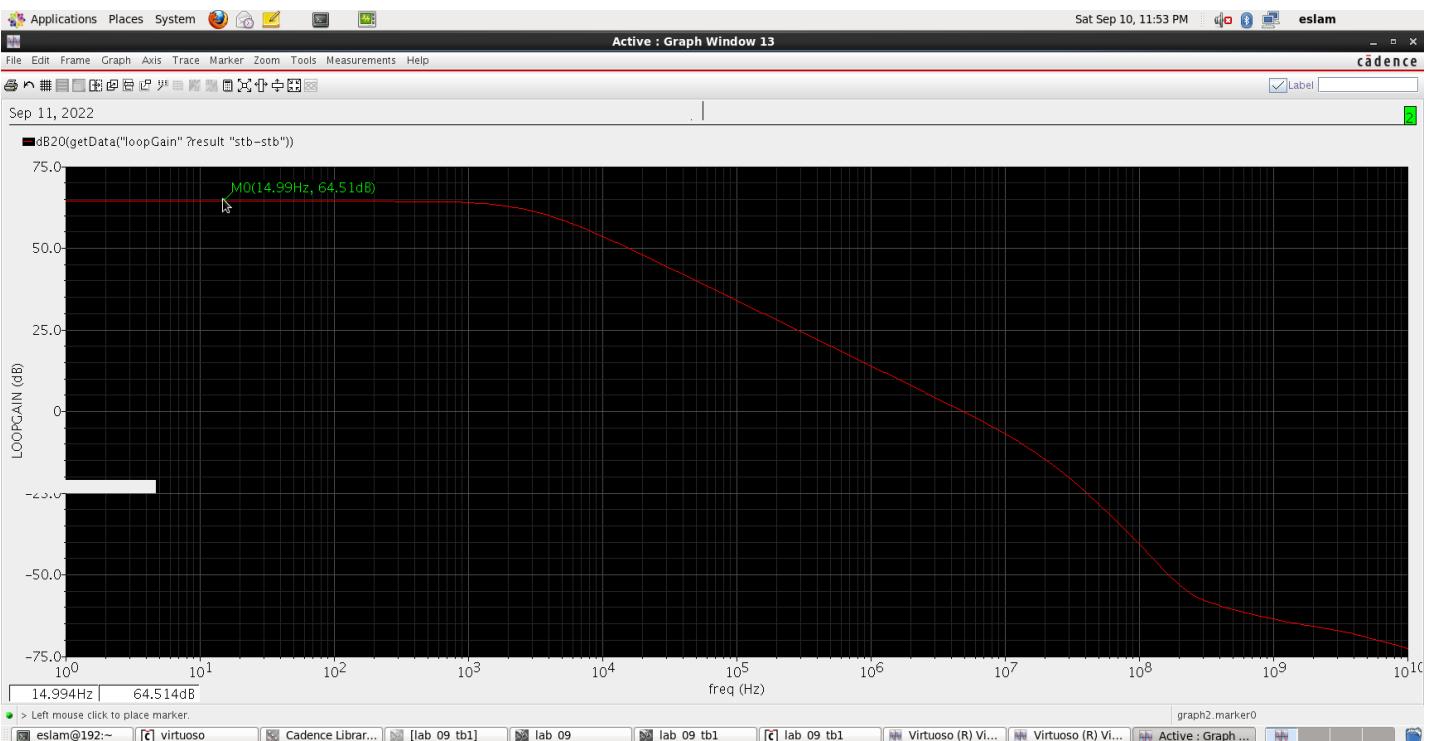
→ no, they are not exactly equal as now it is closed loop with unity gain buffer so the output of the second stage is forced to be approximately equal the input = 600mv so this node became well defined node and there will be no symmetry in the circuit.

Loop gain:

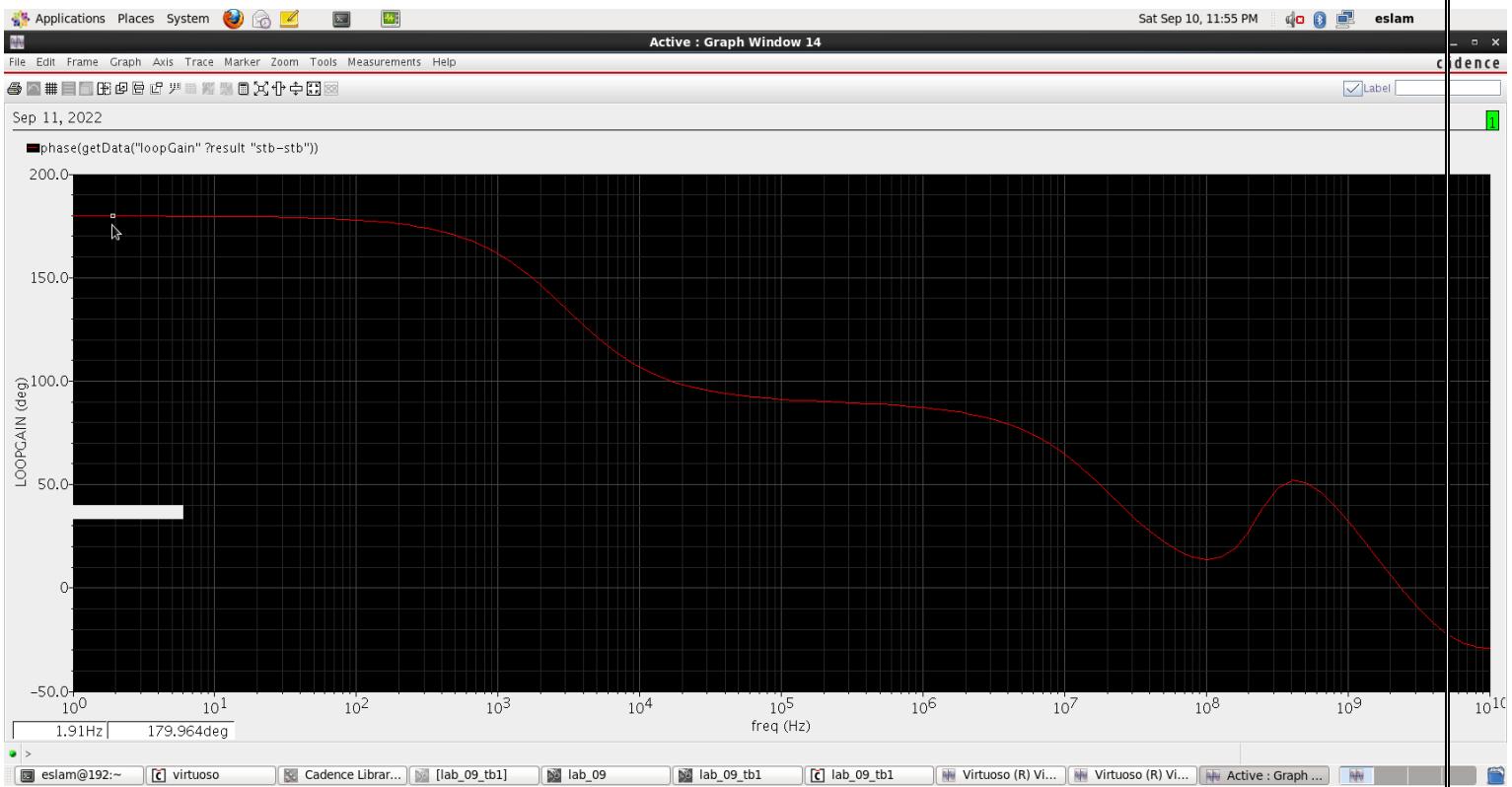
Loop gain graph:



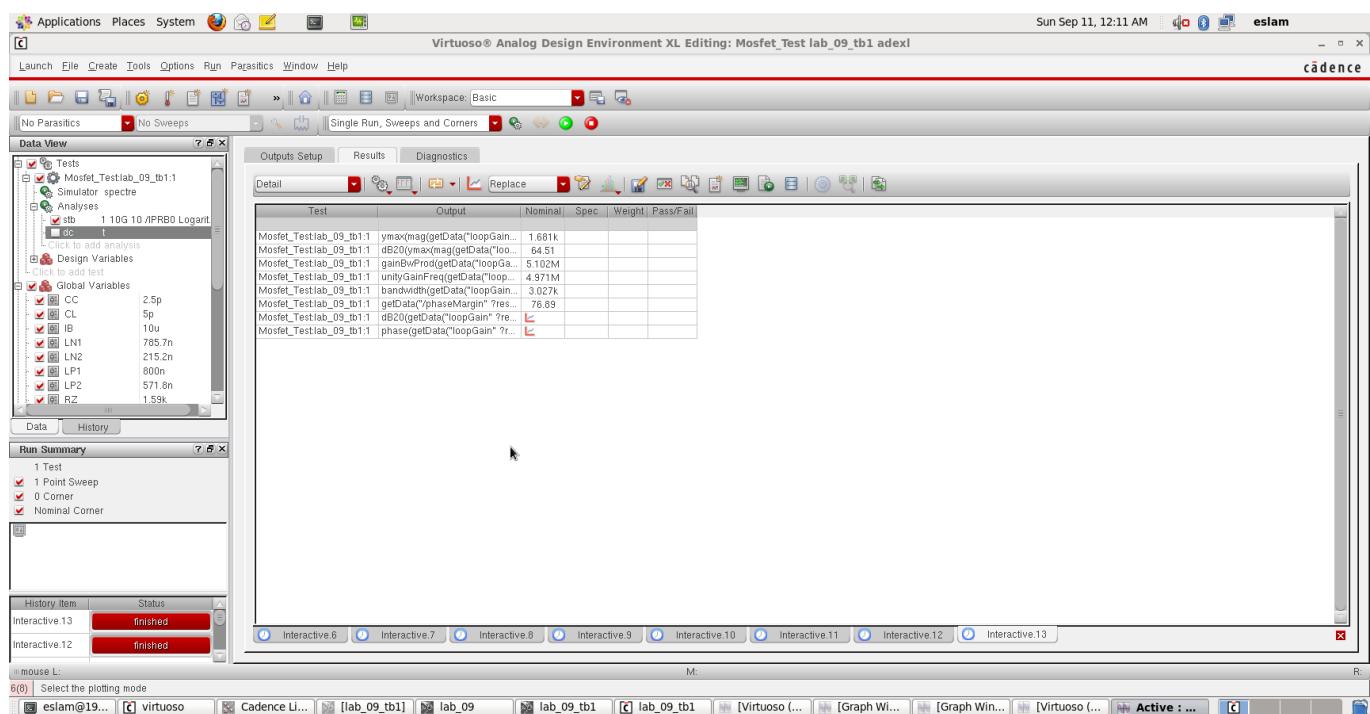
Loop gain in db:



Phase of loop gain:



Parameters of loop gain:



Comparison with open loop:

Test	Output	Nominal	Spec	Weight	Pass/Fail
Mosfet_Testlab_09_tb1:1	unityGainFreq(v("//VOUT" ?res...)	4.949M			
Mosfet_Testlab_09_tb1:1	ymax(max(mag(v("//VOUT" ?result..	2.122k			
Mosfet_Testlab_09_tb1:1	dB20(ymax(max(mag(v("//VOUT" ?...)	66.53			
Mosfet_Testlab_09_tb1:1	bandwidth(v("//VOUT" ?result..)	2.386k			
Mosfet_Testlab_09_tb1:1	gainBwProd(v("//VOUT" ?res...	5.074M			

Test	Output	Nominal	Spec	Weight	Pass/Fail
Mosfet_Testlab_09_tb1:1	yamax(max(getData("loopGain...")))	1.661k			
Mosfet_Testlab_09_tb1:1	dB20(yamax(max(getData("loopGain..."))))	64.51			
Mosfet_Testlab_09_tb1:1	gainBwProd(getData("loopGa..."))	5.102M			
Mosfet_Testlab_09_tb1:1	unityGainFreq(getData("loop..."))	4.371M			
Mosfet_Testlab_09_tb1:1	bandwidth(getData("loopGain..."))	3.027k			
Mosfet_Testlab_09_tb1:1	getData("phaseMargin" ?res...	76.89			
Mosfet_Testlab_09_tb1:1	dB20(getData("loopGain" ?re...	2			
Mosfet_Testlab_09_tb1:1	phase(getData("loopGain" ?re...	2			

Open loop

loop gain

→ They are approximately equal in magnitude as this is unity gain buffer so $\beta = 1$, $loopgain = AOL * \beta = AOL$

And also they have approximately same bandwidth as β

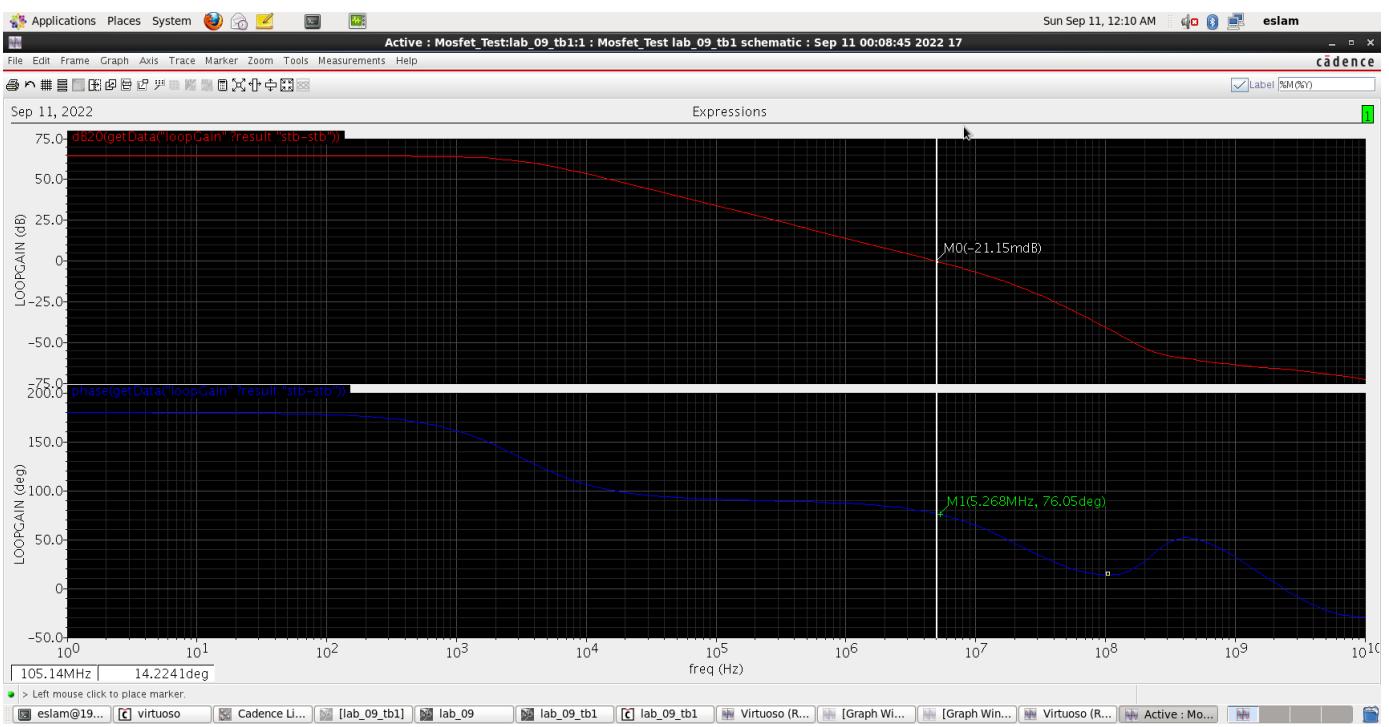
Is independent on frequency so also have approximately same *UGF* and *GBW*.

→ $PM = 76.89^\circ$

→

PM is the difference between phase at which *UGF* is 0db

and 180°



Hand analysis:

$$\rightarrow wp_2 = gmo\text{f} \text{ input of } 2nd \frac{\text{stage}}{2\pi cl} = 21.6 \text{ MHZ}$$

$$\rightarrow \frac{wp_2}{wu} = 4.34$$

$$\rightarrow \frac{wp_2}{wu} \quad PM$$

$$4 \quad 76.3$$

$$4.34$$

$\rightarrow PM \approx 77^\circ$ from table of PM.

Hand analysis	simulation
77	76.89

Hand analysis:

$$\rightarrow LG = AOL * \beta = AOL = 2000$$

$$\rightarrow LG \text{ in db} = 20 \log 2000 = 66$$

$$\rightarrow BW \text{ of } LG =$$

BW of open loop as β independent on f = 2.47kHz as calculated in part3.

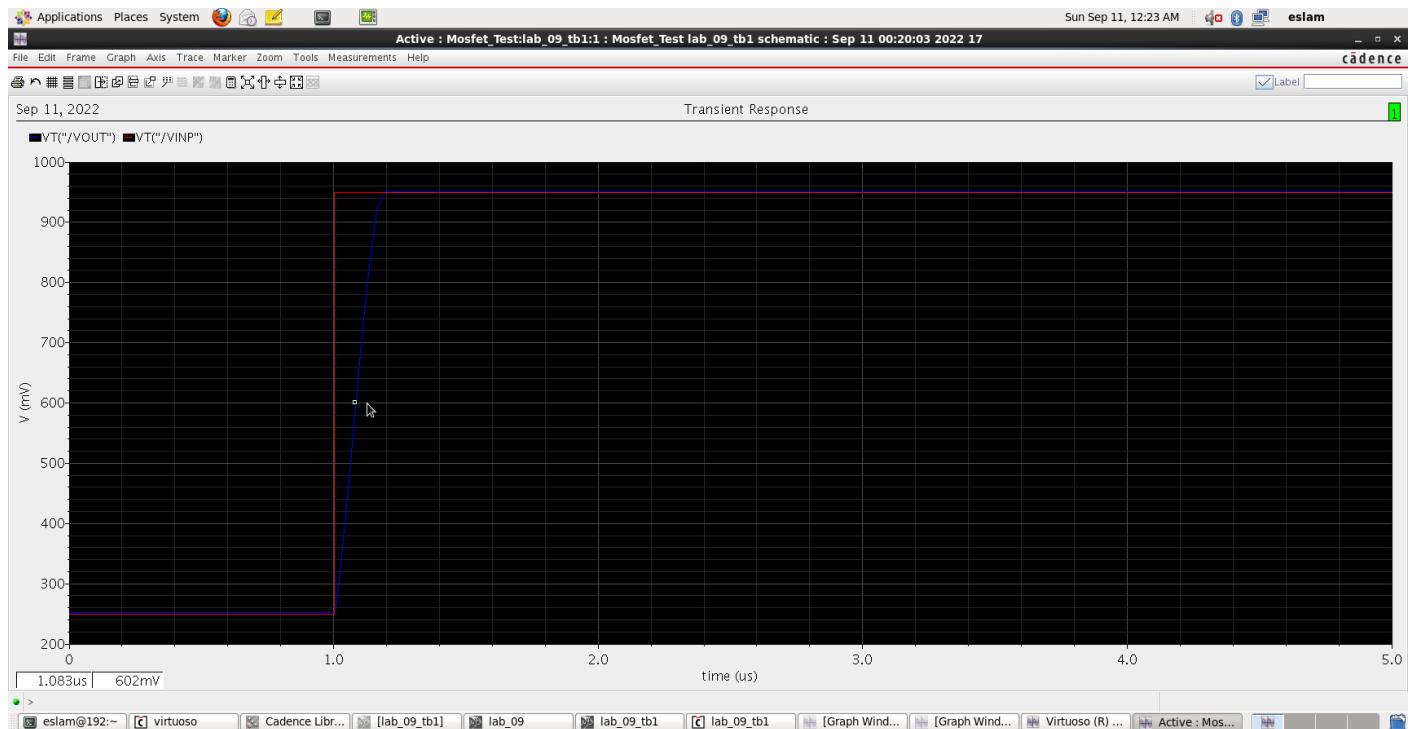
*$\rightarrow GBW = BW * LG \approx GBW \text{ of open loop} = 5.2MHz$ as calculated in part3.*

Comparison:

parameter	Hand analysis	simulation
Dc gain	2k	1.68k
BW	2.47k	3.027k
GBW	5.02M	5.102M
UFG	5.02M	4.97M

Slew rate:

Vin and vout overlaid:



Slew rate:

Table Window (XL)	
Name (unk...	slewRate(VTC"/...
1.000	4.412E6
10.00	4.412E6

To have larger slew rate that satisfies specs I decreased cc to 2.2pf and this does not affect other specs values only increases BW for small value but same gain so this value for cc is acceptable and satisfies the specs.

Modified slew rate:

Test	Output	Nominal	Spec	Weight	Pass/Fail
Mosfet_Test:lab_09_tb1:1	slewRate(VT."/VOUT") 1e-06...	5.032M			

Hand analysis:

$$\rightarrow SR = \frac{IB1}{Cc} = \frac{12.74\mu}{2.2p} = \frac{5.79v}{\mu s}$$

Comparison:

<u>Hand analysis</u>	<u>simulation</u>
<u>5.79</u>	<u>5.032</u>

Settling time:

Rise time at cc=2.5pf

Table Window (XL)		
Name (unk...	riseTime(VC"/VO...	
1,000	56.99E-9	
10.00	56.99E-9	

Rise time at cc=2.2pf

Table Window (XL)		
Name (unk...	riseTime(VC"/VO...	
1,000	49.77E-9	
10.00	49.77E-9	

→ we can see that decreasing cc increases UGF so increases the BW closed loop so decreases time constant and rise time as shown.

Hand analysis:

For cc=2.5pf

$$\rightarrow UGF = \frac{gm of input pair}{2\pi cc} = \frac{1}{\tau} = \frac{83.01\mu}{5\pi p} = 5.28MHz, \tau = 30ns, rise time = 66.3ns$$

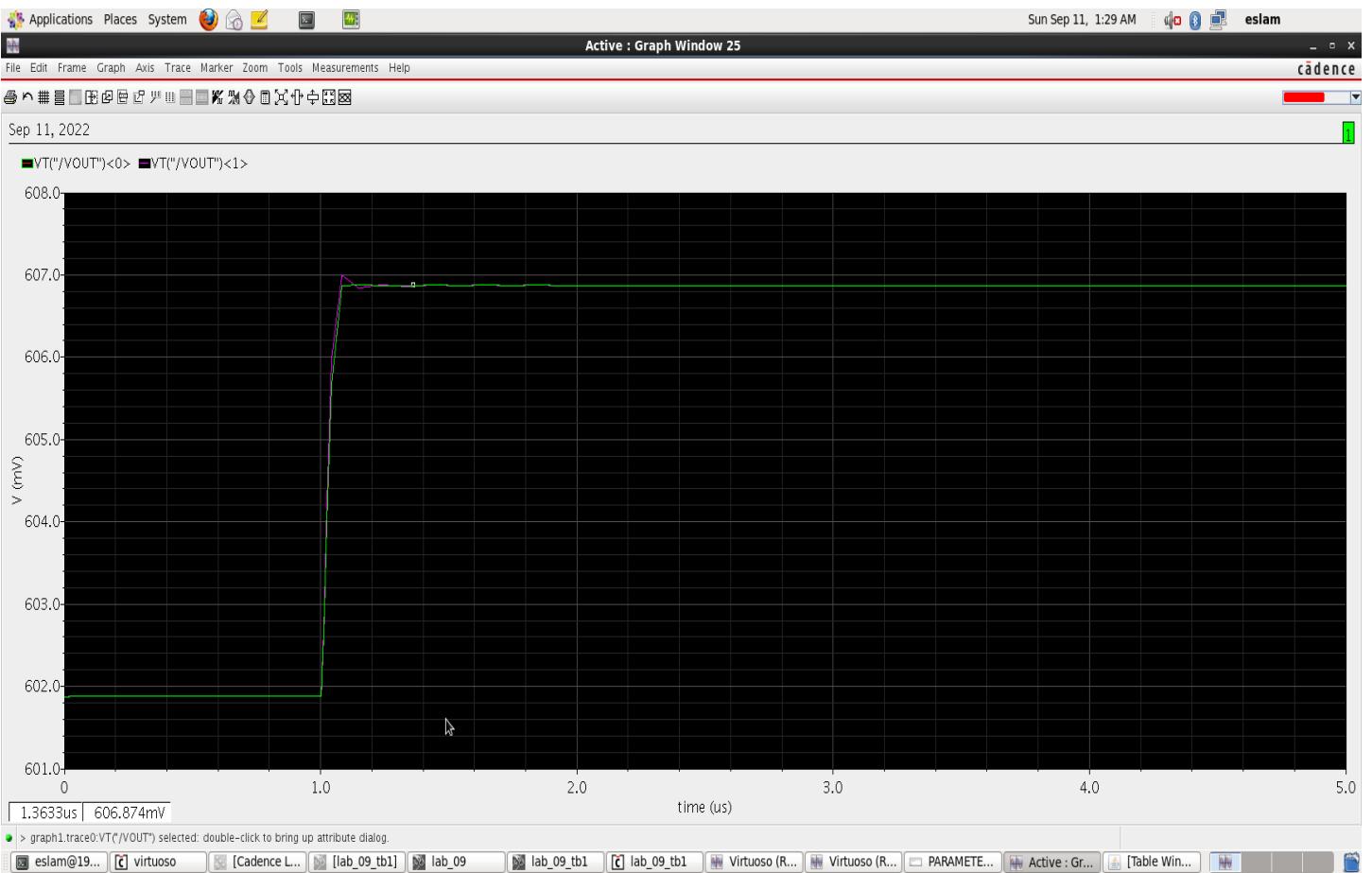
For cc=2.2pf

$$\rightarrow UGF = \frac{gm of input pair}{2\pi cc} = \frac{1}{\tau} = \frac{83.01\mu}{4.4\pi p} = 6MHz, \tau = 26.5ns, rise time = 58.3ns$$

Comparison:

Cc	Hand analysis	simulation
2.2p	58.3n	49.7n
2.5p	66.3n	56.9n

2Vout graph at the 2 values of Cc:



→the graph which has very small ringing in time domain is at $C_c=2.2\text{pf}$ as decreasing C_c increases UGF which decreases settling time and also decreases phase margin which cause much ringing in time domain as shown.

And as phase margin is large in 2 cases then ringing is very small that can be considered only overshoot not ringing as $\text{PM}>45$ degrees.