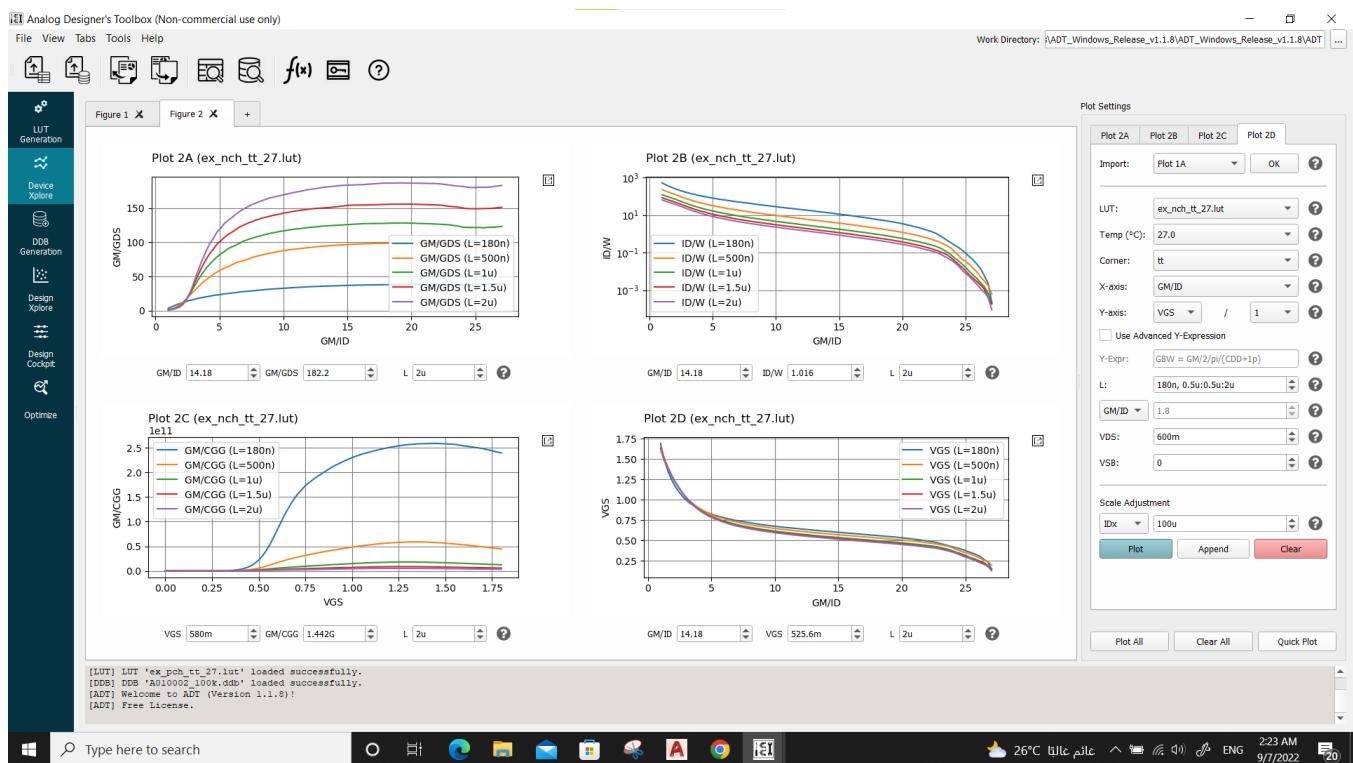


# Lab 11

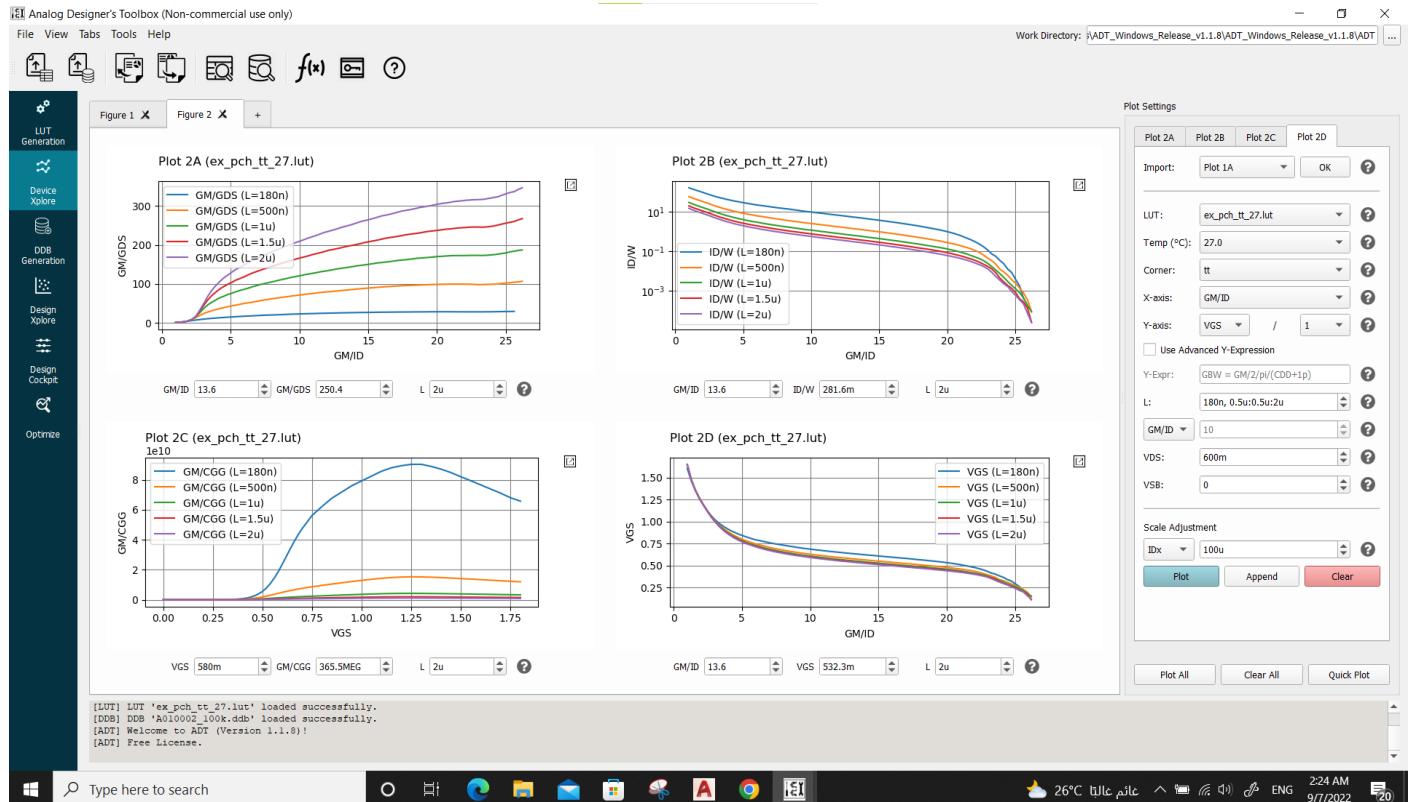
## Part 1

### Graphs from adt:

#### Nmos:

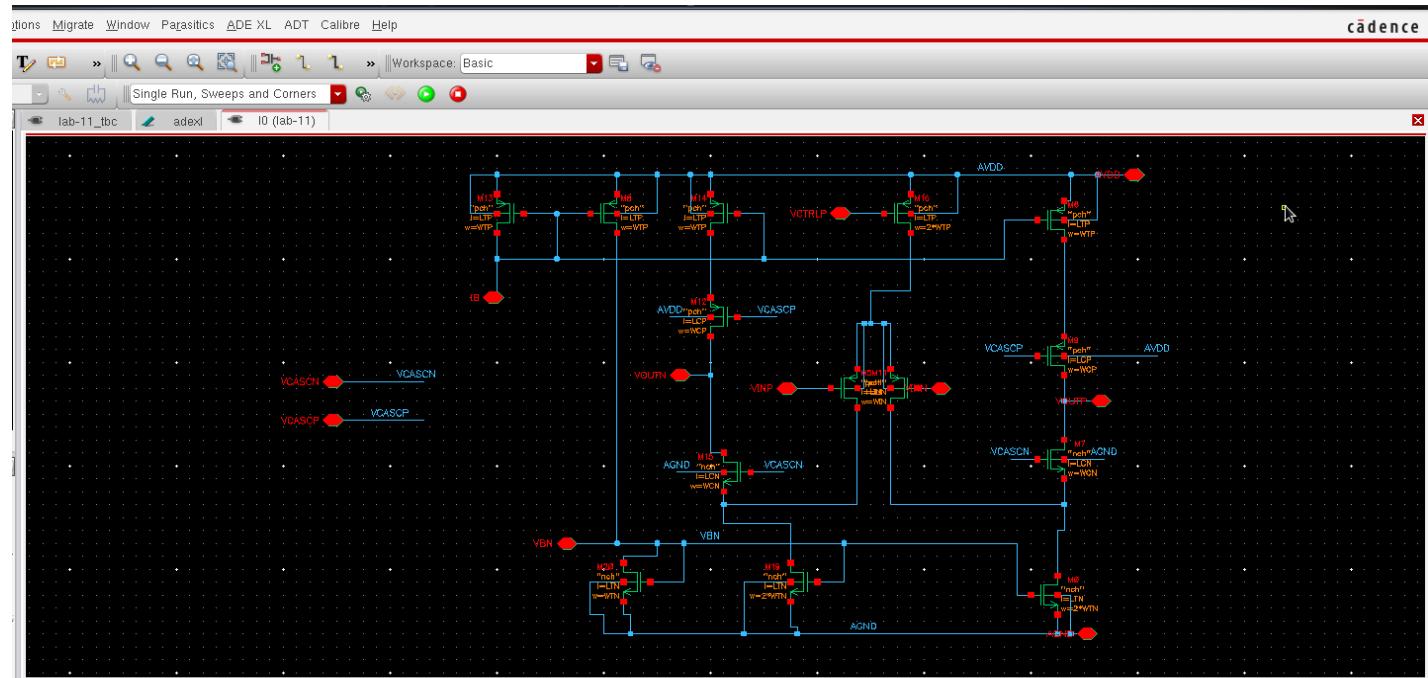


## Pmos:



## Part2

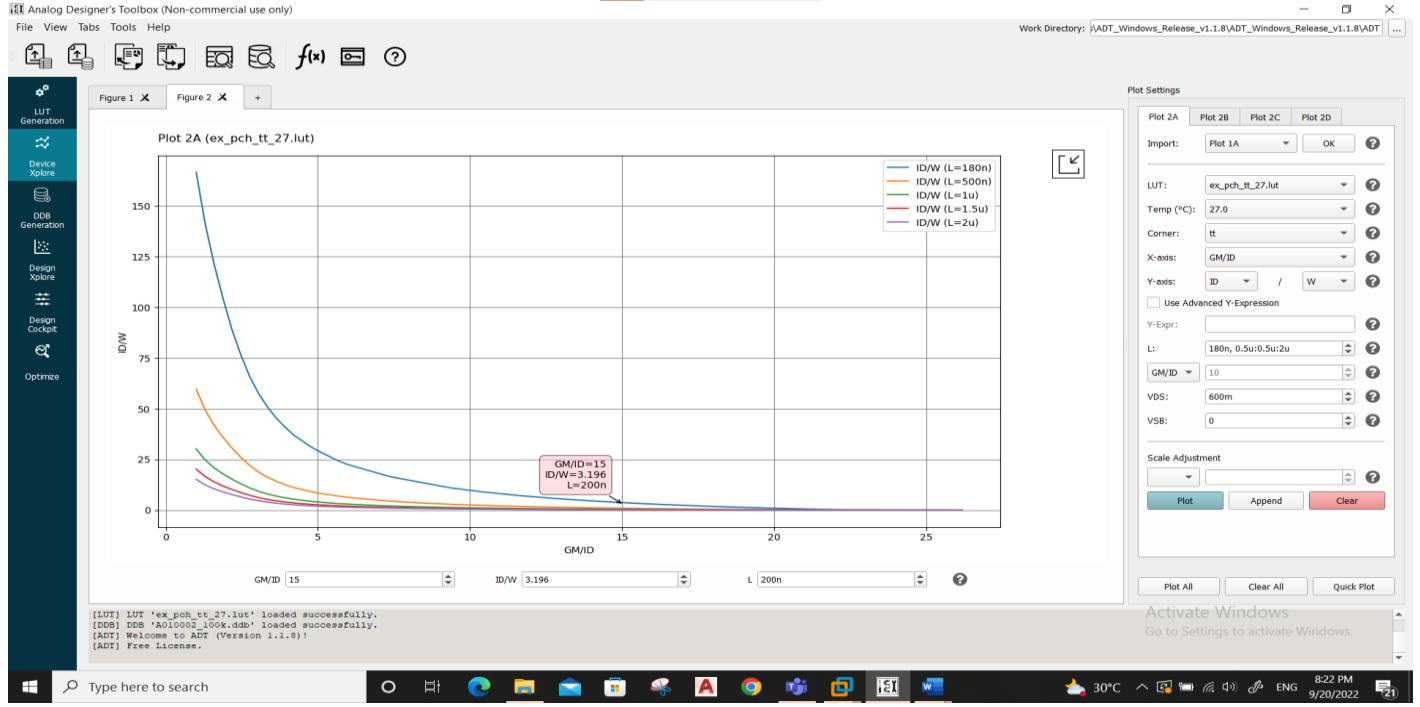
### Folded cascode schematic:



## Design procedure:

→ I devided the  $80\mu A$  as explained.  
→ from CMIR spec we found that low is <0 and high is faraway VDD so we chose PMOS as input pair.  
→ for input pair we chose min length as this will minimize input capacitance which represent loading effect affects on  $\beta$  in capacitive inverting feedback in part 5, also we chose large  $\frac{gm}{id}$  so in MI or also WI in tuning to achieve the reacquired specs in gain and BW to maximize the openloop gain and also maximize GBW which will be affected very large in capacitive inverting feedback.  
→ I used  $\frac{gm}{id} = 15$  and  $l = 0.2\mu m$  at first and get  $W$  for  $i = 20\mu A$ .

## id/w chart:



$$\rightarrow w = 6.25\mu m$$

$\rightarrow$  for current source transistors we chose large length to maximize output resistance and maximize the gain as result, but we chose small  $\frac{gm}{id}$  as  $gm$  will not contribute to gain or BW but only increase noise.

$\rightarrow$  I chose  $l = 1\mu m$  and  $\frac{gm}{id} = 10$  at first and then got  $w$  at  $id = 20\mu A$  and from sizing we mirror different values of current.

### Id/w chart (nmos):



$$\rightarrow w = \frac{20}{4.66} = 4.29\mu m$$

## Id/w chart(pmos):



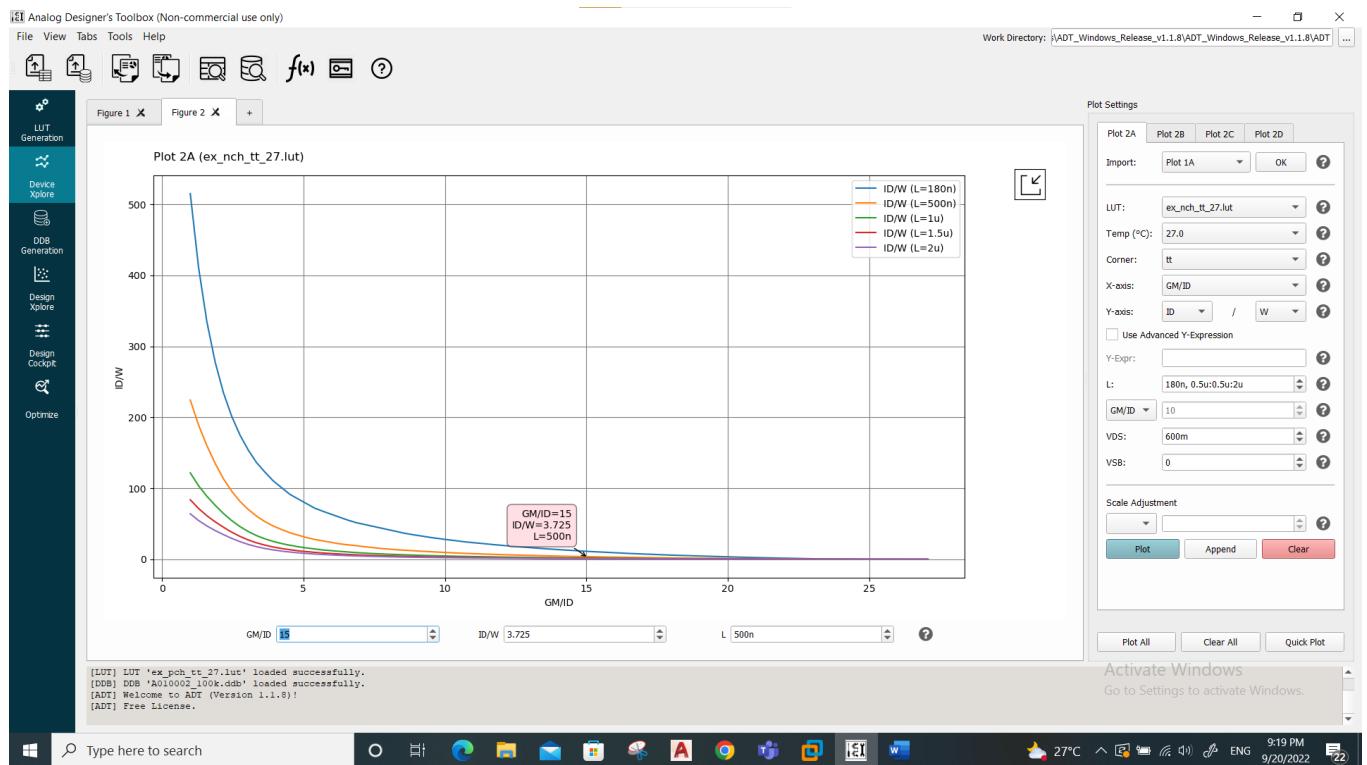
$$\rightarrow w = \frac{20}{1.184} = 16.89\mu m$$

→ for cascode we need large length and also, we need large  $\frac{gm}{id}$  as we need large gm as they will boast rout

And as result boast the gain.

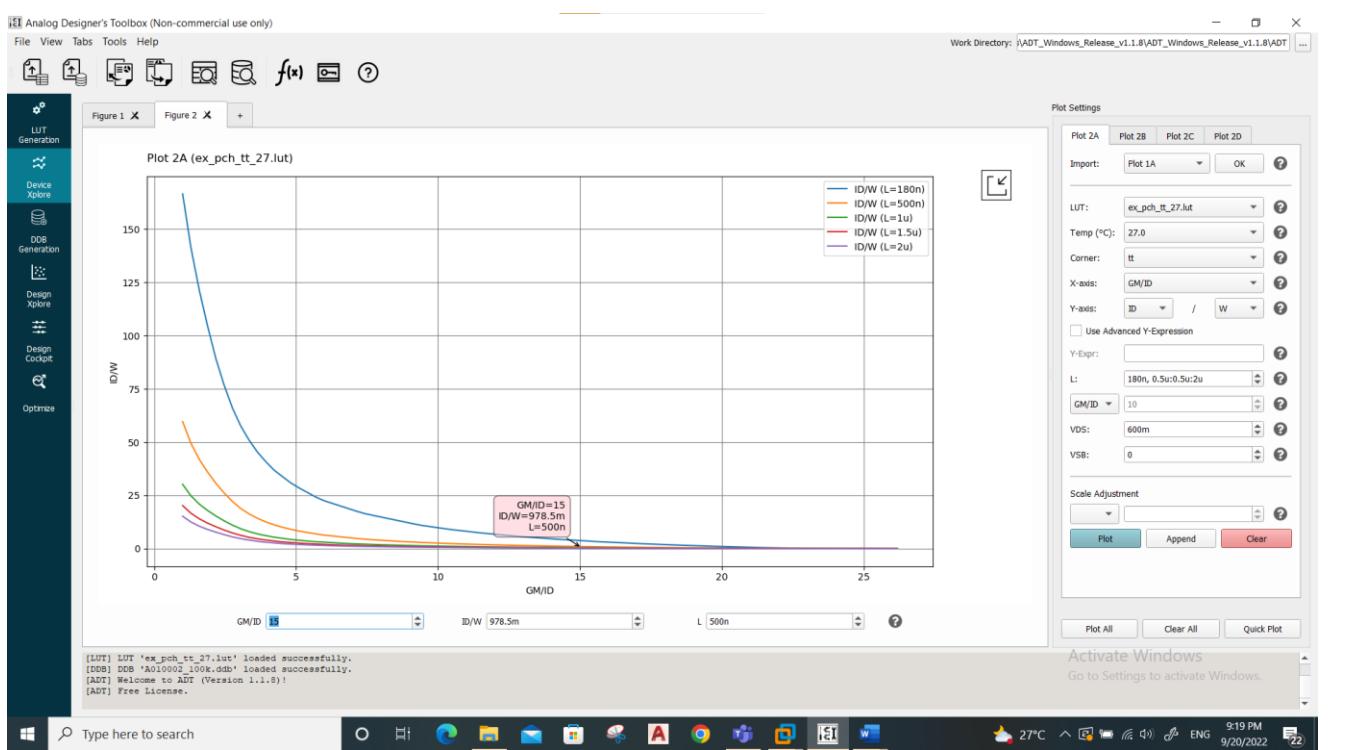
→ I chose  $l = 0.5\mu m$  and  $\frac{gm}{id} = 15$  and get w from charts.

## Id/w chart(nmos):



$$\rightarrow w = \frac{20}{3.725} = 5.369\mu m$$

## d/w chart(pmos):



$$\rightarrow w = \frac{20}{978.5m} = 20.439\mu m$$

$\rightarrow$  from these sizing values we can get values of VCASCN and VCASCP (bias voltage for cascode transistors).

$$\begin{aligned}\rightarrow VCASCN &= vgscascn + v * tailcsnmos \\ &= 0.5695 + 0.2 = 0.7695v\end{aligned}$$

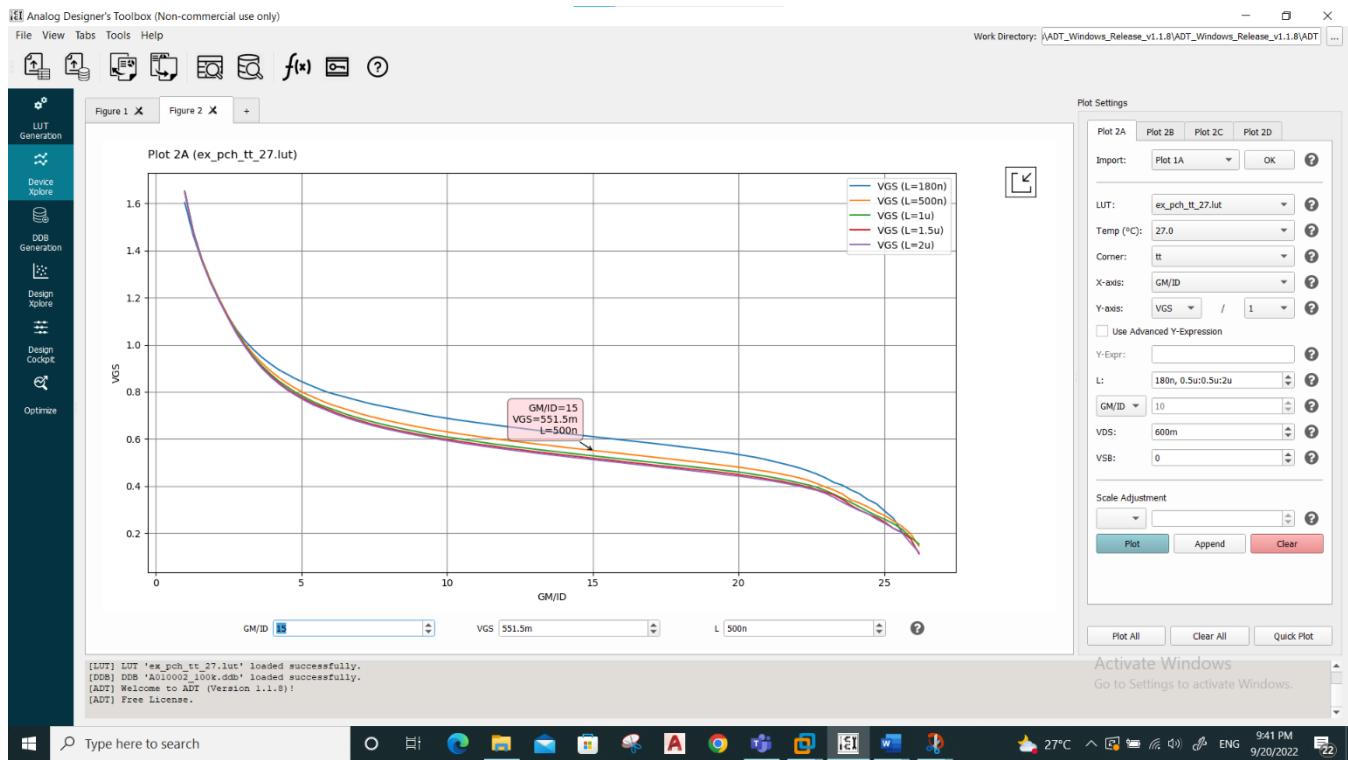
$$\begin{aligned}\rightarrow VCASCP &= VDD - v * tailcspmos - vgscascp \\ &= 1.8 - 0.2 - 0.5515 = 1.0485v\end{aligned}$$

$\rightarrow$  vgs charts for cascode:

$\rightarrow$  nmos:



→pmos:

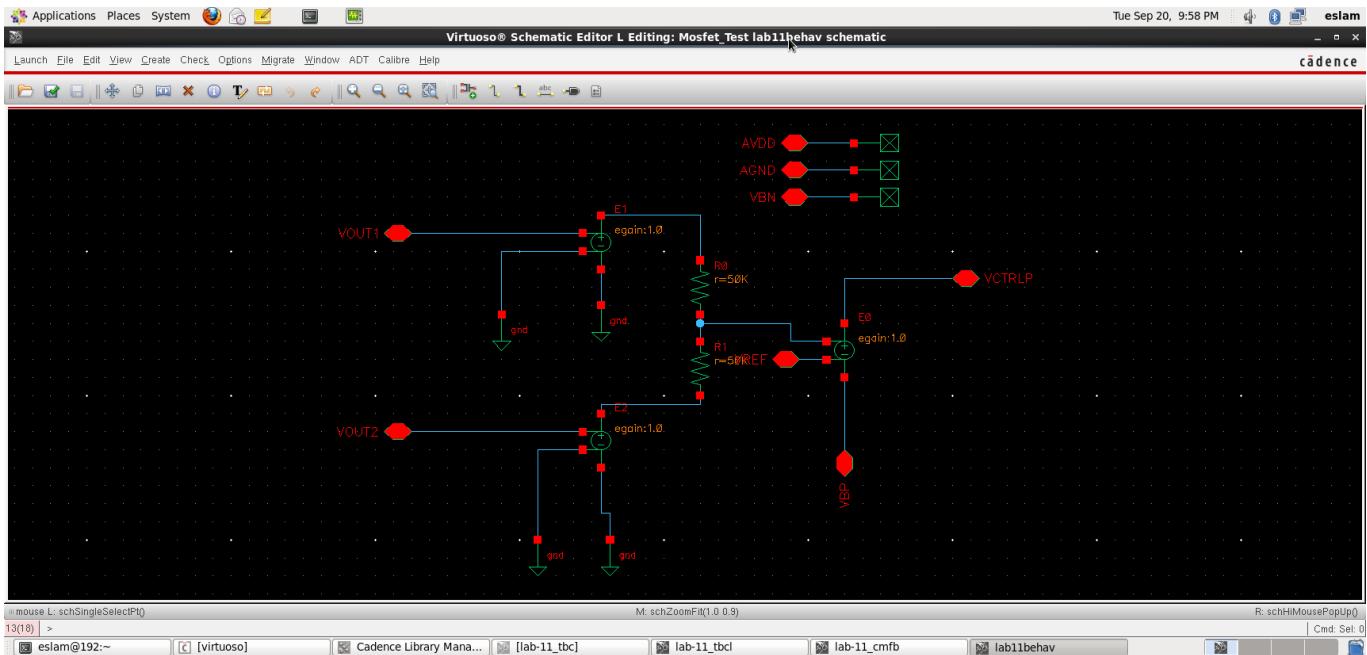


→dimensions from charts:

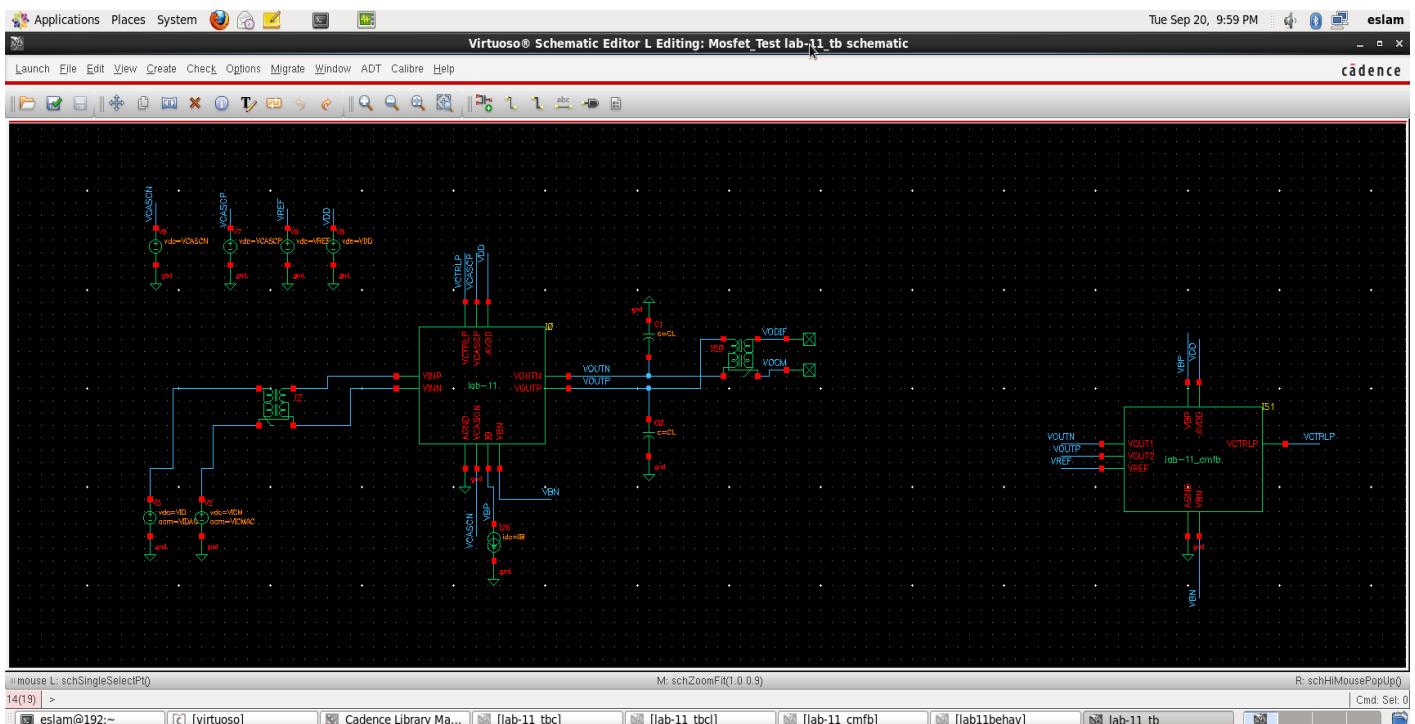
parameter	I	w
Input pair	0.2u	6.25u
Current source nmos	1u	4.29u
Current source pmos	1u	16.89u
Cascode nmos	0.5u	5.369u
Cascode pmos	0.5u	20.439u

# Part3

## Cmfb behavioral schematic:



# Test bench schematic:



→ I used the dimensions I got from charts from part2 but to achieve the required specs I want open loop gain to be more than 3k and also GBW open loop to be about 60M

As  $\beta v \approx \frac{cf}{cf+cin} \approx \frac{1}{3}$  so to achieve this specs in open loop as it was expected to achieve the required closed loop specs, I tuned in these dimensions using ADT charts and also tuned VCASCN and VCASCP to make fine VDS margin to make all transistors in saturation so,

→ I used large  $\frac{gm}{id} = 20$  for input pair to achieve high GBW in open loop which will be more affected due to capacitances in this inverting feedback and also this large value helped me get large open loop gain, but also used same small length as these increases parasitic cap.

→ I used large  $\frac{gm}{id} = 17$  for cascode to have higher ROUT then higher open loop gain to achieve the required spec in closed loop gain and also used higher length to achieve the required loop gain in part5 .

→ I used  $\frac{gm}{id} = 11$  to achieve the required swing and also not very large value as it will increase noise and also I used same length in order not increasing parasitic.

→ I tuned VCASCN and VCASCP to achieve fine margin for VDS and all transistors be in sat and also tuning these values tunes VDS so tuning ro of tail cs transistors which affects the gain.

So, I tuned these parameters more times until I achieved the required specs in closed loop part as closed loop gain and BW and loop gain and phase margin and these final values that achieved these specs in closed loop will be attached in table.

parameter	I	w
Input pair	0.2u	23.8u
Current source nmos	1u	5.231u
Current source pmos	1u	20.56u
Cascode nmos	1.4u	24.22u
Cascode pmos	1u	69.73u

→  $i$  tuned VCASCN to be =  $0.8v$

and VCASCP to be =  $0.75v$

### Op point:

Applications Places System eslam

File Edit View Search Tools Documents Help

Open Save Undo

transistors.scs

```
1
2
3 Name      /I0/M0      /I0/M11     /I0/M12      /I0/M13      /I0/M14      /I0/M15      /I0/M16      /I0/M19      /I0/M20      /I0/M5       /I0/M6      /I0/M7      /
4 gds      7.214u    10.95u     2.086u     1.723u     1.908u     2.31u      3.431u     7.214u     1.898u     10.95u     1.908u     2.31u
5 gm       1.622u    2.086u
6 id       228.1u    336.8u     416.3u     336.8u     219.6u     216.8u     342.6u     451.4u     437.2u     224.9u     416.3u     216.8u     342.6u
7 region   -21.0lu   -19.7u     -20.89u    -19.7u     -20u        -19.7u     19.7u      -41.79u    40.59u     21.01u     -20.89u    -19.7u     19.7u
8 vds      278m      -791.1m    -480m      -589.9m    -422.7m    619.4m     -731m      278m      600.1m     -791.1m    -422.7m    619.4m
9 vdsat    -1.2      -480m
10 vgs     147.3m    -67.32m    -96.09m    -152.1m    -152.1m    90.85m     -154.6m    147.3m     148.1m     -67.32m    -152.1m    90.85m
11 vth     -152.1m   -96.09m    -627.3m    -589.9m    -589.9m    572m       -592.6m    600.1m     600.1m     -519m      -589.9m    572m
-589.9m
-627.3m
-408m     -488.8m    -540.4m    -411.1m    -411.1m    476.6m     -411.2m    408m      406.1m     -488.8m    -411.1m    476.6m
-411.1m
-540.4m
```

$$\rightarrow v_{inlow} = v * -v_{thininput} = \frac{2}{11} - 488.8m = -0.31v$$

$\rightarrow v_{inhigh} = VDD - v_{sginput} - v *= 1.1v$

→ *cmir* is satisfied.

$$\rightarrow output\ swing = VDD - 2v * casc - 2v * tail = 1.2v$$

→ output swing is satisfied.

## What is cm level at OTA output:

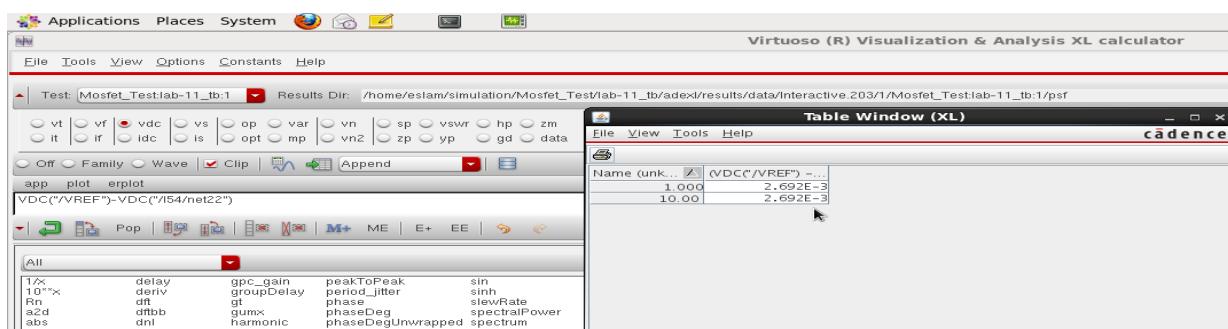


→this value is approximate to 0.9 which is vref as  
cmfb circuit is to set the common mode output of  
OTA to specific value vref which is equal 0.9v

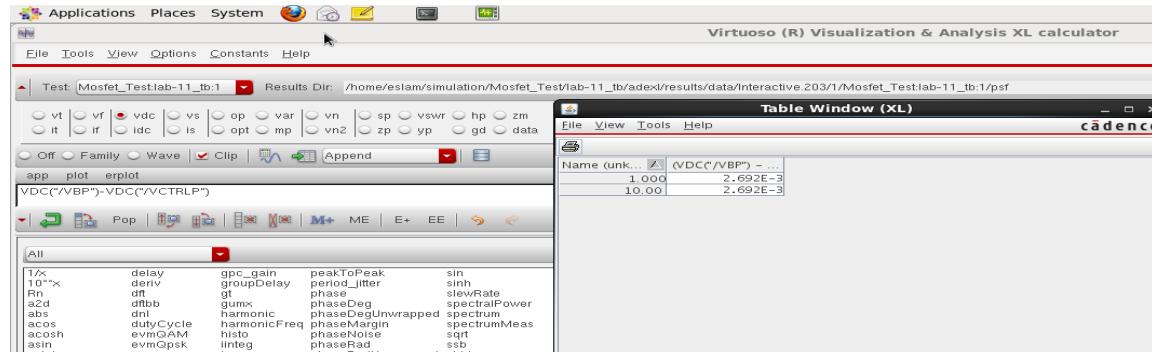
## What is diff input and op of error amplifier and the relation between them:

→dif input = $v_{ref} - v_{com}$  = 2.692mV

→small value as cmfb circuit sets vocm to be equal vref.



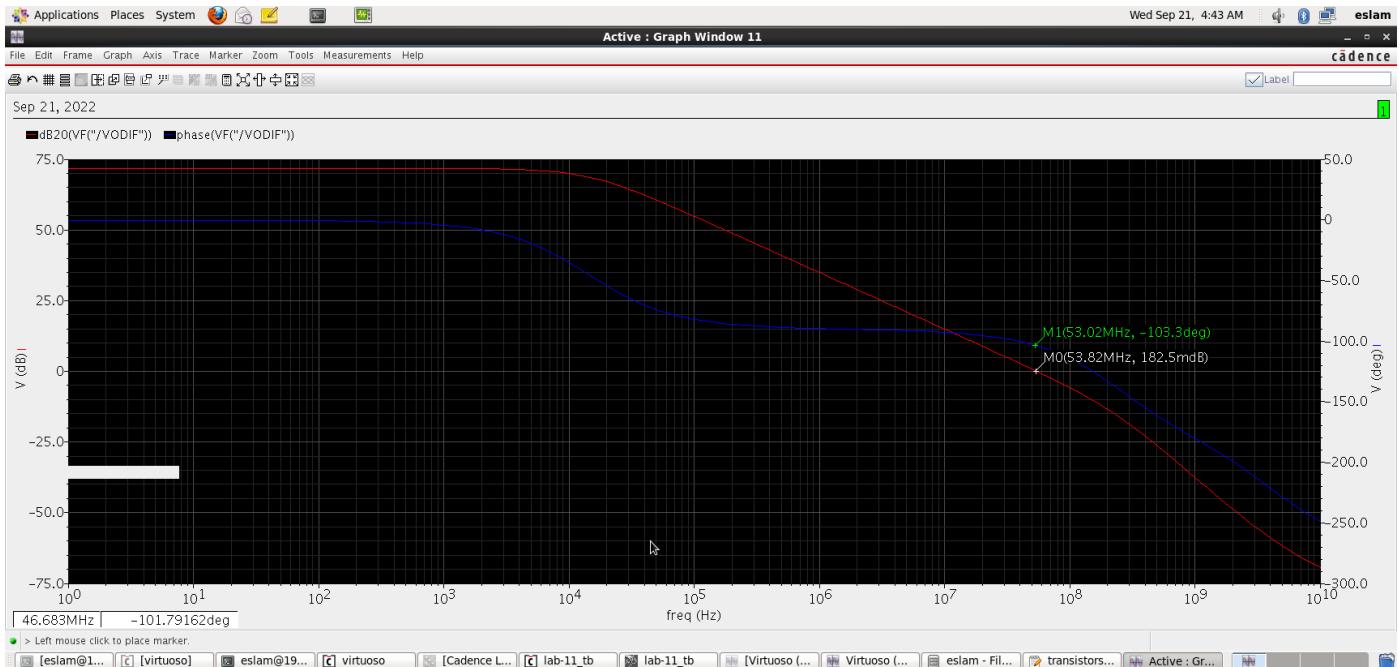
$$\rightarrow \text{diff op} = v_{bp} - v_{ctrlp} = 2.692mv$$



$\rightarrow$  they are equal as the relation between them is the error amplifier gain which is ideal =1 so  $v_{odiff}=v_{indiff}$  as shown.

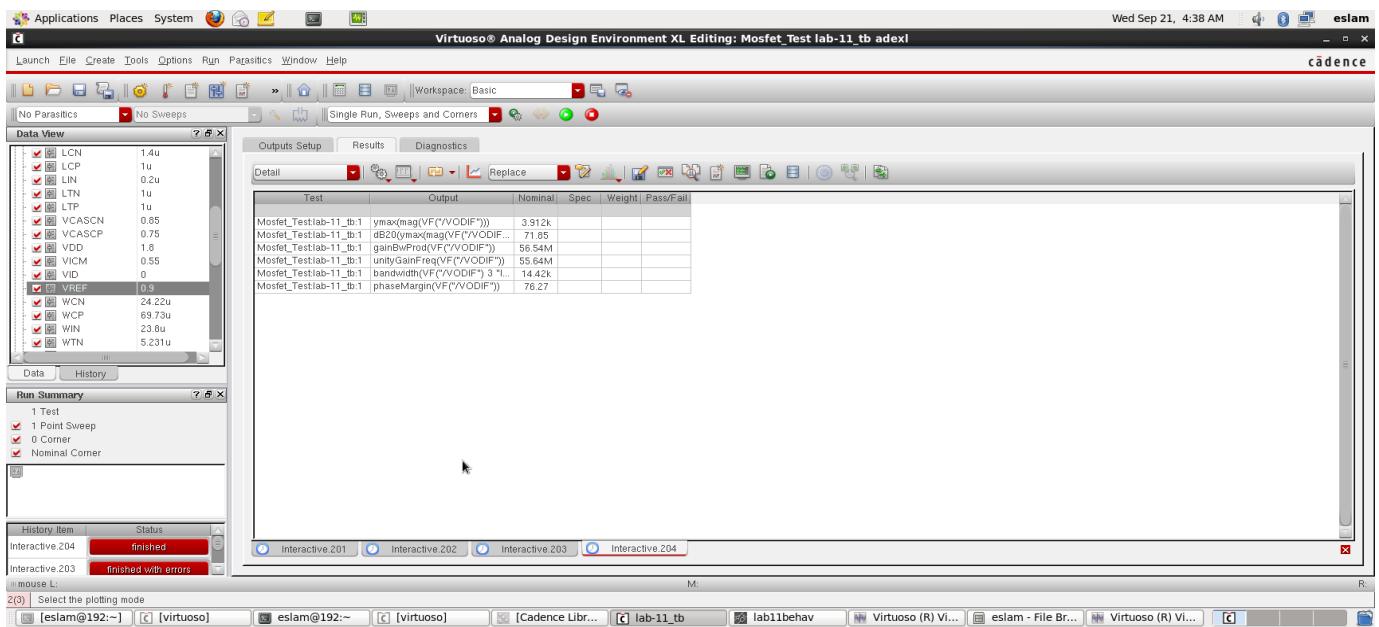
## Diff small signal ccs:

### Diff gain :



→phase margin is at 0db =  $180 - 103.3 = 76.7^\circ$

### Parameters :



### Hand analysis:

$$\rightarrow gain = gminput * rout$$

$$\rightarrow rout = r1parallelr2$$

$$\rightarrow r1 = rcascn(1 + gmcascn(rtialparallelrin)) = 8.6M.$$

$$\rightarrow r2 = rcascp(1 + gmcascp * rtail) = 85.1M$$

$$\rightarrow gain = 3.23k$$

$$\rightarrow GBW = \frac{gminput}{2\pi cl} = 66.25MHz$$

$$\rightarrow BW = \frac{GBW}{GAIN} = 20.51KHz$$

$$\rightarrow wp2 \approx \frac{WT}{4} = \frac{gminput}{4*2\pi cgg} = 333.95MHz$$

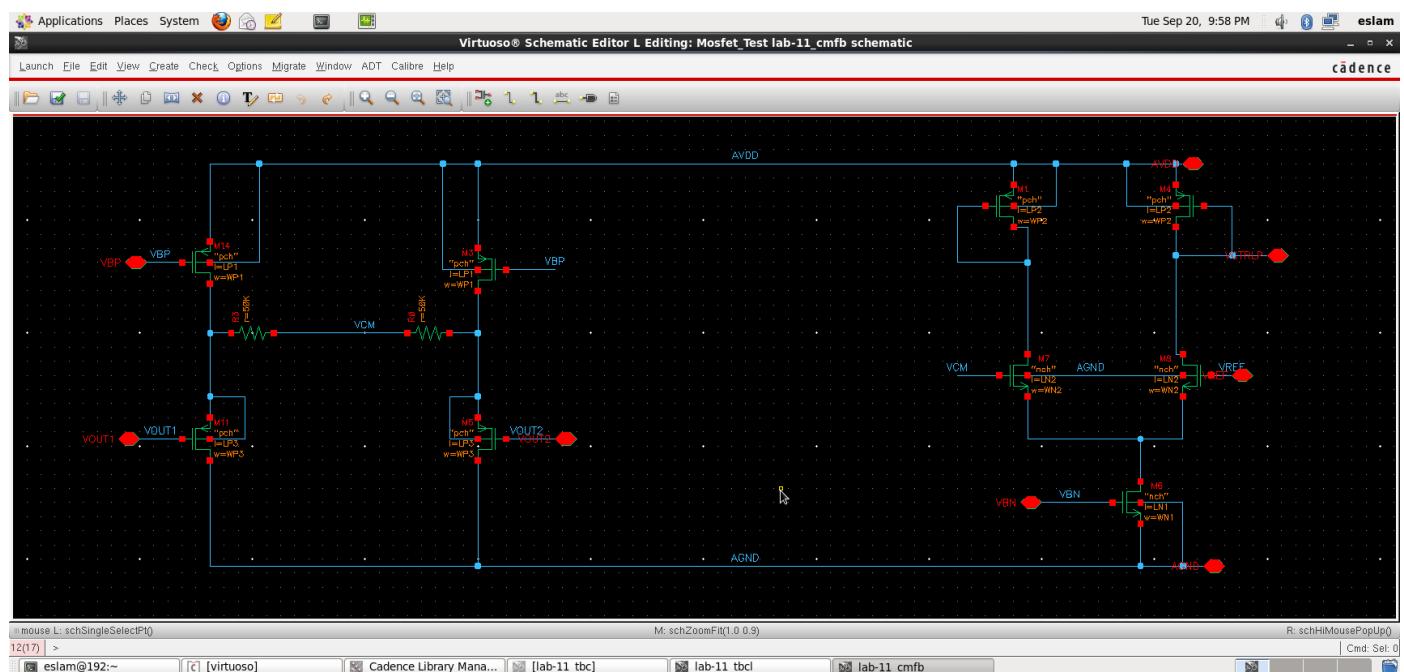
$$\rightarrow PM = 90 - \tan^{-1} \left( \frac{wu}{wp2} \right) = 78.7^\circ$$

parameter	Hand analysis	simulation
Dc gain	3.23K	3.913
Gain db	70.18	71.85
BW	20.51KHz	14.42KHz
GBW	66.25MHz	56.54MHz
UGF	66.25MHz	55.65MHz
PM	78.7	76.27

→ we can notice difference significant in GBW result from simulation and hand analysis , this because I used large gm/id for input pair =20 which increases w and increases parasitic caps and as simulation takes this parasitic caps in consideration and I did not take in hand analysis so the simulation result will be smaller than my hand analysis calculation for this reason.

## Part4

### Cmfb schematic:



→ M1, M4, M14, M3, M6 are designed before in part 3 and gm/id and length are known.

→ other transistors are designed using ADT charts using given length and gm/id as shown:

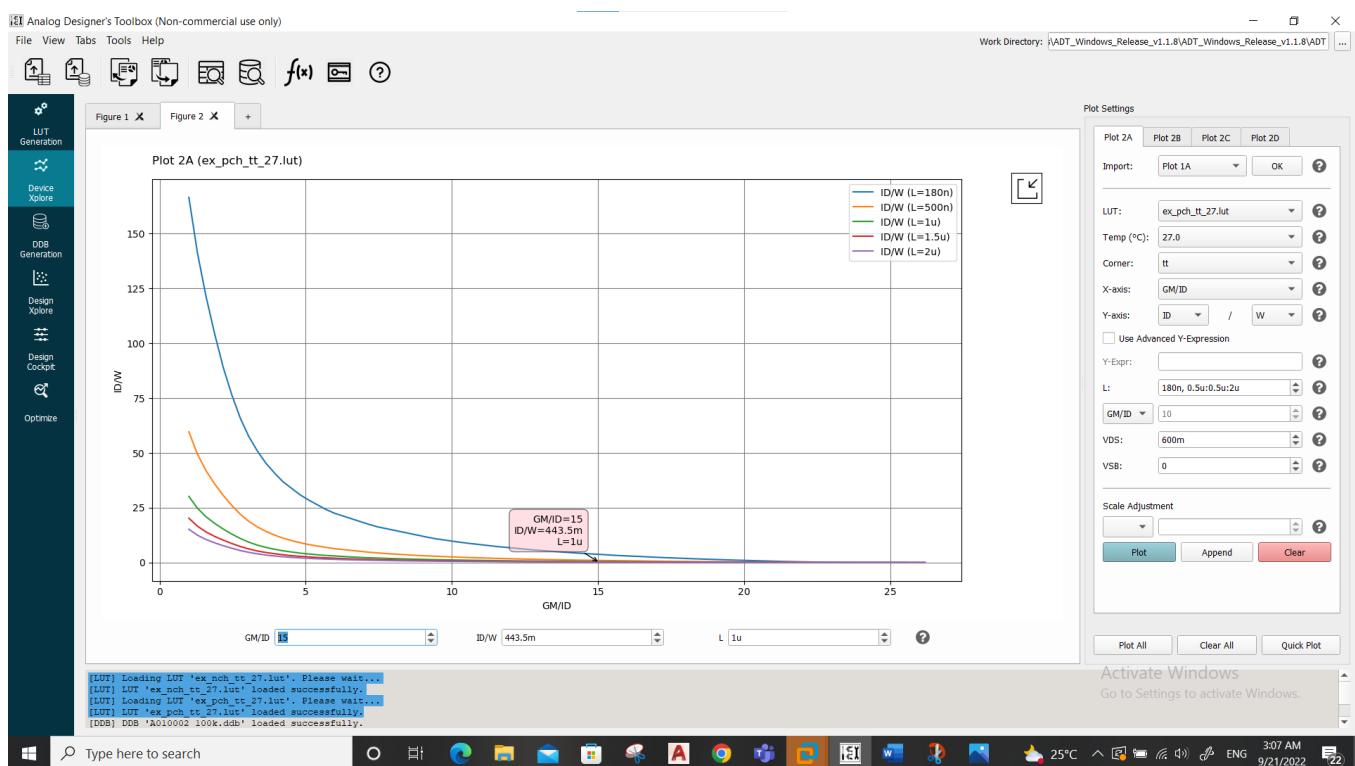
→ we got vref as  $v_{ref} =$

$$\frac{(VDD - VGSP - v_*) + 2v_*}{2} = 0.726$$

→ then I added it to vgs of CD so  $v_{ref} = 1.25v$

Id /w charts:

→ for CD:

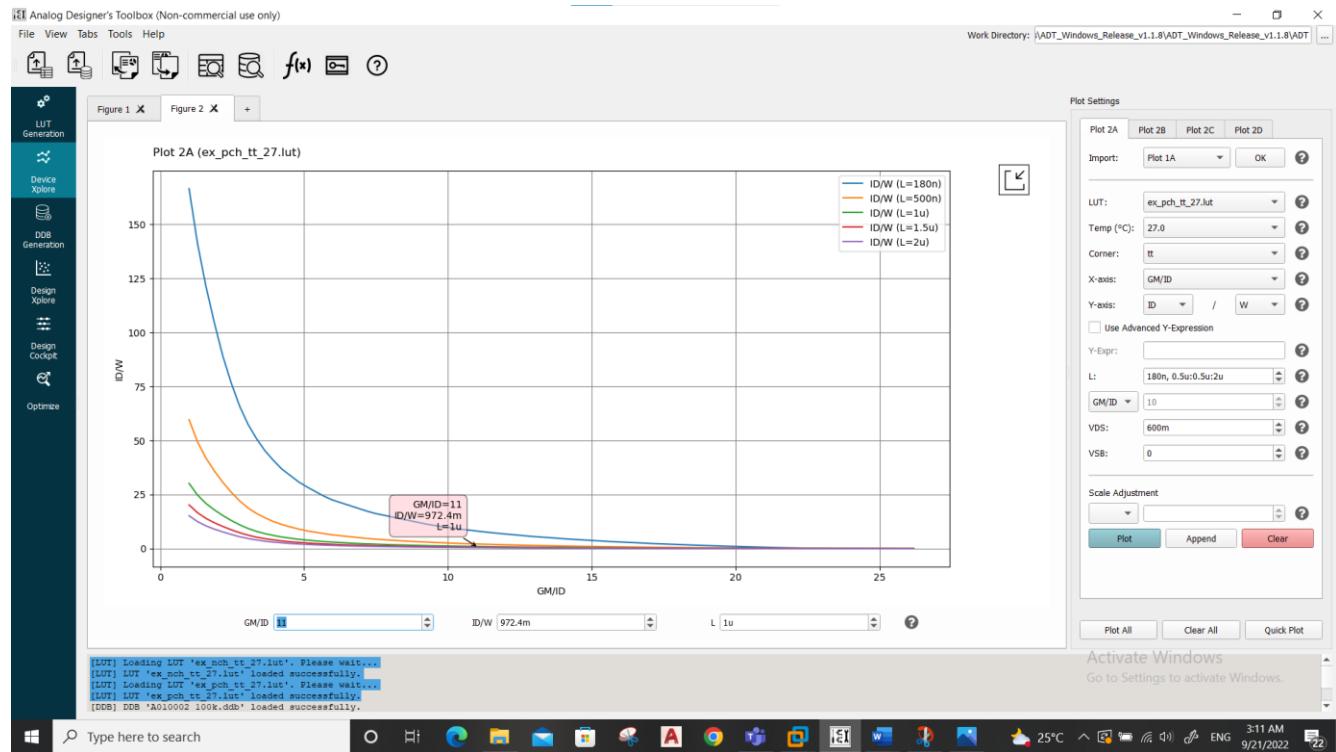


$$\rightarrow W = 10 / 443.5 \text{m} = 22.54 \mu\text{m}$$



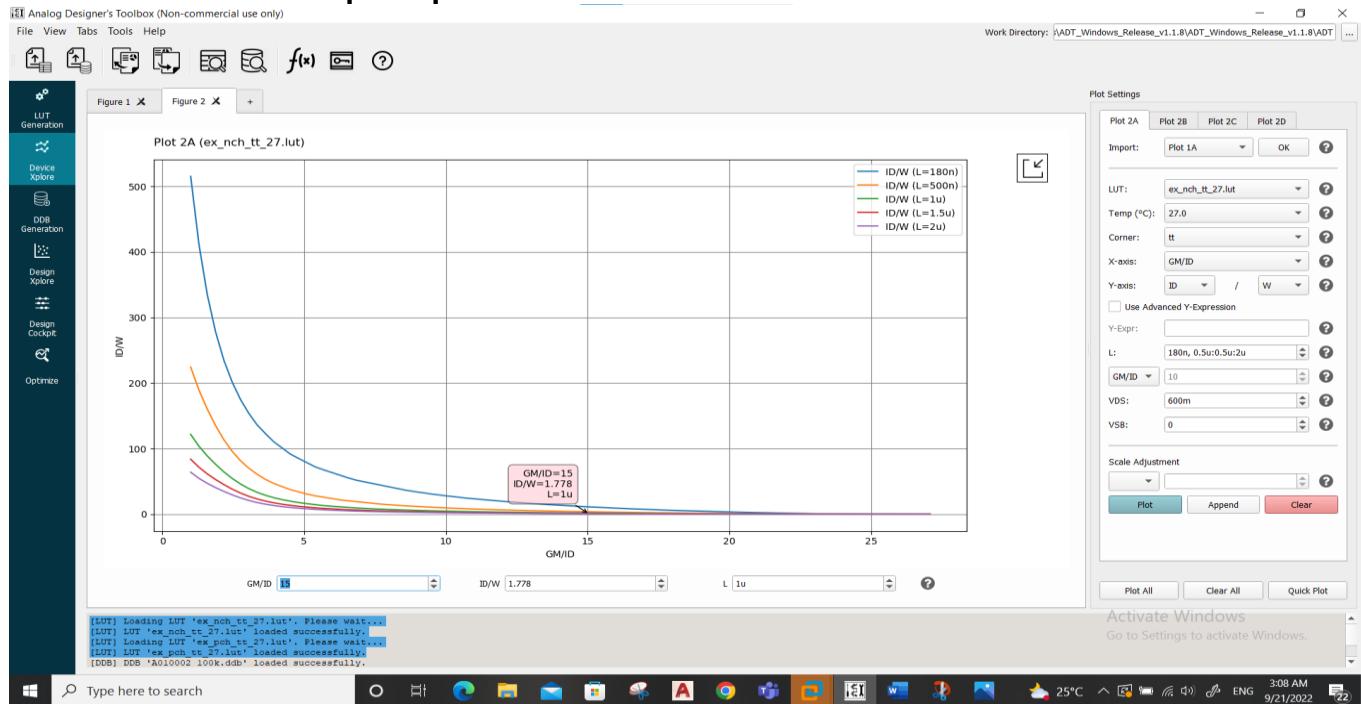
$$\rightarrow v_{gs}=528.6 \text{mv}$$

$\rightarrow$  for pmos:

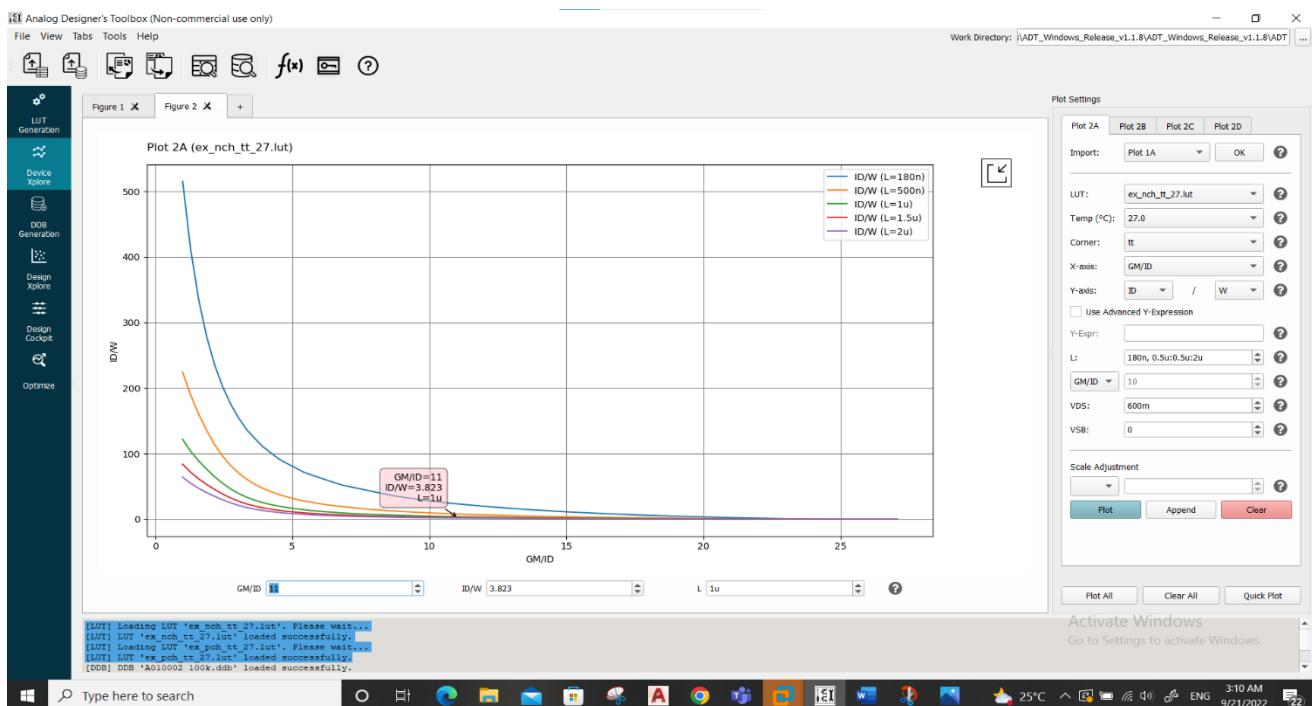


$$W=10/972.4m=10.28\mu m$$

For nmos input pair:



For tail nmos:



$$\rightarrow w = 20 / 3.823 = 5.23\mu m$$

**→** for folded cascode the dimensions as same as part 3 as these dimensions I tuned them as I explained before to achieve the closed loop specs so these dimensions attached before are final dimensions in folded that achieved the specs, so I will only attach table for dimensions of cmfb circuit:

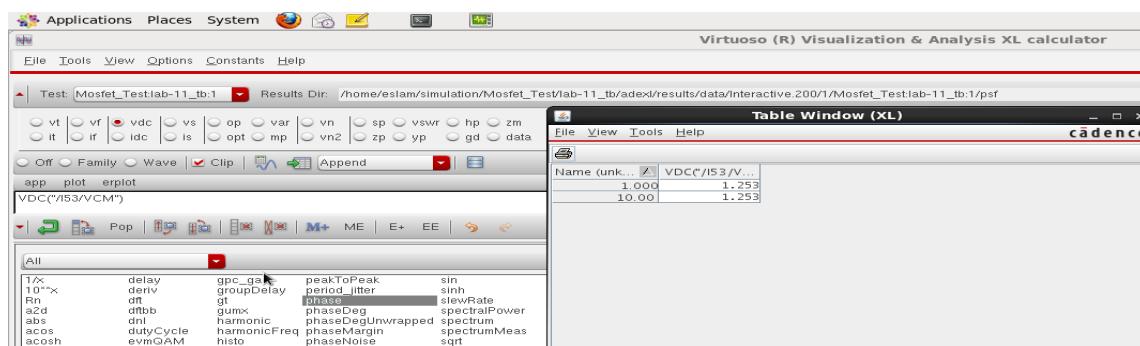
parameter	l	w
pmos	1u	10.28u
CD	1u	22.54u
Input pair nmos	1u	5.624u
Load pmos	1u	10.28u
Tail cs nmos	1u	5.23u

## Op point:

The screenshot shows a terminal window titled 'transistors.scs (~) - gedit'. The file contains a netlist for a circuit simulation. The code includes various component definitions like resistors (1, 2), transistors (I0/M8, I0/M9, I0/M11, I0/M12, I0/M13, I0/M14, I0/M15, I0/M16, I0/M19, I0/M20, I0/M5, I0/M6, I0/M7), and other parameters such as vdsat, vgs, vth, and regions. The terminal window also displays the command line at the bottom.

```
1
2
3 Name      /I0/M0      /I0/M11     /I0/M12      /I0/M13      /I0/M14      /I0/M15      /I0/M16      /I0/M19      /I0/M20      /I0/M5      /I0/M6      /I0/M7      /
4 gds      7.262u    10.94u     1.996u     1.723u     1.906u     2.415u     3.43u      7.262u     1.898u     10.94u     1.906u     2.415u
5 gm      1.622u    1.996u     906n      909.1n     871.3n     877.7n     909.1n     1.299u     1.261u      10.94u     1.906u     2.415u
6 id      228.1u    337.6u     113.5u     158.4u     189u       189u       150.4u     224.4u     160.5u     156.3u      216.9u     342.4u
7 region   437.1u    416.2u     337.6u     219.6u     216.9u     342.4u     451.3u     437.1u      224.9u     416.2u      216.9u     342.4u
8 vds      277m      -791.9m    -648m     -589.9m     -423.4m     451.5m     -731m      277m      600.1m     -791.9m     -423.4m     451.5m
9 vdsat   147.3m    -67.31m    -95.46m    -152.1m     -152.1m     91.05m     -154.5m     147.3m     148.1m     -67.31m     -152.1m     91.05m
10 vgs     600.1m    -519m      -626.6m    -589.9m     -589.9m     573m      -592.5m     600.1m     600.1m     -519m      -589.9m     573m
11 vth     -589.9m    -626.6m    -596.4m     -524.2m     -589.9m     -589.9m     -592.5m     -524.2m     600.1m     685m       682.2m     -488.8m
12 vth     -411.1m    -408.8m     -540.7m     -411.1m     -411.1m     -411m      -411m      -411.1m     406.1m     406.3m     565m      565m
13 vth     -411.1m    -411m      -411.1m     -411m      -411m      -411m      -411m      -411.1m     406.3m     565m      565m
```

## What is the cm level at the OTA op and why:



→the cm level at op of OTA =1.253v as cmfb circuit is to set cm op at specific value =vref

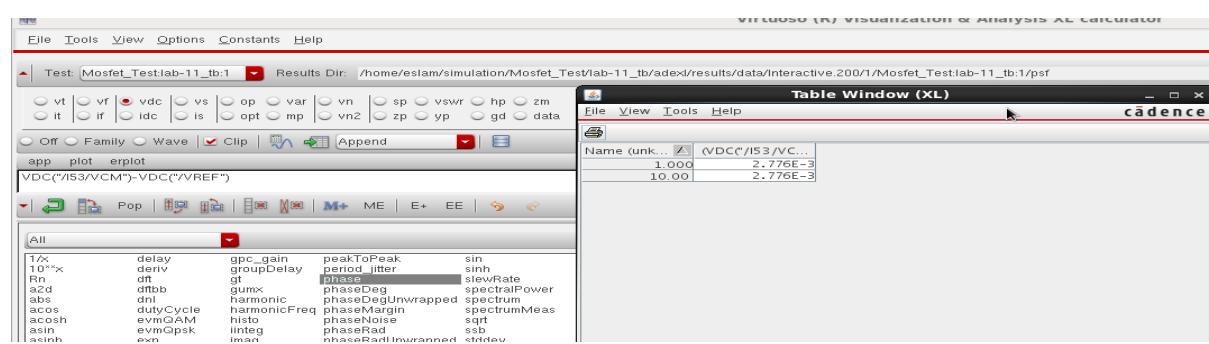
And vref is chosen to be 0.726v as I explained before and as op of OTA is passing through CD so the cm output will have DC shift =VGS of this CD which I got before from charts to be =528.6mv

So the op cm of OTA = $0.726 + 528.6m = 0.1254v$  as this value is measured at op of CD so shifted by its VGS .

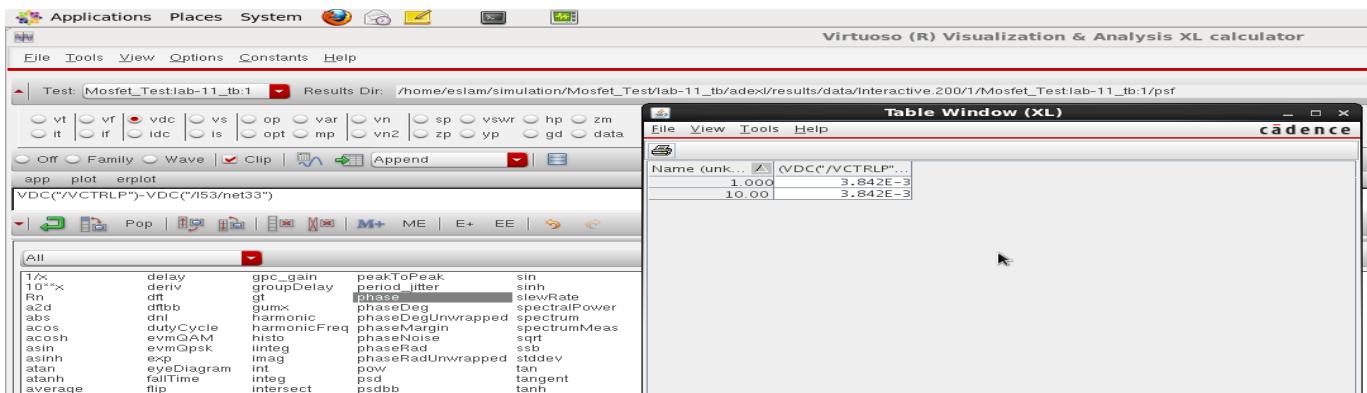
What are diff input and op of error amplifier and what is the relation:

→diff input= $v_{ocm} - v_{ref} = 2.776mv$

This is small value as cmfb is to set  $v_{ocm}$  to be =vref so the difference between them which is differential input of error amplifier is very small as shown.



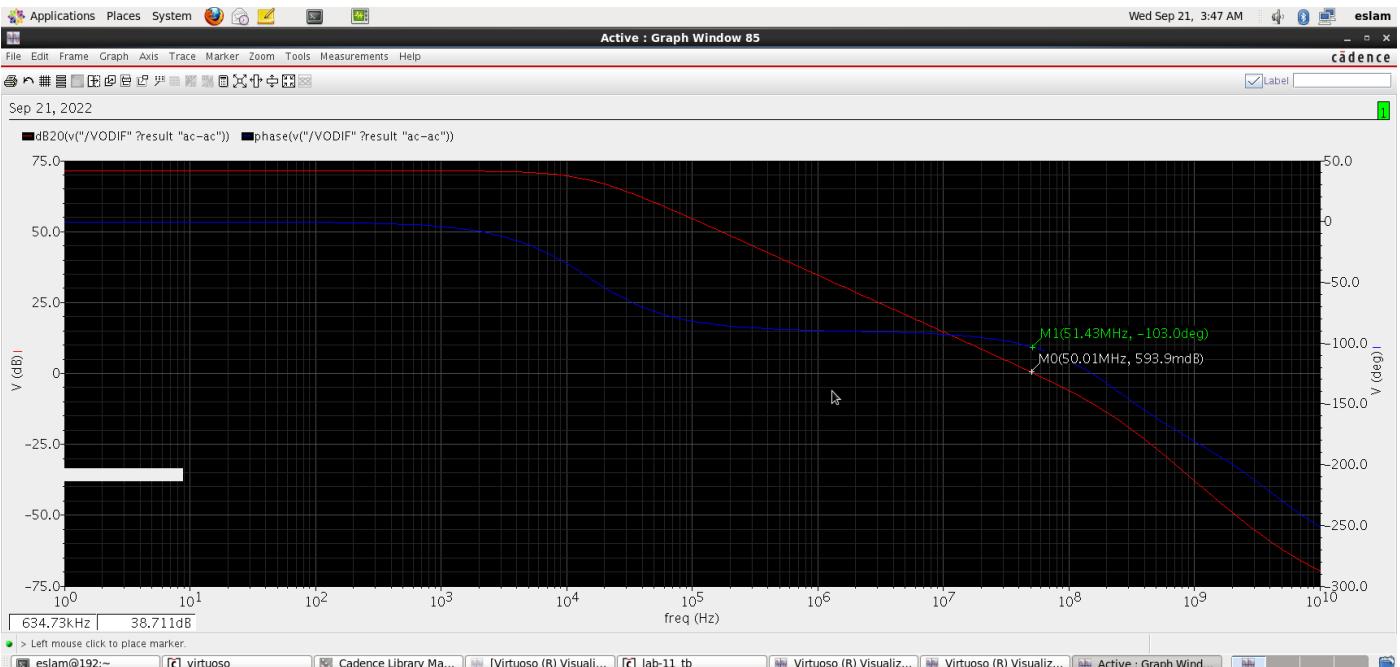
→ $v_{odif}=3.842\text{mV}$



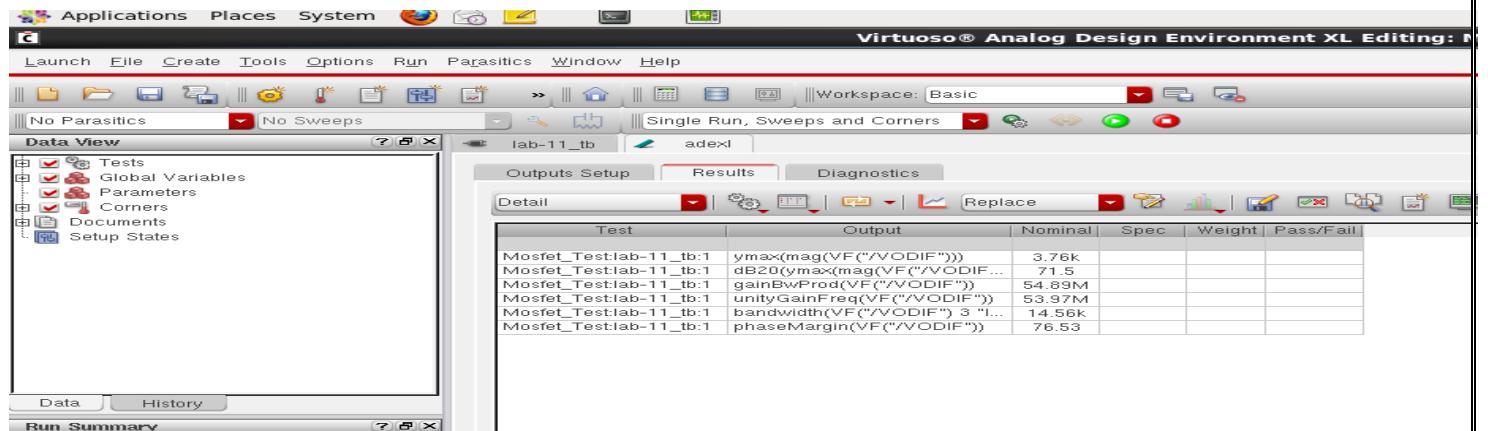
The relation between them is error amplifier gain

$$\rightarrow \text{error amp gain} = \frac{gm_7cmfb}{gm_1} = 1.4$$

Diff small signal ccs:

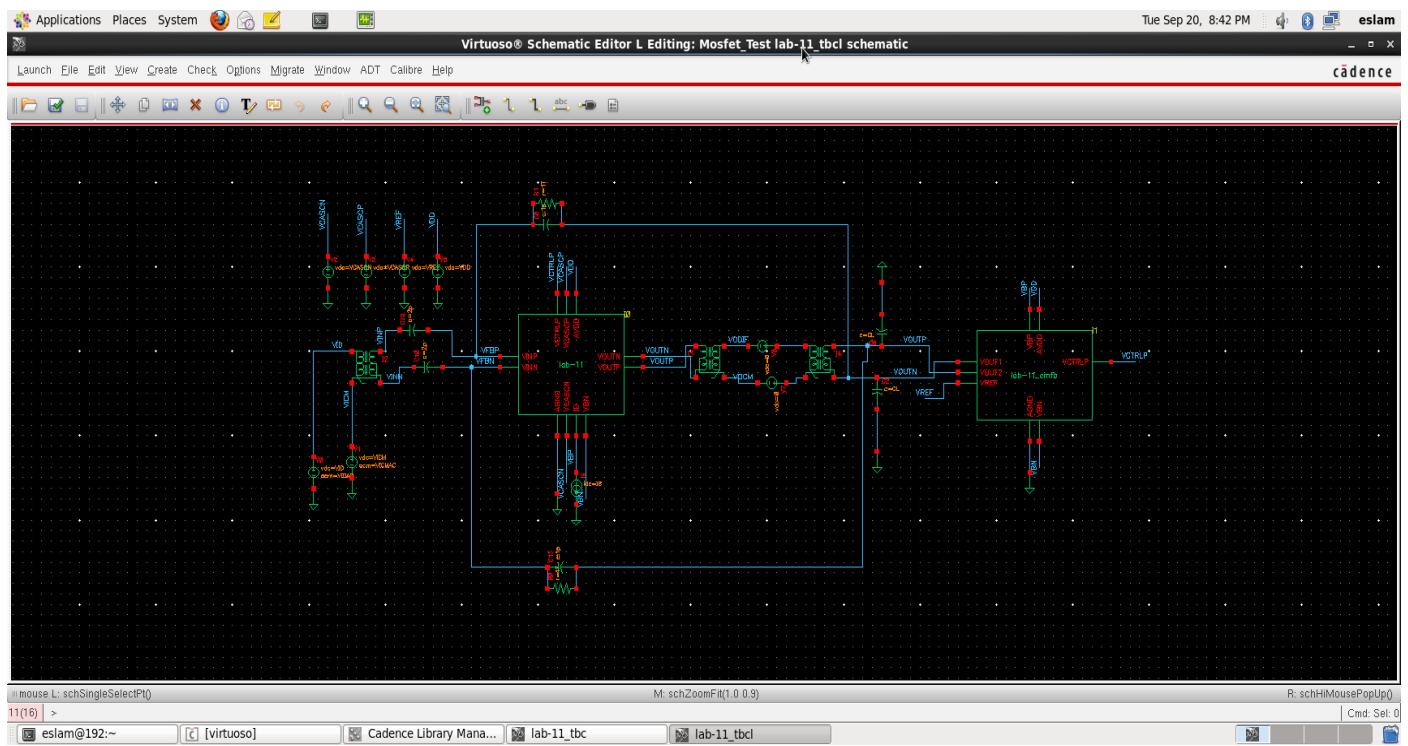


## Parameters:



## Part 5

### Schematic of test bench:



→as I wanted to achieve specs in closed loop so I tuned in sizing in open loop until I achieved in closed loop so the dimensions that I attached in part3 and part4 are same here as they were chosen to achieve these specs in this part and I attached the final sizing parameters in these parts before in tables.

## Op point:

```

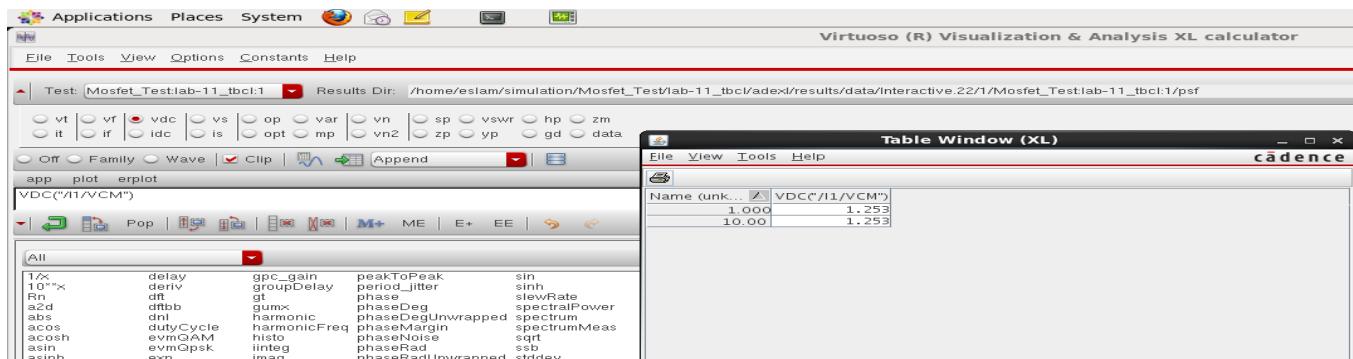
1
2
3 Name          /I0/M0      /I0/M11     /I0/M12      /I0/M13      /I0/M14      /I0/M15      /I0/M16      /I0/M19      /I0/M20      /I0/M5       /I0/M6       /I0/M7
4 IO/M8         /I0/M9      /I1/M1      /I1/M11     /I1/M14      /I1/M3       /I1/M4       /I1/M5       /I1/M6       /I1/M7       /I1/M8       1.906u
5 gds          1.622u     1.996u     10.48u     10.12u     1.996u     2.369u     3.57u      10.48u     1.898u     10.12u     1.906u     2.369u
6 gm           431.9u     418u      987.3n     909n      871.4n     871.4n     989n      1.926u     1.3u        1.259u
7 lu           228.1u     337.6u     113.6u     150.4u     109u       109u       110.9u     224.4u     160.7u     156.1u     216.9u     341.7u
8 id           40.24u     40.24u     -20.54u    -19.7u     -19.7u     -19.7u     -41.09u    40.24u     21.01u     -20.54u    -19.7u     19.7u
9 vds          -21.01u    -19.7u     -10.71u    -9.922u    -9.922u    -9.922u    -10.23u    20.94u     10.71u     10.23u
10 region      2          2          2          2          2          2          2          2          2          2          2          2
11 vds          2          2          2          2          2          2          2          2          2          2          2          2
12 vds          -1.004     -647.7m    -596.5m    -1.253     -547m      -547m      -592.3m    -1.253     567.9m     635.6m     639.8m
13 vdsat        147.1m    65.67m     -95.46m    -156.4m    -105.4m    -151.4m    -152.1m    90.74m     147.1m     148.1m     -65.67m
14 vgs          608.1m    -512.8m    -626.6m    -596.5m    -524.2m    -589.9m    -589.9m    -592.3m    112.6m     110.6m     -512.8m
15 vgs          -589.9m    -626.6m    -596.5m    -524.2m    -589.9m    -589.9m    -592.3m    -524.2m    660.1m     685.2m     -589.9m
16 vth          408.3m    -486.8m    -540.7m    -411.1m    -411.1m    -411.1m    -411.1m    -411.1m    662.1m     686.1m     562.5m
17 vth          -411.1m    -540.7m    -411.1m    -411.1m    -411.1m    -411.1m    -411.1m    -411.1m    406.3m     486.1m     -411.1m
18 vth          -411.1m    -540.7m    -411.1m    -411.1m    -411.1m    -411.1m    -411.1m    -411.1m    565m      486.8m     465.8m

```

## What is the cm level at OTA op:

→cm level at OTA op approximately = vref as cmfb circuit is to set the cm level of OTA op to specific value which =

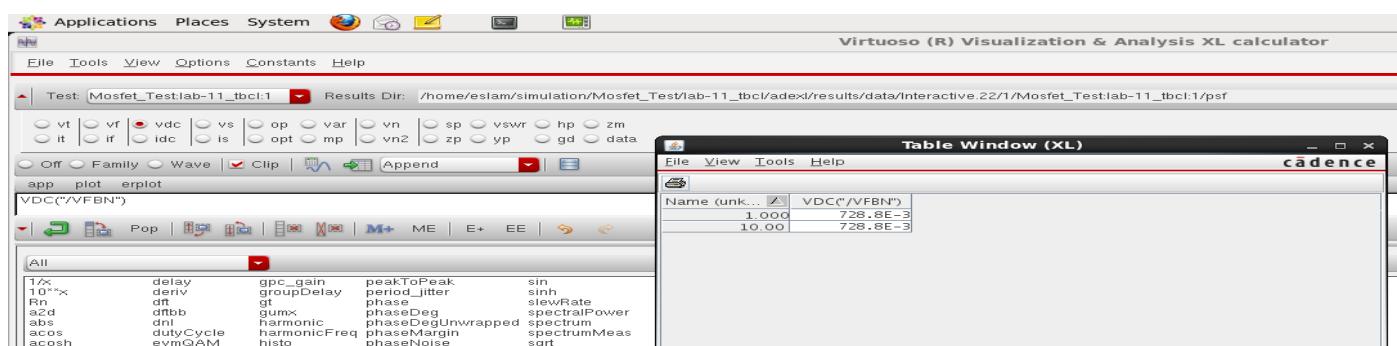
vref so it is =1.253v as it is measured as op of CD so it is shifted vy VGS of CD but its real value of CM level of OTA op is equal vref = 0.726v



What is the cm level at OTA ip:

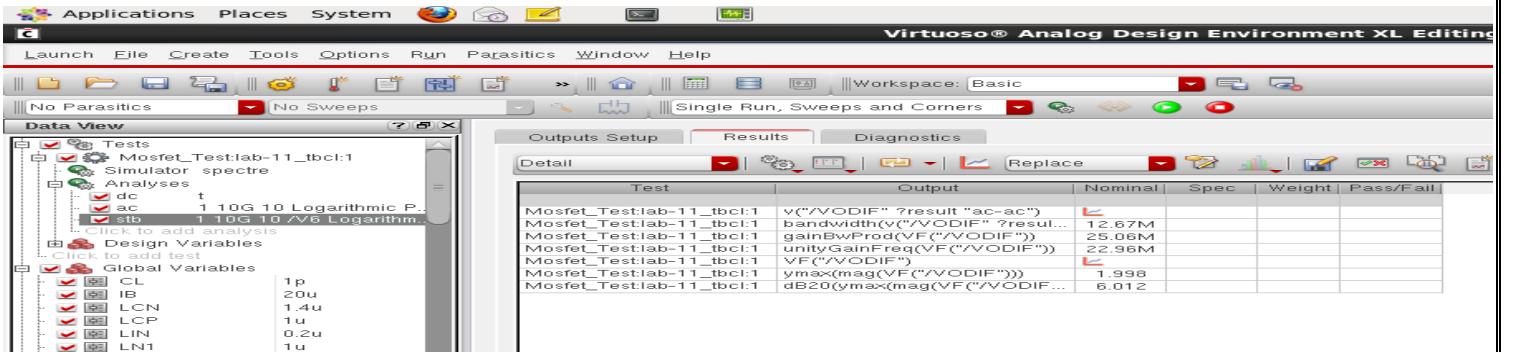
→the cm level at OTA input is approximately = the cm level at the OTA op as cin is coupling cap which blocks the DC signal and as we used very large resistance as feed back it has very low drop on it so the cm input level is approximately = the cm ooutput level =0.726v

As this is the actual cm op level which equal vref which is measured before passing through the CD.

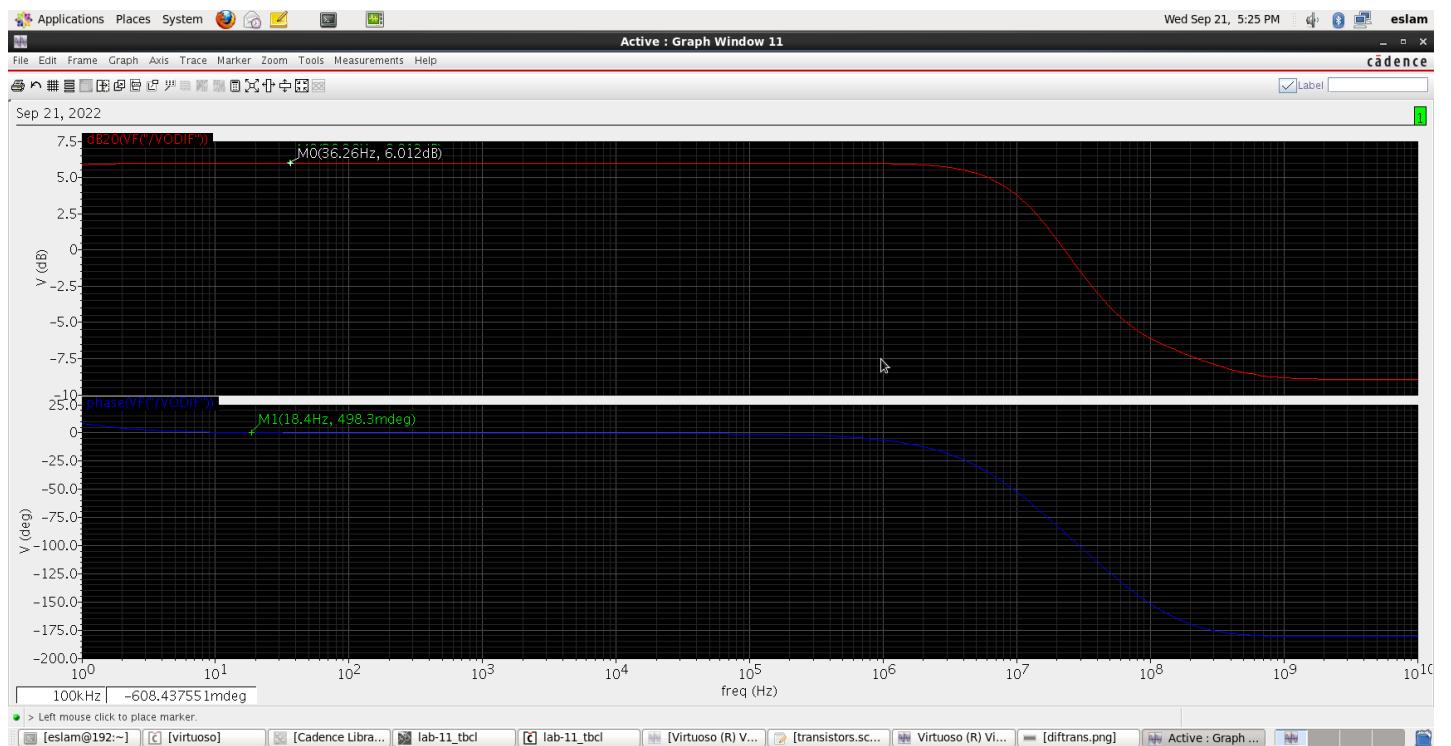


## Diff closed loop response:

## Parameters:



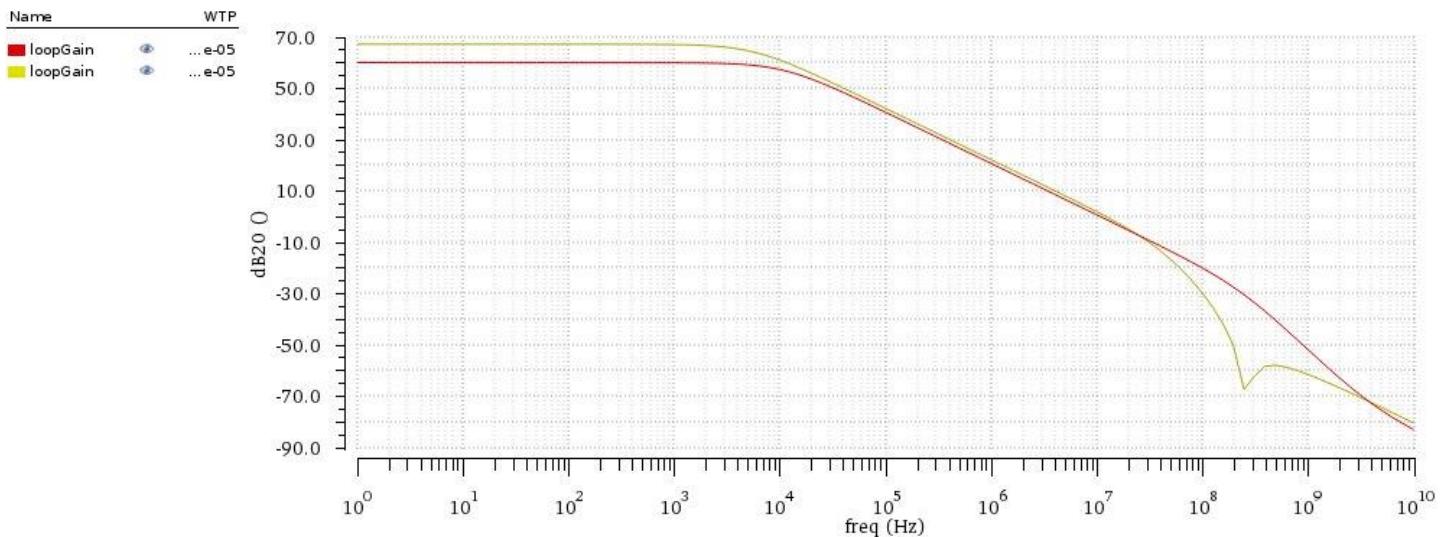
## Vodiff graph:



## Loop gain in db:

Stability Analysis 'stb': freq = (1 Hz -> 10 GHz)

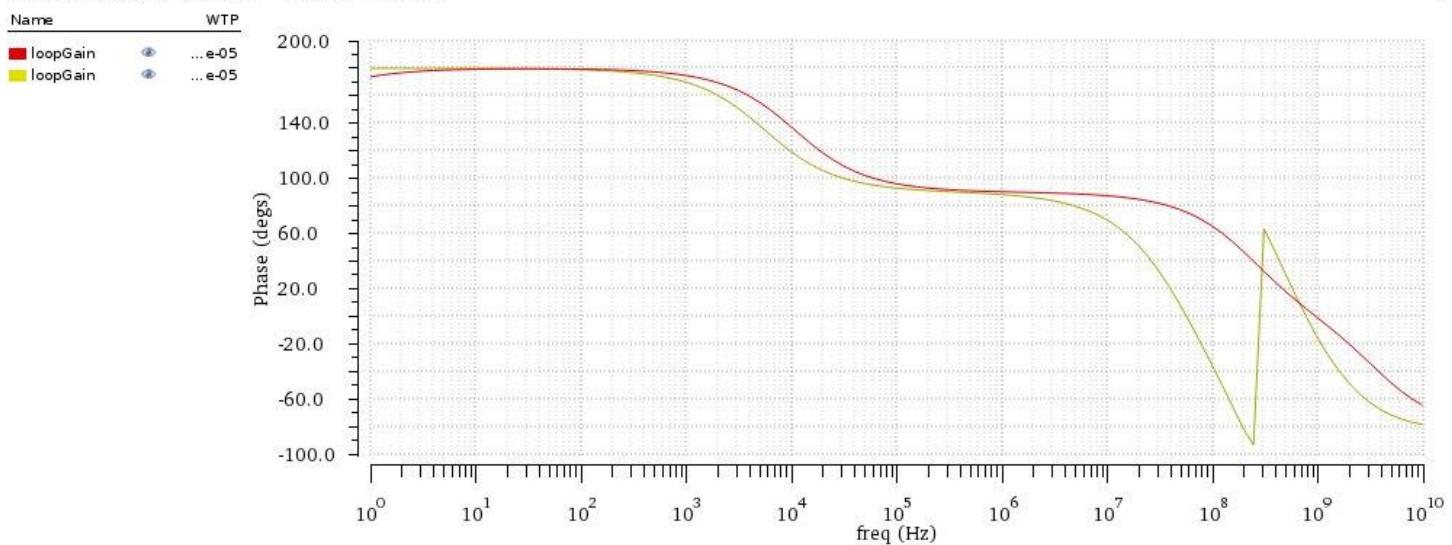
1



## Phase:

Stability Analysis 'stb': freq = (1 Hz -> 10 GHz)

1



## Diff parameters :

The screenshot shows the Virtuoso Analog Design Environment interface. The main window title is "Virtuoso® Analog Design Environment XL Editing: Analog\_CMOS". The menu bar includes Launch, File, Create, Tools, Options, Run, EAD, Parasitics/LDE, Window, and Help. The toolbar has various icons for file operations and simulation. The left sidebar is titled "Data View" and contains sections for "Variables" (WN2, WP4, WP2, WP3, WFTN, WTP) and "Global Variables" (LCN, LCP, LIN, LN1, LN2, LP1, LP2). A message "Click to add variable" and "Click to add test" is displayed. The right panel shows a "Results" table with columns "Test", "Output", and "Nominal". The table lists parameters for the Analog\_CMOS\_IC:reem:1 model.

Test	Output	Nominal
Analog_CMOS_IC:reem:1	ymax(mag(getData("loopGai..."))	1.02k
Analog_CMOS_IC:reem:1	dB20(ymax(mag(getData("lo...)))	60.17
Analog_CMOS_IC:reem:1	bandwidth(mag(getData("loo...)))	10.71k
Analog_CMOS_IC:reem:1	gainBwProd(mag(getData("l...)))	10.95M
Analog_CMOS_IC:reem:1	unityGainFreq(mag(getData("...)))	11.18M
Analog_CMOS_IC:reem:1	getData("/phaseMargin" ?res...))	87.25

## Cmfb parameters:

The screenshot shows the Virtuoso Analog Design Environment interface. The main window title is "Virtuoso® Analog Design Environment XL Editing: Analog\_CMOS". The menu bar includes Launch, File, Create, Tools, Options, Run, EAD, Parasitics/LDE, Window, and Help. The toolbar has various icons for file operations and simulation. The left sidebar is titled "Data View" and contains sections for "Tests" (Analog\_CMOS\_IC:reem:1, Simulator spectre), "Analyses" (stb, ac, dc), and "Design Variables" (LCN, LCP, LIN, LN1, LN2). A message "Click to add analysis" is displayed. The right panel shows a "Results" table with columns "Test", "Output", and "Nominal". The table lists parameters for the Analog\_CMOS\_IC:reem:1 model.

Test	Output	Nominal
Analog_CMOS_IC:reem:1	ymax(mag(getData("loopGai...)))	2.31k
Analog_CMOS_IC:reem:1	dB20(ymax(mag(getData("lo...)))	67.27
Analog_CMOS_IC:reem:1	bandwidth(mag(getData("loo...)))	5.681k
Analog_CMOS_IC:reem:1	gainBwProd(mag(getData("l...)))	13.15M
Analog_CMOS_IC:reem:1	unityGainFreq(mag(getData("...)))	12.51M
Analog_CMOS_IC:reem:1	getData("/phaseMargin" ?res...))	65.47

## Compare GBW and PM for diff and CMFB:

<u>Parameter</u>	<u>DIFF</u>	<u>CMFB</u>
<u>GBW</u>	<u>10.95M</u>	<u>13.15M</u>
<u>PM</u>	<u>87.25</u>	<u>65.47</u>

→they have approximate GBW which means that CMFB circuit is fast and can recover quickly from CM disturbance.

→PM of differential is high which means no peaking in FD or ringing in TD but PM of CMFB circuit is low which means peaking in FD and ringing in TD and also meaning poor settling time as we explained that has GBW comparable to diff circuit which means fast response and poor settling time as low PM.

→GBW of CM is larger than differential as shown as it has larger gain

→PM of CM is smaller than diff as it has UGF greater than UGF of diff circuit as shown.

parameter	DIFF LOOP	OPEN LOOP
GBW	10.95M	54.89M
DC LG	1.02K	3.76K

→ we notice that to get the LG the open loop is multiplied by factor less than 1/3

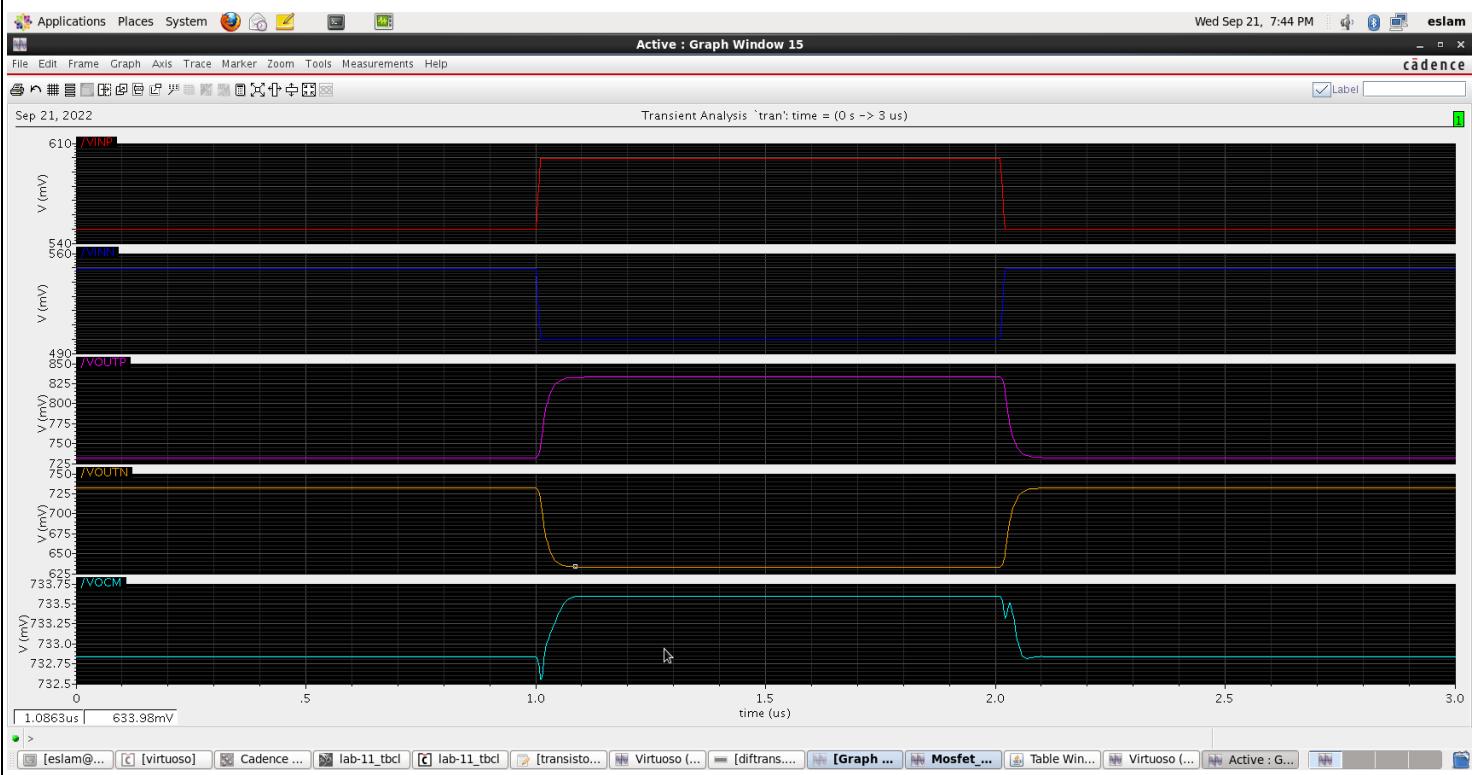
As  $\beta = \frac{cf}{cin+cf+cparasitics}$  which is less than 1/3

→ we notice that GBW in LG is multiplied by factor less than 0.25

As  $GBWLG = \frac{gminput}{cin+cf+cl+cparasitics}$  and  $GBWOL = \frac{gminput}{cl}$ .

## Part6

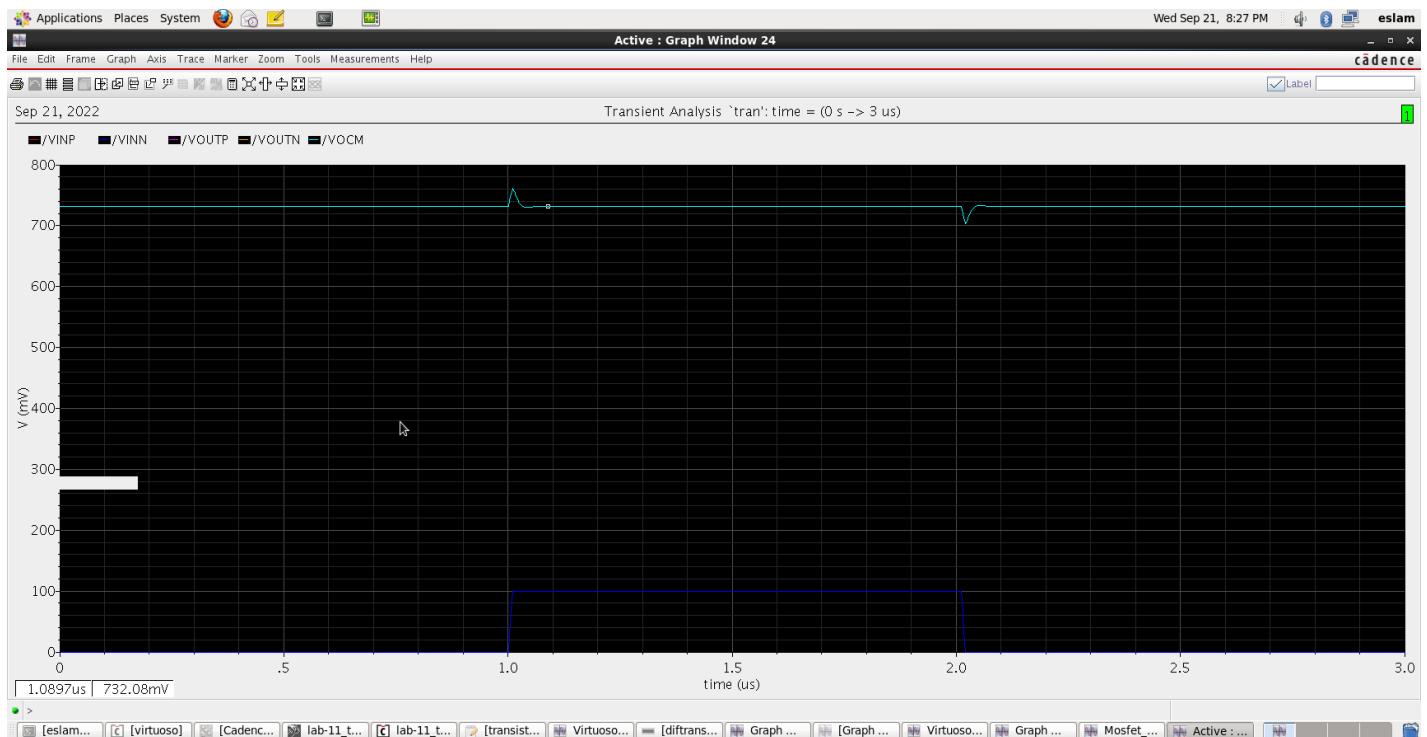
### Diff ip pulse:

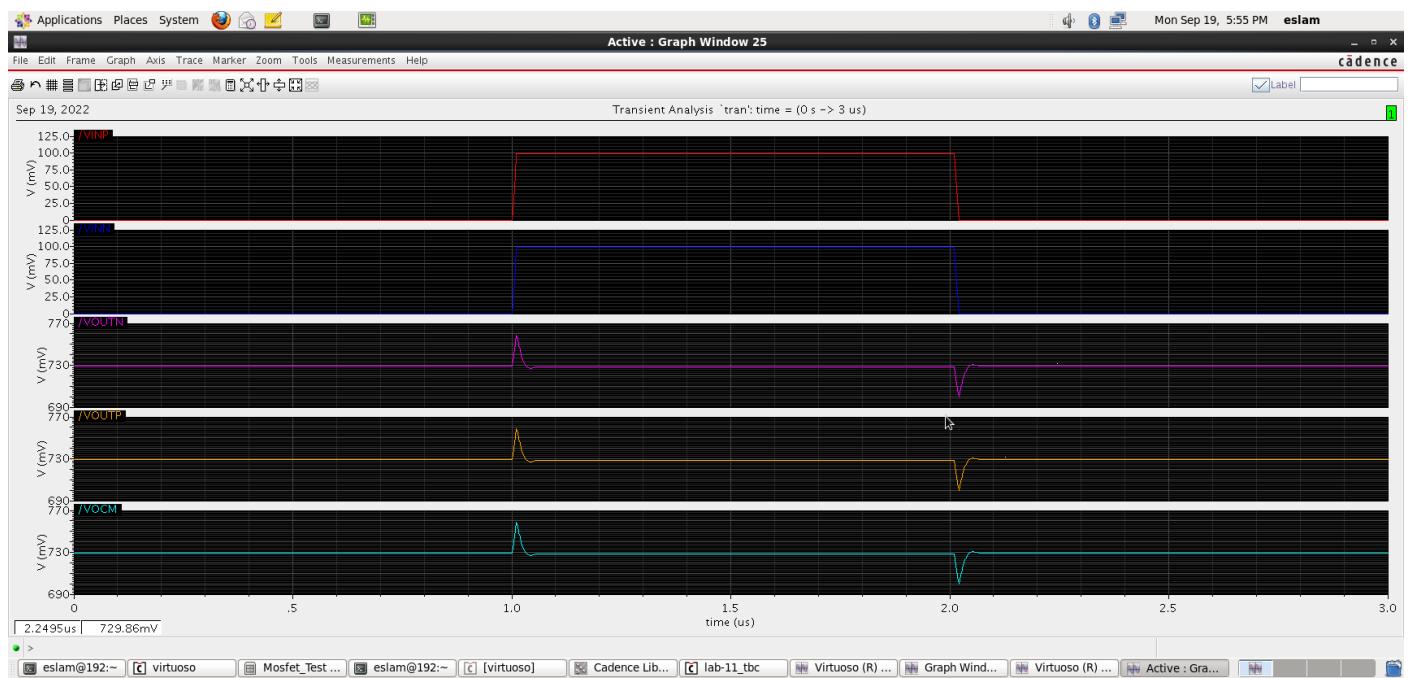


→ I notice no differential ringing as I explained before that PM is high =87 so no ringing or peaking but I notice CM ringing as PM is low =65 so it has poor settling time and there will be ringing as shown.

→ the 2 loops are stable as shown but DIFF loop is stable with adequate PM as no ringing in TD as shown but CMFB is stable but with no adequate PM as there is some ringing in TD.

## CM ip pulse:

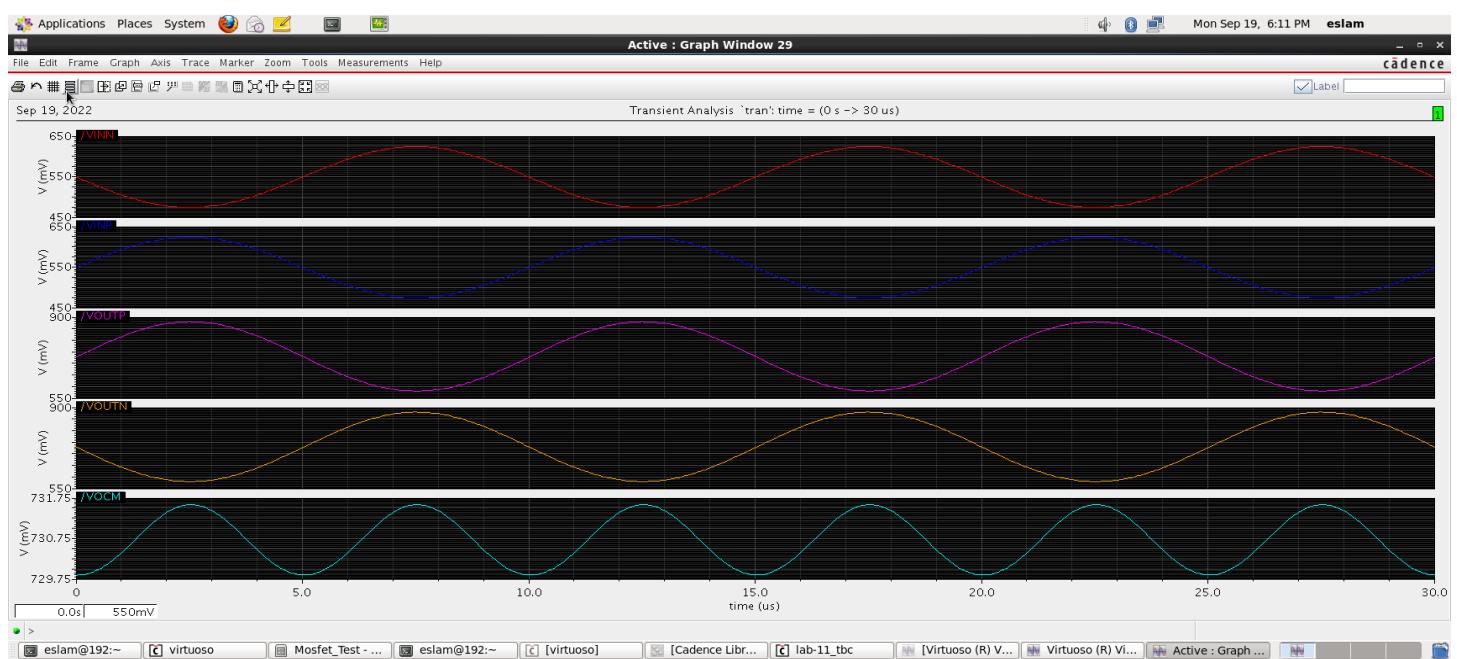
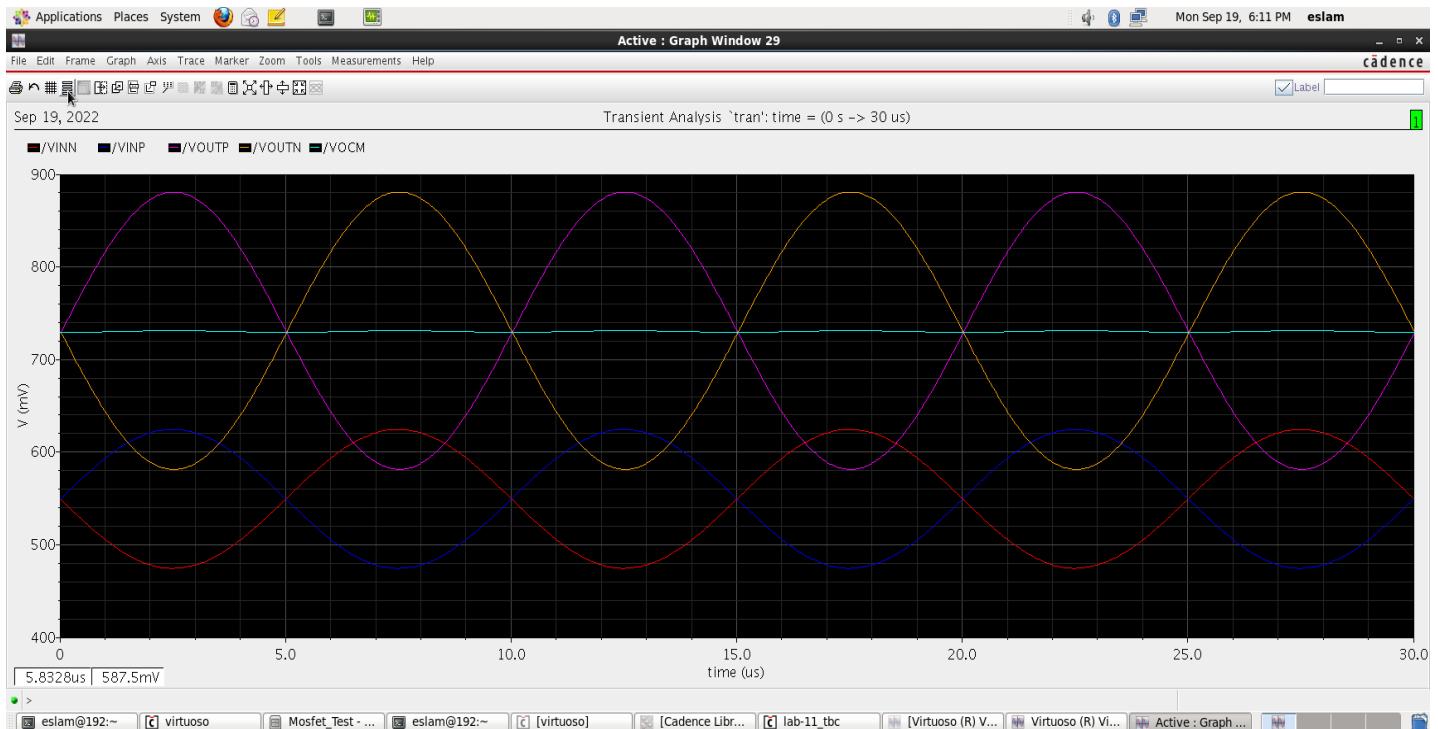




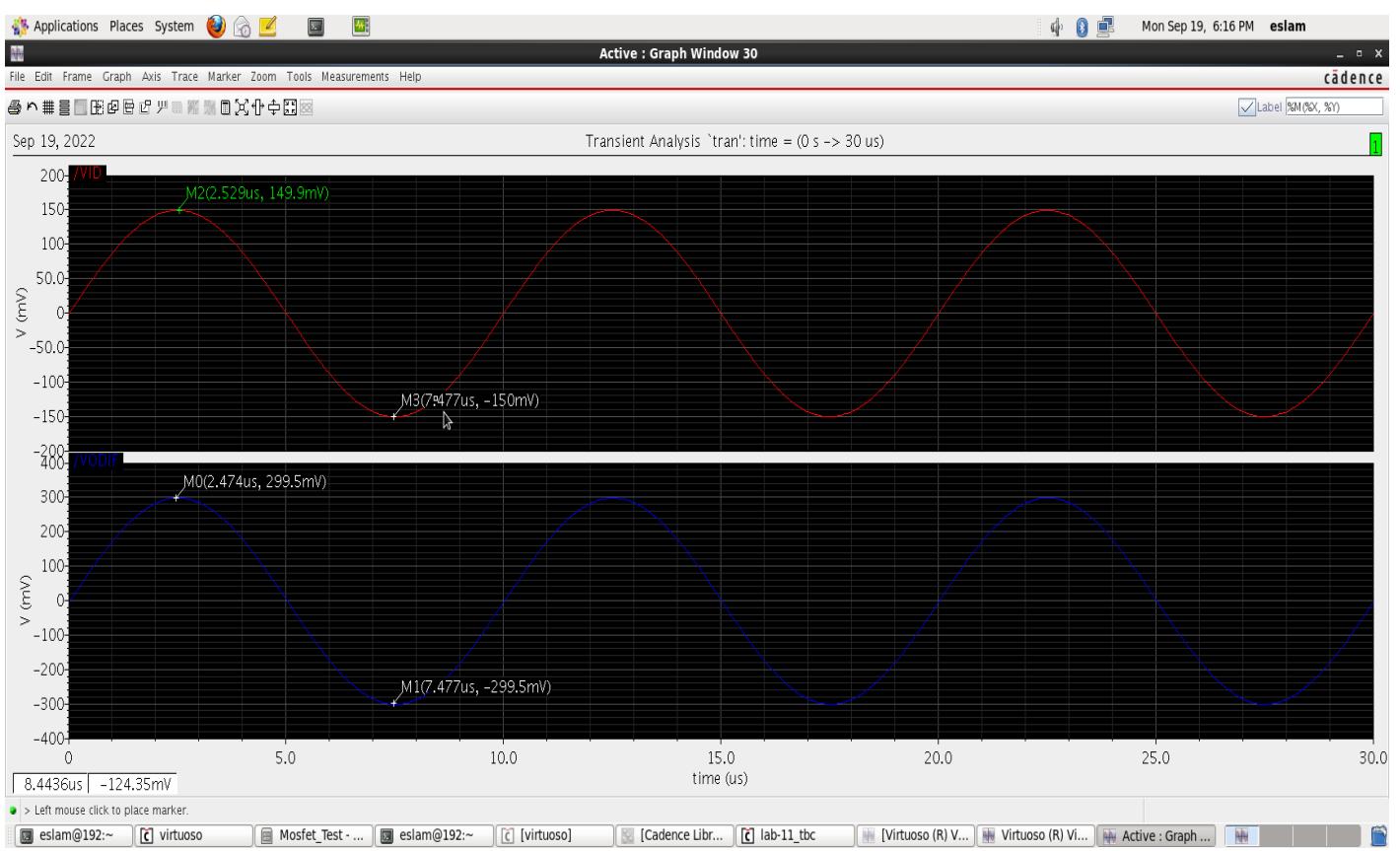
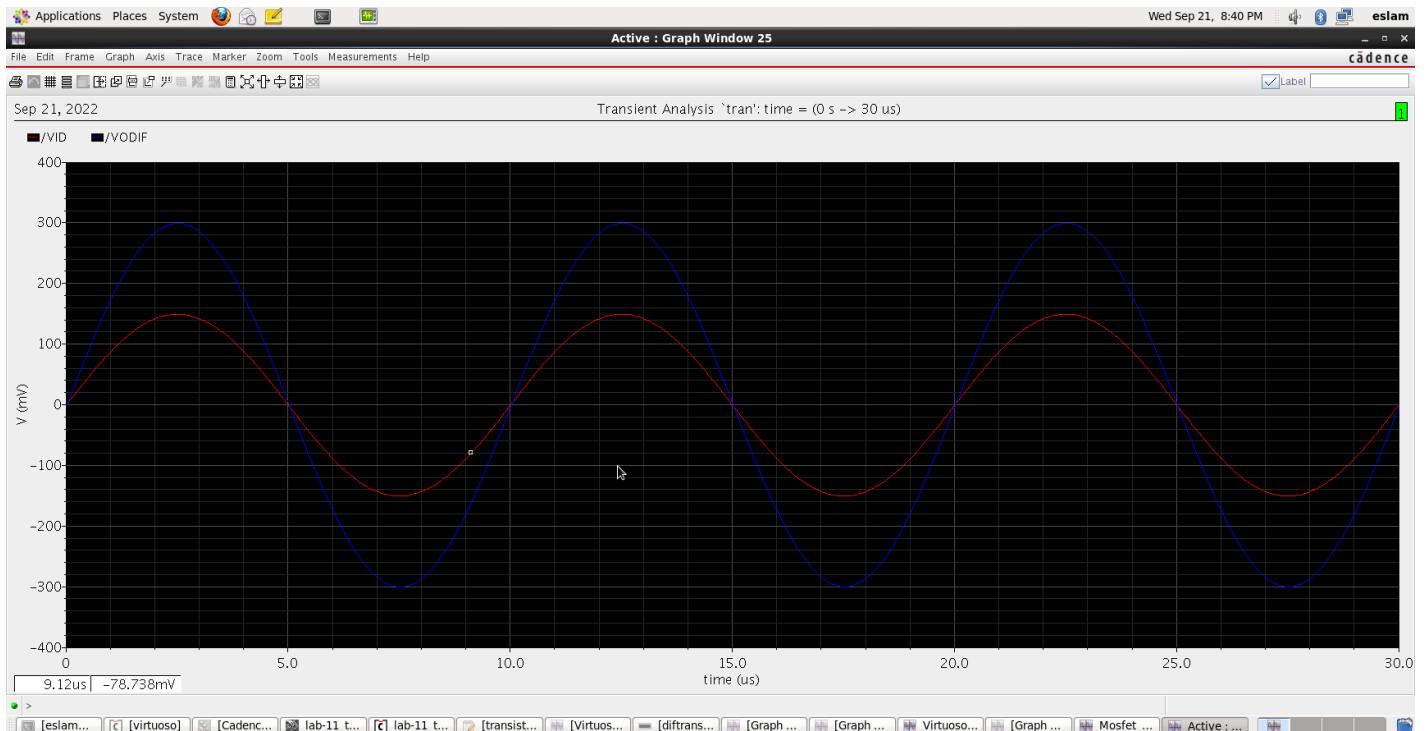
→ I notice CM ringing as PM is low =65 so it has poor settling time and there will be ringing in TD as shown and no ringing in DIFF loop in DIFF pulse graph as shown before as it has high PM as I explained before.

→ the 2 loops are stable as shown but DIFF loop is stable with adequate PM as no ringing in TD as shown but CMFB is stable but with no adequate PM as there is some ringing in TD.

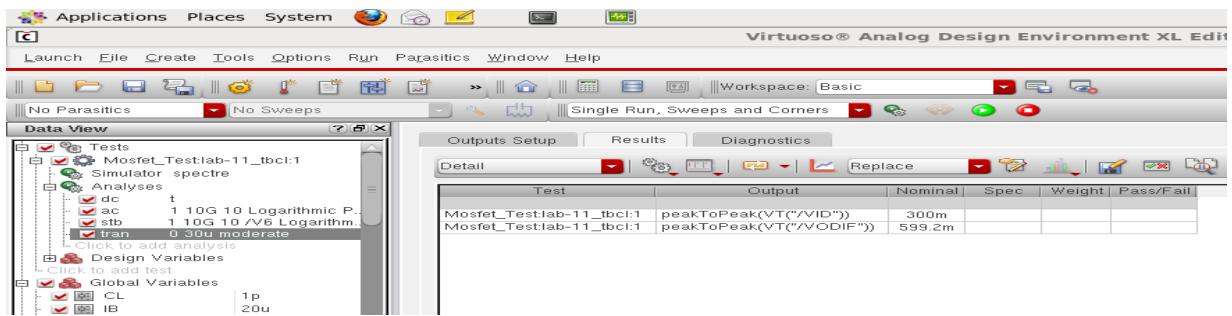
## Output swing:



## vidiff &vodiff graph:



## Peak to peak:



<u>Peak to peak input</u>	<u>300m</u>
<u>Peak to peak output</u>	<u>599.2m</u>
<u>Closed loop gain</u>	<u>1.998</u>

→closed loop gain I got before in part5

→we can see that  $vptopinput * Acl = vptopoutput$

→ $vptopinput * Acl = 599.4mv \approx vptopoutput.$