ATARI INTEROFFICE MEMORANDUM

To: Phil Suen
From: Peter and Dave
Date: 8-10-84
Subject: 65105 (Muffy) Schedule

Task Description	End Date	Comments
Complete block diag.	8-2-84 *	
Complete logic design	8-8 *	Schematics captured on Daisy/Mentor
" prototype	(8-10)	Using 2 Freddies,S189rams,20L10 PALs
Start Test program	(8-10)	Sentry 20 tester required (68pin 14MHz) ASG or outside contractor with ASG help
Logic verification	(8-13)	Simulation on VAX with Hspice on Tpd with loading on outputs (worst case)
Debug prototype	(8-14)	Using 800XL with 128Kbyte memory
Pin assignment	(8-15)	Final pinout for PCB design
Chip logic released	8-15	For mask generation
Layout Manual/Auto	8-24	For accurate and completed routing
Masks (2) completed	(8-27)	Metal interconnect and contact layers
Metalisation	(8-31)	Gate arrays assumed
Test program review	8-31	Review for diode, leakage and Tpd
Packaging	(9-5)	68 pin ceramic

Testing	(9-5)	Wafer functional and packaged tested at 14Mhz
Delivery of cut'n'gos	(9-14)	
PCB debug	(9-15)	