

ATARI INTEROFFICE MEMORANDUM

To: Phil Suen  
Date: 8-3-84  
From: David Sovey and Peter Ateshian  
Subject: MUFFY STATUS

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ACCOMPLISHMENTS:

- o Completed functional definition to 95% confidence level.
- o Completed functional block diagram to 95% confidence level.
- o Completed I/O & Memory Maps to 95% confidence level.
- o Design of simulation hardware is 40% complete.
- o Two vendors (NCR & Matra) contacted for feasibility estimate.  
Delivery of first silicon on 9-7-84 has a 10% probability.  
Delivery of first silicon on 9-14-84 has a 50% probability.  
Matra suggested a two chip partition with two 40 pin devices  
with a 9-7-84 schedule. 68 pins could be achieved if the gate  
count is less than 1240.
- o First cut "block" schematic sent to vendors 8-3-84.

PLANS:

- o Second cut 95% confidence level schematic to vendors 8-8-84.
- o Begin construction of simulator 8-8-84

PROBLEMS:

- o Need ASG or outside contractor to write test tapes for device.
- o ASG has no 68 pin production test capability. They will need  
to buy the equipment and train people or contract the production  
test of the devices to an outside house with 68 pin handlers and  
capacity to test 14.318180 Mhz operation.