ATARI INTEROFFICE MEMORANDUM

To: George Nishiura
Date: 8-24-84
From: Peter Ateshian
Subject: 65105 STATUS

ACCOMPLISHMENTS:

- Initiated chip development with NCR, Universal Semiconductor and ASG

NCR

Completed hardware and software modifications for NCR std cell implementation on Daisy at 275 (required 8087-3).

Completed critical path simulation through multiplexors and output buffer using worst case . Result : 58 - 80 ns for a 60 ns path. A 24 mA output driver was then selected (not yet available in Daisy models) to guarantee 60 ns. Impact : multiple grounds required to minimize internal ' current spiking' therefore /TEST and PCLK pins were converted to GND1 and GND2 respectively.

Completed design of register array for 65105 on Daisy ; verification in progress. Modified FREDDIE is 55% complete on Daisy schematic entry.

Design review is being scheduled for 8-29/30 with NCR and if all goes well silicon should be available in five weeks later with a PO. Silicon expected 10-7-84 worst case.

The TEGAS test vectors will be derived from the DLS simulation

files and minimum difficulty is anticipated by NCR.Production test programs will be developed upon receit of a production order. Device characterization programs have not been considered.

Universal Semiconductor Inc

After futile efforts to use USI minimally supported Daisy software Joel Silverman suggested that Atari enter our schematics on the IBM PC XT running Future Net to expedite the design process . Randy Hoopai spent two days learning and using the PC to enter the modified FREDDIE schematic which is 90% complete. Register array is the next logical block for schematic entry and should be complete by Monday. Critcal path simulation from USI was yesterday but some timing problems were encountered. Half of the propagation delay is used up by the input pad to the input of the output pad driver. The output driver uses the other half of the prop delay driving 160 pF. Initial results show 40ns typical and 87ns worst case; further efforts are in progress to improve on propagation delay .
USI seems quite amenable to working with for the prospect of future purchase order.

The design review for USI 3 micron gate array (1500) is planned for 8-28 and if all goes well silicon is expected on 9-21 with second pass silicon 9-28 worst case.

The test program will be derived from the SILOS input and output files . I have not reviewed their abilty to perform this task but will be very soon.

ASG

Carl Nielsen has submitted a schedule for this effort and is proceeding with it using a hand crafted standard cell approach.

Layout of a modified FREDDIE and register array are complete and layout of decode logic is in progress. Complete simulation is not

yet verified. Critical path timing has been estimated using FREDDIE data. Tpd is 90ns worst case and is being improved.

Roland,Lyle and Mike are implementing the cells,blocks and logic respectively. Jeff Leong has been given the 65105 description and will be modifing a FREDDIE test program to test the 65105 - no date has been esttablished for the completion of the test program.

PROBLEMS:

- Need ASG or outside contractor to write test tapes for device.
- ASG has no 68 pin production test capability. They will need to buy the equipment and train people or contract the production test of the devices to an outside house with 68 pin handlers and capacity to test 14.318180 Mhz operation.

Note: The 65105 is about 1300 gates (4 transistors per gate) of which FREDDIE (modified) comprises 30% ; the 16 X 8 register is 45% and the decode and disk control is 25%.