TO: Jack Tramiel

Tony Tokai -- Atari Japan

CC: Sam Tramiel

Shiraz Shivji

H. Suga

Leonard Tramiel

Phil Suen

Y. Okubo -- Atari Japan

FR: Tom Brightman

RE: Engineering Weekly Report

1.0 XL COMPUTER PRODUCT FAMILY

1.1 Overview

Final feature level definitions of the 6500 family computer products were completed. The computer product family will be called the "XL" family and will consist of five machines:

- 1. "XL": The 64K 800XL with 3.5" FDD support and new DOS.
- 2. "XL/Writer: A 64K computer with integral 80 column monochrome monitor, 3.5" FDD, letter quality printer, and word processing software.
- 3. "XL/CMOS": A portable 64K computer with built-in word processor, 3.5" FDD support, new DOS and 40/80 column optional LCD.
- 4. "XL/M": An XL with AMY built-in. (The music machine).
- 5. "XL/P": A 128K RAM version of the XL.

In addition, a 3.5" drive and a color monitor must be developed. The 3.5" FDD will be the same unit as used in the 68000 product family.

Development schedules for the XL family machines must focus on having the XL and the XL/Writer in production as soon as posible but no later than 1-Jan-1985. The XL/CMOS and the XL/M must be completed to the pre-production level by 1-Jan-1985. The XL/P will be designed as a fallout of the XL design and should be at a production status concurrent with the XL.

The XL family development consists of the following major activities:

- 1. 65105 Memory management IC development.
- 2. 3.5" Floppy disk drive interface development.
- 3. DOS enhancements to support 3.5" FDD.
- 4. ROM based DOS development.
- 5. Housing development.

These activities are common to all XL projects and will be reported on individually each week. The activities required to produce the specialized versions of the machines are: AMY, 80-column display, 40/80 column LCD, and Word Processor (WP) software. These activities will also be reported on each week.

1.2 65105 Memory Management IC.

1.2.1 Accomplishments -

The 65105 memory management chip required by the XL machines has been defined and initial logic design is complete and prototyped in discrete ICs.

1.2.2 Plans -

Complete debug and checkout of the prototype and verify logic design via simulation. Release logic design to vendors.

1.3 3.5" FDD Interface

1.3.1 Accomplishments -

The design for the 6500 based machines is based on an 8049 uP and a Western Digital 1770 controller. The controller will provide a 14-pin interface to the disk drive suitable for use with a DIN connector. This hardware is wire wrapped and presently connects to an SA-450 interface for debugging purposes.

1.3.2 Plans -

This activity cannot be completed until the DOS is available. In the interim we will generate test drivers to exercise the interface.

1.4 DOS Support For 3.5" FDD.

1.4.1 Accomplishments -

Techniques to provide total compatiblity between the present 5.25" and the new 3.5" drive were identified. This will allow files to be transferred between drives of different sizes and for present day 5.25" software to be easily migrated to 3.5" media.

1.4.2 Plans -

Detailed design of the handler software will proceed this week. Scheduled completion is 15-Sep-1984.

1.5 ROM Based File Manager System (FMS).

1.5.1 Accomplishments -

A workable technique to implement a ROM based file manager was identified. This technique will allow compatibility with existing software and will eliminate the need for new software products to incorporate their own file manager. This item is the longest lead time item in the schedule to introduce the new XL machines.

1.5.2 Plans -

Detailed design of the FMS will not begin until 15-Sep-1984. We have the option to delete this feature and accelerate the program schedule by 2--3 weeks.

1.6 Housing Development

1.6.1 Accomplishments -

A design concept for a family of housings for both the 6500 machines and the 68000 machines was approved. This allows design control drawings to be released 1 week behind the original schedule.

1.6.2 Plans -

Obtain the design control drawings and digitize for PCB layout ASAP.

1.7 AMY Development

1.7.1 Accomplishments -

Additional errors were found in the AMY device layout which will require that PG release be delayed until 31-Aug-1984. These errors were caught by simulation of the clock and RAM sections of the device and are considered very serious. Barring detection of additional very serious errors the schedule for prototypes on 21-Sep-1984 will not be affected.

1.7.2 Plans -

Continue circuit simulation and continuity checking efforts to assure design correctness at first pass. Implement fixes required to correct clock and RAM problems.

1.8 80 Column Display

1.8.1 Accomplishments -

Definition fo the features of the XL/Writer was completed which allowed the functionality of the 80 column display to be defined. The display should operate in a bit-mapped mode to support user selectable and mixable fonts, italics, bolding, underling, and possibly superscripting.

1.8.2 Plans -

Evaluate design tradeoffs to provide lowest cost display hardware which retains maximum compatibility with the XL products. This means that we would like to support BASIC and other applications packages in 80 column mode if there is no unit cost impact.

1.9 40/80 Column LCD

This is an area of concern. If at all possible, the XL/CMOS unit should incorporate the same built-in software as the XL/Writer. To do so will require that the 80 column display architecture be functionally compatible with the 80 column CRT display. To achieve this goal it may be necessary to complete the definition of the XL/Writer system and software before the XL/CMOS design can be completed.

 ** Y. Okubo: Please advise me of your approach on the 80 column LCD.

1.10 Word Processor Software

1.10.1 Accomlishments -

Performance goals for this package were established. The XL/Writer package should provide "what you see is what you get" functionality and should provide features equal to or better than any competitive product. In particular, our goal is to exceed the performance of the ADAM system and to provide competitive performance with 80 column Apple II series systems.

1.10.2 Plans -

Complete feature definition and comparative analysis of $\ensuremath{\mathtt{ADAM}}$ and $\ensuremath{\mathtt{Apple}}$ systems.

2.0 68000 PRODUCT FAMILY

Shiraz Shivji developed a detailed cost analysis. which confirmed the unit cost goals of the low-end 68000 system. The earlier definition of the low end 68000 machine was changed to delete the AMY chip in favor of the GI sound chip. This change simplifies the system memory control and helps support the required costs.

2.1 Color Pallete/Video Shifter

2.1.1 Accomplishments -

Both AMI,NCR and National were approached on the subject of a 32 MHZ semi-custom IC to implement the color palette/video shifter. AMI is confident that they can achieve the 32 MHZ speed in present day production CMOS processes.

2.1.2 Plans -

Obtain National's and NCR's assessments of the $32\,$ MHZ requirement. Contact and obtain an evaluation of $32\,$ MHZ from TI and Universal.

3.0 32-BIT PRODUCT FAMILY

A meeting was held with National (NSC) to obtain the status of the 32000 product family. National was able to commit to supply on 200K units of the 32016 in 1985 and $500 \, \mathrm{Ku}$ in 1986. NSC was unable to commit to any supply of the 32032.

At a prior meeting with TI's Jerry Rogers (32000 family program manager) he stated that several "bugs" existed in the 32016 and that NSC was depending on TI to clean them up. He also indicated that TI would not have any 32032 product until at least 3Q85.

4.0 ENGINEERING OPERATIONS

4.1 Memory Sourcing

Both NCR and AMI provided detailed information on their 64 K/128 K/256 K ROM products. AMI recommends design for 300 nsec access in all their products in 1984 production and 250 nsec for 1985 production. These times were their recommended times to maximize device yield and minimize device cost. They also recommended very strongly that we design our systems to provide 0.6V Vil(max) and 2.2V Vih(min) rather than 0.8V and 2.0V respectively. This is worth 3-5% on device yield.

NCR presented information supporting 450 nsec data sheet access times as their lowest cost devices for 1985

production. This spec is unrealistic for 256K parts and $% \left(1\right) =0$ we will have to explore with them their real needs.

NCR's primary focus was on improving incoming test correlation with Atari on present day product. We presently test their 300 nsec parts for room temperature access times of 250 nsec to simulate the effects of elevated temperature. This should be stopped.

4.2 Organization

The engineering contacts by functional area are defined for your information:

- 1. Document Center: Ron.
- 2. CAD/PCB Layout: Williams.
- 3. XL Family Engrg: Phil Suen.
- 4. MOS design/Test: Carl.
- 5. 68000 Family: Shiraz Shivji.6. VAX Systems: Bill Galcher.

Please communicate directly to these people when they can be of assistance and on issues you feel may affect them.

4.3 Equipment For Japan

We have assembled the kit of equipment you have requested and are prepared to ship it to you when U.S.A. export approval and Japan import approval are obtained.

Tom Brightman