ESE555 VLSI System Design

Assignment 3

Reetam Mandal

114353881

reetam.mandal@stonybrook.edu

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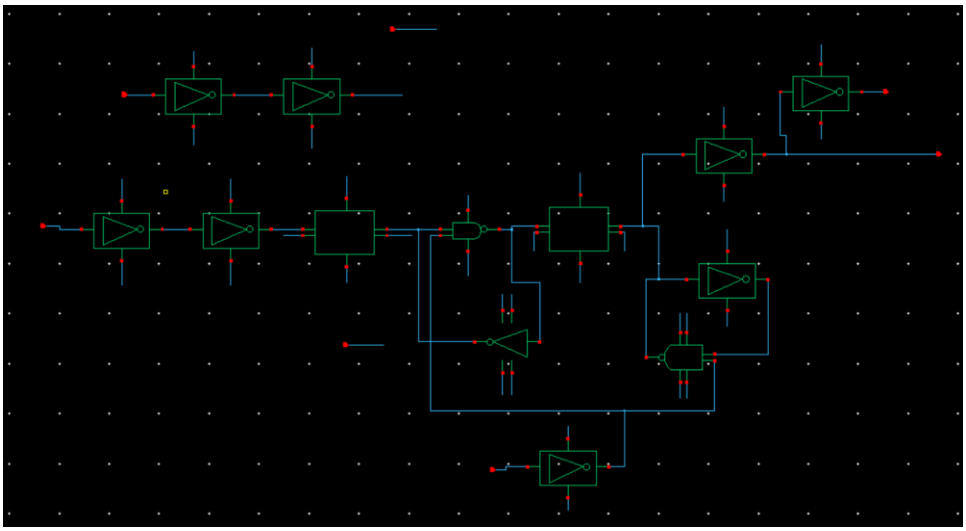
Q. CMOS positive (rising) edge triggered master-slave D type flip-flop with an asynchronous reset (active at logic high) using 45 nm static CMOS technology.

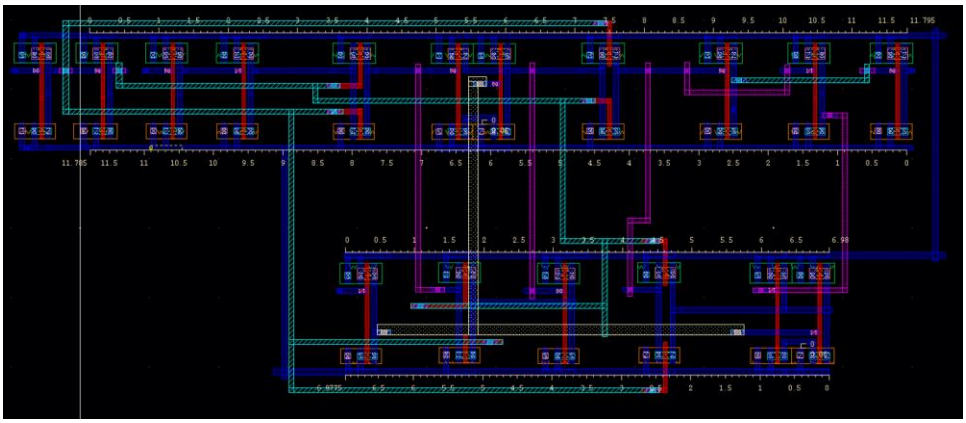
Three inputs (data, clock, and reset) and two outputs (Q and Q bar). Supply voltage is set to 1.1 Volts. External load of 5 fF. 20 ps of rise/fall times for the data and clock signals. 50% duty cycle for both signals.

D Flip-Flop

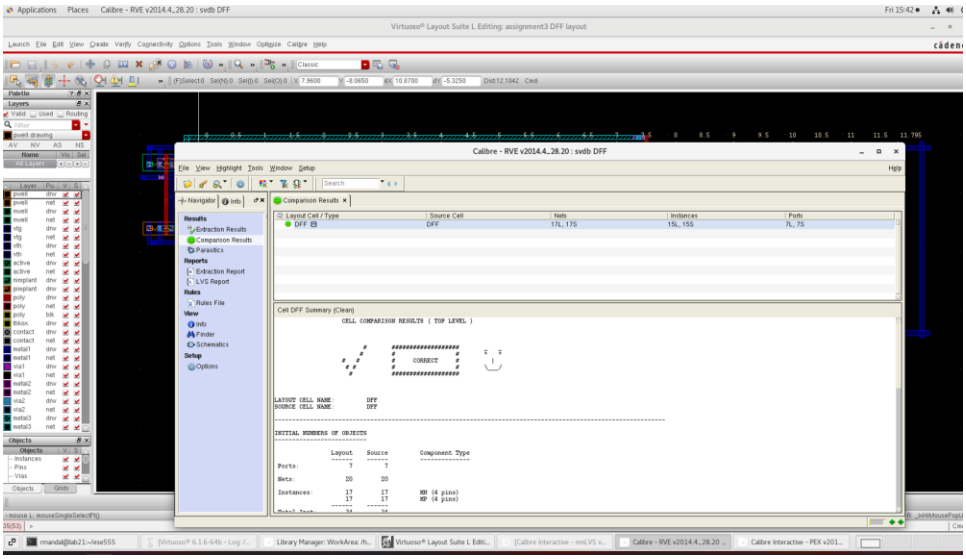
Schematic

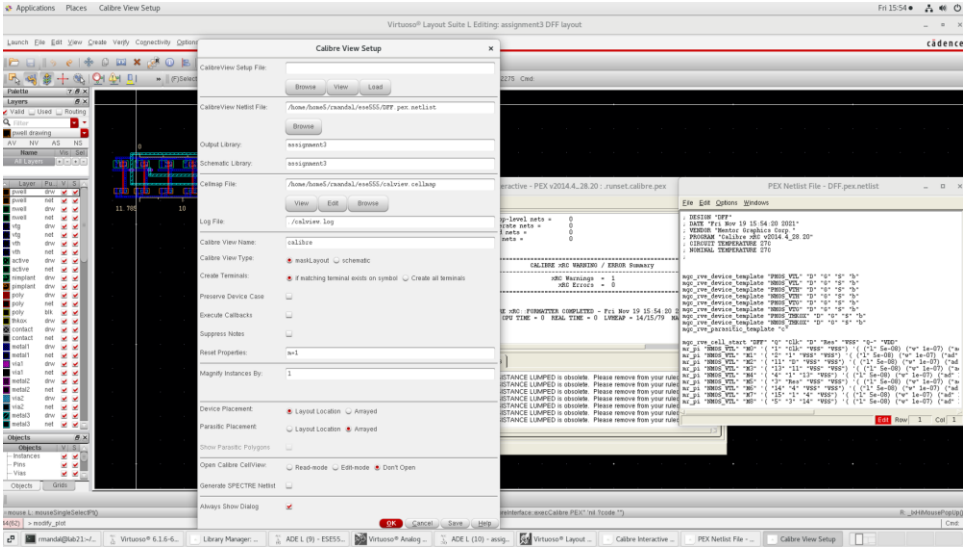


Layout

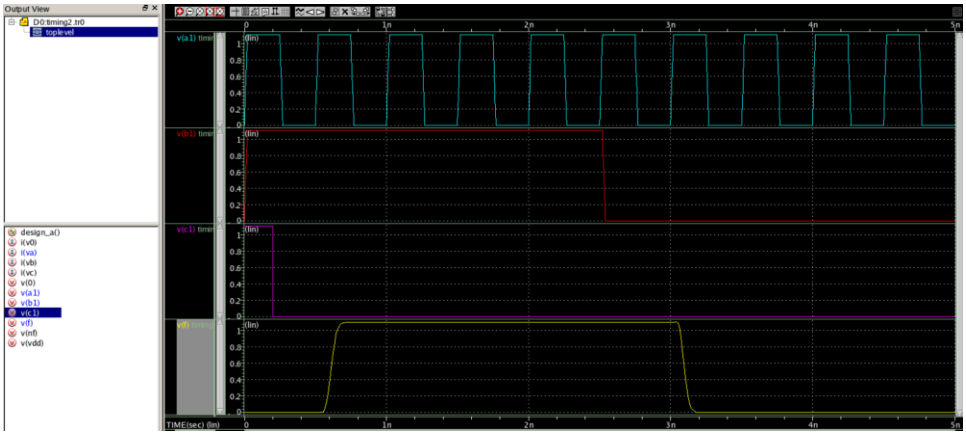


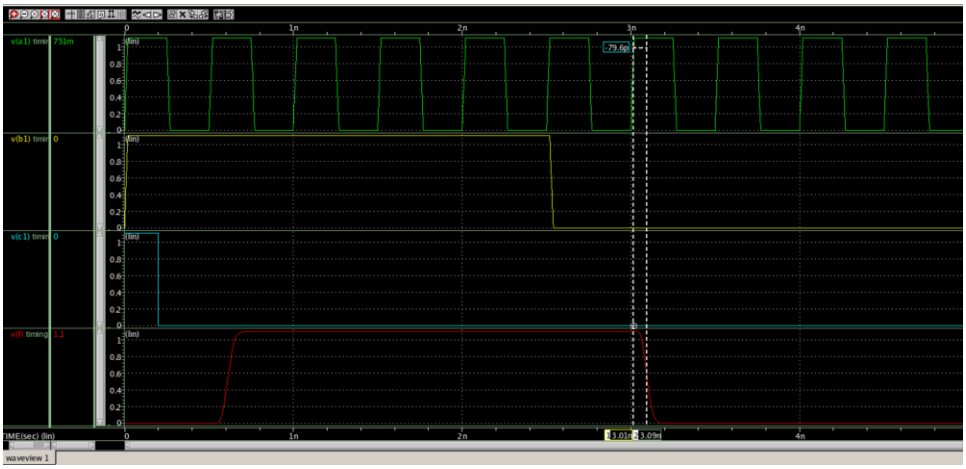
Layout DRC & LVS verification and PEX netlist extraction





DFF Post Layout Simulation



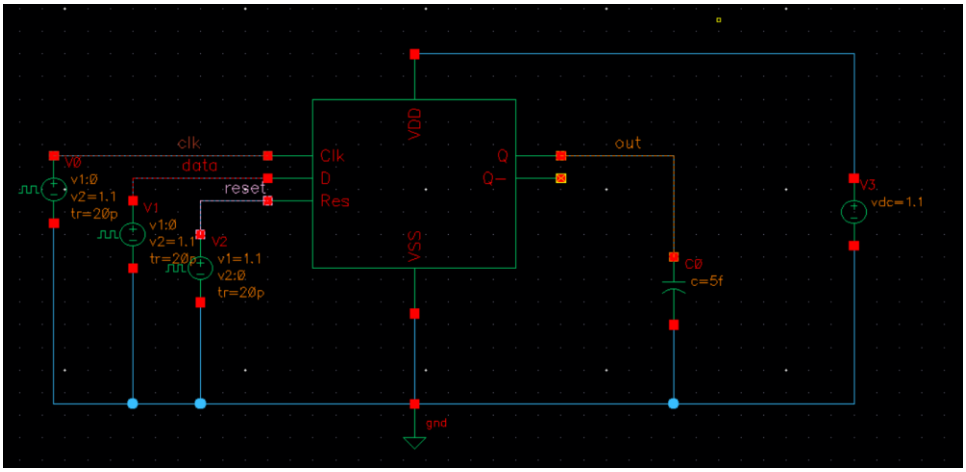


Clock-to-Q delay

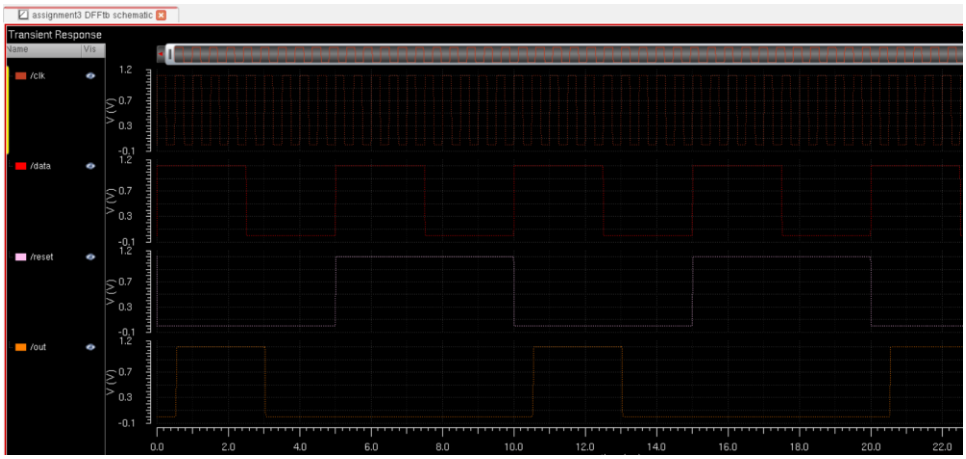
- *latching logic-low = ~79ps*
- *latching logic-high= ~79ps*

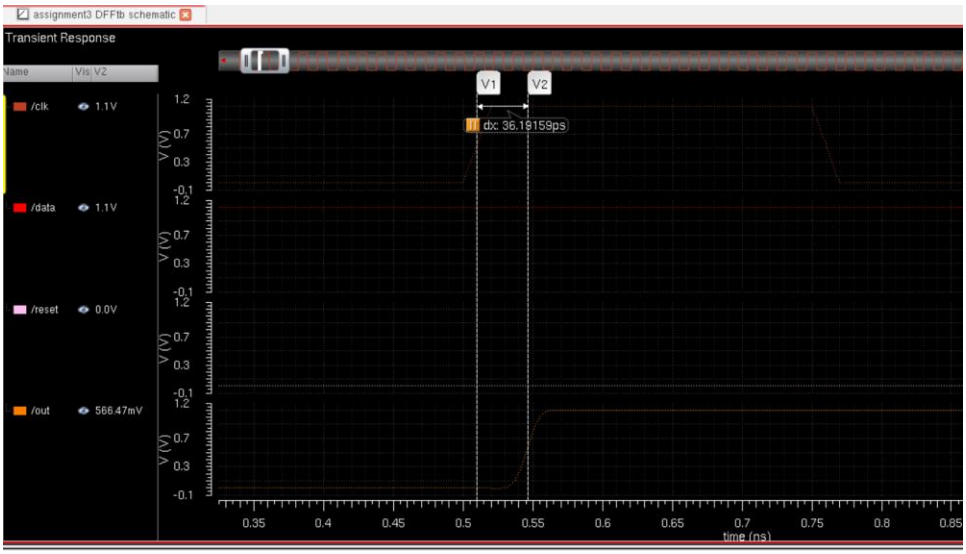
D Flip Flop Working:

DFF Test Bench



Simulation

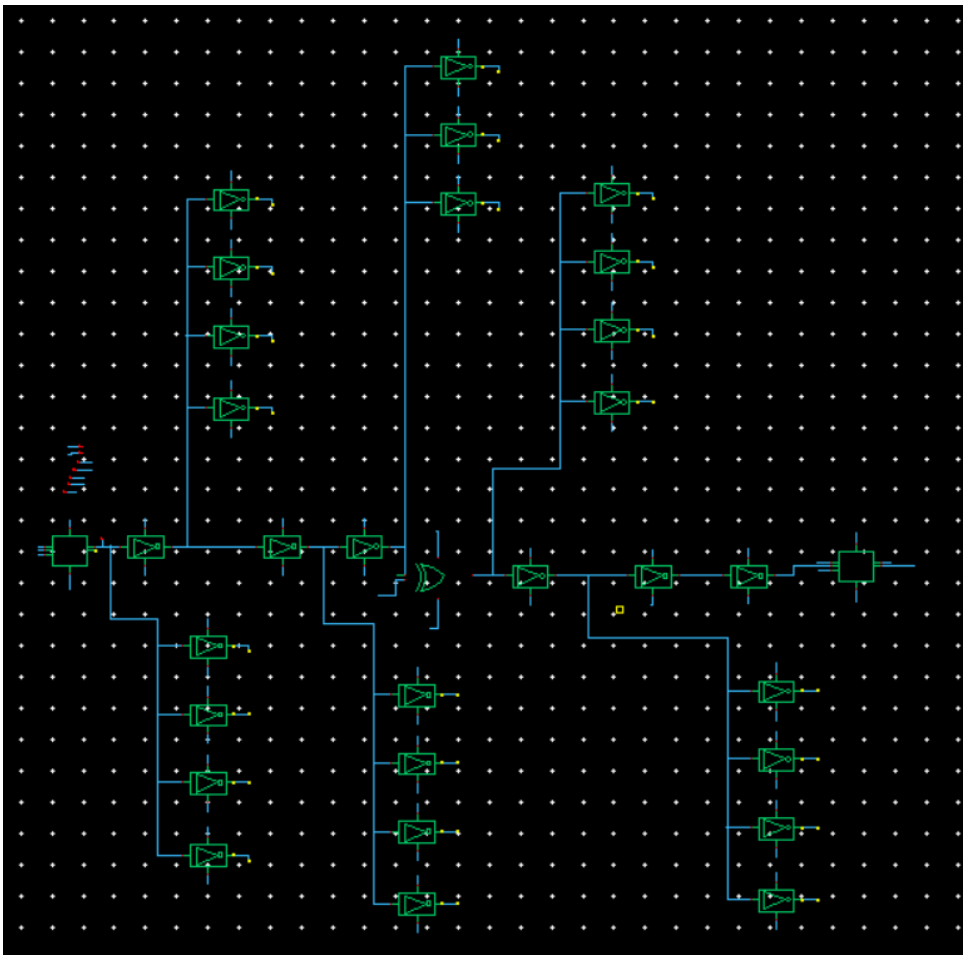




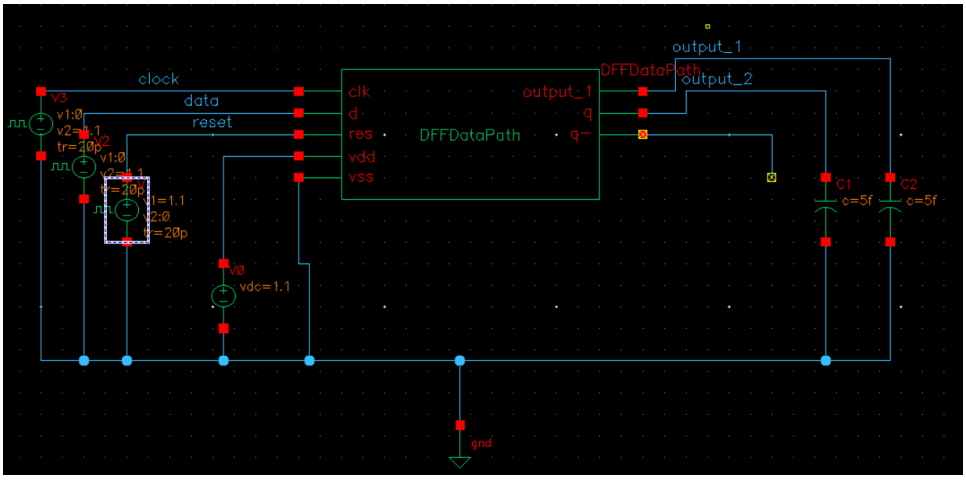
Clock to Output delay at 5fF load = ~36ps

Data Path

Schematic



Simulation



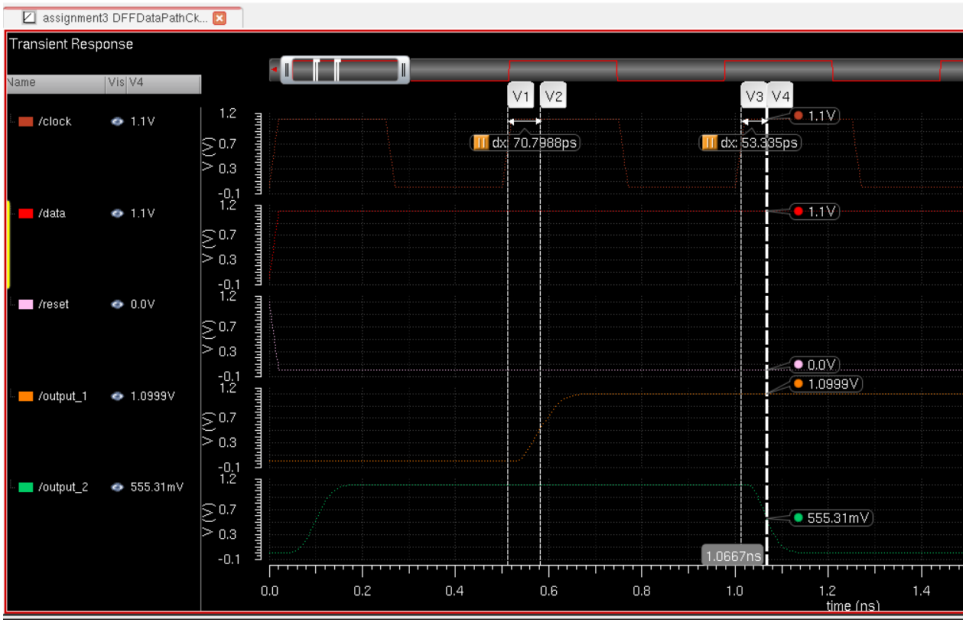
*Input: Clock, Data=1/10 * Clock, Async Reset= 2* Data.*

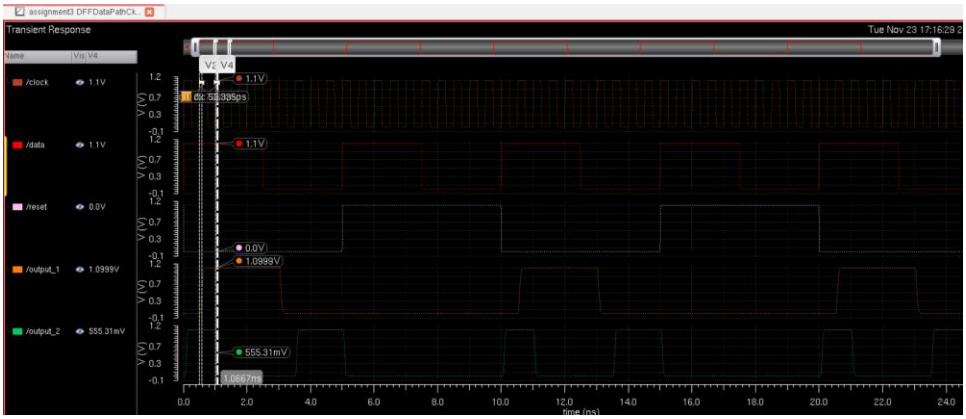
Output: Output_1(Q, from 1st flip-flop in data path), Output_2(Q, from 2nd flip-flop in data path)

Load: 5fF

Analysis Time: 25n for 2Ghz, 10n for others.

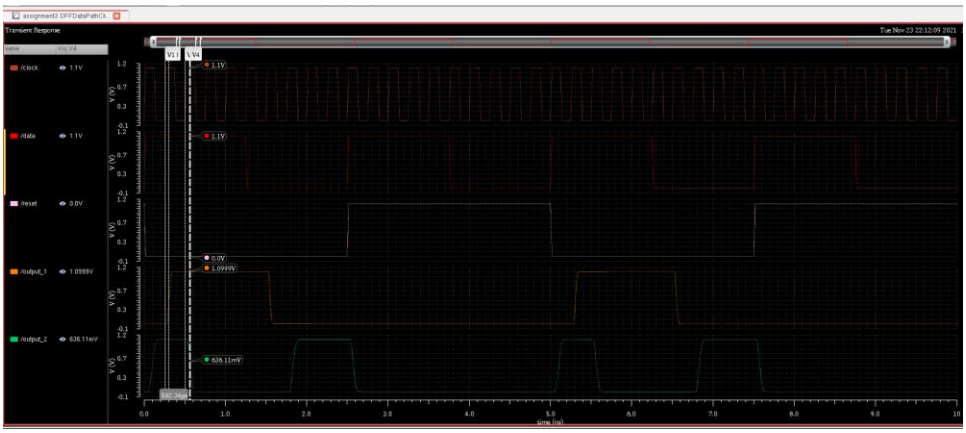
Clock = 2Ghz





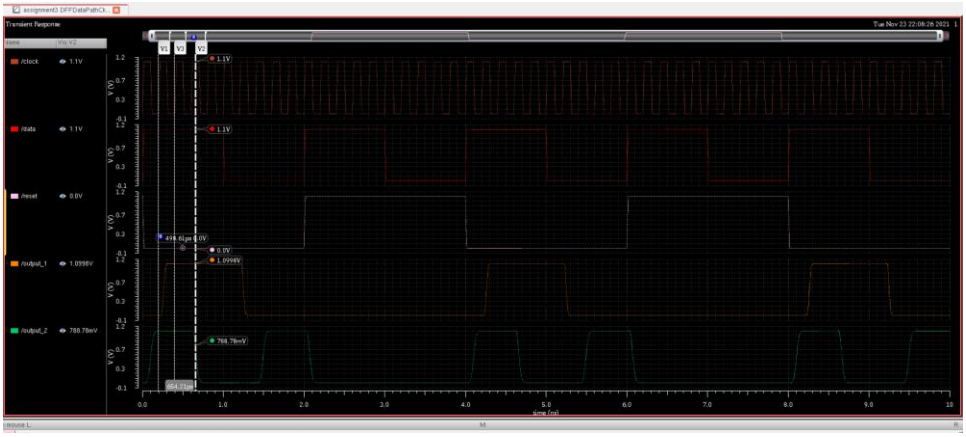
Clock to Output delay @ 2Ghz for latching low = ~70ps and for latching high = ~53.ps

Clock Frequency 4Ghz (Maximum Clock Frequency of Operation)



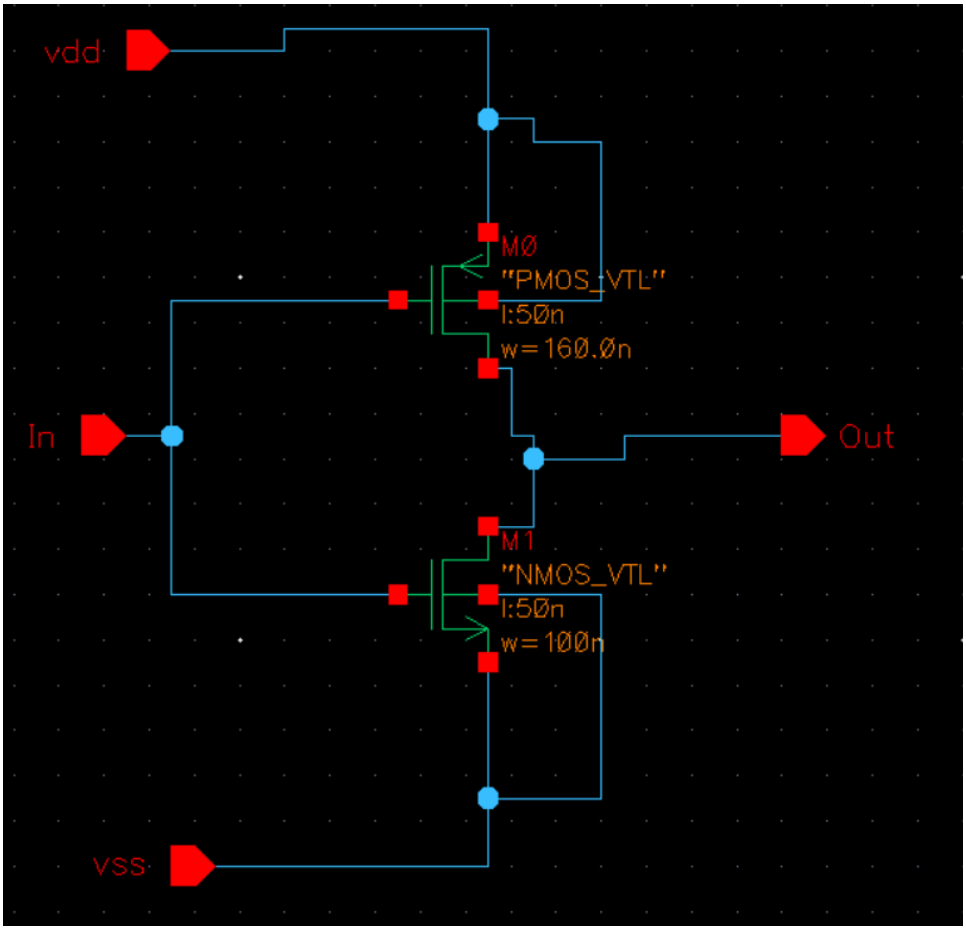
Clock Frequency of failure 5Ghz (*Waveforms showing failure if the maximum frequency is exceeded*

- max delay constraint violation)

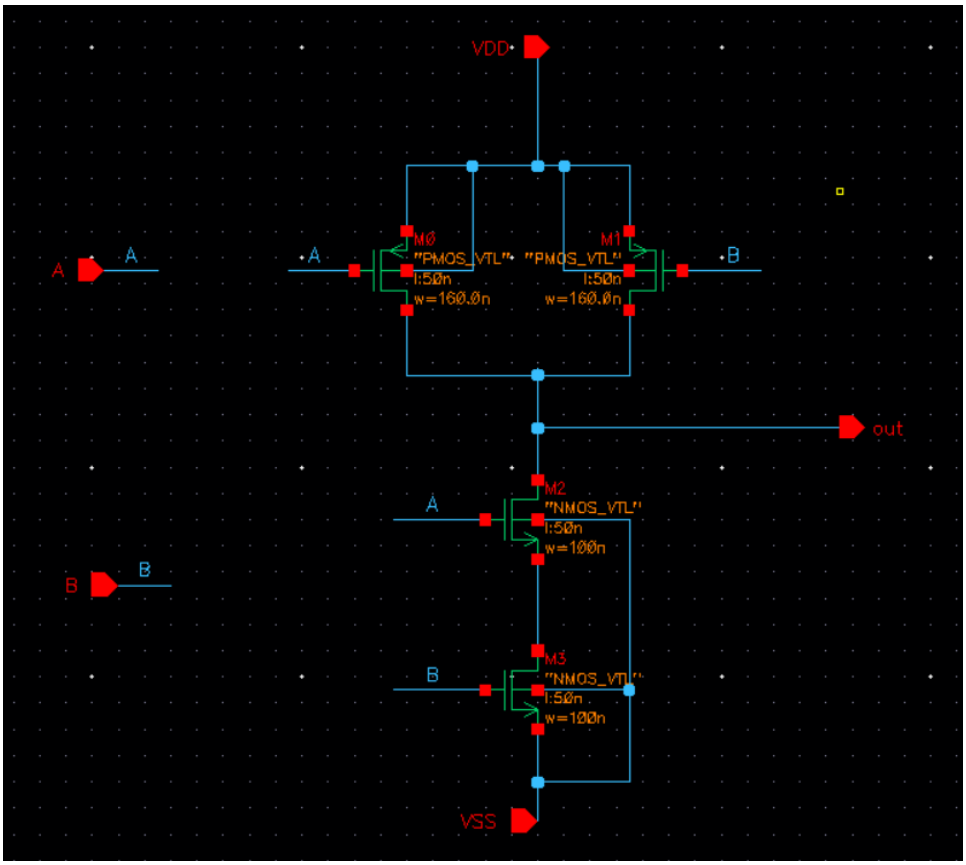


Appendix

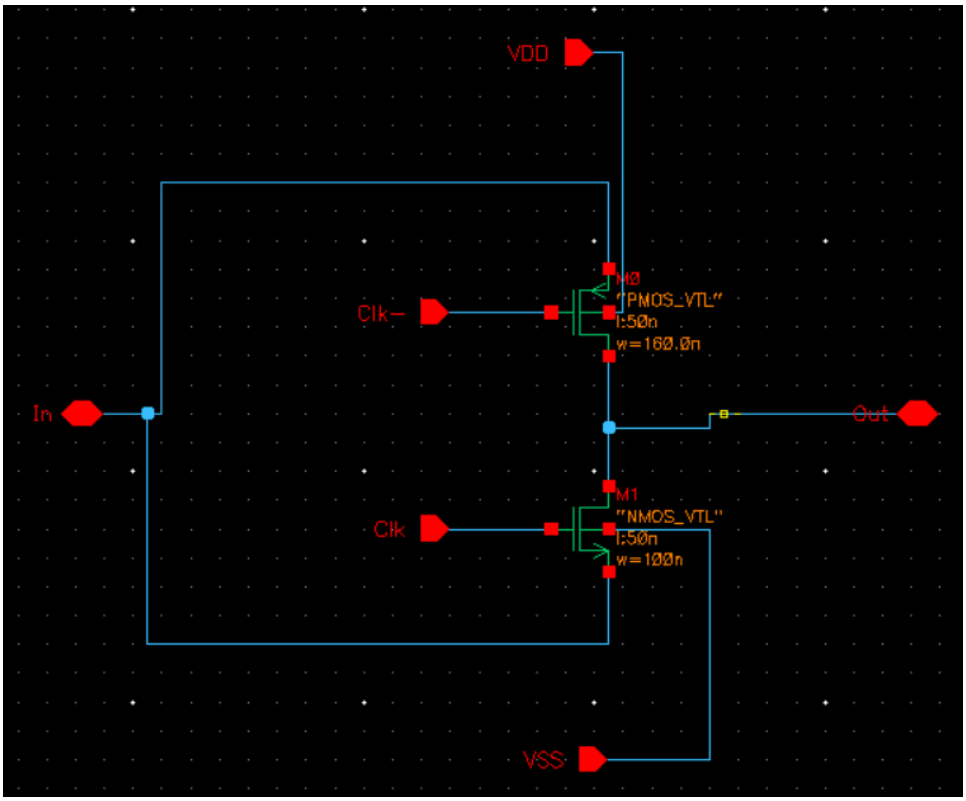
Inverter



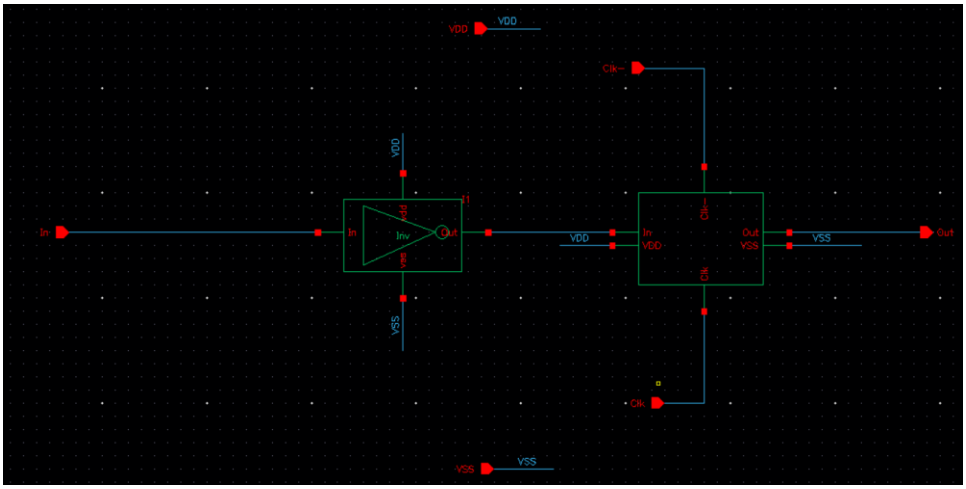
NAND Schematic



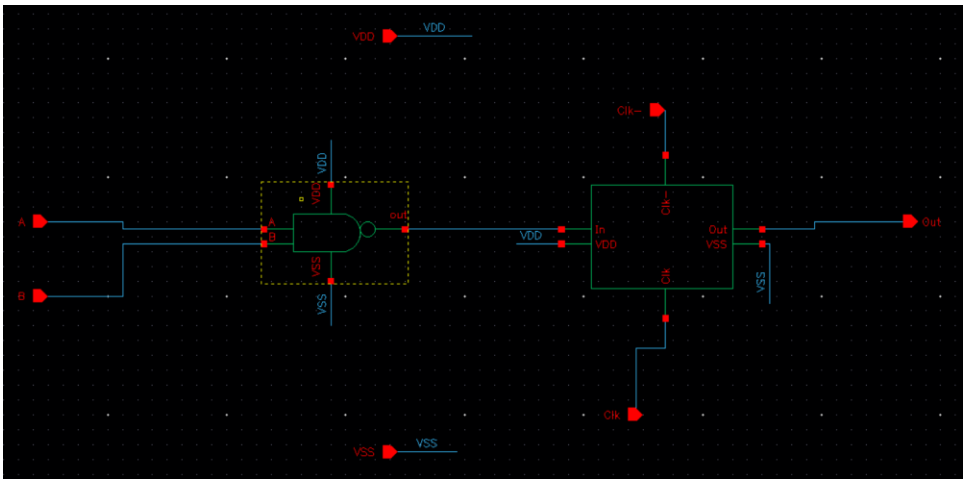
Transmission Gate



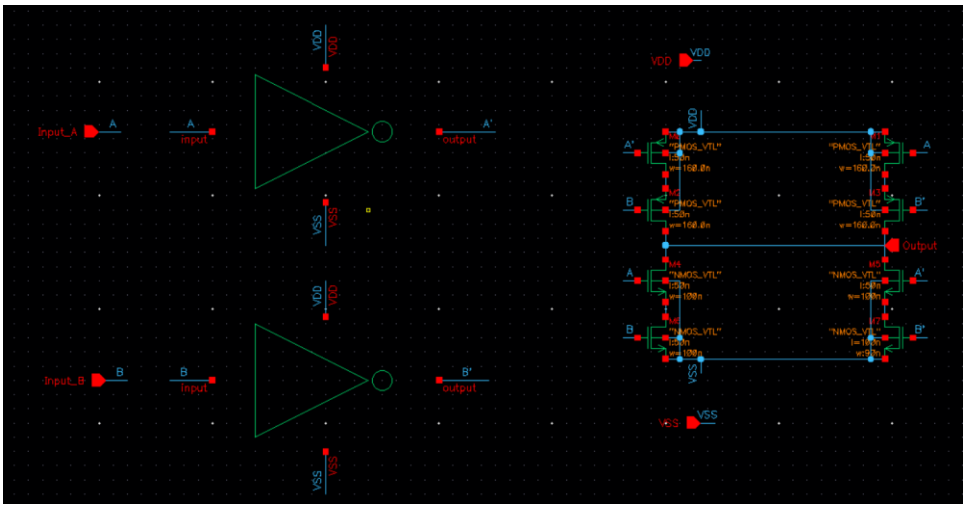
Tristate Inverter



Tristate NAND



XOR



DFF Post Extraction Netlist

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; DESIGN "DFF"

; DATE "Fri Nov 19 15:54:20 2021"

; VENDOR "Mentor Graphics Corp."

; PROGRAM "Calibre xRC v2014.4_28.20"

; CIRCUIT TEMPERATURE 27C

; NOMINAL TEMPERATURE 27C

;



mgc_rve_device_template "PMOS_VTL" "D" "G" "S" "b"
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mgc_rve_device_template "NMOS_VTL" "D" "G" "S" "b"

mgc_rve_device_template "PMOS_VTH" "D" "G" "S" "b"

mgc_rve_device_template "NMOS_VTH" "D" "G" "S" "b"

mgc_rve_device_template "PMOS_VTG" "D" "G" "S" "b"

mgc_rve_device_template "NMOS_VTG" "D" "G" "S" "b"

mgc_rve_device_template "PMOS_THKOX" "D" "G" "S" "b"

mgc_rve_device_template "NMOS_THKOX" "D" "G" "S" "b"

mgc_rve_parasitic_template "c"


mgc_rve_cell_start "DFF" "Q" "Clk" "D" "Res" "VSS" "Q-" "VDD"

mr_pi "NMOS_VTL" "M0" '( "1" "Clk" "VSS" "VSS") '( ("l" 5e-08) ("w" 1e-07) ("ad" 1.2e-14) ("as" 1.2e-14)
("pd" 4.4e-07) ("ps" 4.4e-07) ("lpe" 1) ) '(-0.5825 -3.66)

mr_pi "NMOS_VTL" "M1" '( "2" "1" "VSS" "VSS") '( ("l" 5e-08) ("w" 1e-07) ("ad" 1.2e-14) ("as" 1.2e-14)
("pd" 4.4e-07) ("ps" 4.4e-07) ("lpe" 1) ) '(0.305 -3.66)

mr_pi "NMOS_VTL" "M2" '( "11" "D" "VSS" "VSS") '( ("l" 5e-08) ("w" 1e-07) ("ad" 1.2e-14) ("as" 1.2e-14)
("pd" 4.4e-07) ("ps" 4.4e-07) ("lpe" 1) ) '(1.3125 -3.66)

mr_pi "NMOS_VTL" "M3" '( "13" "11" "VSS" "VSS") '( ("l" 5e-08) ("w" 1e-07) ("ad" 1.2e-14) ("as" 1.2e-14)
("pd" 4.4e-07) ("ps" 4.4e-07) ("lpe" 1) ) '(2.335 -3.66)

mr_pi "NMOS_VTL" "M4" '( "4" "1" "13" "VSS") '( ("l" 5e-08) ("w" 1e-07) ("ad" 1.2e-14) ("as" 1.2e-14)
("pd" 4.4e-07) ("ps" 4.4e-07) ("lpe" 1) ) '(4.0175 -3.6625)

mr_pi "NMOS_VTL" "M5" '( "3" "Res" "VSS" "VSS") '( ("l" 5e-08) ("w" 1e-07) ("ad" 1.2e-14) ("as" 1.2e-14)
("pd" 4.4e-07) ("ps" 4.4e-07) ("lpe" 1) ) '(4.1175 -6.8975)

mr_pi "NMOS_VTL" "M6" '( "14" "4" "VSS" "VSS") '( ("l" 5e-08) ("w" 1e-07) ("ad" 1.2e-14) ("as" 1.2e-14)
("pd" 4.4e-07) ("ps" 4.4e-07) ("lpe" 1) ) '(5.4325 -3.6675)

mr_pi "NMOS_VTL" "M7" '( "15" "1" "4" "VSS") '( ("l" 5e-08) ("w" 1e-07) ("ad" 1.2e-14) ("as" 1.2e-14)
("pd" 4.4e-07) ("ps" 4.4e-07) ("lpe" 1) ) '(5.5375 -6.885)

mr_pi "NMOS_VTL" "M8" '( "5" "3" "14" "VSS") '( ("l" 5e-08) ("w" 1e-07) ("ad" 1.2e-14) ("as" 1.2e-14)
("pd" 4.4e-07) ("ps" 4.4e-07) ("lpe" 1) ) '(6.0425 -3.6675)

mr_pi "NMOS_VTL" "M9" '( "15" "5" "VSS" "VSS") '( ("l" 5e-08) ("w" 1e-07) ("ad" 1.2e-14) ("as" 1.2e-14)
("pd" 4.4e-07) ("ps" 4.4e-07) ("lpe" 1) ) '(6.9675 -6.8975)

mr_pi "NMOS_VTL" "M10" '( "6" "2" "5" "VSS") '( ("l" 5e-08) ("w" 1e-07) ("ad" 1.2e-14) ("as" 1.2e-14)
("pd" 4.4e-07) ("ps" 4.4e-07) ("lpe" 1) ) '(7.6125 -3.6625)

mr_pi "NMOS_VTL" "M11" '( "17" "1" "6" "VSS") '( ("l" 5e-08) ("w" 1e-07) ("ad" 1.2e-14) ("as" 1.2e-14)
("pd" 4.4e-07) ("ps" 4.4e-07) ("lpe" 1) ) '(8.42 -6.885)

mr_pi "NMOS_VTL" "M12" '( "Q" "6" "VSS" "VSS") '( ("l" 5e-08) ("w" 1e-07) ("ad" 1.2e-14) ("as" 1.2e-14)
("pd" 4.4e-07) ("ps" 4.4e-07) ("lpe" 1) ) '(9.31 -3.6625)

mr_pi "NMOS_VTL" "M13" '( "16" "8" "VSS" "VSS") '( ("l" 5e-08) ("w" 1e-07) ("ad" 1.2e-14) ("as" 1.2e-14)
("pd" 4.4e-07) ("ps" 4.4e-07) ("lpe" 1) ) '(10.035 -6.8925)

mr_pi "NMOS_VTL" "M14" '( "8" "6" "VSS" "VSS") '( ("l" 5e-08) ("w" 1e-07) ("ad" 1.2e-14) ("as" 1.2e-14)
("pd" 4.4e-07) ("ps" 4.4e-07) ("lpe" 1) ) '(10.58 -3.6625)

mr_pi "NMOS_VTL" "M15" '( "17" "3" "16" "VSS") '( ("l" 5e-08) ("w" 1e-07) ("ad" 1.2e-14) ("as" 1.2e-14)
("pd" 4.4e-07) ("ps" 4.4e-07) ("lpe" 1) ) '(10.645 -6.8925)
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("pd" 4.4e-07) ("ps" 4.4e-07) ("lpe" 1) ) '(11.77 -3.6625)

mr_pi "PMOS_VTL" "M17" '( "1" "Clk" "VDD" "VDD") '( ("l" 5e-08) ("w" 1.6e-07) ("ad" 1.92e-14) ("as" 1.92e-
14) ("pd" 5.6e-07) ("ps" 5.6e-07) ("lpe" 1) ) '(-0.5825 -2.57)

mr_pi "PMOS_VTL" "M18" '( "2" "1" "VDD" "VDD") '( ("l" 5e-08) ("w" 1.6e-07) ("ad" 1.92e-14) ("as" 1.92e-
14) ("pd" 5.6e-07) ("ps" 5.6e-07) ("lpe" 1) ) '(0.305 -2.57)

mr_pi "PMOS_VTL" "M19" '( "11" "D" "VDD" "VDD") '( ("l" 5e-08) ("w" 1.6e-07) ("ad" 1.92e-14) ("as" 1.92e-
14) ("pd" 5.6e-07) ("ps" 5.6e-07) ("lpe" 1) ) '(1.3125 -2.57)

mr_pi "PMOS_VTL" "M20" '( "13" "11" "VDD" "VDD") '( ("l" 5e-08) ("w" 1.6e-07) ("ad" 1.92e-14) ("as" 1.92e-
14) ("pd" 5.6e-07) ("ps" 5.6e-07) ("lpe" 1) ) '(2.335 -2.57)

mr_pi "PMOS_VTL" "M21" '( "4" "2" "13" "VDD") '( ("l" 5e-08) ("w" 1.6e-07) ("ad" 1.92e-14) ("as" 1.92e-14)
("pd" 5.6e-07) ("ps" 5.6e-07) ("lpe" 1) ) '(4.0175 -2.5725)

mr_pi "PMOS_VTL" "M22" '( "3" "Res" "VDD" "VDD") '( ("l" 5e-08) ("w" 1.6e-07) ("ad" 1.92e-14) ("as" 1.92e-
14) ("pd" 5.6e-07) ("ps" 5.6e-07) ("lpe" 1) ) '(4.1175 -5.7425)

mr_pi "PMOS_VTL" "M23" '( "5" "4" "VDD" "VDD") '( ("l" 5e-08) ("w" 1.6e-07) ("ad" 1.92e-14) ("as" 1.92e-
14) ("pd" 5.6e-07) ("ps" 5.6e-07) ("lpe" 1) ) '(5.4325 -2.5775)

mr_pi "PMOS_VTL" "M24" '( "15" "2" "4" "VDD") '( ("l" 5e-08) ("w" 1.6e-07) ("ad" 1.92e-14) ("as" 1.92e-14)
("pd" 5.6e-07) ("ps" 5.6e-07) ("lpe" 1) ) '(5.5375 -5.73)

mr_pi "PMOS_VTL" "M25" '( "5" "3" "VDD" "VDD") '( ("l" 5e-08) ("w" 1.6e-07) ("ad" 1.92e-14) ("as" 1.92e-
14) ("pd" 5.6e-07) ("ps" 5.6e-07) ("lpe" 1) ) '(6.0425 -2.5775)

mr_pi "PMOS_VTL" "M26" '( "15" "5" "VDD" "VDD") '( ("l" 5e-08) ("w" 1.6e-07) ("ad" 1.92e-14) ("as" 1.92e-
14) ("pd" 5.6e-07) ("ps" 5.6e-07) ("lpe" 1) ) '(6.9675 -5.7425)

mr_pi "PMOS_VTL" "M27" '( "6" "1" "5" "VDD") '( ("l" 5e-08) ("w" 1.6e-07) ("ad" 1.92e-14) ("as" 1.92e-14)
("pd" 5.6e-07) ("ps" 5.6e-07) ("lpe" 1) ) '(7.6125 -2.5725)

mr_pi "PMOS_VTL" "M28" '( "17" "2" "6" "VDD") '( ("l" 5e-08) ("w" 1.6e-07) ("ad" 1.92e-14) ("as" 1.92e-14)
("pd" 5.6e-07) ("ps" 5.6e-07) ("lpe" 1) ) '(8.42 -5.73)

mr_pi "PMOS_VTL" "M29" '( "Q" "6" "VDD" "VDD") '( ("l" 5e-08) ("w" 1.6e-07) ("ad" 1.92e-14) ("as" 1.92e-
14) ("pd" 5.6e-07) ("ps" 5.6e-07) ("lpe" 1) ) '(9.31 -2.5725)

mr_pi "PMOS_VTL" "M30" '( "17" "8" "VDD" "VDD") '( ("l" 5e-08) ("w" 1.6e-07) ("ad" 1.92e-14) ("as" 1.92e-
14) ("pd" 5.6e-07) ("ps" 5.6e-07) ("lpe" 1) ) '(10.035 -5.7375)

mr_pi "PMOS_VTL" "M31" '( "8" "6" "VDD" "VDD") '( ("l" 5e-08) ("w" 1.6e-07) ("ad" 1.92e-14) ("as" 1.92e-
14) ("pd" 5.6e-07) ("ps" 5.6e-07) ("lpe" 1) ) '(10.58 -2.5725)

mr_pi "PMOS_VTL" "M32" '( "17" "3" "VDD" "VDD") '( ("l" 5e-08) ("w" 1.6e-07) ("ad" 1.92e-14) ("as" 1.92e-
14) ("pd" 5.6e-07) ("ps" 5.6e-07) ("lpe" 1) ) '(10.645 -5.7375)

mr_pi "PMOS_VTL" "M33" '( "Q-" "Q" "VDD" "VDD") '( ("l" 5e-08) ("w" 1.6e-07) ("ad" 1.92e-14) ("as" 1.92e-
14) ("pd" 5.6e-07) ("ps" 5.6e-07) ("lpe" 1) ) '(11.77 -2.5725)

mr_pp 'c "c_15" '("1" "0") 1.45486f

mr_pp 'c "c_29" '("2" "0") 0.896487f

mr_pp 'c "c_43" '("3" "0") 0.717847f

mr_pp 'c "c_53" '("4" "0") 0.409943f

mr_pp 'c "c_63" '("5" "0") 0.432322f

mr_pp 'c "c_74" '("6" "0") 0.647828f

mr_pp 'c "c_80" '("Q" "0") 0.274777f

mr_pp 'c "c_89" '("8" "0") 0.344307f
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```
mr_pp 'c "c_93" '("Clk" "0") 0.127004f
mr_pp 'c "c_99" '("D" "0") 0.123218f
mr_pp 'c "c_106" '("11" "0") 0.194212f
mr_pp 'c "c_111" '("Res" "0") 0.130848f
mr_pp 'c "c_118" '("13" "0") 0.155021f
mr_pp 'c "c_124" '("14" "0") 0.0262129f
mr_pp 'c "c_133" '("15" "0") 0.13715f
mr_pp 'c "c_138" '("16" "0") 0.030296f
mr_pp 'c "c_147" '("17" "0") 0.216275f
mr_pp 'c "c_167" '("VSS" "0") 1.48851f
mr_pp 'c "c_172" '("Q-" "0") 0.0512863f
mr_pp 'c "c_190" '("VDD" "0") 1.52598f

mr_ni "1" 0 1.45486e-15 8.4165e-16 '( "M0_d" "M17_d" "M11_g" "M18_g" "M1_g" "M27_g" "M4_g" "M7_g" )

mr_ni "2" 0 8.96487e-16 7.43071e-16 '( "M18_d" "M1_d" "M10_g" "M21_g" "M24_g" "M28_g" )

mr_ni "3" 0 7.17847e-16 7.93396e-16 '( "M22_d" "M5_d" "M15_g" "M25_g" "M32_g" "M8_g" )

mr_ni "4" 0 4.09943e-16 5.48802e-16 '( "M21_d" "M4_d" "M23_g" "M6_g" "M24_s" "M7_s" )

mr_ni "5" 0 4.32322e-16 7.19965e-16 '( "M23_d" "M25_d" "M8_d" "M26_g" "M9_g" "M10_s" "M27_s" )

mr_ni "6" 0 6.47828e-16 6.31438e-16 '( "M10_d" "M27_d" "M12_g" "M14_g" "M29_g" "M31_g" "M11_s" "M28_s" )

mr_ni "Q" 0 2.74777e-16 2.65503e-16 '( "M12_d" "M29_d" "M16_g" "M33_g" )

mr_ni "8" 0 3.44307e-16 4.8763e-16 '( "M14_d" "M31_d" "M13_g" "M30_g" )

mr_ni "Clk" 0 1.27004e-16 8.60344e-17 '( "M0_g" "M17_g" )

mr_ni "D" 0 1.23218e-16 9.85828e-17 '( "M19_g" "M2_g" )

mr_ni "11" 0 1.94212e-16 2.31832e-16 '( "M19_d" "M2_d" "M20_g" "M3_g" )

mr_ni "Res" 0 1.30848e-16 8.66606e-17 '( "M22_g" "M5_g" )
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mr_ni "13" 0 1.55021e-16 3.69349e-16 '( "M20_d" "M3_d" "M21_s" "M4_s" )


mr_ni "14" 0 2.62129e-17 1.19966e-16 '( "M6_d" "M8_s" )


mr_ni "15" 0 1.3715e-16 4.83737e-16 '( "M24_d" "M26_d" "M7_d" "M9_d" )


mr_ni "16" 0 3.0296e-17 1.94151e-16 '( "M13_d" "M15_s" )


mr_ni "17" 0 2.16275e-16 5.42936e-16 '( "M11_d" "M15_d" "M28_d" "M30_d" "M32_d" )


mr_ni "VSS" 0 1.48851e-15 9.9875e-16 '( "M0_b" "M10_b" "M11_b" "M12_b" "M13_b" "M14_b" "M15_b" "M16_b"
"M1_b" "M2_b" "M3_b" "M4_b" "M5_b" "M6_b" "M7_b" "M8_b" "M9_b" "M0_s" "M12_s" "M13_s" "M14_s" "M16_s"
"M1_s" "M2_s" "M3_s" "M5_s" "M6_s" "M9_s" )


mr_ni "Q-" 0 5.12863e-17 1.22813e-16 '( "M16_d" "M33_d" )


mr_ni "VDD" 0 1.52598e-15 1.55749e-15 '( "M17_b" "M18_b" "M19_b" "M20_b" "M21_b" "M22_b" "M23_b" "M24_b"
"M25_b" "M26_b" "M27_b" "M28_b" "M29_b" "M30_b" "M31_b" "M32_b" "M33_b" "M17_s" "M18_s" "M19_s" "M20_s"
"M22_s" "M23_s" "M25_s" "M26_s" "M29_s" "M30_s" "M31_s" "M32_s" "M33_s" )

mr_pp 'c "cc_1" '("1" "2") 0.0944472f

mr_pp 'c "cc_2" '("1" "3") 0.081034f

mr_pp 'c "cc_3" '("1" "4") 0.022948f

mr_pp 'c "cc_4" '("1" "5") 0.00846422f

mr_pp 'c "cc_5" '("1" "6") 0.0106405f

mr_pp 'c "cc_6" '("1" "Clk") 0.0529978f

mr_pp 'c "cc_7" '("1" "D") 0.0062527f

mr_pp 'c "cc_8" '("1" "11") 0.0142488f

mr_pp 'c "cc_9" '("1" "Res") 0.00634216f

mr_pp 'c "cc_10" '("1" "13") 0.0331385f

mr_pp 'c "cc_11" '("1" "15") 0.0233248f

mr_pp 'c "cc_12" '("1" "17") 0.00518841f

mr_pp 'c "cc_13" '("1" "VSS") 0.256344f

mr_pp 'c "cc_14" '("1" "VDD") 0.226279f

mr_pp 'c "cc_15" '("2" "3") 0.132855f

mr_pp 'c "cc_16" '("2" "4") 0.0822836f

mr_pp 'c "cc_17" '("2" "5") 0.0625091f

mr_pp 'c "cc_18" '("2" "6") 0.0398841f
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mr_pp 'c "cc_19" '("2" "D") 0.0116471f
mr_pp 'c "cc_20" '("2" "11") 0.0231992f
mr_pp 'c "cc_21" '("2" "13") 0.0539008f
mr_pp 'c "cc_22" '("2" "14") 0.00464732f
mr_pp 'c "cc_23" '("2" "15") 0.0648656f
mr_pp 'c "cc_24" '("2" "17") 0.00551412f
mr_pp 'c "cc_25" '("2" "VSS") 0.06423f
mr_pp 'c "cc_26" '("2" "VDD") 0.103088f
mr_pp 'c "cc_27" '("3" "4") 0.0236991f
mr_pp 'c "cc_28" '("3" "5") 0.11446f
mr_pp 'c "cc_29" '("3" "6") 0.00997633f
mr_pp 'c "cc_30" '("3" "8") 0.0124708f
mr_pp 'c "cc_31" '("3" "Res") 0.0468965f
mr_pp 'c "cc_32" '("3" "14") 0.0190166f
mr_pp 'c "cc_33" '("3" "15") 0.016254f
mr_pp 'c "cc_34" '("3" "16") 0.0965151f
mr_pp 'c "cc_35" '("3" "17") 0.101266f
mr_pp 'c "cc_36" '("3" "VSS") 0.0804548f
mr_pp 'c "cc_37" '("3" "VDD") 0.0584969f
mr_pp 'c "cc_38" '("4" "5") 0.0318866f
mr_pp 'c "cc_39" '("4" "13") 0.0849844f
mr_pp 'c "cc_40" '("4" "14") 0.00881291f
mr_pp 'c "cc_41" '("4" "15") 0.106439f
mr_pp 'c "cc_42" '("4" "VSS") 0.0607003f
mr_pp 'c "cc_43" '("4" "VDD") 0.127048f
mr_pp 'c "cc_44" '("5" "6") 0.0843873f
mr_pp 'c "cc_45" '("5" "14") 0.0219361f
mr_pp 'c "cc_46" '("5" "15") 0.147654f
mr_pp 'c "cc_47" '("5" "VSS") 0.0579175f
mr_pp 'c "cc_48" '("5" "VDD") 0.19075f
mr_pp 'c "cc_49" '("6" "Q") 0.106296f
mr_pp 'c "cc_50" '("6" "8") 0.0489639f
mr_pp 'c "cc_51" '("6" "15") 0.00518068f
mr_pp 'c "cc_52" '("6" "17") 0.0943822f
mr_pp 'c "cc_53" '("6" "VSS") 0.0741088f
mr_pp 'c "cc_54" '("6" "VDD") 0.157618f
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```
mr_pp 'c "cc_55" '("Q" "8") 0.0098328f
mr_pp 'c "cc_56" '("Q" "VSS") 0.0304838f
mr_pp 'c "cc_57" '("Q" "Q-") 0.0480251f
mr_pp 'c "cc_58" '("Q" "VDD") 0.0708653f
mr_pp 'c "cc_59" '("8" "16") 0.00824292f
mr_pp 'c "cc_60" '("8" "17") 0.197771f
mr_pp 'c "cc_61" '("8" "VSS") 0.0440362f
mr_pp 'c "cc_62" '("8" "Q-") 0.00334068f
mr_pp 'c "cc_63" '("8" "VDD") 0.162971f
mr_pp 'c "cc_64" '("Clk" "VSS") 0.00619429f
mr_pp 'c "cc_65" '("Clk" "VDD") 0.0268423f
mr_pp 'c "cc_66" '("D" "11") 0.0470787f
mr_pp 'c "cc_67" '("D" "VSS") 0.00622779f
mr_pp 'c "cc_68" '("D" "VDD") 0.0273764f
mr_pp 'c "cc_69" '("11" "13") 0.0533944f
mr_pp 'c "cc_70" '("11" "VSS") 0.0303642f
mr_pp 'c "cc_71" '("11" "VDD") 0.063547f
mr_pp 'c "cc_72" '("Res" "VSS") 0.00668547f
mr_pp 'c "cc_73" '("Res" "VDD") 0.0267365f
mr_pp 'c "cc_74" '("13" "VSS") 0.0538571f
mr_pp 'c "cc_75" '("13" "VDD") 0.0900742f
mr_pp 'c "cc_76" '("14" "VSS") 0.0655529f
mr_pp 'c "cc_77" '("15" "VSS") 0.0410858f
mr_pp 'c "cc_78" '("15" "VDD") 0.0789329f
mr_pp 'c "cc_79" '("16" "17") 0.0220546f
mr_pp 'c "cc_80" '("16" "VSS") 0.0673386f
mr_pp 'c "cc_81" '("17" "VSS") 0.0262769f
mr_pp 'c "cc_82" '("17" "VDD") 0.0904822f
mr_pp 'c "cc_83" '("VSS" "Q-") 0.0209771f
mr_pp 'c "cc_84" '("VSS" "VDD") 0.00591489f
mr_pp 'c "cc_85" '("Q-" "VDD") 0.0504698f
mgc_rve_cell_end
```