

ESE555 VLSI Design

CAD Assignment 1

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Q1.

VLSI

Q1 $(W/L)_n = 100n/50n$
 $(W/L)_p = 200n/50n$

$(V_{th})_n = 0.4106V$

$(V_{th})_p = -0.3892V$

$\mu_n = 270 \text{ cm}^2/V\cdot\text{s}$

$\mu_p = 70 \text{ cm}^2/V\cdot\text{s}$

$\epsilon_{ox} = 3.97 \times \epsilon_0$

$\epsilon_0 = 8.85 \times 10^{-12} \text{ (F/m)}$

$T_{ox, nmos} = 1.14 \times 10^{-9} \text{ (m)}$

$T_{ox, pmos} = 1.26 \times 10^{-9} \text{ (m)}$

Inverter drives capacitive load $2FF$ (C_{load})

Calculate - low-to-high propagation delay
 high-to-low

Nominal Power Supply = $1V$; Input is step function

High to low Propagation delay

$$T_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{th,n})} \left[\frac{2V_{th,n}}{V_{DD} - V_{th,n}} + \ln \left(\frac{4(V_{DD} - V_{th,n})}{V_{DD}} \right) \right]$$

$C_{ox,n} = \frac{\epsilon_{ox}}{T_{ox,n}}$

$= \frac{3.97 \times 8.85 \times 10^{-12}}{1.14 \times 10^{-9} \text{ (m)}}$

$C_{ox,n} = 35.1345 \times 10^{-3} / 1.14$

$C_{ox, nmos} = 3.08197 \times 10^{-2} \text{ F}$

$$k_n = \mu_n C_{ox} \left(\frac{W_n}{L_n} \right)$$

$$= 0.027 \times \cancel{3.08197} \times 10^{-2} \times \frac{150 \times 10^{-9}}{50 \times 10^{-9}}$$

$$k_n = 1.66 \times 10^{-3}$$

$$T_{PHL} = \frac{C_{load}}{(1.66 \times 10^{-3}) (1 - 0.4106)} \left[\frac{2 \times 0.4106}{(1 - 0.4106)} + \ln \left(\frac{4(1 - 0.4106)}{1} - 1 \right) \right]$$

$$= \frac{2 \times 10^{-15}}{9.784 \times 10^{-4}} [1.3932 + 0.3057]$$

$$T_{PHL} = 3.472 \times 10^{-12} \text{ s} = 3.472 \text{ ps}$$

Low to high.

$$t_{PLH} = \frac{C_{load}}{k_p (V_{DD} - |V_{THP}|)} \left[\frac{2|V_{THP}|}{V_{DD} - |V_{THP}|} + \ln \left[\frac{4(V_{DD} - |V_{THP}|)}{V_{DD}} - 1 \right] \right]$$

$$C_{ox} = \frac{3.97 \times 8.85 \times 10^{-12}}{1.26 \times 10^{-9}} = 2.78 \times 10^{-2} \quad // \quad C_{ox} = \frac{\epsilon_{ox}}{T_{ox/p}}$$

$$k_p = \mu_p C_{ox} \left(\frac{W_p}{L_p} \right) = 2.78 \times 10^{-2} \times 7 \times 10^{-3} \times 4$$

$$= 7.784 \times 10^{-4}$$

$$T_{PLH} = \frac{2 \times 10^{-15}}{7.784 \times 10^{-4} (1 - 0.3842)} \left[\frac{2(0.3842)}{(1 - 0.3842)} + \ln \left(\frac{4(1 - 0.3842)}{1} - 1 \right) \right]$$

$$= 4.17456 \times 10^{-12} [1.2478 + \ln(1.4832)]$$

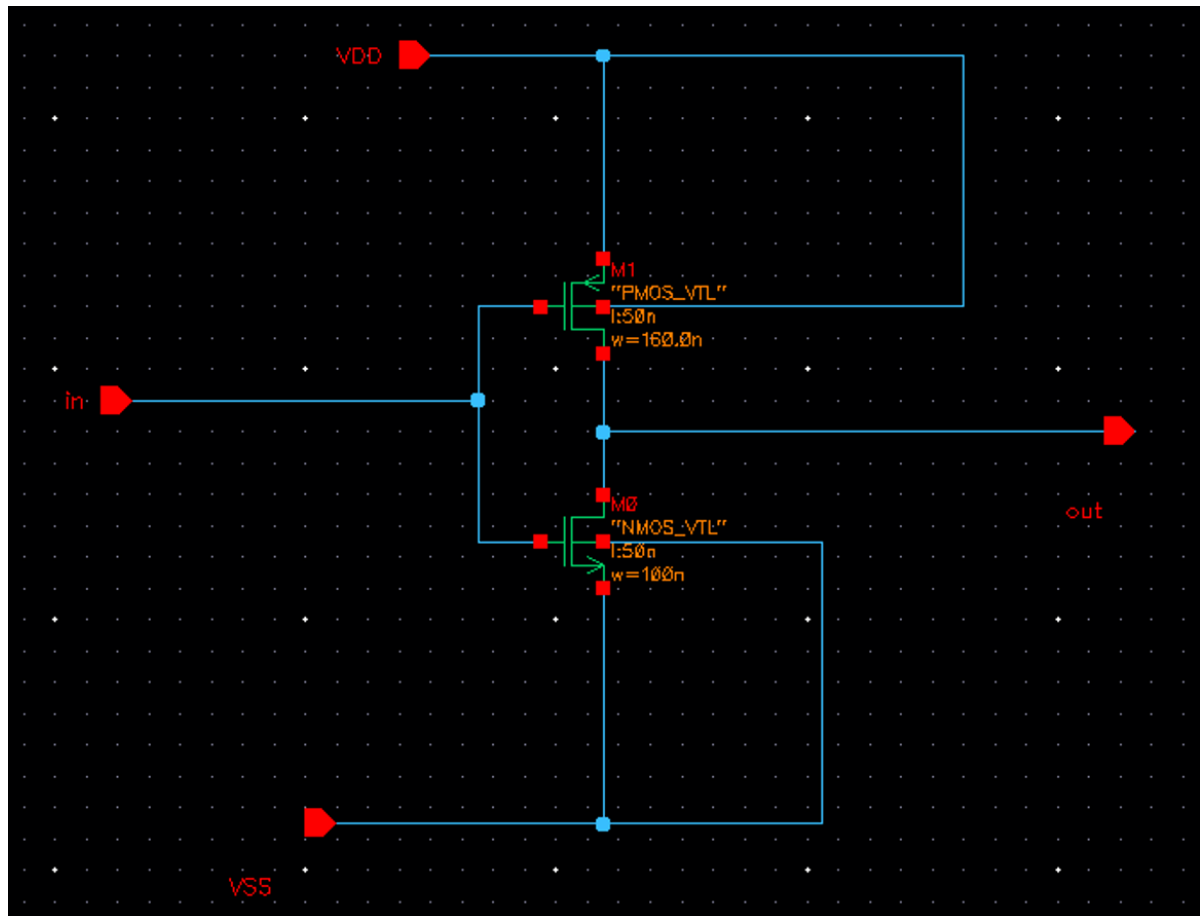
$$= 6.797 \text{ ps}$$

High to Low Propagation Delay: 3.472 ps

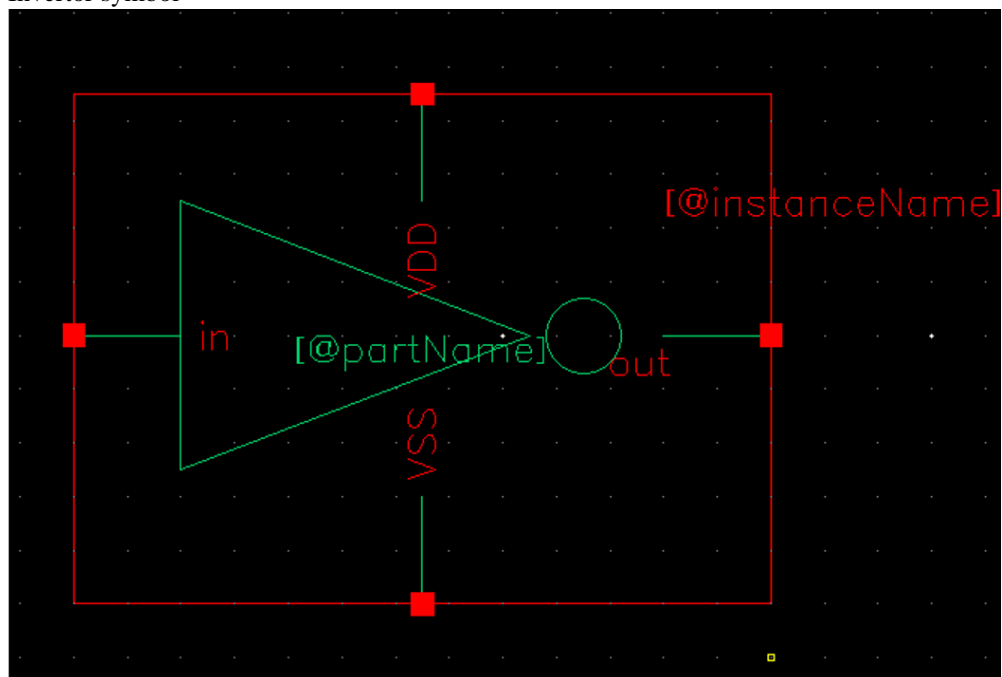
Low to High Propagation Delay: 6.797 ps

Q 2.

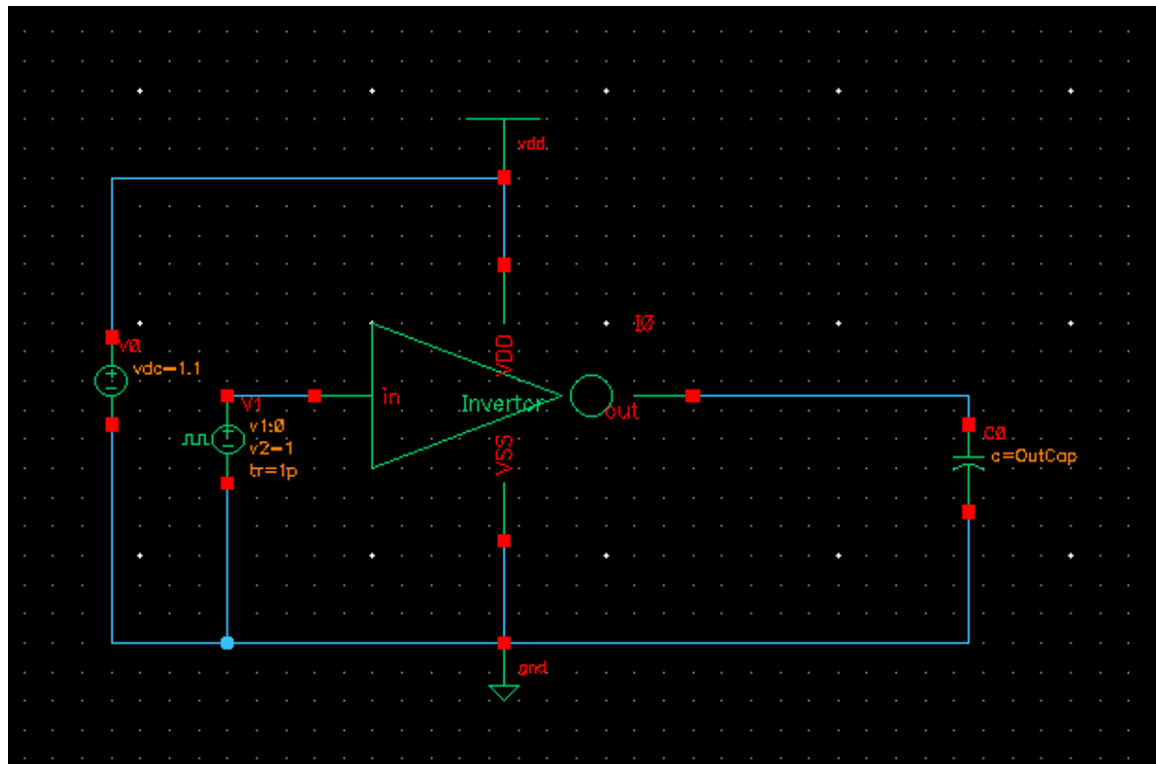
Inverter Schematic view



Invertor symbol

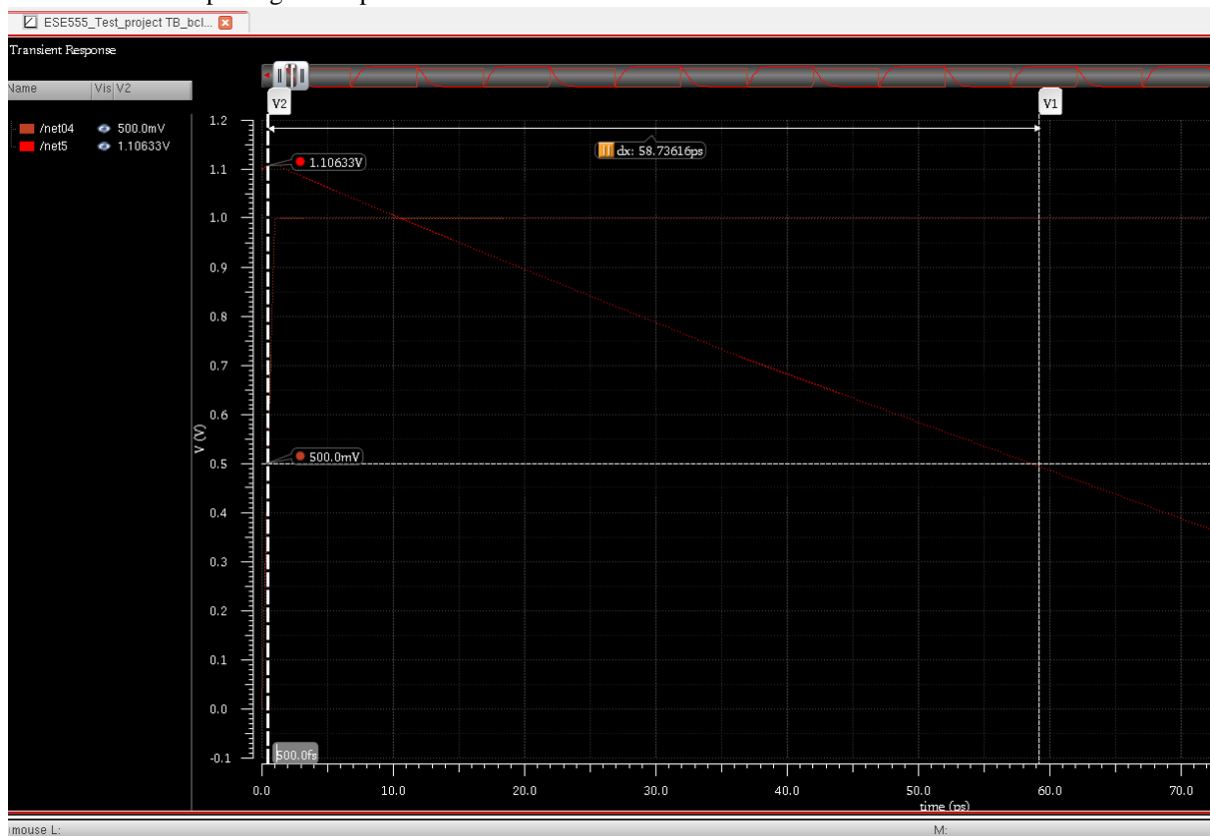


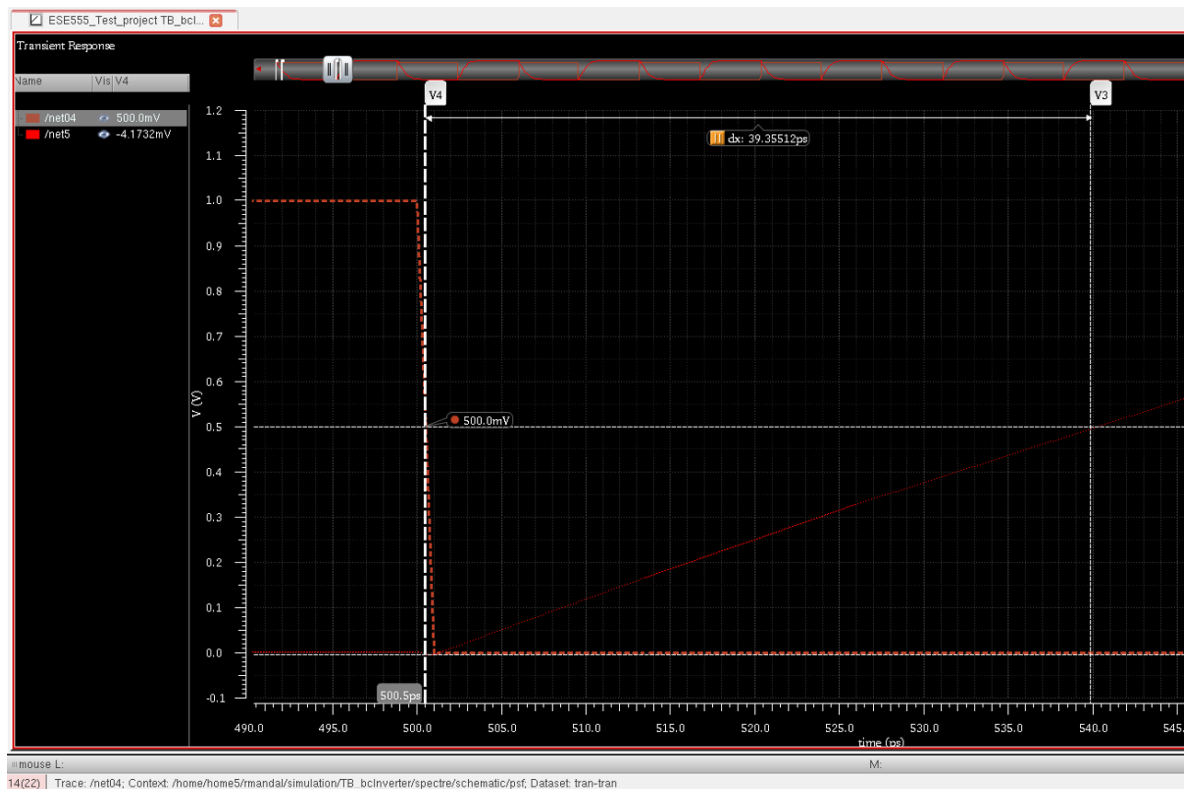
Inverter Circuit



- inverter test – transient analysis – 2nm period/50% duty cycle
- transient analysis(5 clock cycles, 10ns) schematic netlist, high-to-low and low-to-high rise and fall
-

a. Rise and Fall of Input Signal is 1ps

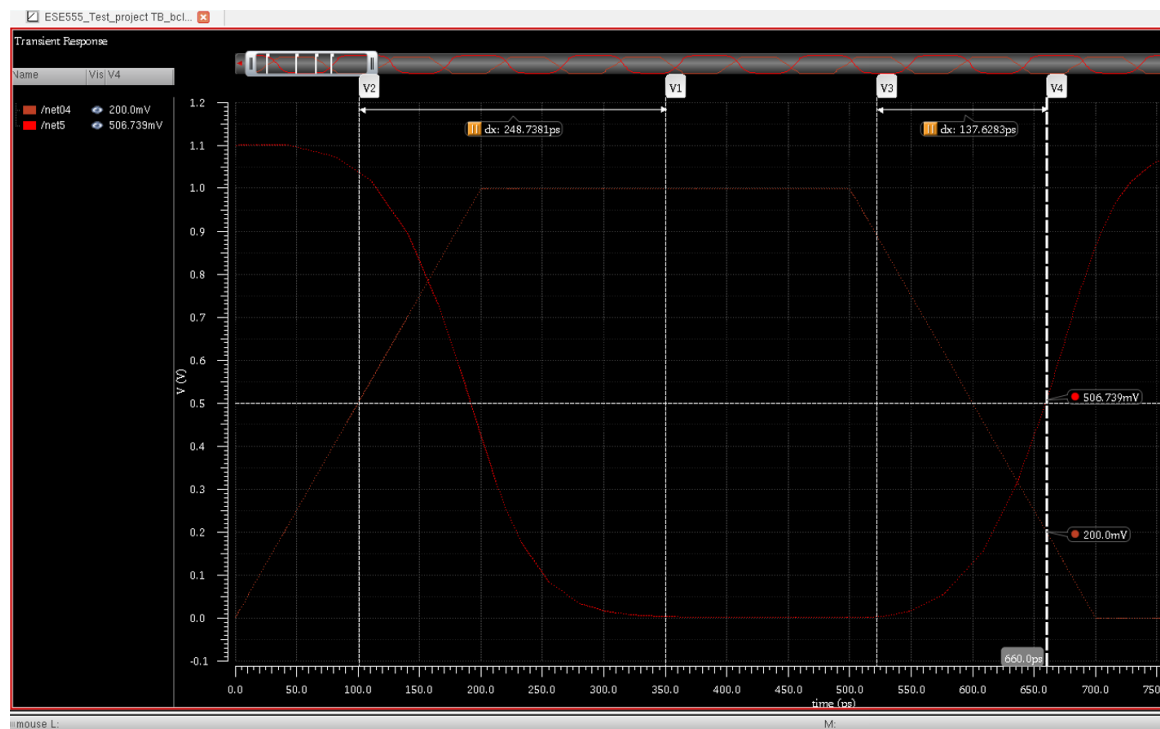




The high to low propagation delay is 58.7361ps

The low to high propagation delay is 39.3551ps

- b. Rise and Fall of Input Signal is 200ps



The high to low propagation delay is 92.7236ps

The low to high propagation delay is 137.6283ps

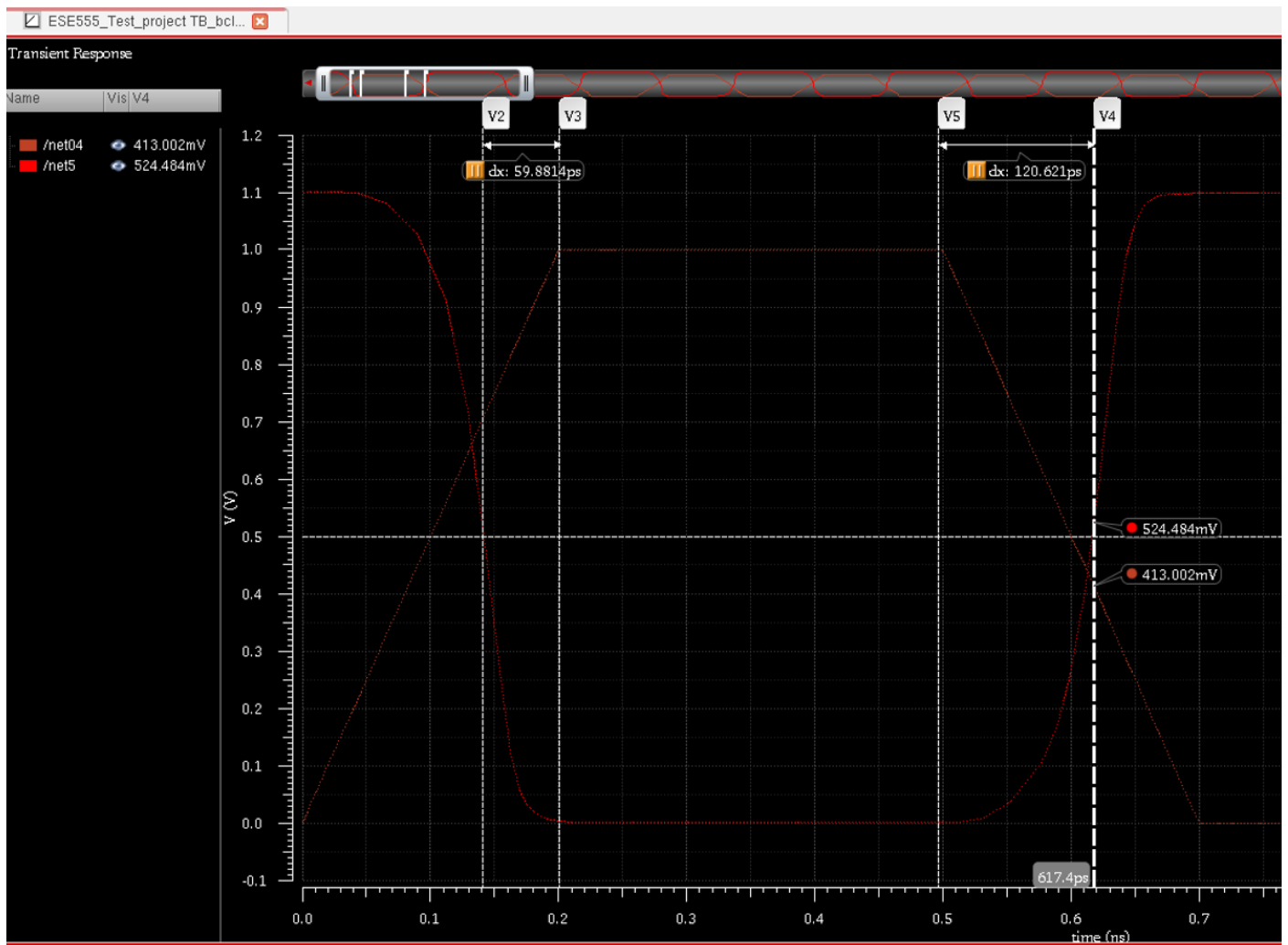
- c. In calculation in Q#1, the results were: High to Low Propagation Delay: 3.47 ps, Low to High Propagation Delay: 6.79 ps.

In simulation in Q#2, results were: high to low propagation delay is 58.7361ps and low to high propagation delay is 39.3551ps for 1ps and high to low propagation delay is 92.7236ps and low to high propagation delay is 137.6283ps for 200ps.

The simulation shows us higher values. This difference in observations is because of components like junction capacitance and such properties that the input signal will now need to overcome.

When we are doing the layout, we need to consider other such factors, so the resultant delay is usually even higher.

Q 3.



The high to low propagation delay is 59.8914ps

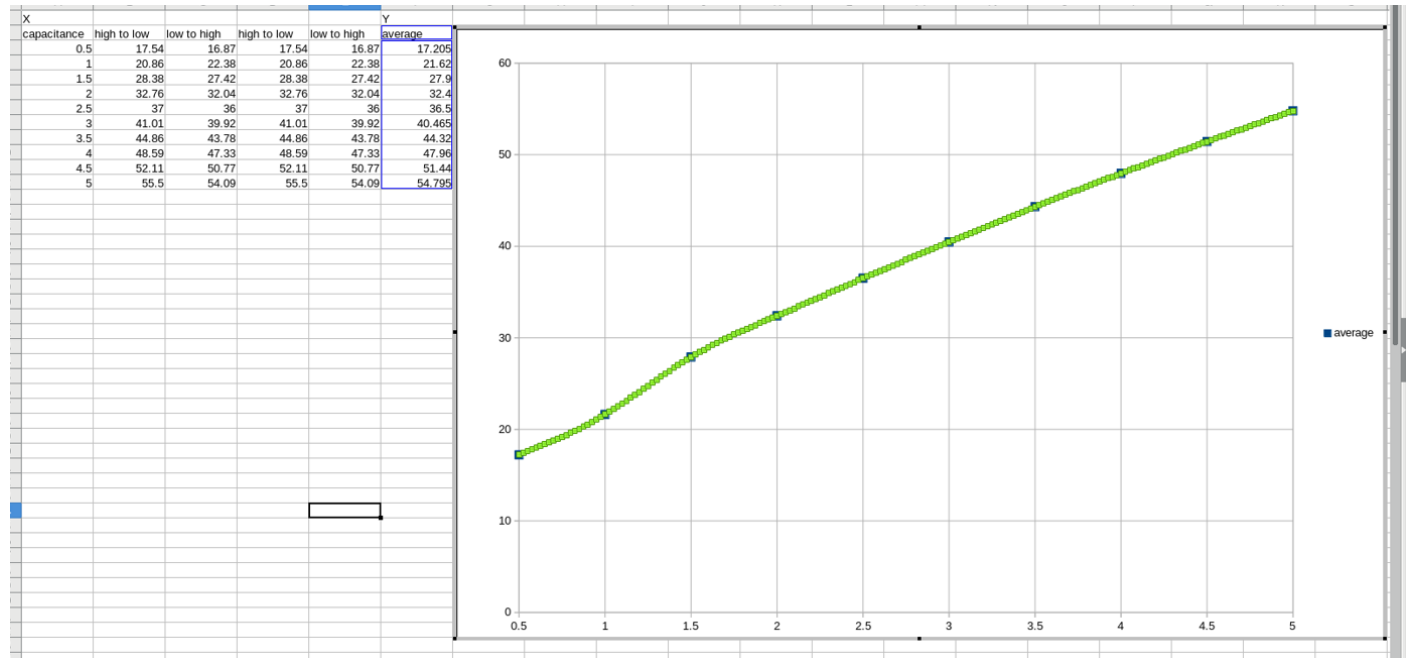
The low to high propagation delay is 120.621ps

Q 4.

Load capacitance: 0.5fF-5fF (in steps of 0.5fF)

Transient analysis was done to find low-to-high and high-to-low propagation delays.

Plot of average propagation delay $((\text{low-to-high} + \text{high-to-low})/2)$ versus output load capacitance:



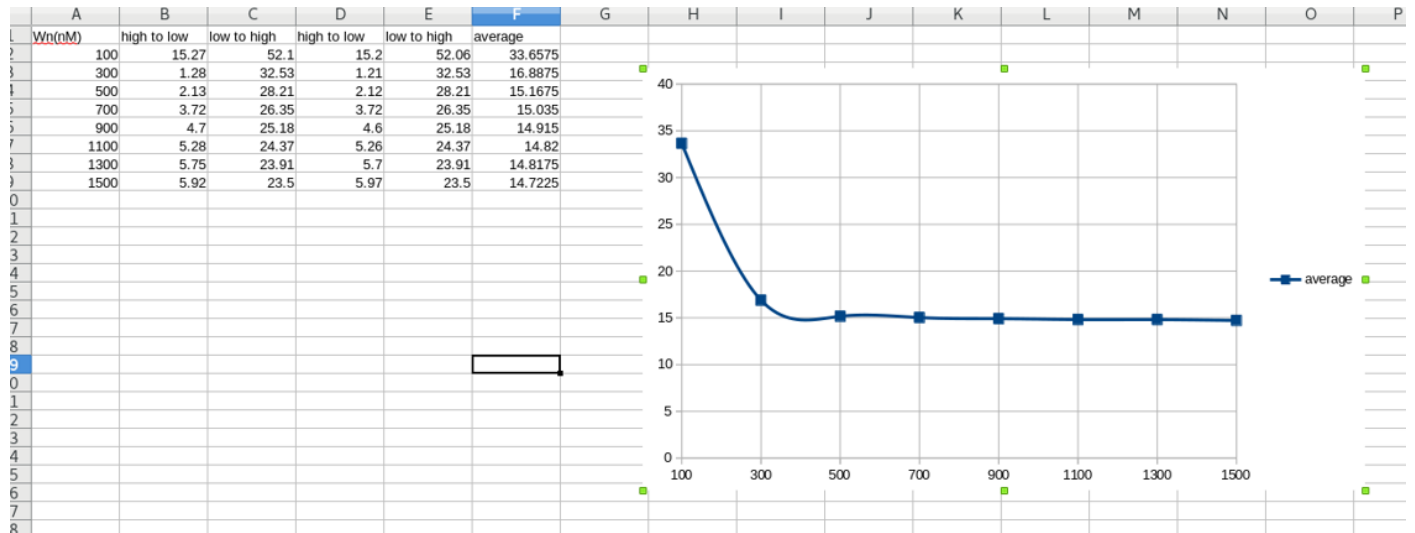
Q 5.

Output load is kept constant at 2fF

Wn is swept until 1.5 um (with step size of 200 nm) while keeping Wp/Wn constant,

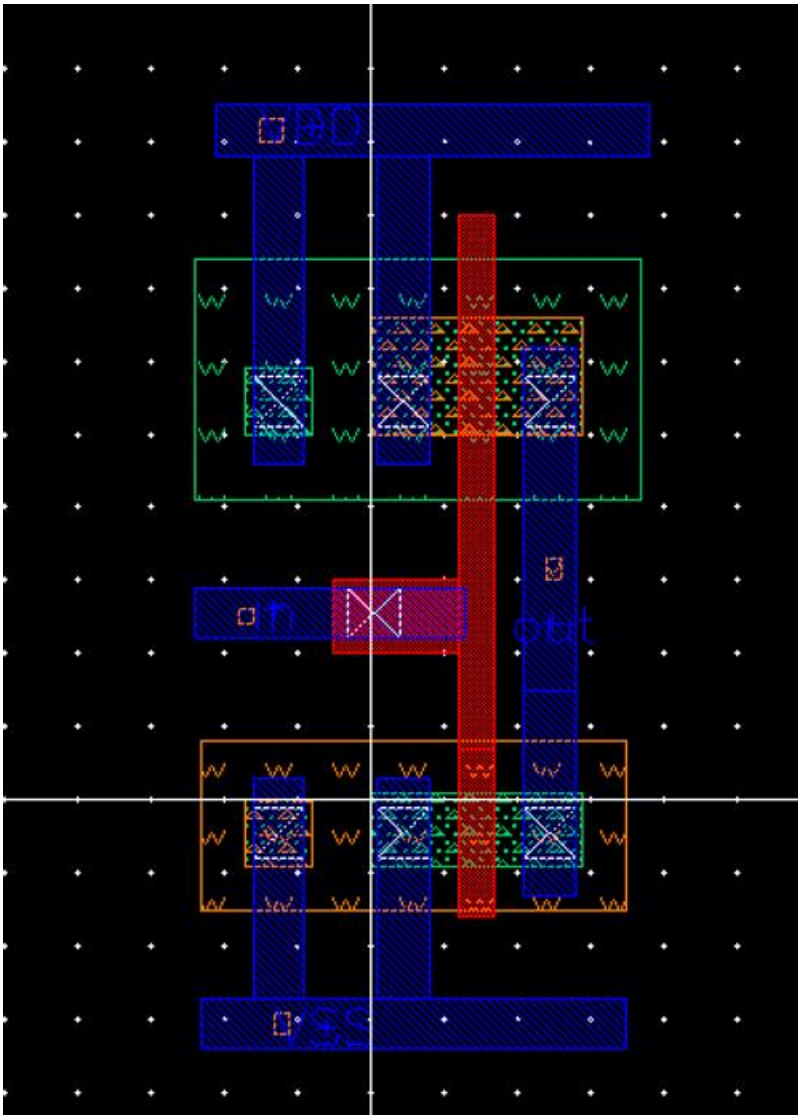
Transient analysis is done to determine low-to-high and high-to-low propagation delays.

Plot of average propagation delay ((low-to-high+high-to-low)/2) versus Wn:



Q 6.

Inverter Physical Layout



Pass DRC & LVS

Calibre - RVE v2014.4_28.20 : Inverter.drc.results

Calibre Interactive - nmDRC v2014.4_28.20 : runset.calibre.drc

DRC Summary Report - Inverter.drc.summary

File View Highlight Tools Window Setup

File Transcript Setup Help

File Edit Options Windows

Check / Cell Results

Check / Cell	Results
Check Well1	0
Check Well2	0
Check Well4	0
Check Poly1	0
Check Poly2	0
Check Poly3	0
Check Poly4	0
Check Poly5	0
Check Poly6	0
Check Active1	0
Check Active2	0
Check Active3	0
Check Active4	0
Check Implant1	0
Check Implant2	0
Check Implant3	0
Check Implant4	0
Check Implant6	0
Check Contact1	0
Check Contact2	0
Check Contact3	0
Check Contact4	0
Check Contact5	0

Rule File Pathname: /home/home5/rmandal/ese555/Inverter.drc.results

Well and Pwell must not overlap

Rules

Inputs

Outputs

Run Control

Transcript

Run DRC

Start RVE

--- TOTAL RULECHECKS EXECUTED = 167
--- TOTAL RESULTS GENERATED = 0 (0)
--- DRC RESULTS DATABASE FILE = Inverter.drc.results (ASCII)
--- CALIBRE : DRC-H COMPLETED - Thu Sep 23 16:00:33 2021
--- TOTAL CPU TIME = 0 REAL TIME = 0
--- PROCESSOR COUNT = 1
--- SUMMARY REPORT FILE = Inverter.drc.summary
// Calibre v2014.4_28.20 Thu Dec 4 12:46:30 PST 2014
// Calibre Utility Library v0-7-7-2014-2 Thu Jul 8 18:35:09 PDT
// Litho Libraries v2014.4_28.20 Thu Dec 4 12:46:30 PST 2014
//
// Copyright Mentor Graphics Corporation 1996-2014
// All Rights Reserved
// THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
// WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION
// OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
// Mentor Graphics software executing under x86-64 Linux
// Running on 1 CPU
// Graphical User-Interface startup.... Complete.
// calibreddb license acquired.
// RVE authorized
// Loaded ASCII database /home/home5/rmandal/ese555/Inverter.drc.results

==== CALIBRE : DRC-H SUMMARY REPORT
====
Execution Date/Time: Thu Sep 23 16:00:33 2021
Calibre Version: v2014.4_28.20 Thu Dec 4 12:46:29 PST 2014
Rule File Pathname: /home/home5/rmandal/ese555/_calibreDRC.rul_
Rule File Title:
Layout System: GDS
Layout Path(s): Inverter.calibre.db
Layout Primary Cell: Inverter
Current Directory: /home/home5/rmandal/ese555
User Name: rmandal
Maximum Results/RuleCheck: 1000
Maximum Result Vertices: 4096
DRC Results Database: Inverter.drc.results (ASCII)
Layout Depth: ALL
Text Depth: PRIMARY
Summary Report File: Inverter.drc.summary (REPLACE)
Geometry Flagging: ACUTE = NO SKEW = NO ANGLED = NO OFFGRID = NO
NONSIMPLE POLYGON = NO NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping: COMMENT TEXT + RULE FILE INFORMATION
Layers: MEMORY-BASED
Keep Empty Checks: YES
--- RUNTIME WARNINGS

Palette7.8 X
Layers8 X
ValidUsedRouting
Filter
psell drawing

LVS Report File - Invector.lvs.report
FileEditOptionsWindows

##CALIBRE SYSTEM##
##LVS REPORT##

REPORT FILE NAME: Invector.lvs.report
AYOUT NAME: /home/home5/cmandal/ese555/Invector.sp ('Invector')
SOURCE NAME: /home/home5/cmandal/ese555/Invector.src.net ('Invert
SLE FILE: /home/home5/cmandal/ese555/_calibreLVS.rul_
SLE FILE TITLE: LVS Rule File for FreePDK45
REACTION TIME: Thu Sep 23 16:09:04 2021
UNSCRIPT DIRECTORY: /home/home5/cmandal/ese555
USER NAME: cmandal
ALIBRE VERSION: v2014.4_20.20 Thu Dec 4 12:46:29 PST 2014

OVERALL COMPARISON RESULTS

metal2 net
via2 drw
via2 net
metal3 drw
metal3 net
Objects
Objects
Instances
Pins
Vias

FileViewHighlightToolsWindowSetup
Search
Comparison Results x
Layout Cell / TypeSource CellN
InvectorInvector4L
Results
Extraction Resu
Comparison Re
Parasitics
Reports
Extraction Repc
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options

Cell Invector Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)

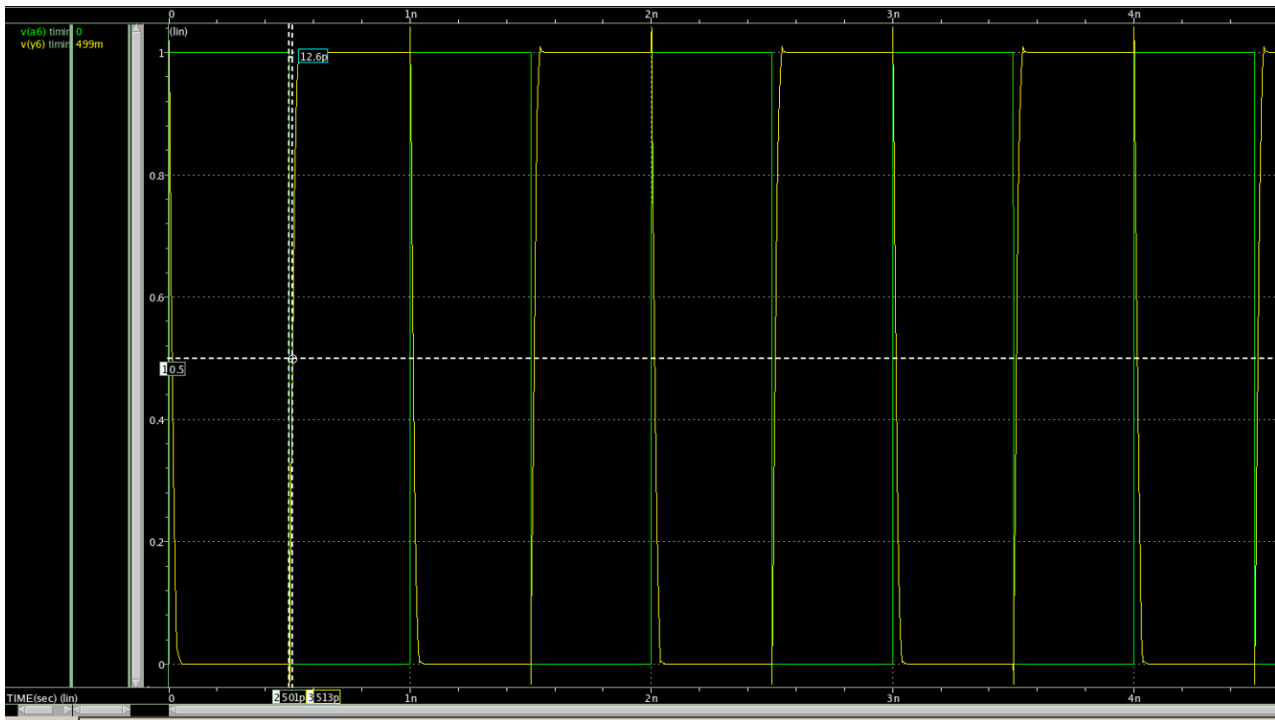
#CORRECT#

LAYOUT CELL NAME: Invector
SOURCE CELL NAME: Invector
INITIAL NUMBERS OF OBJECTS
LayoutSourceComponent Type
Ports:44
Nets:44
Instances:11NM (4 pins)
HP (4 pins)
Metal Total:00

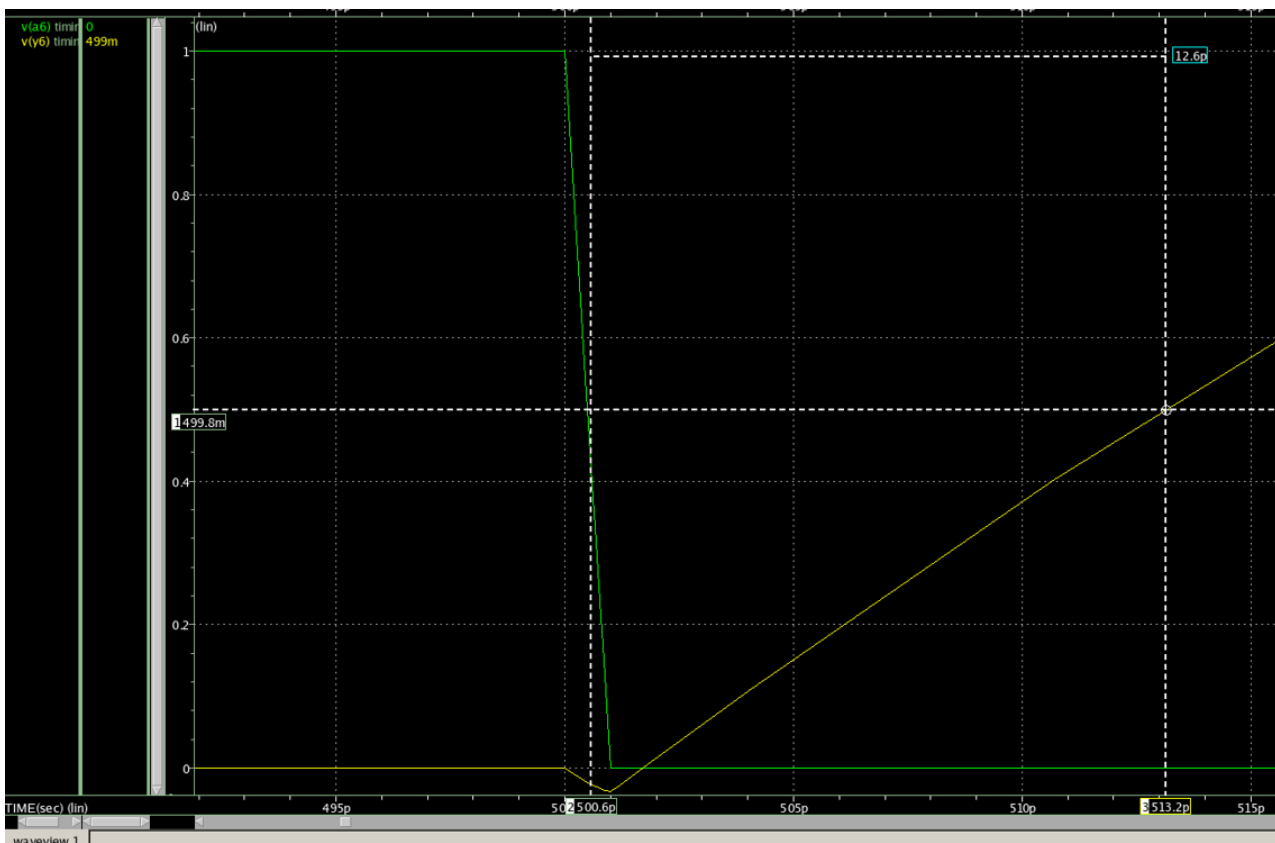
Q7.

HSPICE simulation

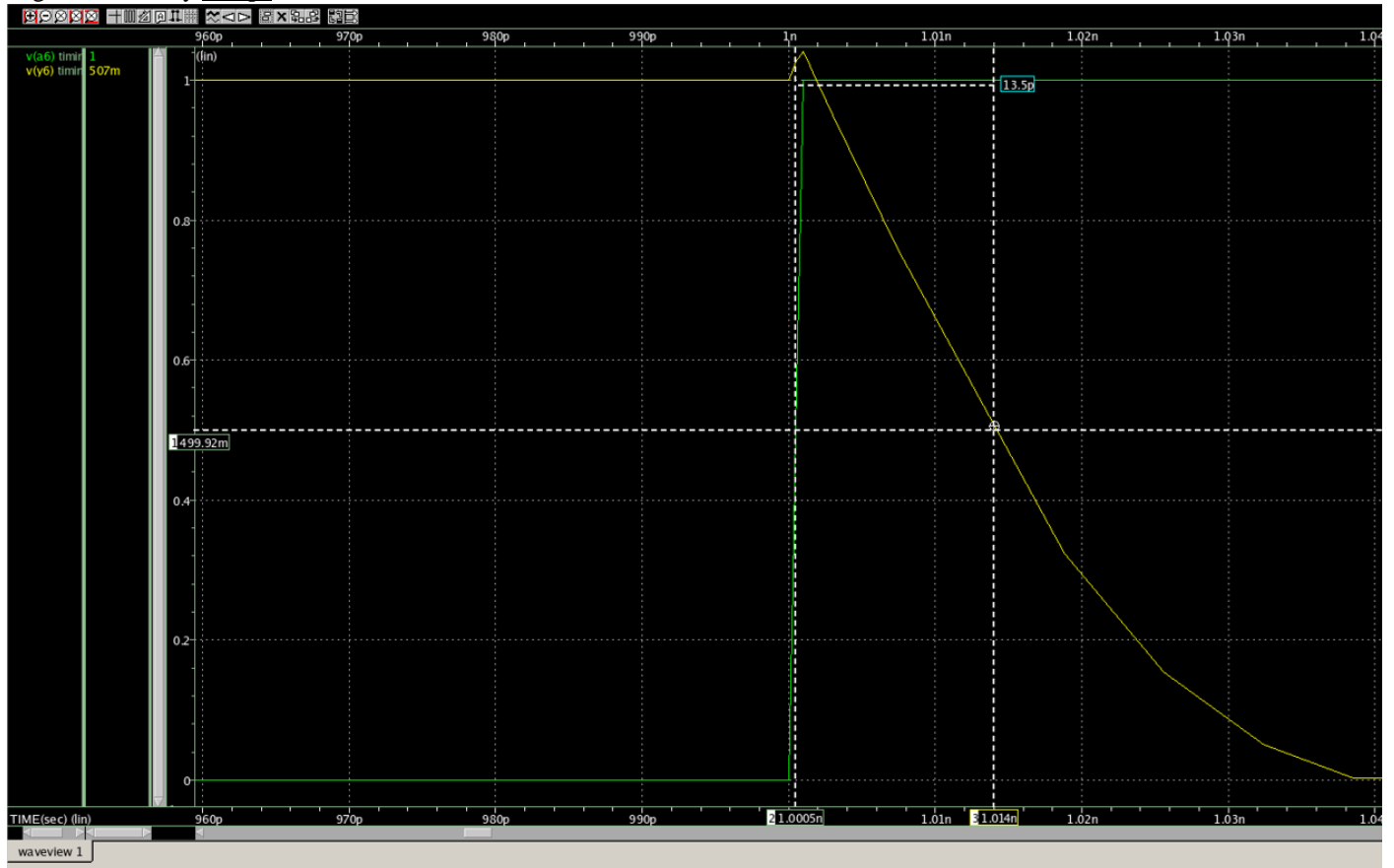
a) Rise & Fall Input Signal is 1ps



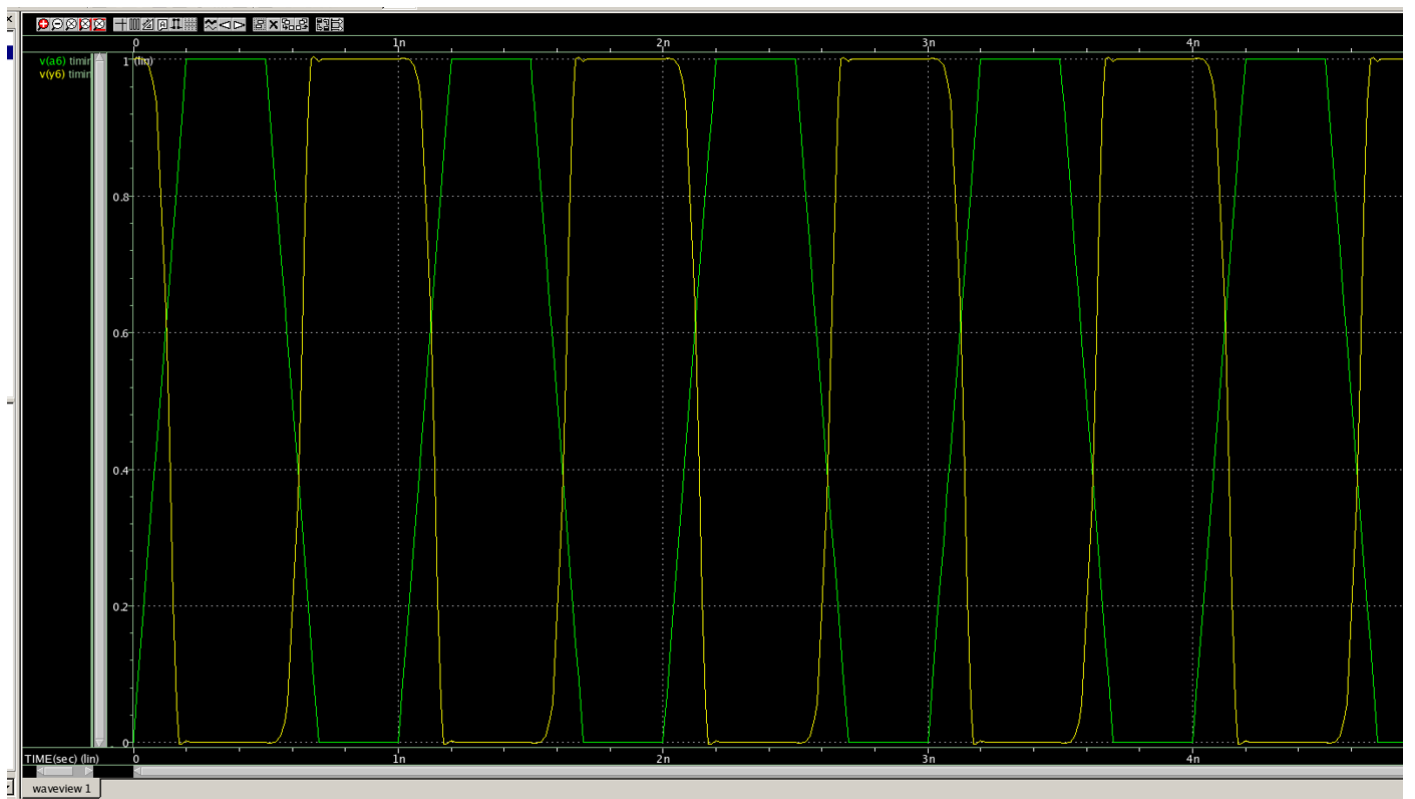
Low to High delay is 12.6ps



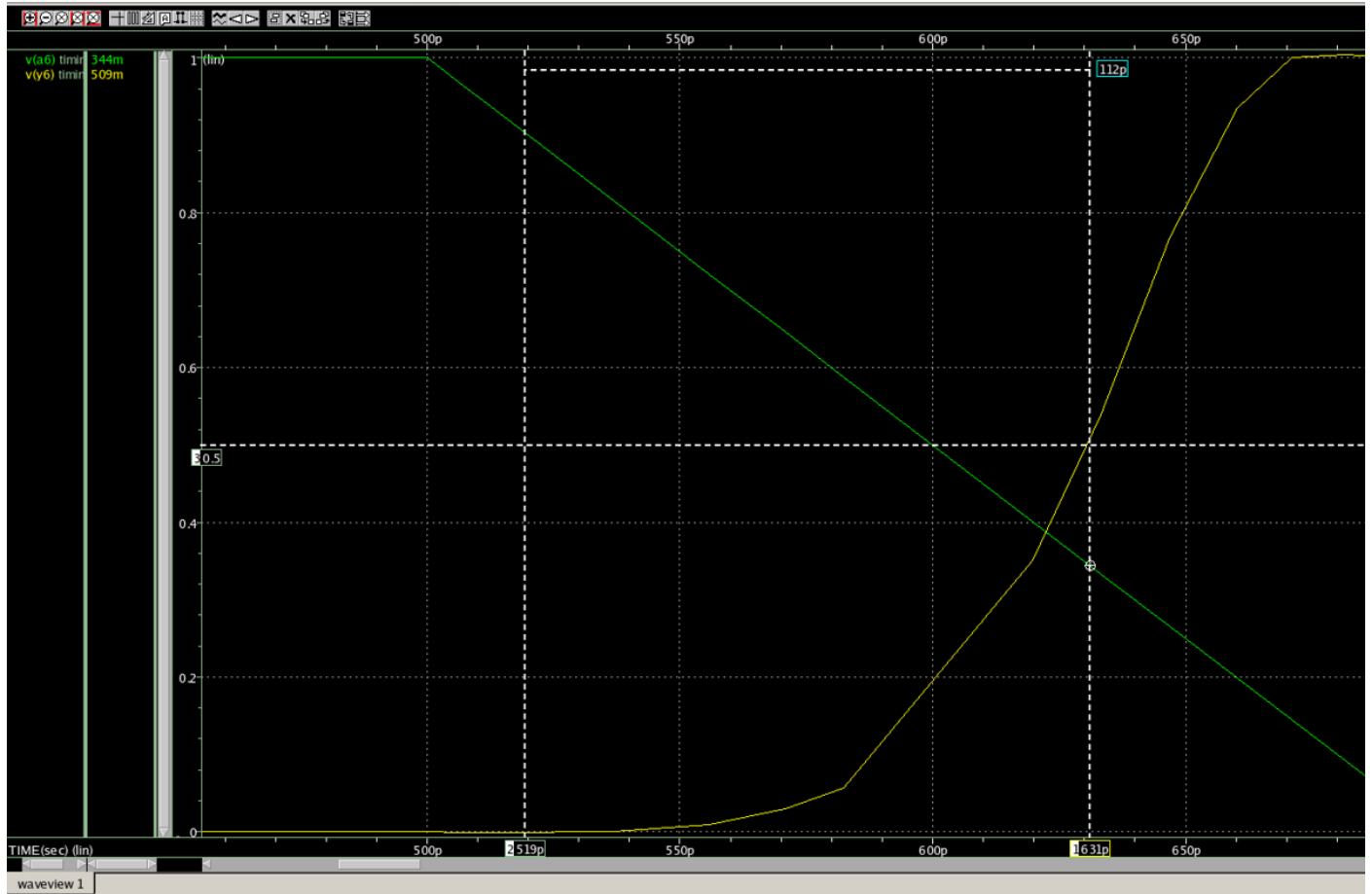
High to low delay 13.5ps



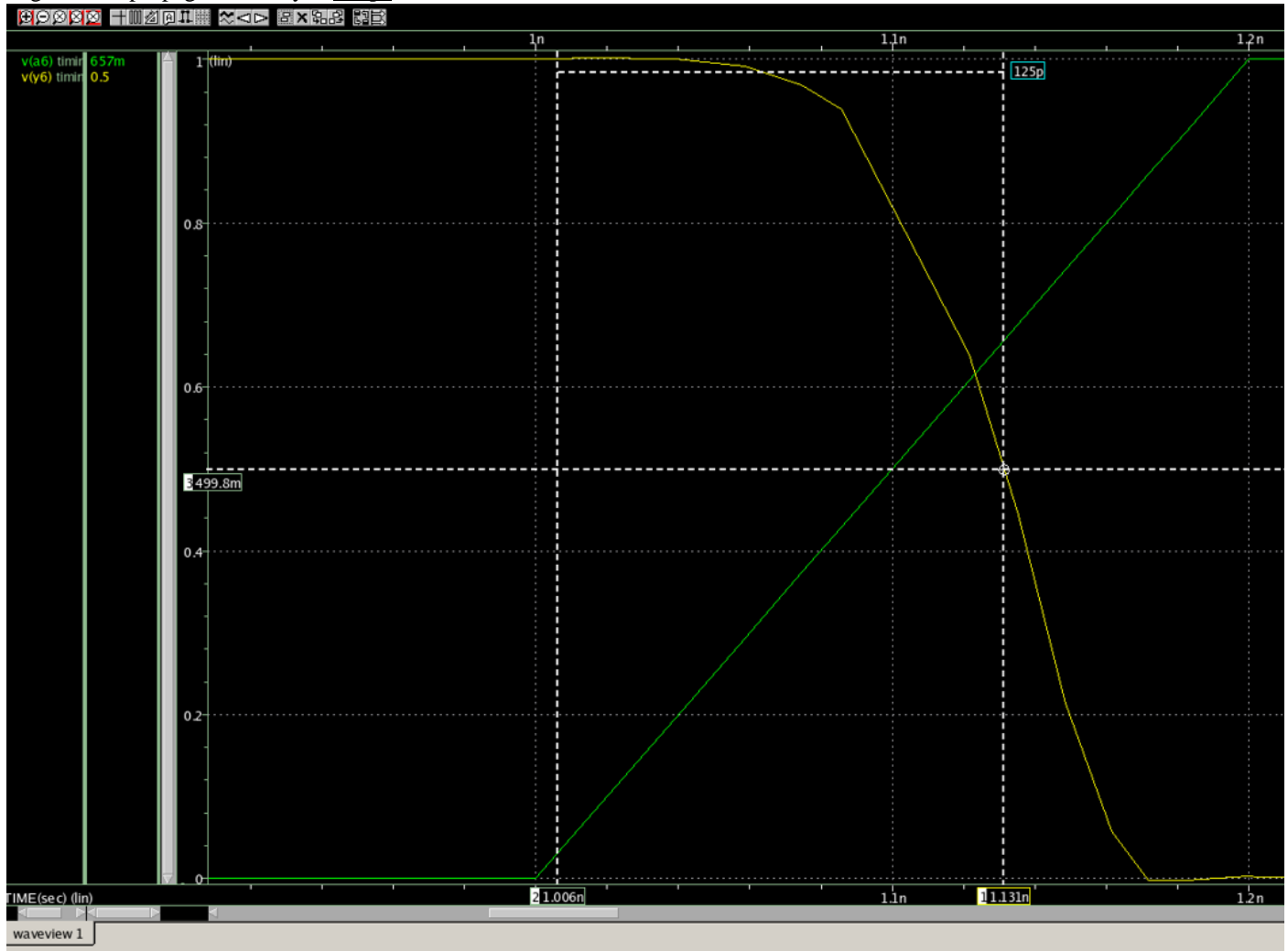
b) Rise & Fall Input Signal is 200ps



Low to high propagation delay is 112ps



High to low propagation delay is 125ps



c) Our extracted netlist simulation results show higher values than schematic netlist. The result is due to factors such as junction capacitance, that input signals will need to overcome and thus add to the delay.