ESE555 VLSI Design

Assignment 2

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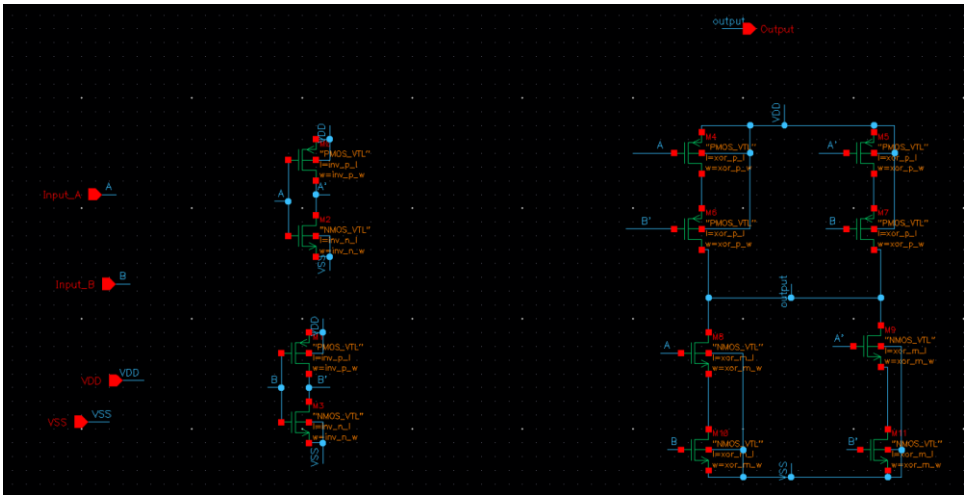
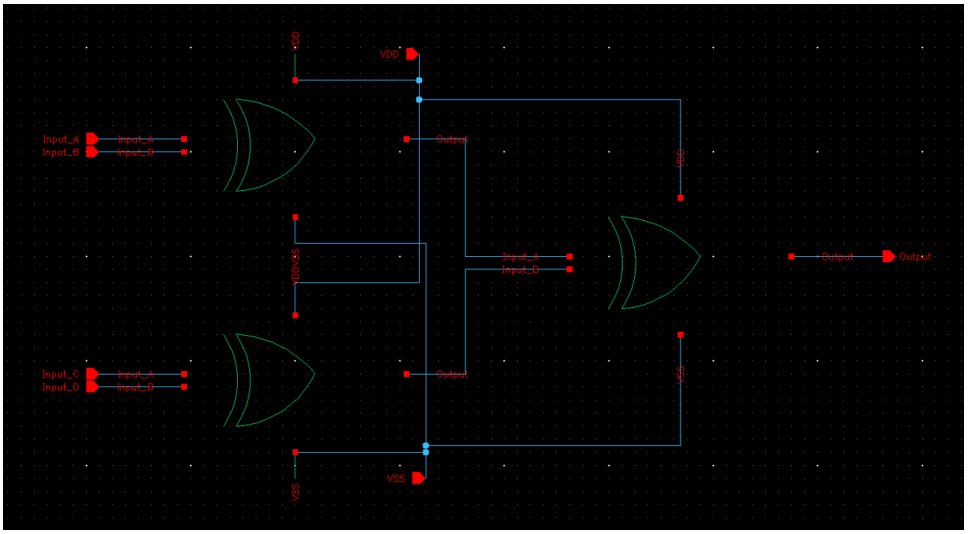
4-Input Parity Generator using 3 XOR gates

Schematic Design

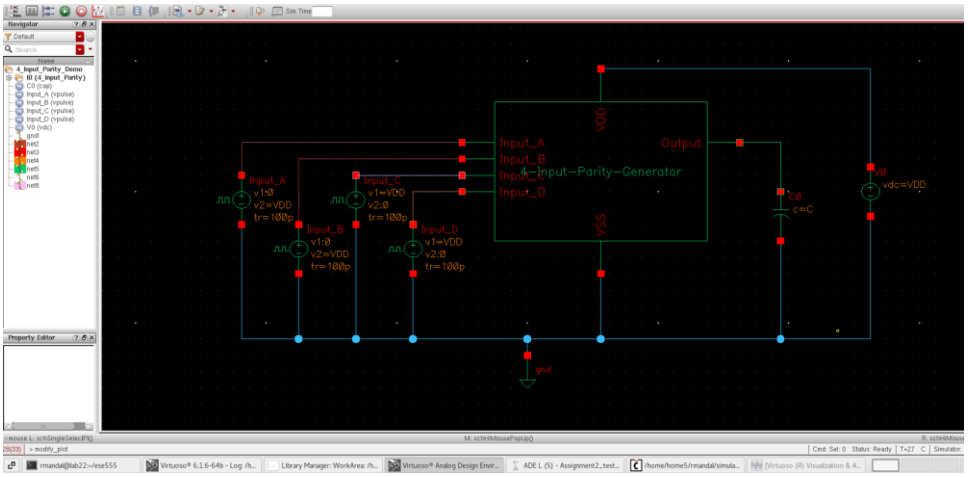
Single XOR Gate Schematic:



3-XOR Parity Generator Schematic



Parity Generator Symbol



ADE L Simulation

Supply Voltages 1.1V

External Load 12fF

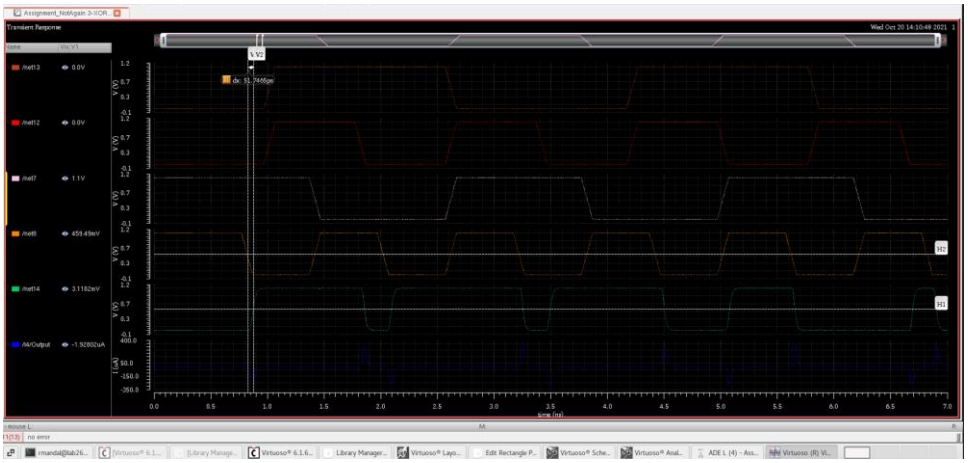
Rise/Fall times 100ps

To drive the 12fF load, I needed the following parameters:

Bigger/First XOR gates Pmos-width 2um, Nmos-width 1um.length50nm

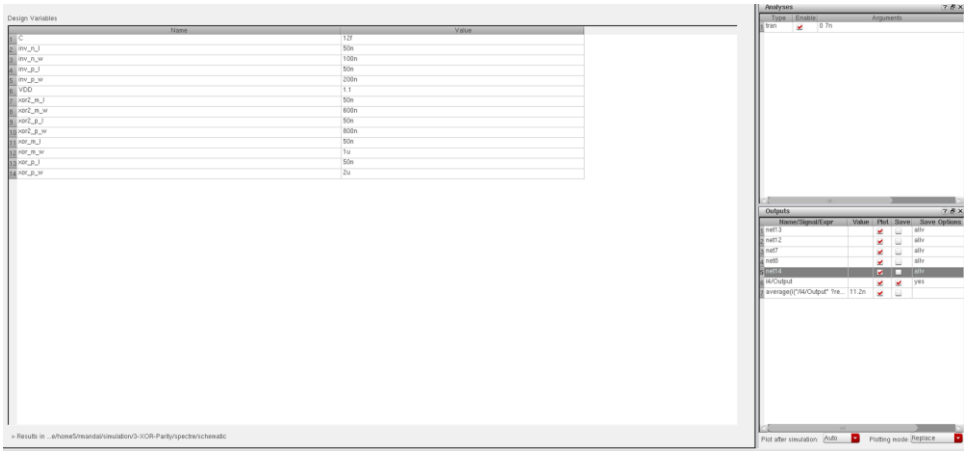
Last XOR gate Pmos-width 800nm, Nmos-width: 600nm. Length 50nm.

Inverter:Pmos-width 200nm, Nmos-width:100nm, Length 50nm.



Propagation Delay= 51ps

Power Calculations



Average Current = 11.2nA

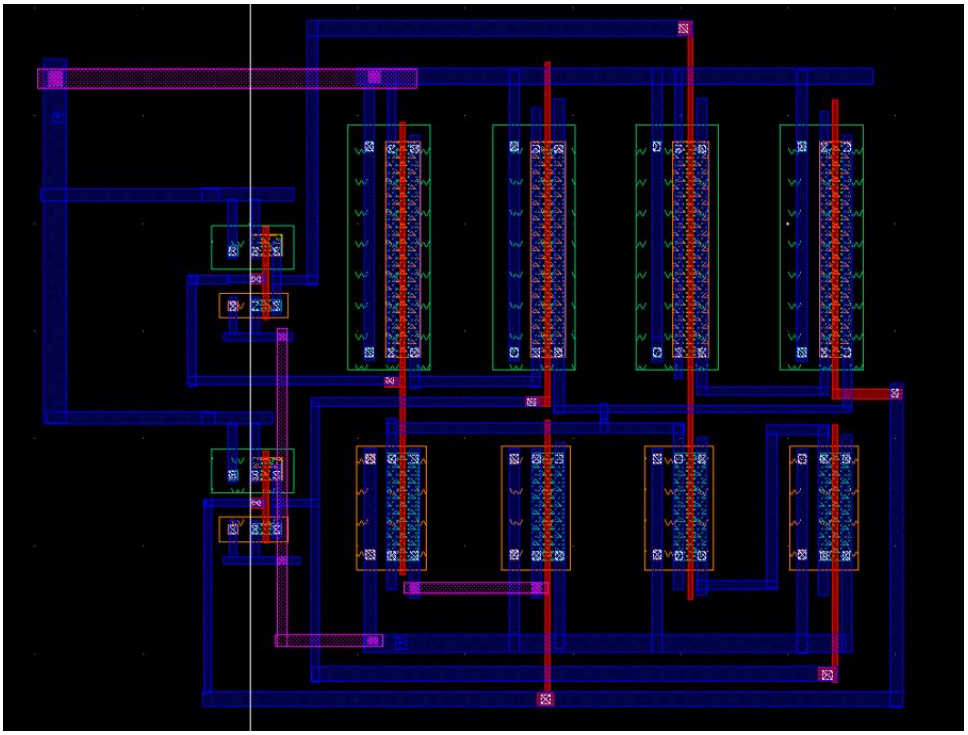
Average power consumption is the overall transient current drawn from the supply times the supply voltage:

= I x Vdd

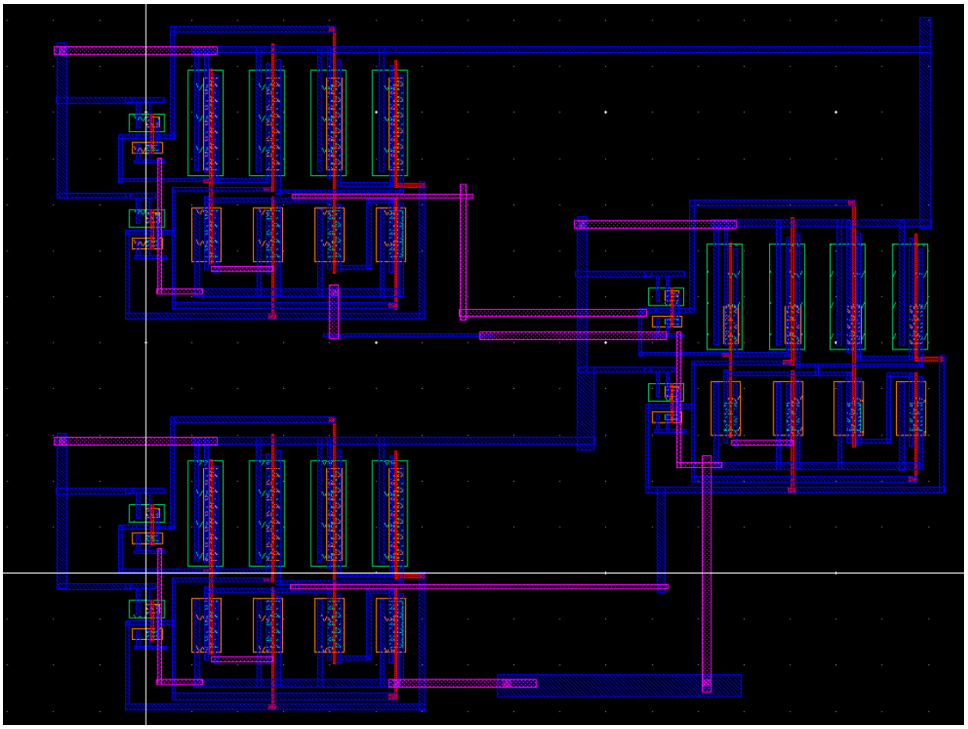
= 1.1V x 11.2 nA

Layout

Single XOR Gate Layout

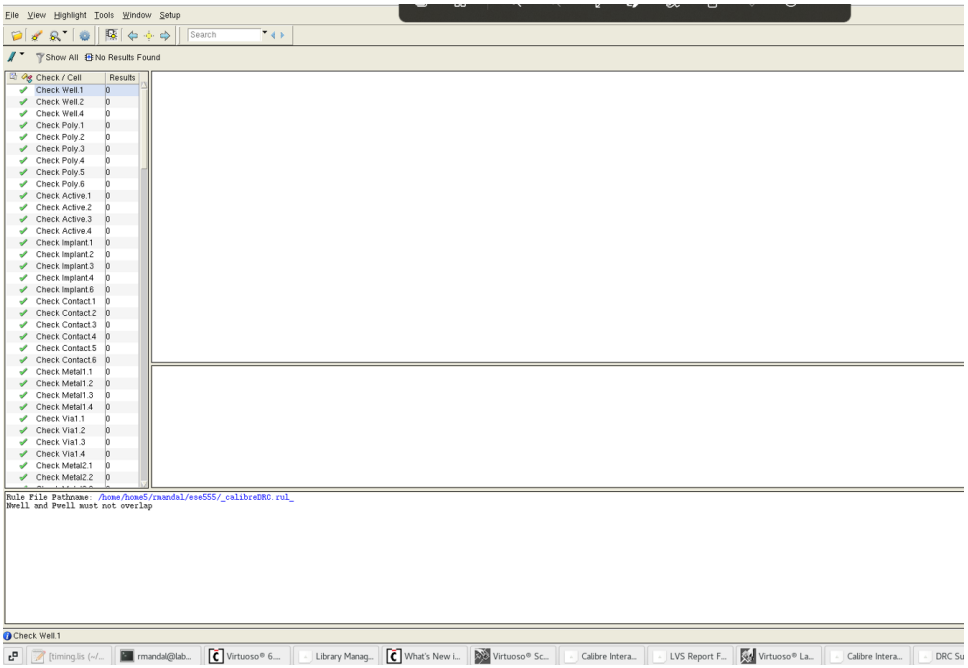


Parity Generator Layout



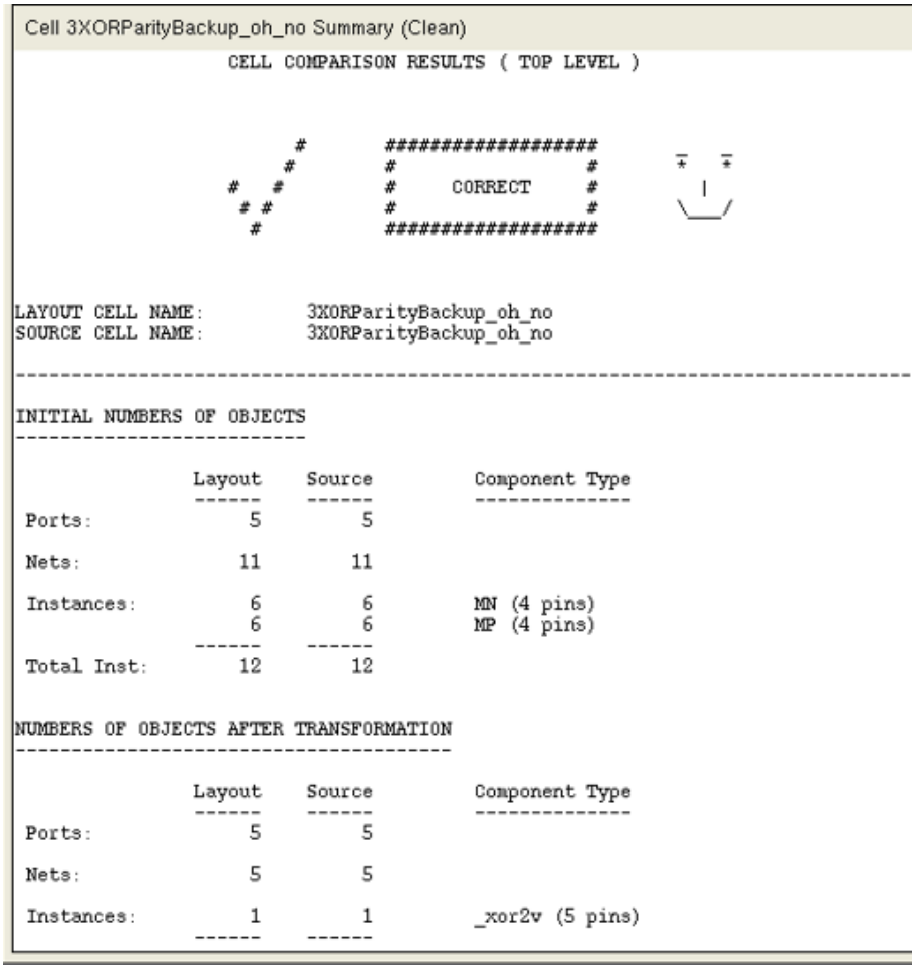
Area of this Layout is 18.985um X 14.8525um

DRC Passed



LVS Passed

PEX results:



```
Cell 3XORParityBackup_oh_no Summary (Clean)
                CELL COMPARISON RESULTS ( TOP LEVEL )


                     #      ##################      ∓   ∓
                    #       #                #       |
                  #   #     #     CORRECT    #      \___/
                   # #      #                #
                    #       ##################


LAYOUT CELL NAME:          3XORParityBackup_oh_no
SOURCE CELL NAME:          3XORParityBackup_oh_no

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INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              5         5

 Nets:              11        11

 Instances:          6         6         MN (4 pins)
                     6         6         MP (4 pins)
                ------    ------
 Total Inst:        12        12


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              5         5

 Nets:               5         5

 Instances:          1         1         _xor2v (5 pins)
                ------    ------
```

Extracted Netlist:

```
* File: 3XORParityBackupohnonotagain.pex.netlist
* Created: Thu Oct 21 20:38:17 2021
* Program "Calibre xRC"
* Version "v2014.4_28.20"
*
.subckt 3XORParityBackupohnonotagain  VDD VSS C A D B OUTPUT
*
mXI5/MM3 XI5/B' D VSS VSS NMOS_VTL L=5e-08 W=1e-07 AD=1.2e-14 AS=1.2e-14
+ PD=4.4e-07 PS=4.4e-07
mXI5/MM2 XI5/A' C VSS VSS NMOS_VTL L=5e-08 W=1e-07 AD=1.2e-14 AS=1.2e-14
+ PD=4.4e-07 PS=4.4e-07
mXI2/MM3 XI2/B' B VSS VSS NMOS_VTL L=5e-08 W=1e-07 AD=1.2e-14 AS=1.2e-14
+ PD=4.4e-07 PS=4.4e-07
mXI2/MM2 XI2/A' A VSS VSS NMOS_VTL L=5e-08 W=1e-07 AD=1.2e-14 AS=1.2e-14
+ PD=4.4e-07 PS=4.4e-07
mXI5/MM8 NET21 C XI5/NET021 VSS NMOS_VTL L=5e-08 W=1e-06 AD=1.25e-13 AS=1.25e-13
```

+ PD=2.25e-06 PS=2.25e-06

mXI2/MM8 NET22 A XI2/NET021 VSS NMOS_VTL L=5e-08 W=1e-06 AD=1.25e-13 AS=1.25e-13

+ PD=2.25e-06 PS=2.25e-06

mXI5/MM10 XI5/NET021 D VSS VSS NMOS_VTL L=5e-08 W=1e-06 AD=1.225e-13 AS=1.35e-13

+ PD=2.245e-06 PS=2.27e-06

mXI2/MM10 XI2/NET021 B VSS VSS NMOS_VTL L=5e-08 W=1e-06 AD=1.225e-13 AS=1.35e-13

+ PD=2.245e-06 PS=2.27e-06

mXI5/MM9 NET21 XI5/A' XI5/NET28 VSS NMOS_VTL L=5e-08 W=1e-06 AD=1.3e-13

+ AS=1.2e-13 PD=2.26e-06 PS=2.24e-06

mXI2/MM9 NET22 XI2/A' XI2/NET28 VSS NMOS_VTL L=5e-08 W=1e-06 AD=1.3e-13

+ AS=1.2e-13 PD=2.26e-06 PS=2.24e-06

mXI5/MM11 XI5/NET28 XI5/B' VSS VSS NMOS_VTL L=5e-08 W=1e-06 AD=1.225e-13

+ AS=1.25e-13 PD=2.245e-06 PS=2.25e-06

mXI2/MM11 XI2/NET28 XI2/B' VSS VSS NMOS_VTL L=5e-08 W=1e-06 AD=1.225e-13

+ AS=1.25e-13 PD=2.245e-06 PS=2.25e-06

mXI6/MM3 XI6/B' NET21 VSS VSS NMOS_VTL L=5e-08 W=1e-07 AD=1.2e-14 AS=1.2e-14

+ PD=4.4e-07 PS=4.4e-07

mXI6/MM2 XI6/A' NET22 VSS VSS NMOS_VTL L=5e-08 W=1e-07 AD=1.2e-14 AS=1.2e-14

+ PD=4.4e-07 PS=4.4e-07

mXI6/MM8 OUTPUT NET22 XI6/NET021 VSS NMOS_VTL L=5e-08 W=6e-07 AD=7.5e-14

+ AS=7.5e-14 PD=1.45e-06 PS=1.45e-06

mXI6/MM10 XI6/NET021 NET21 VSS VSS NMOS_VTL L=5e-08 W=6e-07 AD=7.35e-14

+ AS=8.1e-14 PD=1.445e-06 PS=1.47e-06

mXI6/MM9 OUTPUT XI6/A' XI6/NET017 VSS NMOS_VTL L=5e-08 W=6e-07 AD=7.8e-14

+ AS=7.2e-14 PD=1.46e-06 PS=1.44e-06

mXI6/MM11 XI6/NET017 XI6/B' VSS VSS NMOS_VTL L=5e-08 W=6e-07 AD=7.35e-14

+ AS=7.5e-14 PD=1.445e-06 PS=1.45e-06

mXI5/MM1 XI5/B' D VDD VDD PMOS_VTL L=5e-08 W=2e-07 AD=2.4e-14 AS=2.4e-14

+ PD=6.4e-07 PS=6.4e-07

mXI5/MM0 XI5/A' C VDD VDD PMOS_VTL L=5e-08 W=2e-07 AD=2.4e-14 AS=2.4e-14

+ PD=6.4e-07 PS=6.4e-07

mXI2/MM1 XI2/B' B VDD VDD PMOS_VTL L=5e-08 W=2e-07 AD=2.4e-14 AS=2.4e-14

+ PD=6.4e-07 PS=6.4e-07

mXI2/MM0 XI2/A' A VDD VDD PMOS_VTL L=5e-08 W=2e-07 AD=2.4e-14 AS=2.4e-14

```
+ PD=6.4e-07 PS=6.4e-07
mXI5/MM4 XI5/NET023 C VDD VDD PMOS_VTL L=5e-08 W=2e-06 AD=2.75e-13 AS=2.65e-13
+ PD=4.275e-06 PS=4.265e-06
mXI2/MM4 XI2/NET023 A VDD VDD PMOS_VTL L=5e-08 W=2e-06 AD=2.75e-13 AS=2.65e-13
+ PD=4.275e-06 PS=4.265e-06
mXI5/MM6 NET21 XI5/B' XI5/NET023 VDD PMOS_VTL L=5e-08 W=2e-06 AD=2.9e-13
+ AS=2.55e-13 PD=4.29e-06 PS=4.255e-06
mXI2/MM6 NET22 XI2/B' XI2/NET023 VDD PMOS_VTL L=5e-08 W=2e-06 AD=2.9e-13
+ AS=2.55e-13 PD=4.29e-06 PS=4.255e-06
mXI5/MM5 XI5/NET022 XI5/A' VDD VDD PMOS_VTL L=5e-08 W=2e-06 AD=2.75e-13
+ AS=2.8e-13 PD=4.275e-06 PS=4.28e-06
mXI2/MM5 XI2/NET022 XI2/A' VDD VDD PMOS_VTL L=5e-08 W=2e-06 AD=2.75e-13
+ AS=2.8e-13 PD=4.275e-06 PS=4.28e-06
mXI5/MM7 NET21 D XI5/NET022 VDD PMOS_VTL L=5e-08 W=2e-06 AD=2.65e-13 AS=2.4e-13
+ PD=4.265e-06 PS=4.24e-06
mXI2/MM7 NET22 B XI2/NET022 VDD PMOS_VTL L=5e-08 W=2e-06 AD=2.65e-13 AS=2.4e-13
+ PD=4.265e-06 PS=4.24e-06
mXI6/MM1 XI6/B' NET21 VDD VDD PMOS_VTL L=5e-08 W=2e-07 AD=2.4e-14 AS=2.4e-14
+ PD=6.4e-07 PS=6.4e-07
mXI6/MM0 XI6/A' NET22 VDD VDD PMOS_VTL L=5e-08 W=2e-07 AD=2.4e-14 AS=2.4e-14
+ PD=6.4e-07 PS=6.4e-07
mXI6/MM4 XI6/NET023 NET22 VDD VDD PMOS_VTL L=5e-08 W=8e-07 AD=1.1e-13
+ AS=1.06e-13 PD=1.875e-06 PS=1.865e-06
mXI6/MM6 OUTPUT XI6/B' XI6/NET023 VDD PMOS_VTL L=5e-08 W=8e-07 AD=1.16e-13
+ AS=1.02e-13 PD=1.89e-06 PS=1.855e-06
mXI6/MM5 XI6/NET015 XI6/A' VDD VDD PMOS_VTL L=5e-08 W=8e-07 AD=1.1e-13
+ AS=1.12e-13 PD=1.875e-06 PS=1.88e-06
mXI6/MM7 OUTPUT NET21 XI6/NET015 VDD PMOS_VTL L=5e-08 W=8e-07 AD=1.06e-13
+ AS=9.6e-14 PD=1.865e-06 PS=1.84e-06
c_21 VDD 0 5.78242f
c_42 VSS 0 3.71267f
c_48 XI5/NET021 0 0.148003f
c_54 XI2/NET021 0 0.148003f
c_71 NET22 0 1.54579f
```

c_88 NET21 0 2.10363f

c_94 XI6/NET021 0 0.148003f

c_103 C 0 0.524077f

c_112 A 0 0.524077f

c_120 XI5/A' 0 0.720316f

c_128 XI2/A' 0 0.720488f

c_138 XI5/B' 0 0.761227f

c_148 XI2/B' 0 0.761423f

c_153 XI5/NET023 0 0.206638f

c_158 XI2/NET023 0 0.206638f

c_163 XI5/NET022 0 0.227626f

c_168 XI2/NET022 0 0.227626f

c_174 XI5/NET28 0 0.193542f

c_180 XI2/NET28 0 0.193918f

c_189 D 0 1.07594f

c_198 B 0 1.05263f

c_206 XI6/A' 0 0.719385f

c_216 XI6/B' 0 0.75884f

c_221 XI6/NET023 0 0.206638f

c_226 XI6/NET015 0 0.227626f

c_232 XI6/NET017 0 0.193918f

c_243 OUTPUT 0 0.516443f

*

.include "3XORParityBackupohnonotagain.pex.netlist.3XORPARITYBACKUPOHNONOTAGAIN.pxi"

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.ends

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