ESE555 VLSI Design

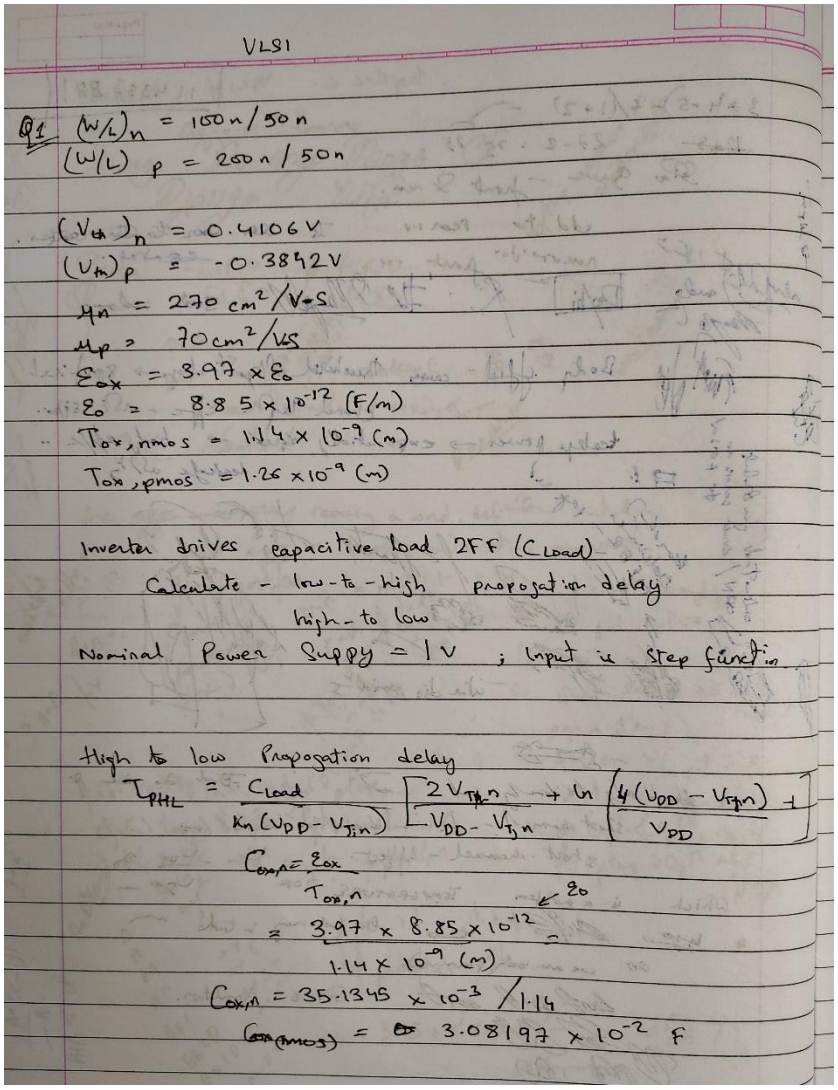
CAD Assignment 1

Reetam Mandal

SBU#114352881

23-Sept-2021

Q 1.



VLSI

Q1 $(W/L)_n = 150n/50n$

$(W/L)_p = 200n/50n$

$(V_{th})_n = 0.4106V$

$(V_{th})_p = -0.3842V$

$\mu_n = 270\ cm^2/V\text{-}s$

$\mu_p = 70\ cm^2/Vs$

$\varepsilon_{ox} = 3.97 \times \varepsilon_0$

$\varepsilon_0 = 8.85 \times 10^{-12}\ (F/m)$

$T_{ox,nmos} = 1.14 \times 10^{-9}\ (m)$

$T_{ox,pmos} = 1.26 \times 10^{-9}\ (m)$

Inverter drives capacitive load 2FF (C_{Load})

Calculate - low-to-high propogation delay

high-to-low

Nominal Power Supply = 1V ; Input is step function

High to low Propogation delay

$$T_{PHL} = \frac{C_{load}}{K_n(V_{DD} - V_{Tn})}\left[\frac{2V_{Tn}}{V_{DD} - V_{Tn}} + \ln\left[\frac{4(V_{DD} - V_{Tn})}{V_{DD}} - 1\right]\right]$$

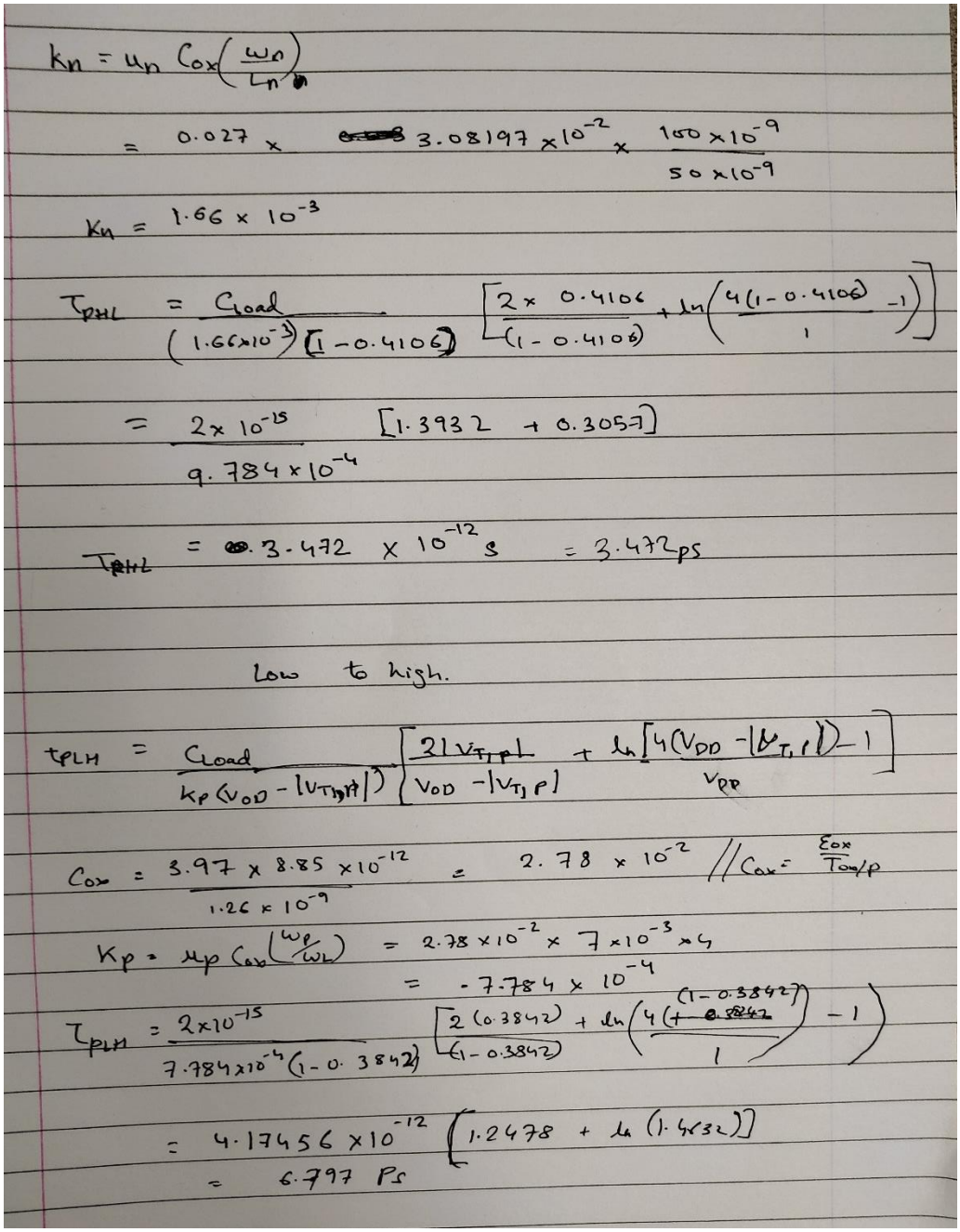
$$C_{ox,n} = \frac{\varepsilon_{ox}}{T_{ox,n}}$$

ε_0

$$= \frac{3.97 \times 8.85 \times 10^{-12}}{1.14 \times 10^{-9}\ (m)}$$

$C_{ox,n} = 35.1345 \times 10^{-3} / 1.14$

$C_{ox(nmos)} = 3.08197 \times 10^{-2}\ F$

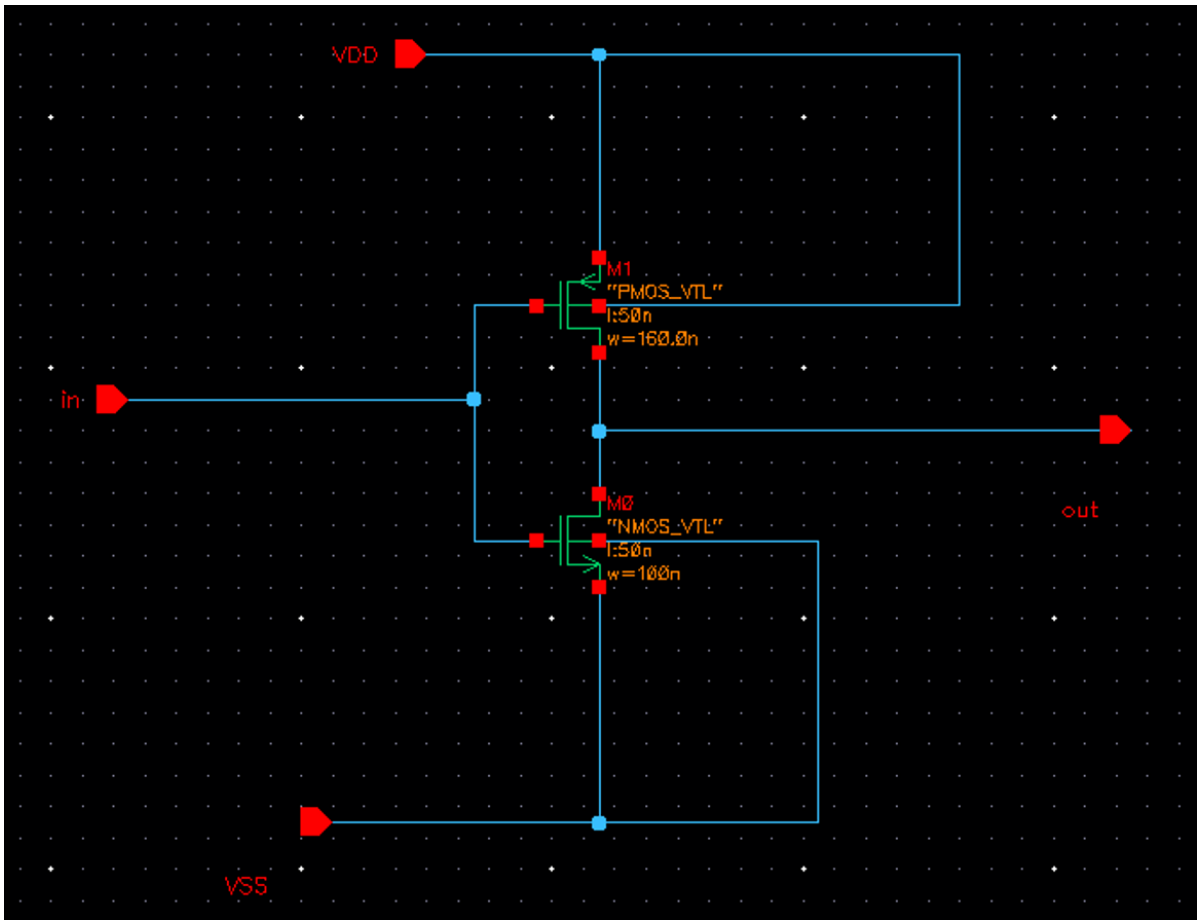


High to Low Propagation Delay: 3.472 ps

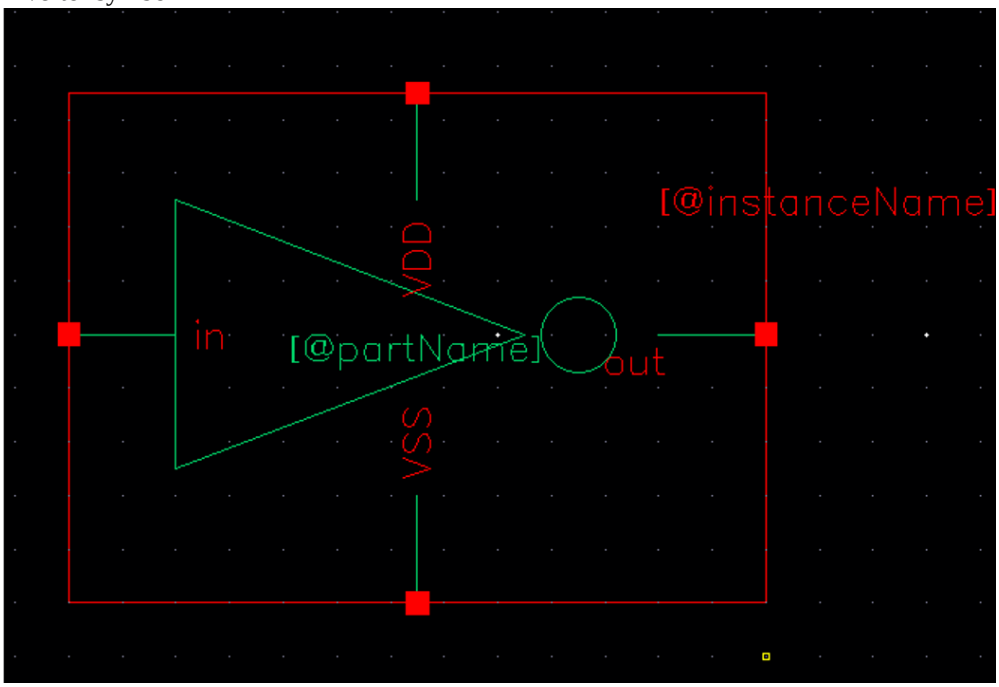
Low to High Propagation Delay: 6.797 ps

Q 2.

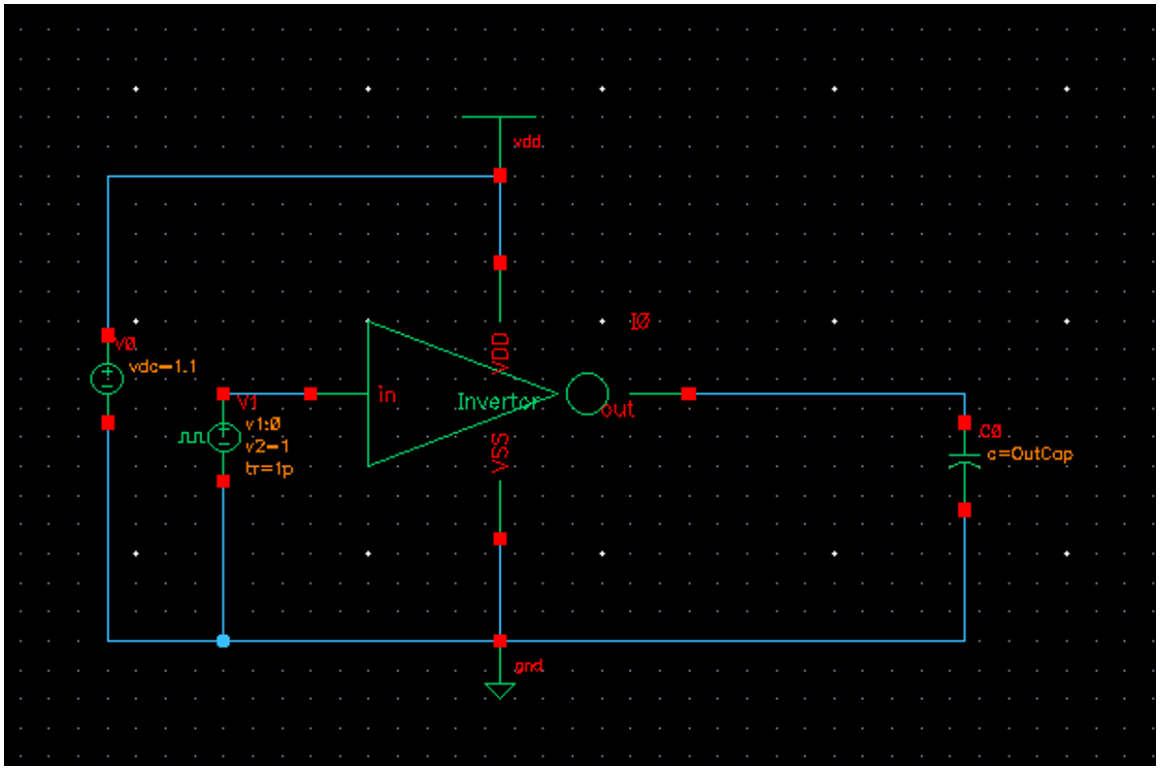
Inverter Schematic view



Invertor symbol

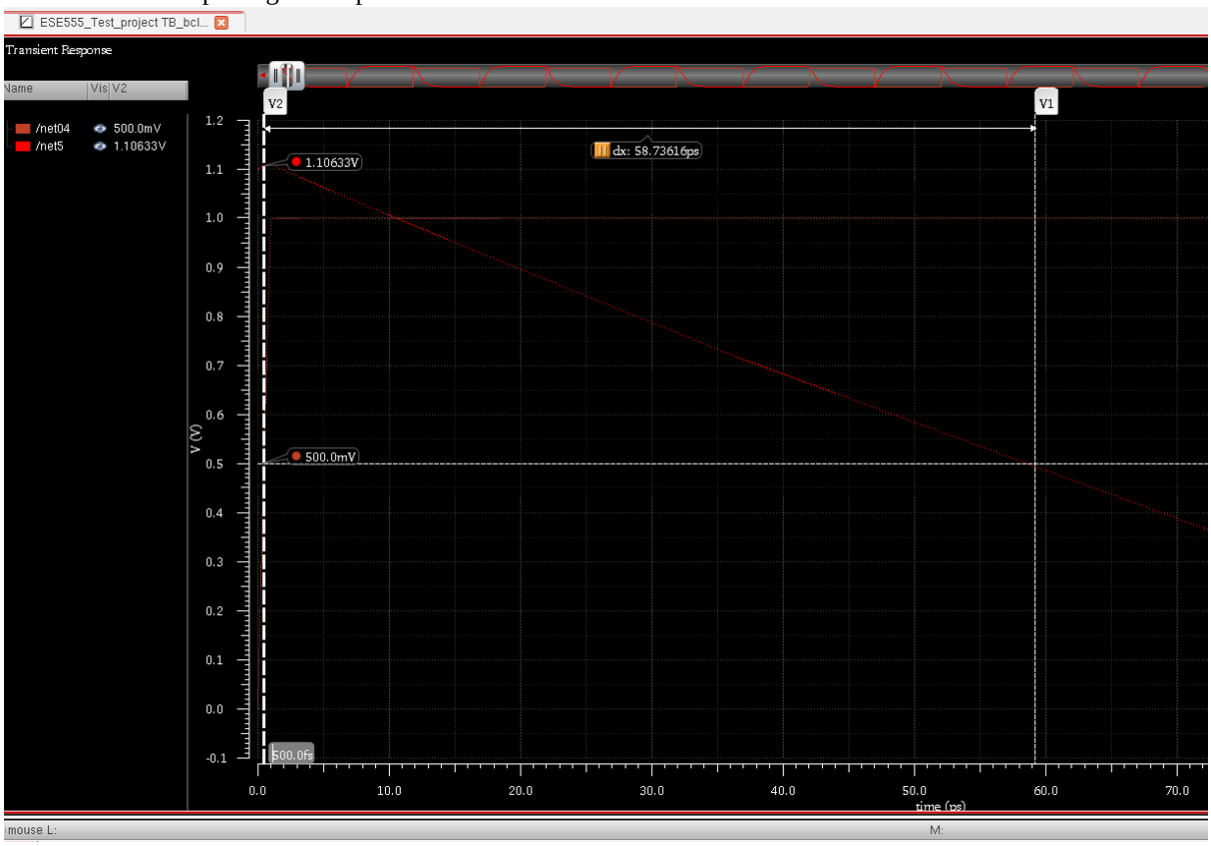


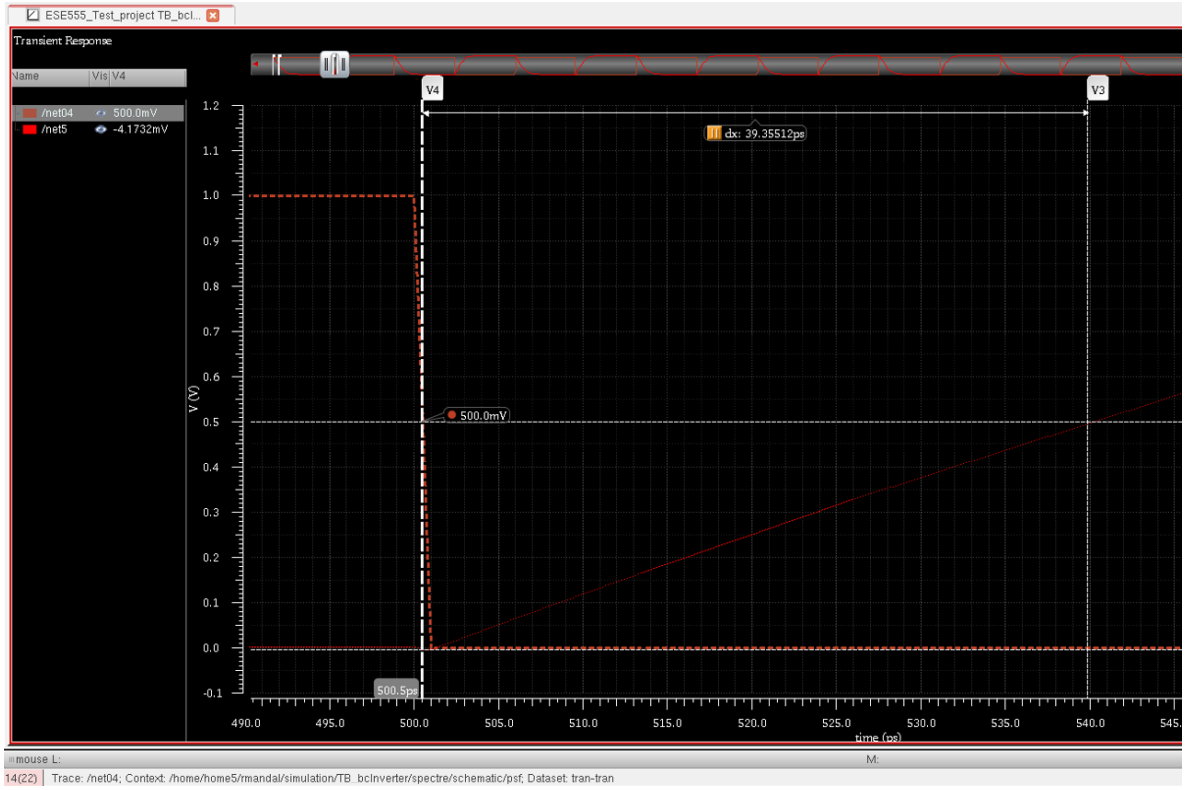
Invertor Circuit



i. inverter test – transient analysis – 2nm period/50% duty cycle
ii. transient analysis(5 clock cycles, 10ns) schematic netlist, high-to-low and low-to-high
iii. rise and fall

a. Rise and Fall of Input Signal is 1ps

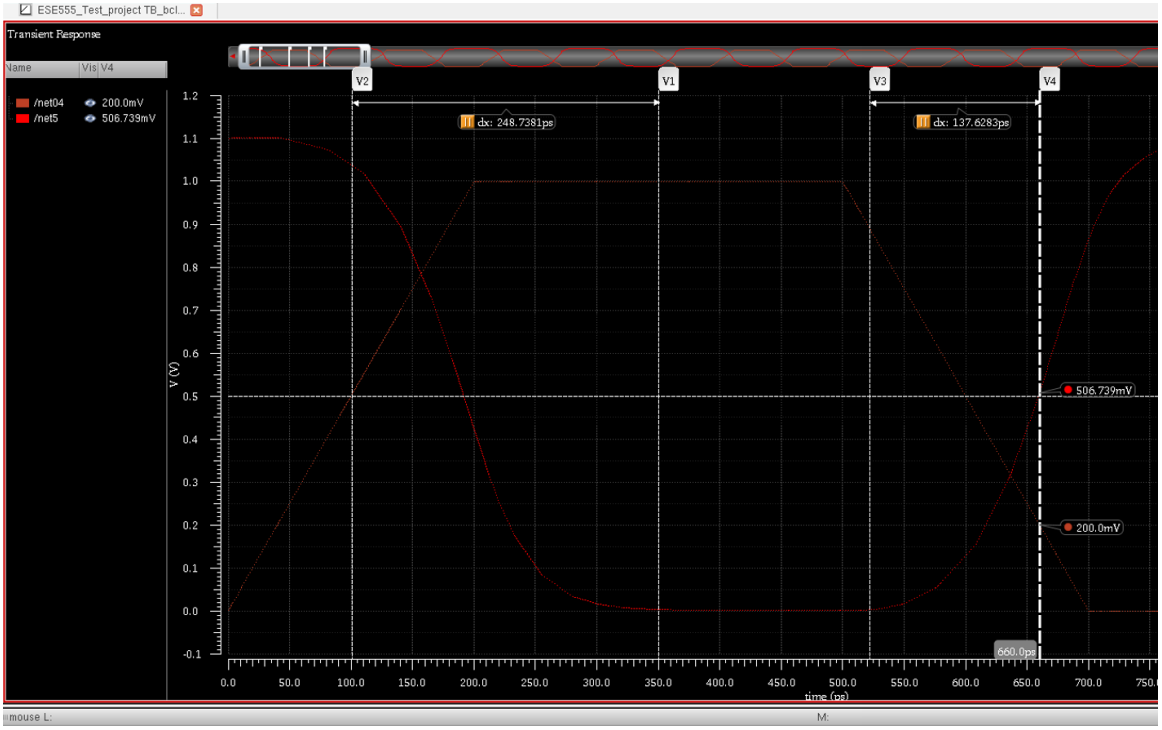




The high to low propagation delay is 58.7361ps

The low to high propagation delay is 39.3551ps

b. Rise and Fall of Input Signal is 200ps



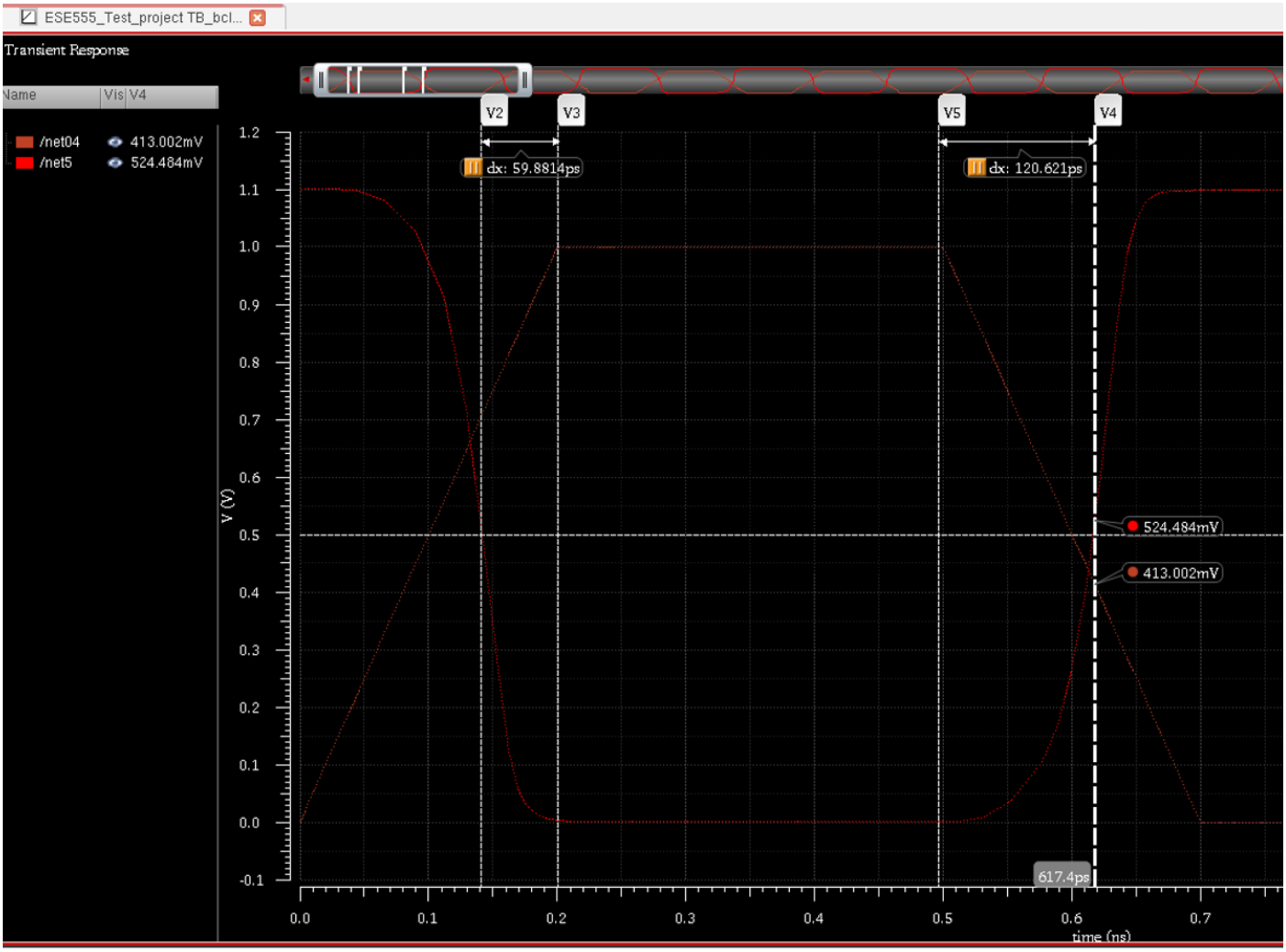
The high to low propagation delay is 92.7236ps

The low to high propagation delay is 137.6283ps

c. In calculation in Q#1, the results were: High to Low Propagation Delay: 3.47 ps, Low to High Propagation Delay: 6.79 ps.

In simulation in Q#2, results were: high to low propagation delay is 58.7361ps and low to high propagation delay is 39.3551ps for 1ps and high to low propagation delay is 92.7236ps and low to high propagation delay is 137.6283ps for 200ps.
The simulation shows us higher values. This difference in observations is because of components like junction capacitance and such properties that the input signal will now need to overcome.
When we are doing the layout, we need to consider other such factors, so the resultant delay is usually even higher.

Q 3.



The high to low propagation delay is 59.8914ps

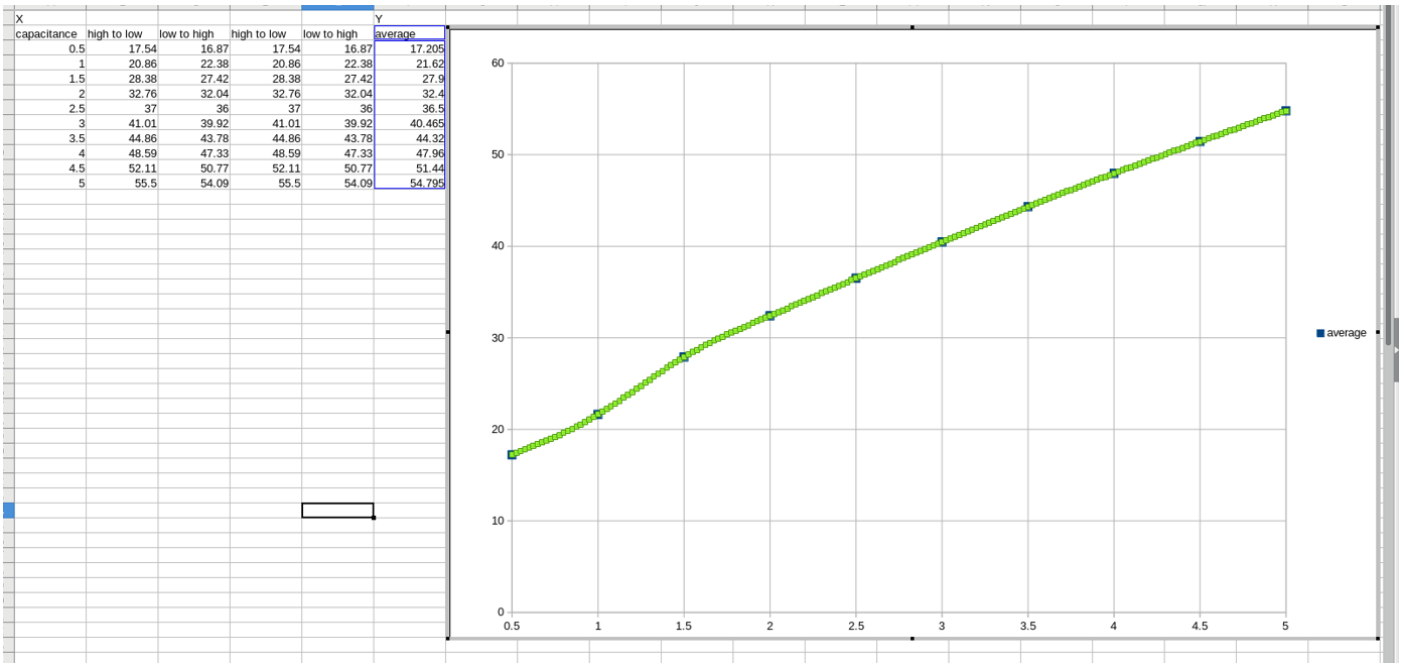
The low to high propagation delay is 120.621ps

Q 4.

Load capacitance: 0.5fF-5fF (in steps of 0.5fF)

Transient analysis was done to find low-to-high and high-to-low propagation delays.

Plot of average propagation delay ((low-to-high+high-to-low)/2) versus output load capacitance:



X			Y		
capacitance	high to low	low to high	high to low	low to high	average
0.5	17.54	16.87	17.54	16.87	17.205
1	20.86	22.38	20.86	22.38	21.62
1.5	28.38	27.42	28.38	27.42	27.9
2	32.76	32.04	32.76	32.04	32.4
2.5	37	36	37	36	36.5
3	41.01	39.92	41.01	39.92	40.465
3.5	44.86	43.78	44.86	43.78	44.32
4	48.59	47.33	48.59	47.33	47.96
4.5	52.11	50.77	52.11	50.77	51.44
5	55.5	54.09	55.5	54.09	54.795

Q 5.

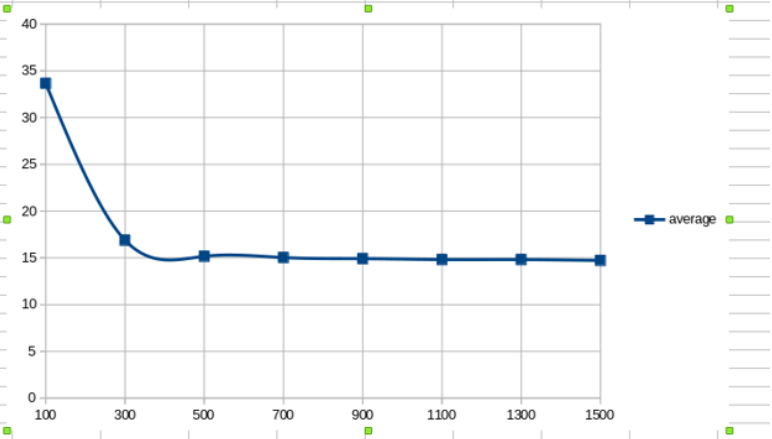
Output load is kept constant at 2fF

Wn is sweeped until 1.5 um (with step size of 200 nm) while keeping Wp/Wn constant,

Transient analysis is done to determine low-to-high and high-to-low propagation delays.

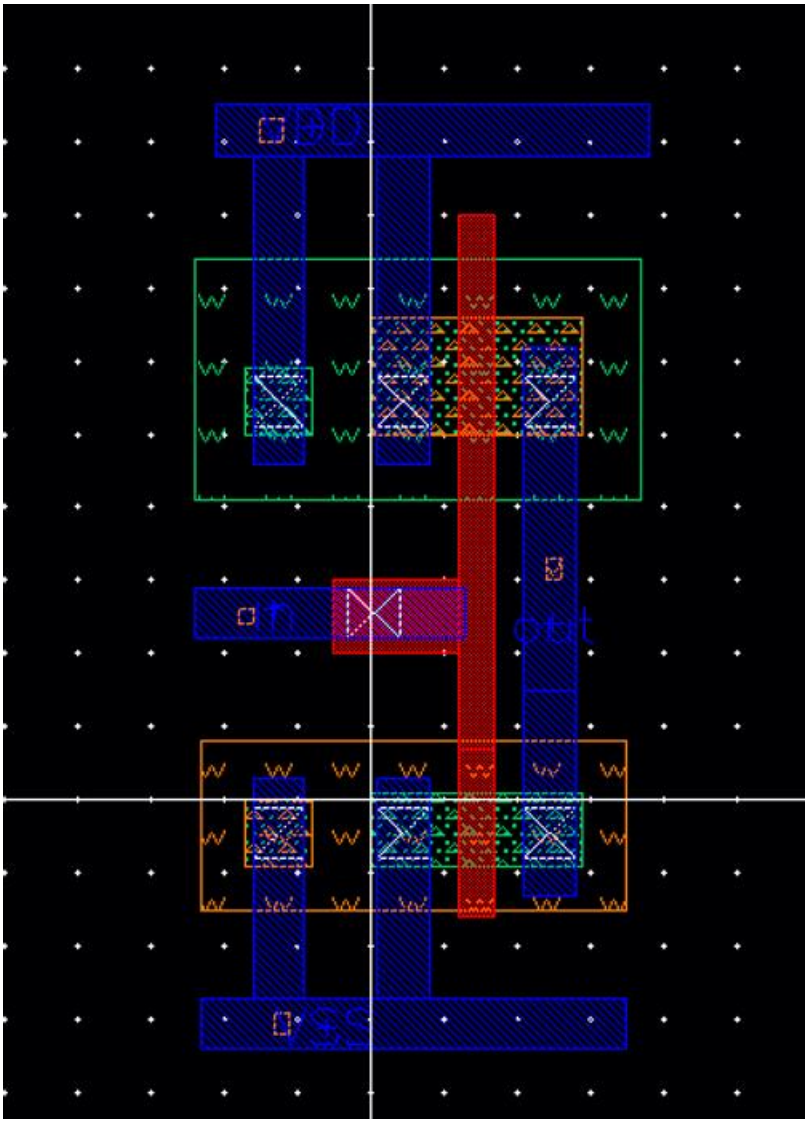
Plot of average propagation delay ((low-to-high+high-to-low)/2) versus Wn:

Wn(nM)	high to low	low to high	high to low	low to high	average
100	15.27	52.1	15.2	52.06	33.6575
300	1.28	32.53	1.21	32.53	16.8875
500	2.13	28.21	2.12	28.21	15.1675
700	3.72	26.35	3.72	26.35	15.035
900	4.7	25.18	4.6	25.18	14.915
1100	5.28	24.37	5.26	24.37	14.82
1300	5.75	23.91	5.7	23.91	14.8175
1500	5.92	23.5	5.97	23.5	14.7225

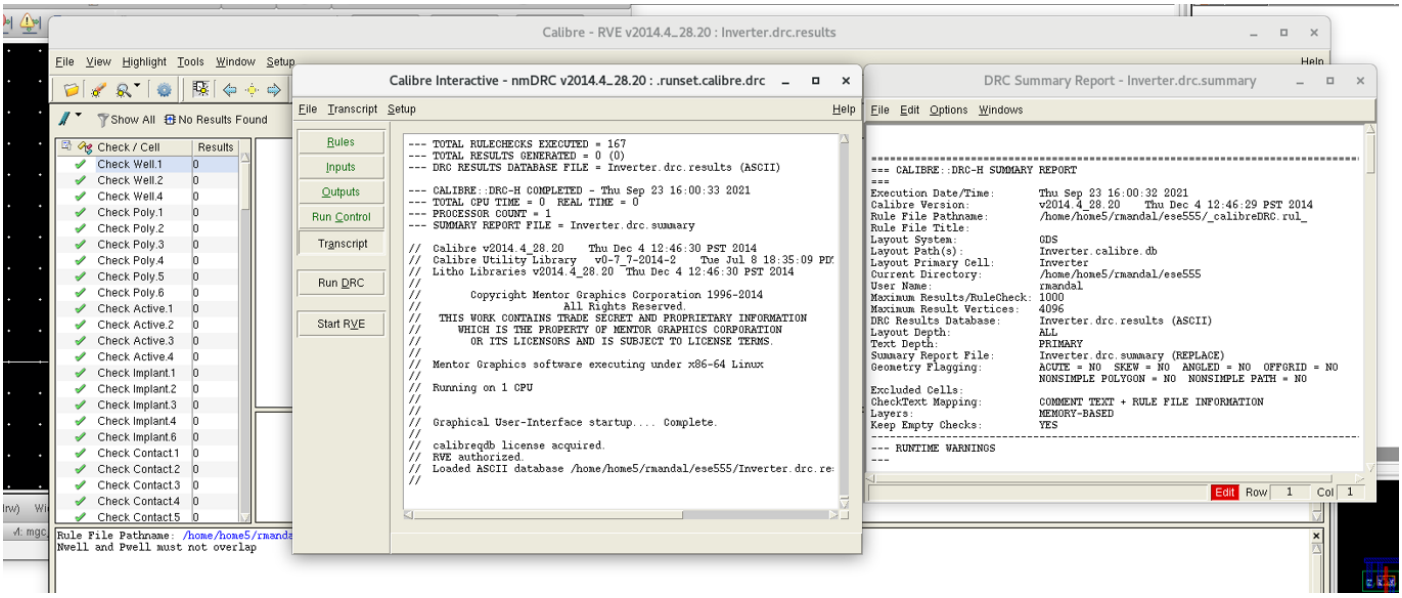


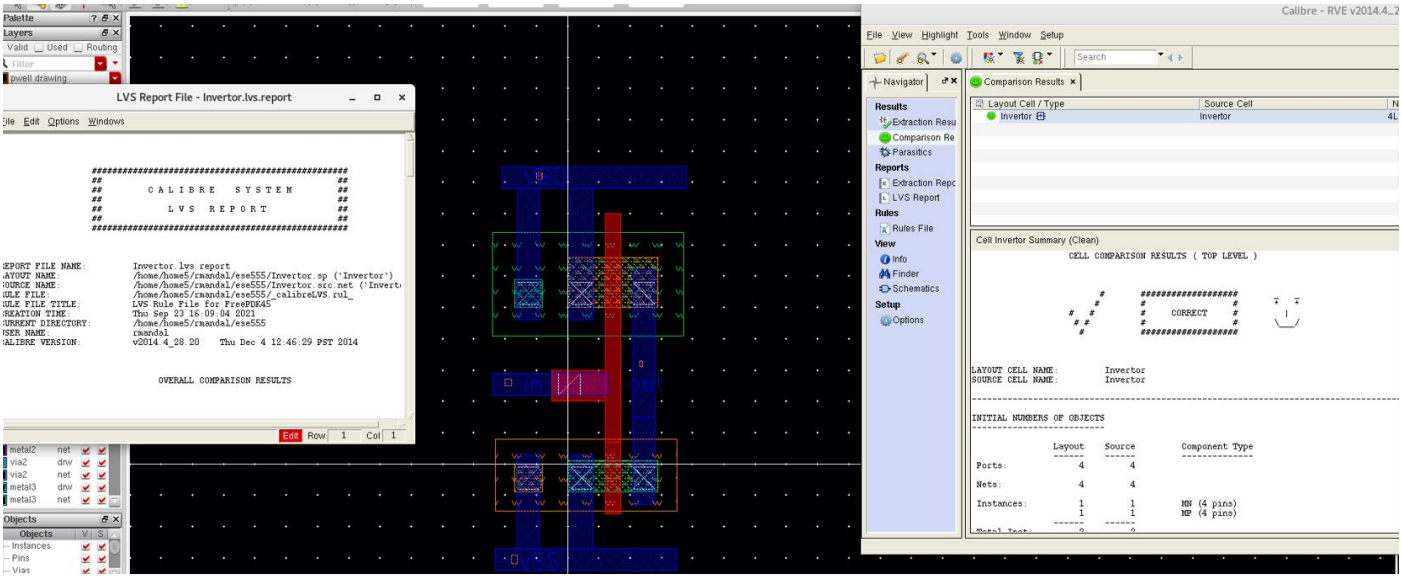
Q 6.

Inverter Physical Layout



Pass DRC & LVS

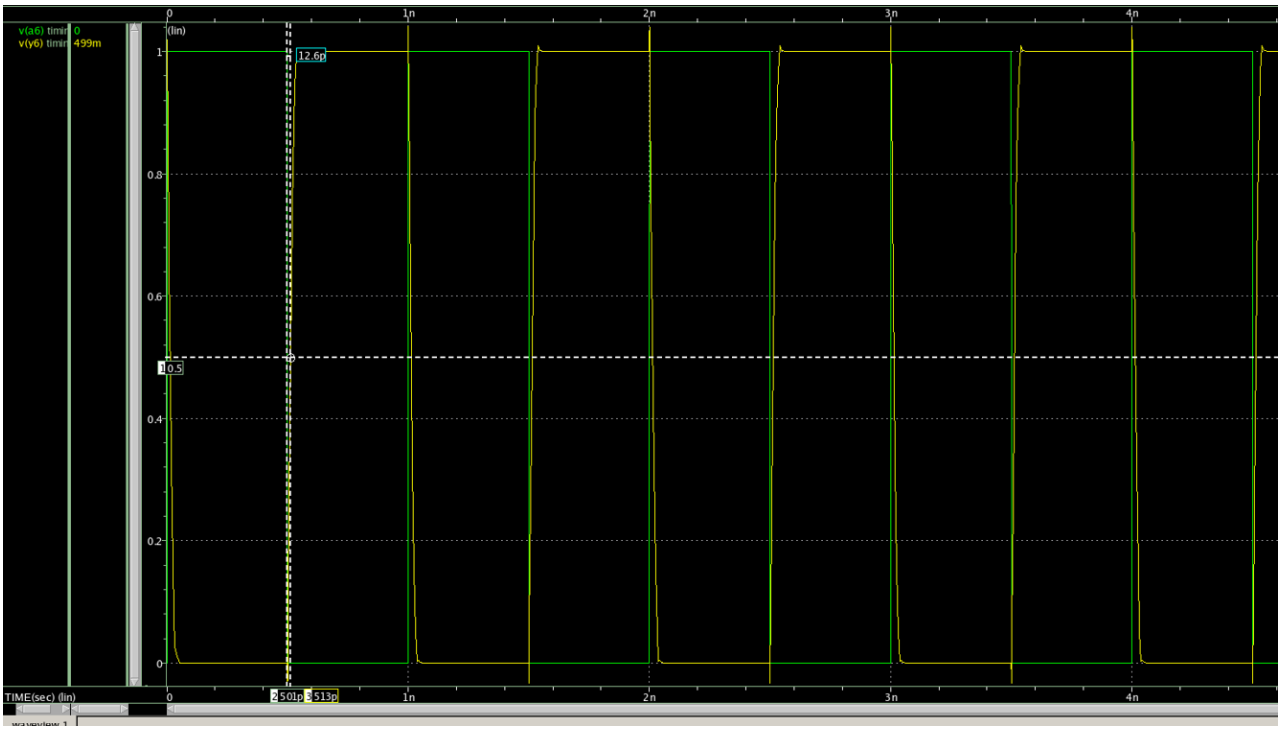



Palette
Layers
Valid
Used
Routing
pwell drawing
LVS Report File - Invertor.lvs.report
File Edit Options Windows
CALIBRE SYSTEM
LVS REPORT
REPORT FILE NAME: Invertor.lvs.report
LAYOUT NAME: /home/home5/rmandal/ese555/Invertor.sp ('Invertor')
SOURCE NAME: /home/home5/rmandal/ese555/Invertor.src.net ('Invertor')
RULE FILE: /home/home5/rmandal/ese555/_calibreLVS.rul_
RULE FILE TITLE: LVS Rule File for FreePDK45
CREATION TIME: Thu Sep 23 16:09:04 2021
CURRENT DIRECTORY: /home/home5/rmandal/ese555
USER NAME: rmandal
CALIBRE VERSION: v2014.4_28.20 Thu Dec 4 12:46:29 PST 2014
OVERALL COMPARISON RESULTS
Edit Row 1 Col 1
Objects
Instances
Pins
Vias
Calibre - RVE v2014.4_2
File View Highlight Tools Window Setup
Search
Navigator
Comparison Results
Results
Extraction Resu
Comparison Re
Parasitics
Reports
Extraction Repc
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Layout Cell / Type
Source Cell
Invertor
Invertor
Cell Invertor Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: Invertor
SOURCE CELL NAME: Invertor
INITIAL NUMBERS OF OBJECTS
Layout Source Component Type
Ports: 4 4
Nets: 4 4
Instances: 1 1 MN (4 pins)
1 1 MP (4 pins)

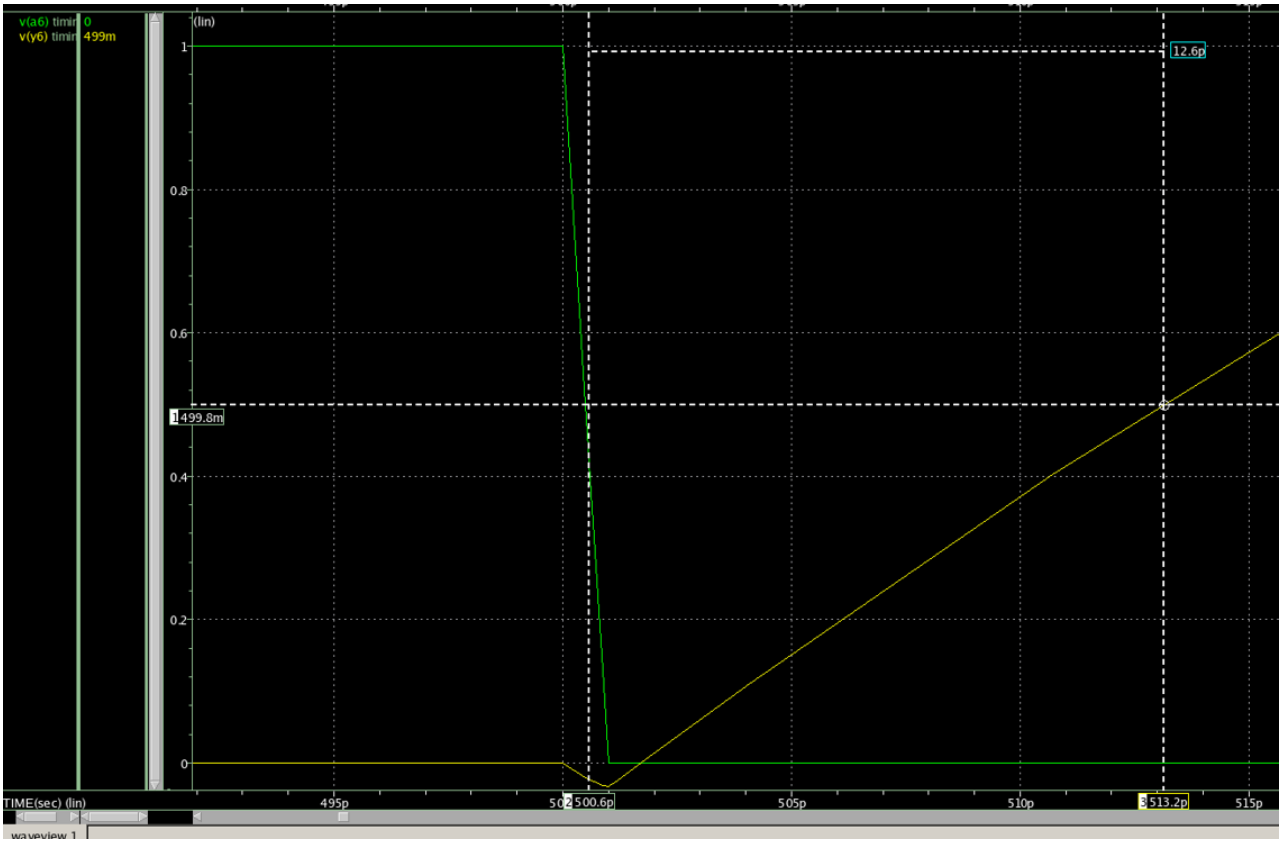
Q 7.

HSPICE simulation

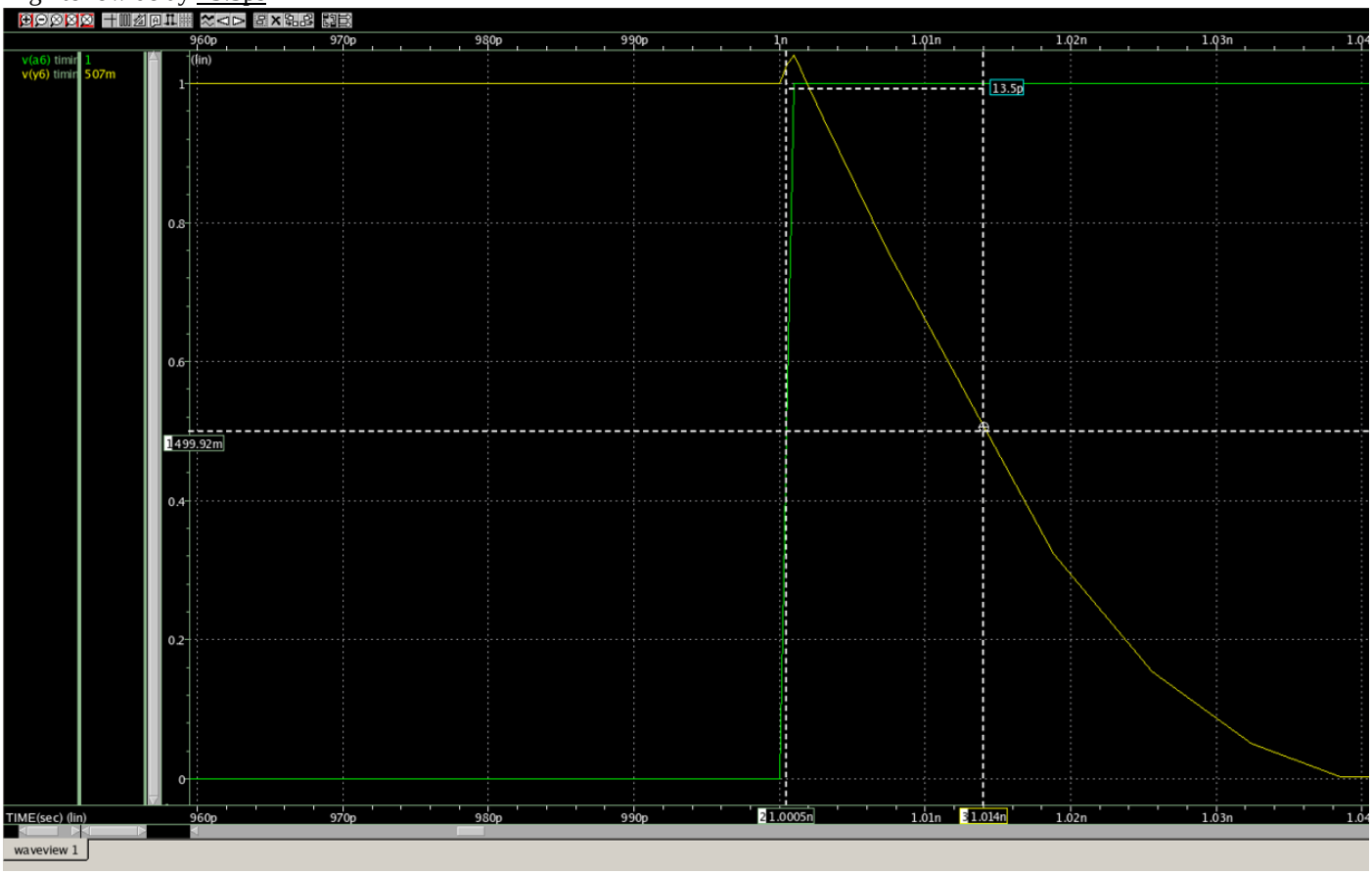
a) Rise & Fall Input Signal is 1ps



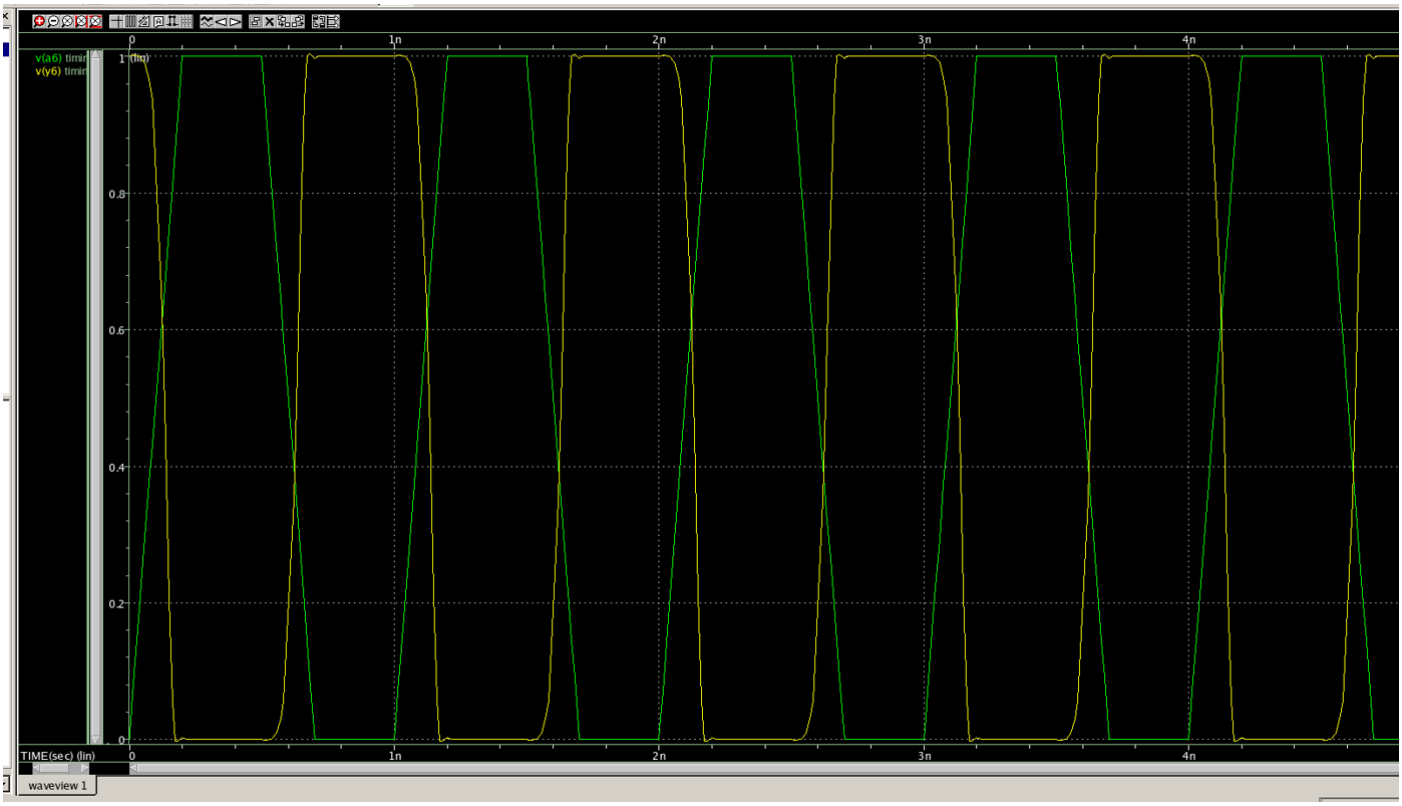
Low to High delay is 12.6ps



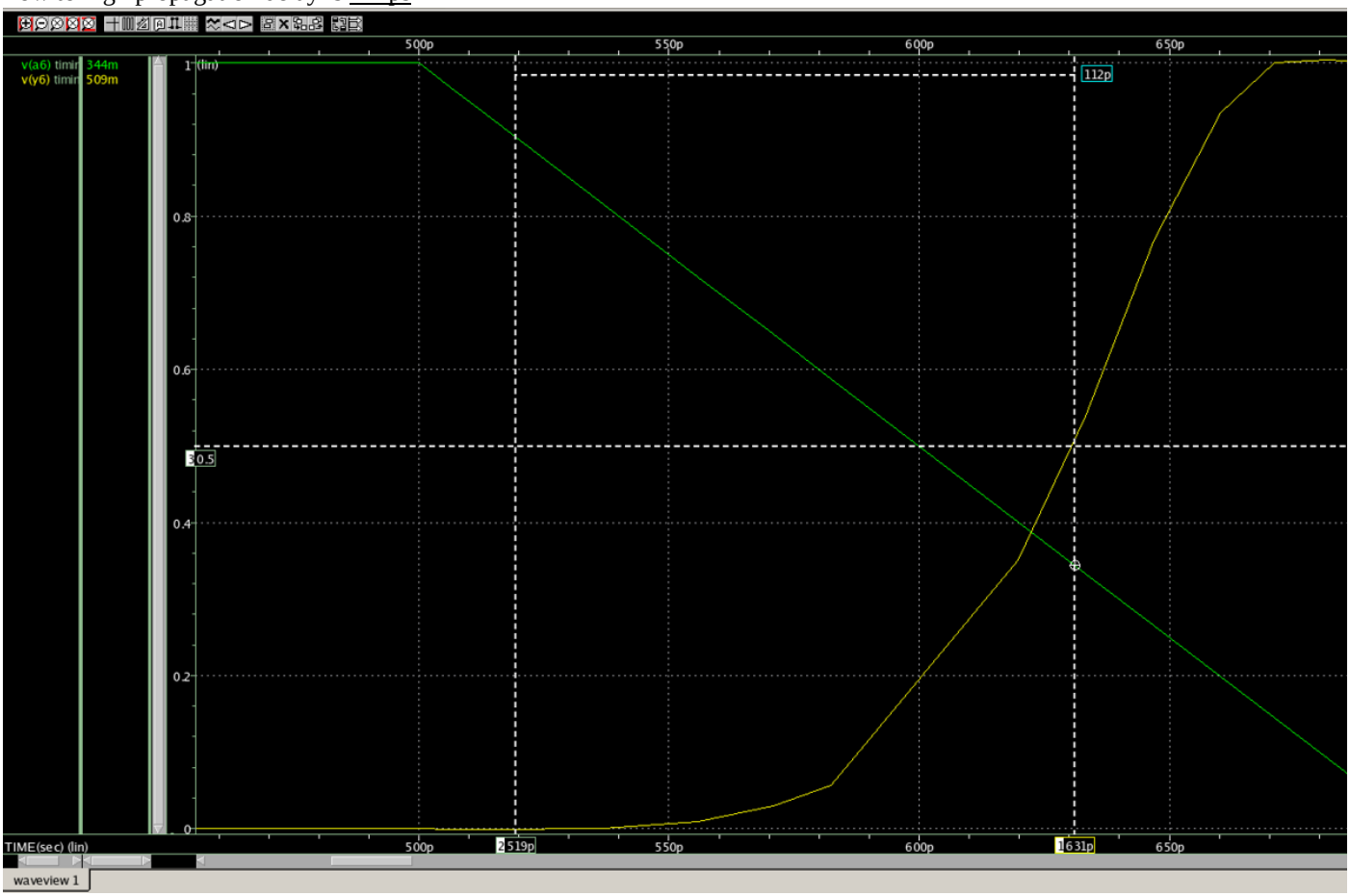
High to low delay 13.5ps



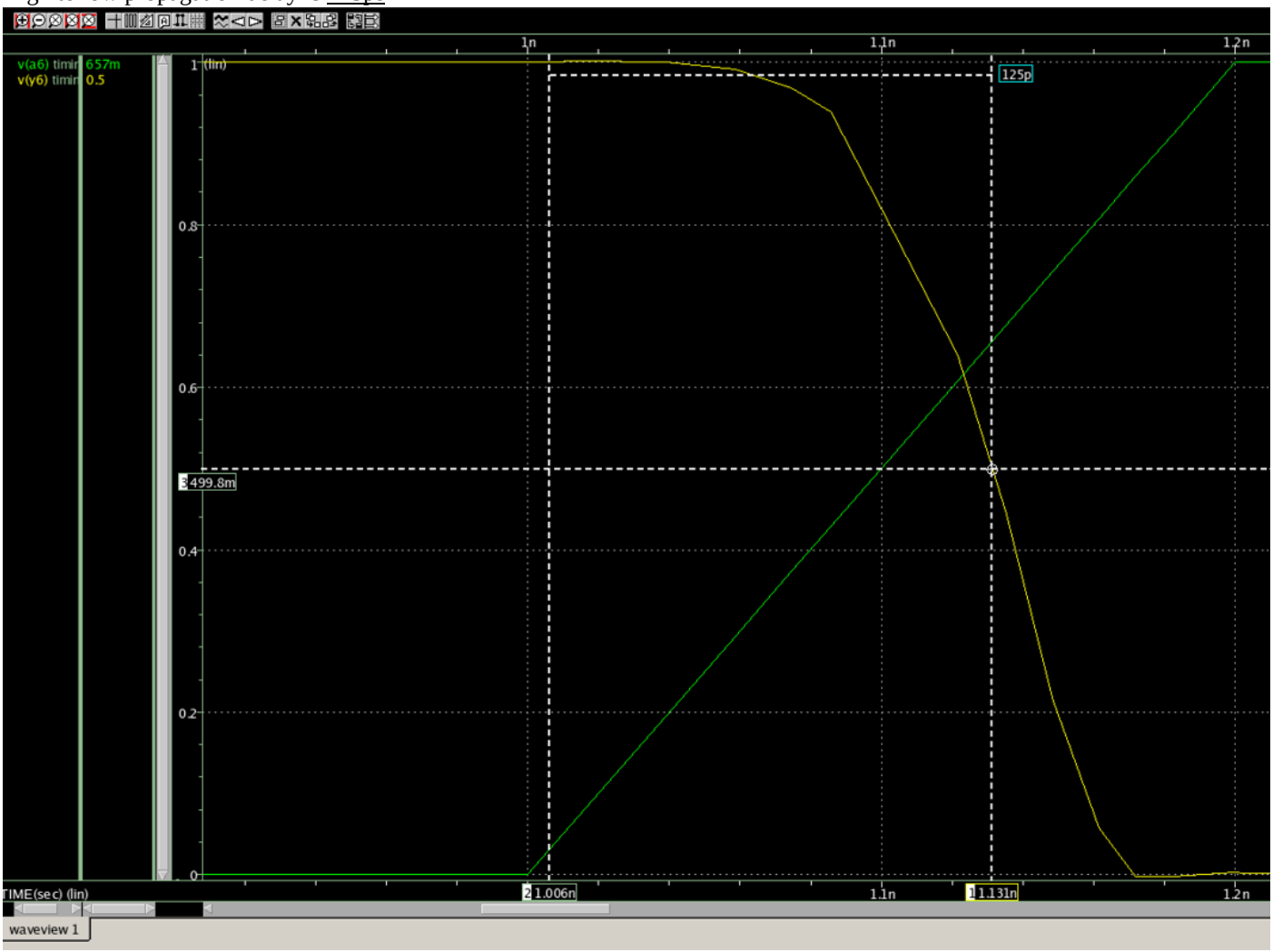
b) Rise & Fall Input Signal is 200ps



Low to high propagation delay is 112ps



High to low propagation delay is 125ps



c) Our extracted netlist simulation results show higher values than schematic netlist. The result is due to factors such as junction capacitance, that input signals will need to overcome and thus add to the delay.