Design and Verification of a Pipelined Synchronous 8-bit Carry Select Adder

ESE555 VLSI System Design Fall 2021 - Project Report

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Abstract

This project demonstrates the designing of the schematic and layout of a pipelined synchronous 8-bit carry select adder, and evaluation of the performance of the same. The system is designed using 45nm CMOS process technology. The 8-bit Carry Select adder is composed of 3, 4-bit ripple carry adders, and a set of multiplexers are used to select the carry. The entire design further uses D-Flip Flops based pipelining at the main input and outputs pin to achieve higher clock frequency. The design is further validated for proper functionality at 4Ghz clock frequency, and the design was optimized to minimize power consumption, so the system consumes an average power of 52.91e-6W.

Introduction

CMOS Adders are digital circuits used for addition of binary numbers. While Half adders just add two input signals and results in a two-bit output, a Full adder takes this further: A Full adder circuit will take 3 logic inputs: A, B and a Carry-In (potentially from another Adder) and provides a 2-bit output – Sum and Carry-out. CMOS Adders use NMOS Pull-Down networks and PMOS Pull-up networks.

Ripple Carry Adders employ a series of full Adders for binary addition of signal inputs, and the carry outputs are propagated serially to the next adder in the circuit. Delay is proportional to the number of input bits.

Carry skip Adders involve using skip logic in processing the carry bits, which speeds up operation by shortening the critical path.

Carry Increment Adders use Ripple Carry Adders and incremental circuity which uses Half adders in a ripple carry chain with a sequential order.

Carry Select adder architecture involves using independent computation of sum and carry signals: both Cin(0) and Cin(1) are processed concurrently, and subsequently a multiplexer is employed to select the sum based on the carry input. This reduces the delay at the cost of increased circuit complexity. We will be using this architecture in our project.

Carry Select Adder Design

The 8-bit Carry Select Adder design employs multiple Mirror Full Adders for single bit addition, Multiplexers for the selection stage, and flip flops for optimizing the circuit.

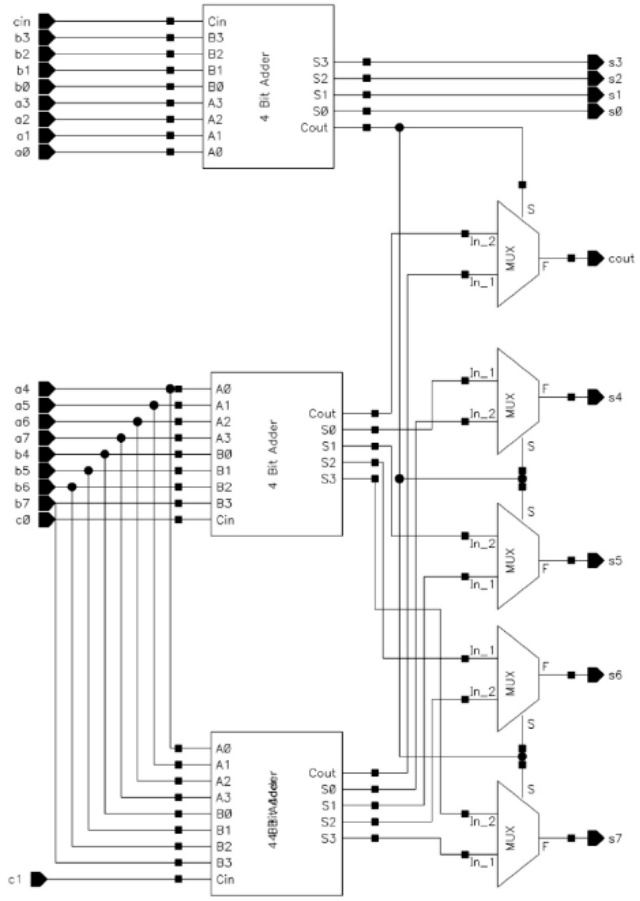
We cover the detailed design of the building blocks in the following subsections:

<u>Block Level Architecture</u>

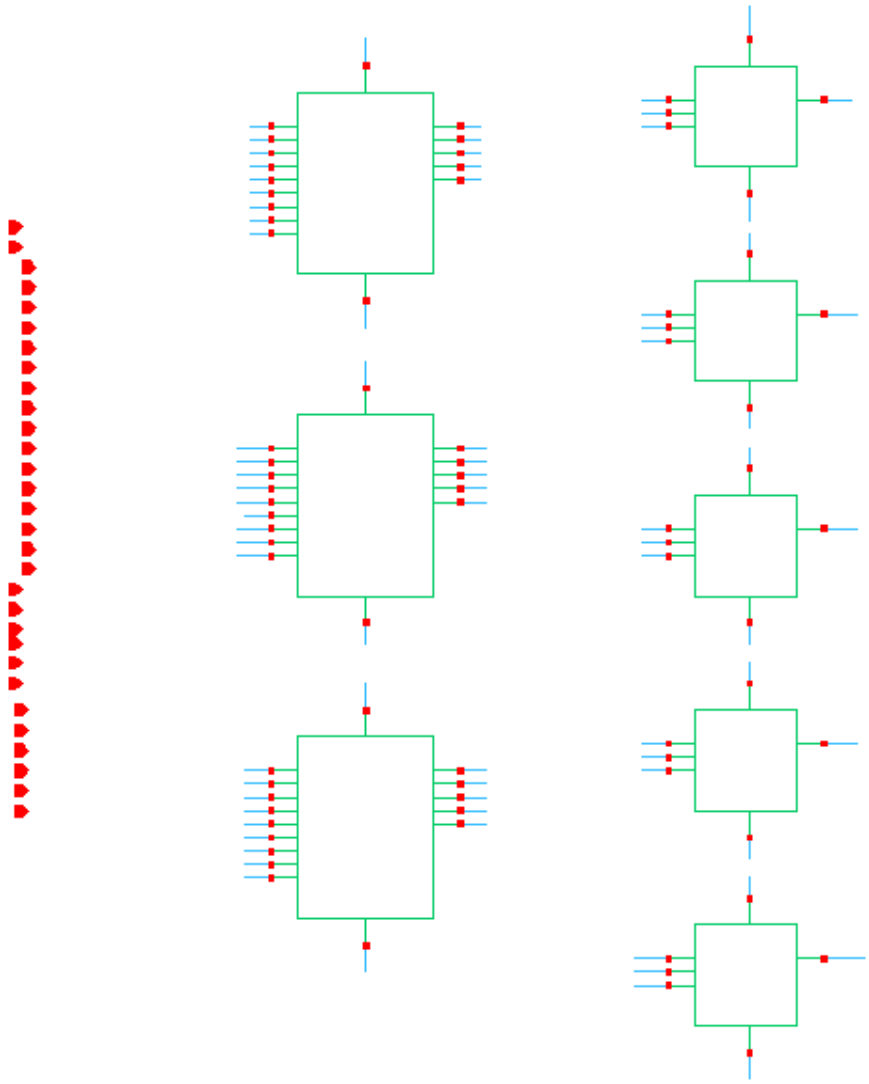
The 8-bit CSA has 2 groups:

Lower order bits (a3...a0 & b3...b0) fed into the first 4-bit adder, for the lower sum bits (s3...s0), and the carry out of this is used to select the higher order bits.

Two 4-bit adders, each compute the sum of s4...s7 and Cout, for both cases when Cin is 0 or 1, and a Mux is used to select the correct result based on the carry out of the first.



Schematic



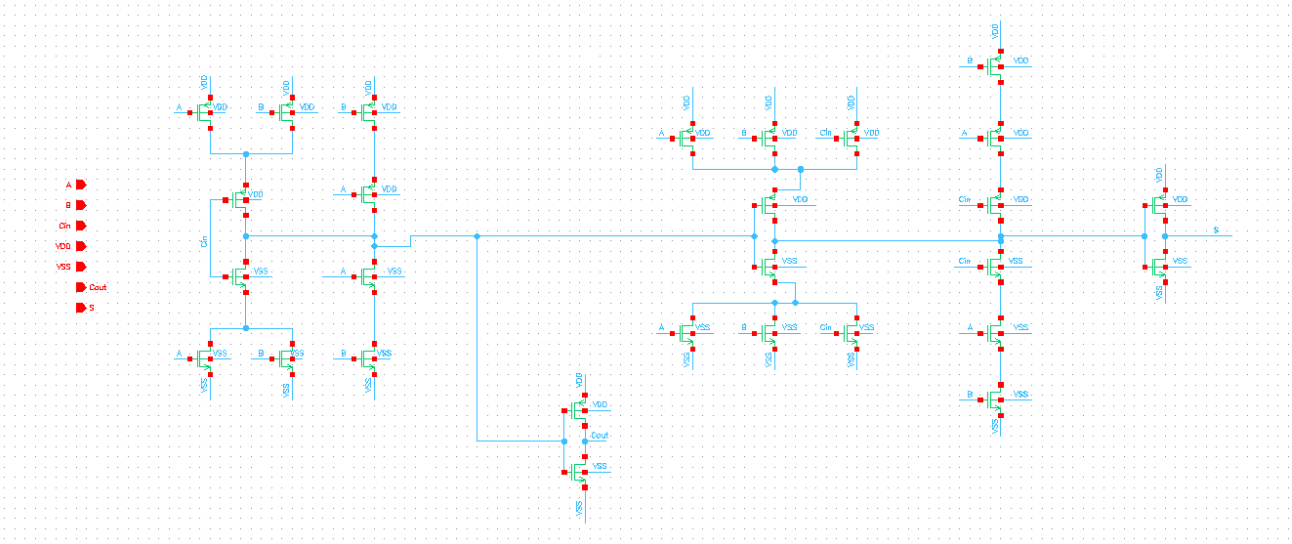
1 Bit Full Mirror Adder

In our design, Static CMOS logic is used for the full adder due to the advantages over other architectures in speed, power and delay. Our Full Mirror Adder is optimized by reusing the Cout signals to compute the Sum, as demonstrated with the following equations:

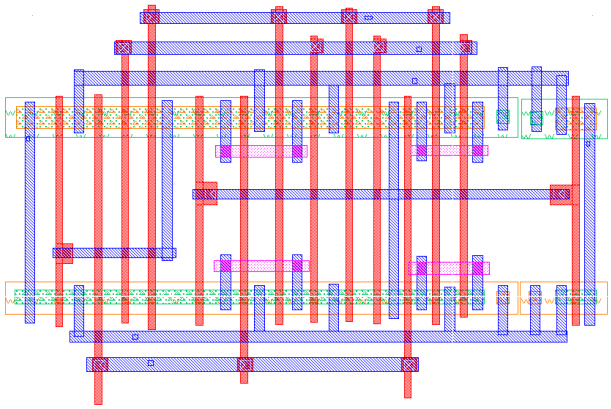
$$S = ABC_{in} + (A + B + C)\overline{C_{out}} \qquad (1)$$

$$C_{out} = AB + BC_{in} + AC_{in} \qquad (2)$$

Schematic:

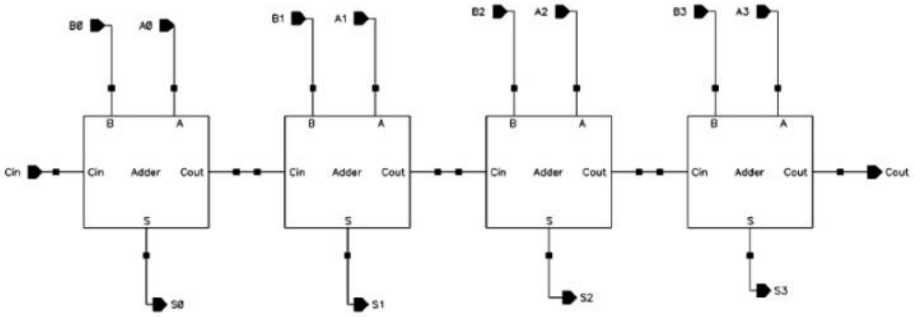


Layout:

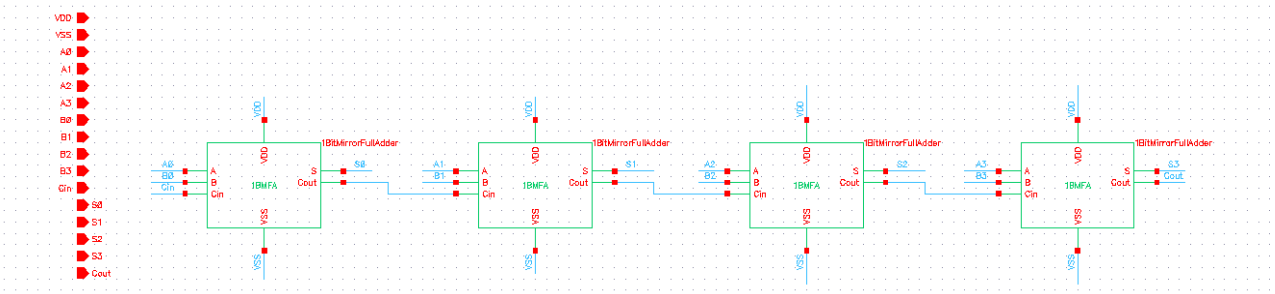


4 Bit Ripple Carry Adder

The RCA design involves “rippling” carry bit from the last adder to the next. Cin is the input carry signal. Two binary numbers, a3...a0 & b3..b0 are computed. Cout of each adder is fed into the Cin of the next adder. Cout of the final adder is the output carry, and the sum outputs of each one bit adder forms the output sum.



Schematic:



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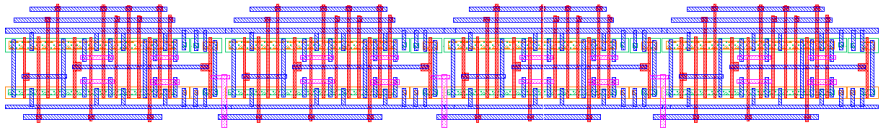
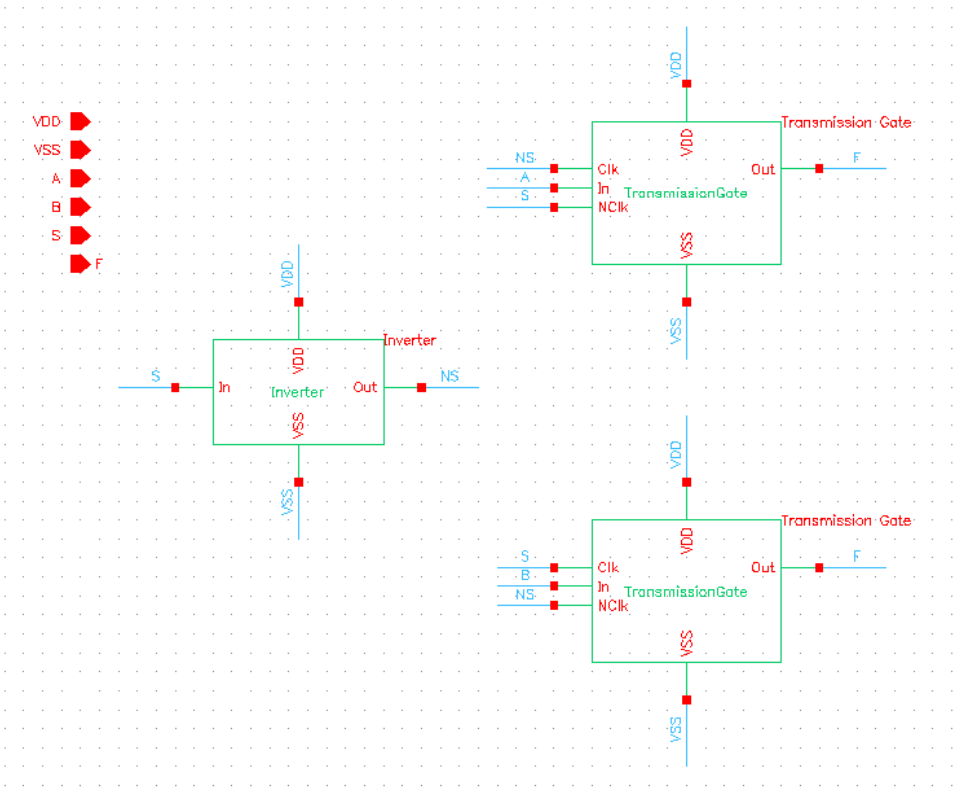


2x1 Multiplexer

A 2x1 Multiplexer composed of Transistor gates is used in the adder design for selecting the higher order sum bits, based on the carry-out of the lower order bits adder. The two Transmission gates are implemented to perform the selection based on the Select Signals.

Schematic:



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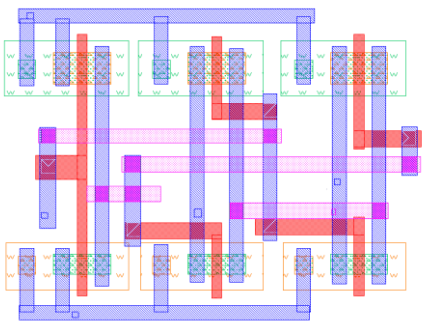
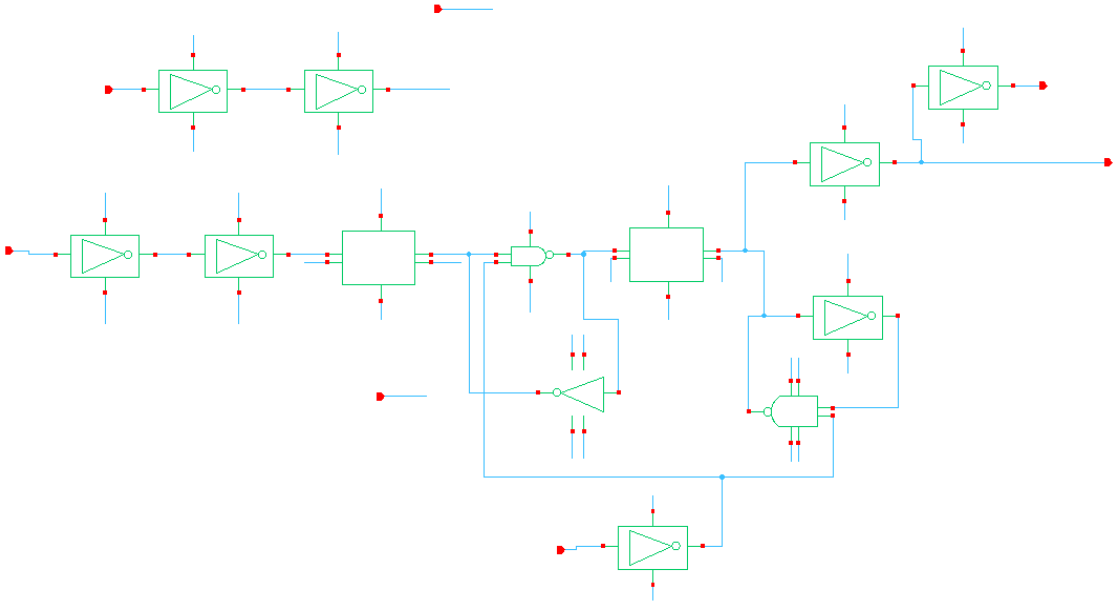


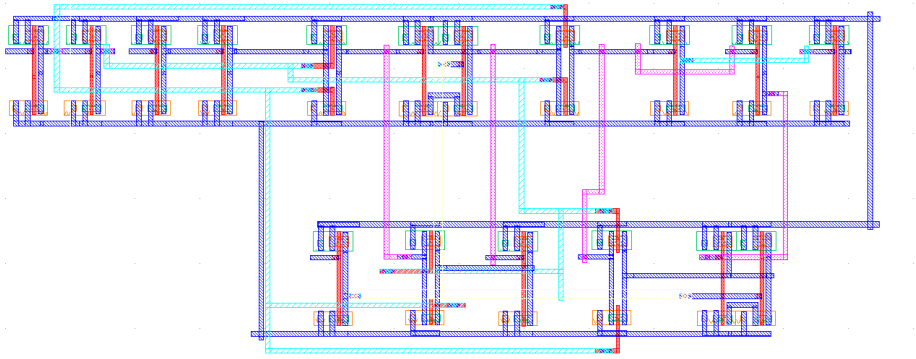
D Flip Flops

Flips flops are implemented in our design for pipelining in order to improve the frequency of operation of our adder. The system is pipelined with flip flops at both the primary inputs and outputs. A CMOS based, Positive edge-triggered master-slave D-type flip-flop was used in this design using a collection of inverters, Transmision gates, NAND gates.

Schematic



Layout



Simulation Results and Discussion

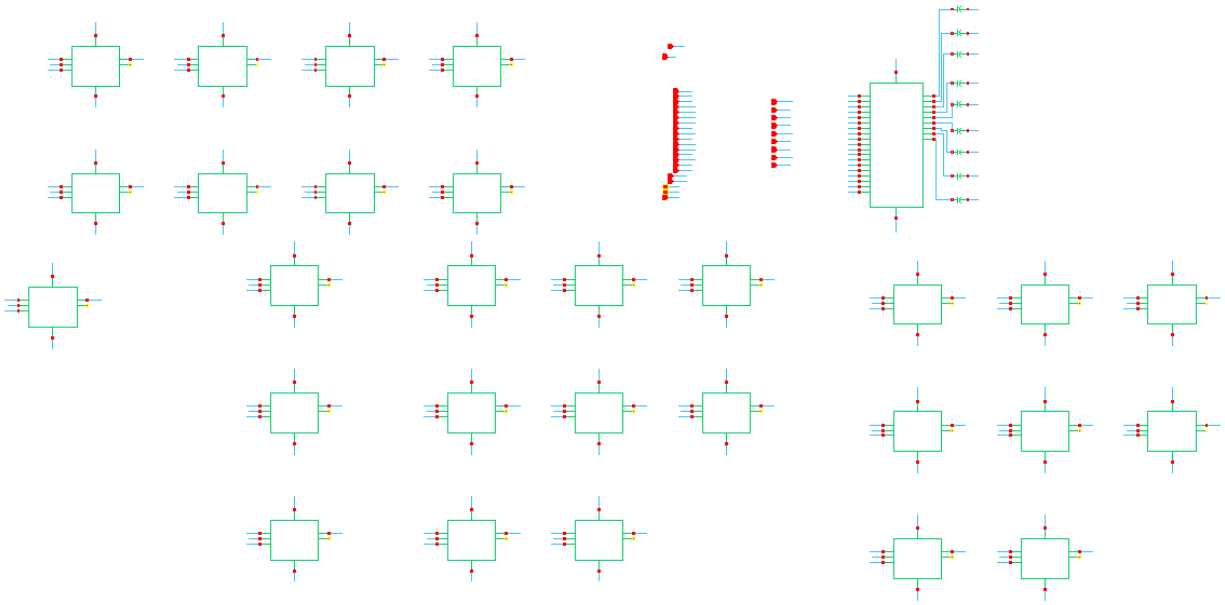
DFFs and Load:

The Adder is designed so that the outputs (s0...s7, Cout) of the adder can drive5fF capacitive load and maintain accurate functioning.

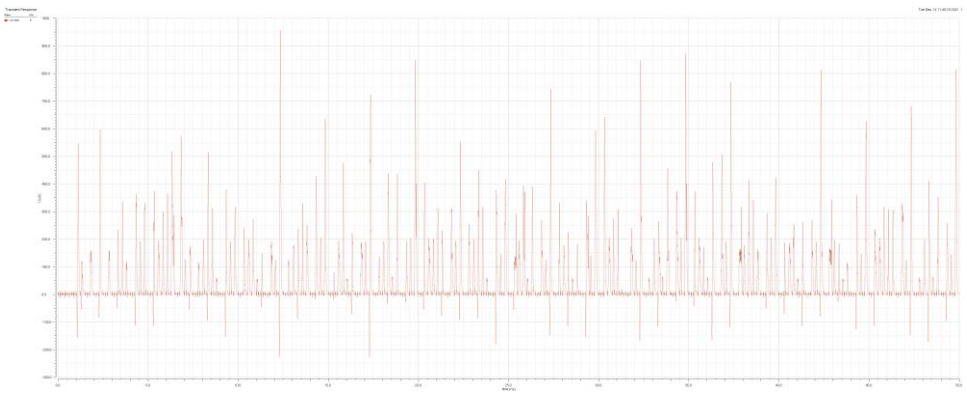
There are two stages of pipelining:

19 Flip-flops at each of the 19 Inputs (a0...a7, b0...b7, Cin, C0, C1)

9 Flip-flops at each of the 9 outputs (s0...s7, Cout)



Power:



Avg Current drawn from VDD over 50ns: 48.1e-6A

VDD: 1.1V

Avg Power: V x I = 52.91e-6W

Power consumption is proportional to (square of) Supply Voltage and Frequency. We operate the circuit at 1.1V supply and at 4Ghz, which are the design constraints of the project. In order to optimize power consumption, we have used 160nm/50nm PMOS gates and 100nm/50nm NMOS gates for the design for proper balance of power consumption and performance.

Simulation Result:

Test Specifications:

Load Capacitance:(s0...s7, Cout): 5fF

Clock Frequency: 4GHz

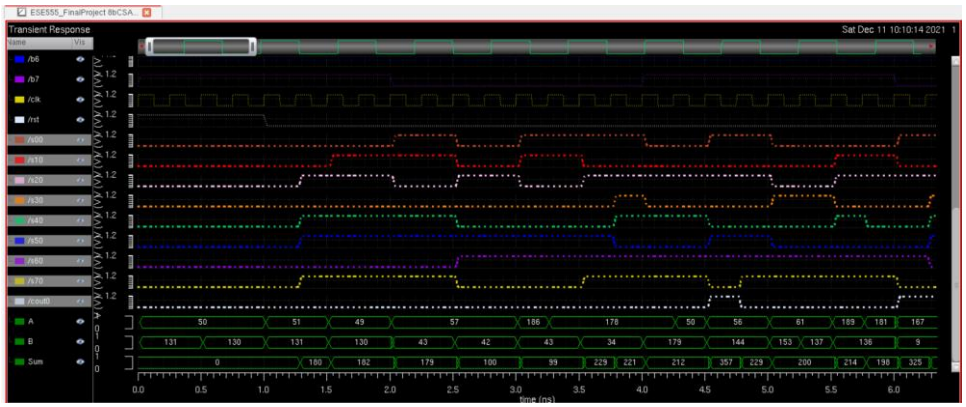
Duty Cycle: 50%

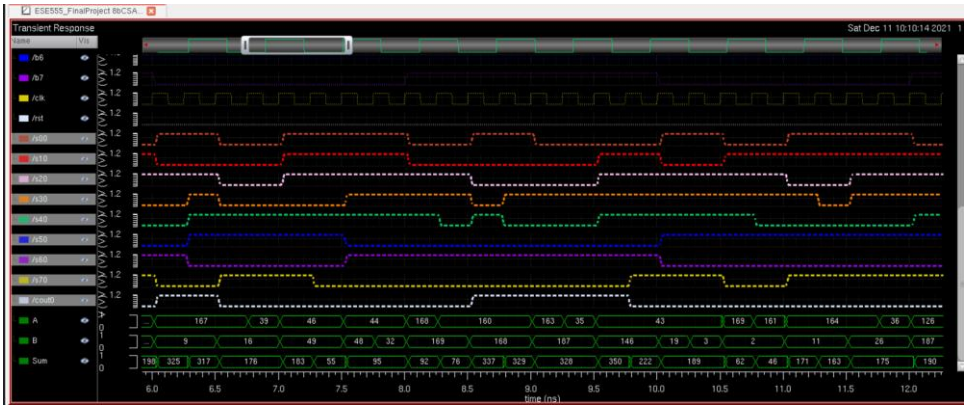
Rise & Fall times(Input & Clock): 25ps

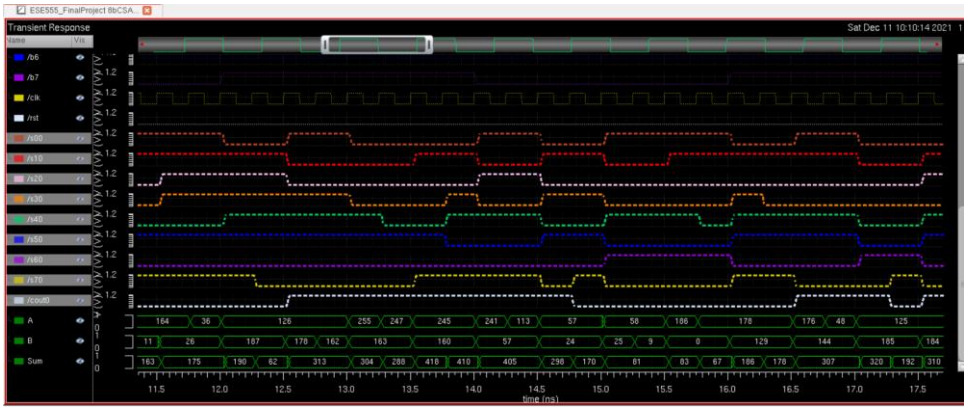
Supply Voltage: 1.1V

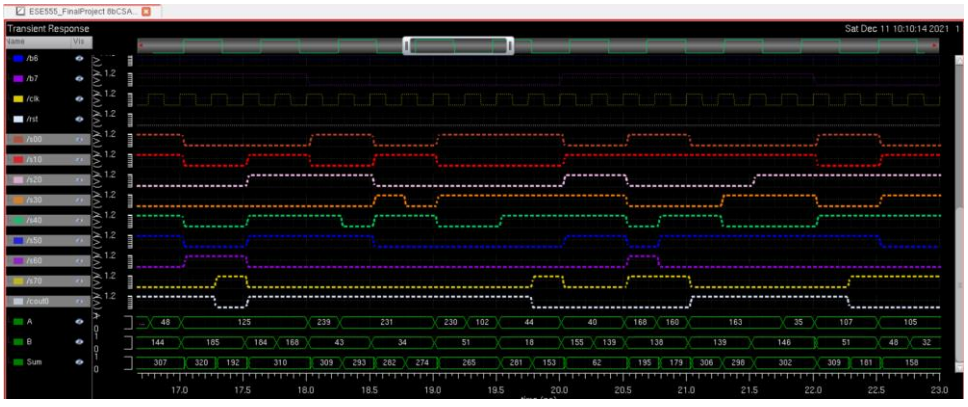
The design is tested at 4GHz frequency; It is observed that operating at higher frequencies can increase glitches in output waveform and increases power consumption.

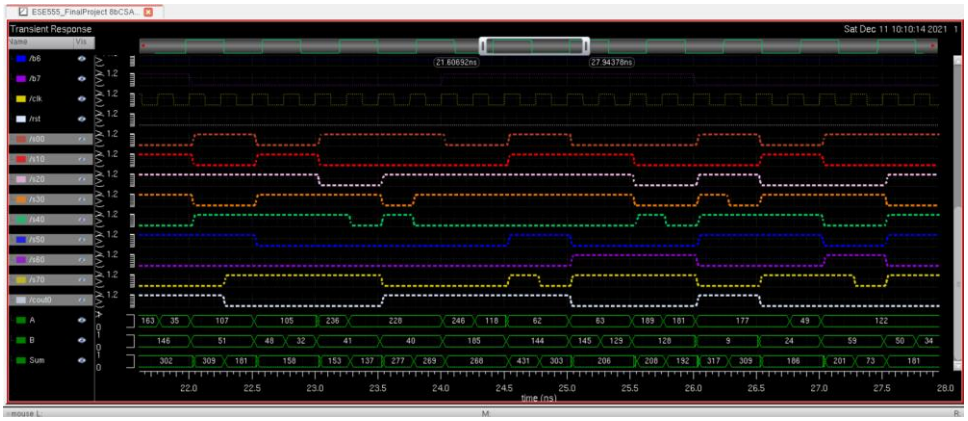
The system is designed to minimize power consumption while ensuring correct functionality at 4Ghz.







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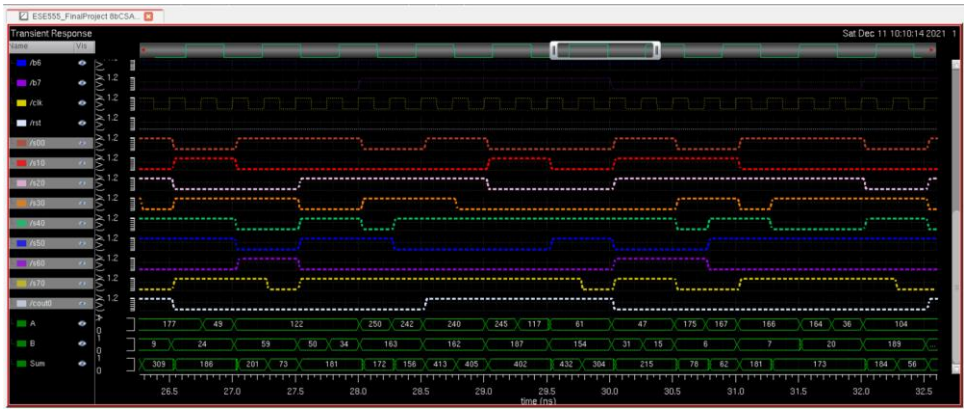
Transient Response
Sat Dec 11 10:10:14 2021
21.60692ns
27.94378ns
/b6
/b7
/clk
/rst
/s00
/s10
/s20
/s30
/s40
/s50
/s60
/s70
/cout0
A
B
Sum
time (ns)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Transient Response
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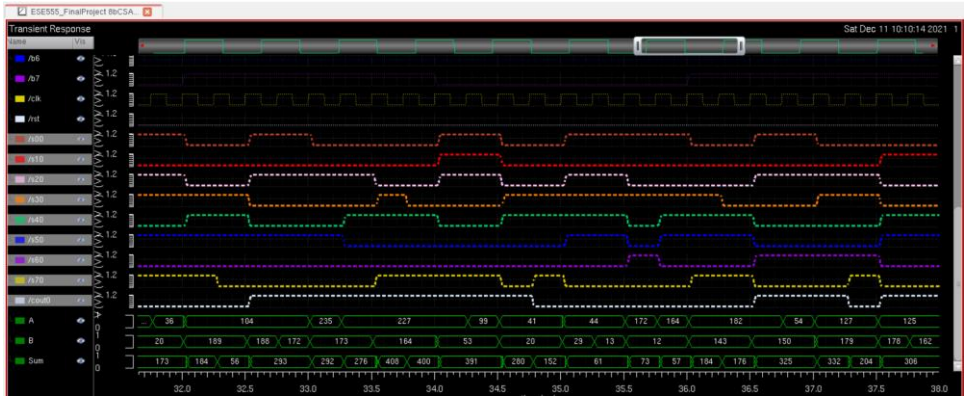
/b6
/b7
/clk
/rst
/s00
/s10
/s20
/s30
/s40
/s50
/s60
/s70
/cout0
A
B
Sum
time (ns)


ESE555_FinalProject 8bCSA..
Transient Response
Sat Dec 11 10:10:14 2021
/b6
/b7
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/rst
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/cout0
A
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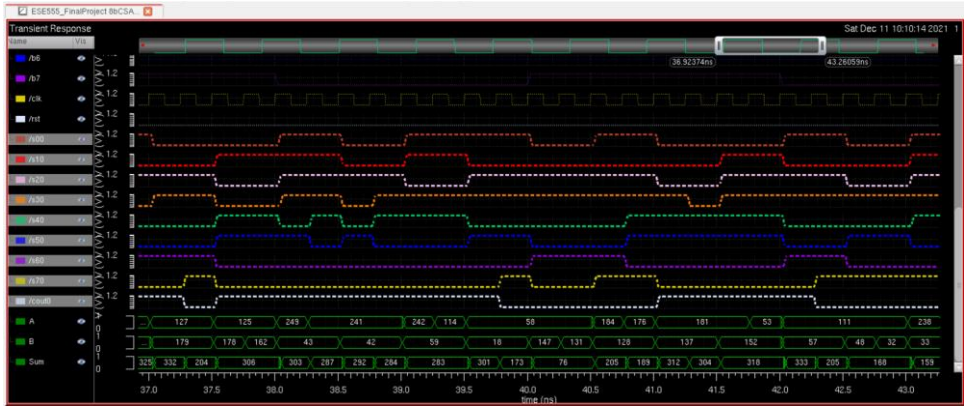
Sum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Transient Response
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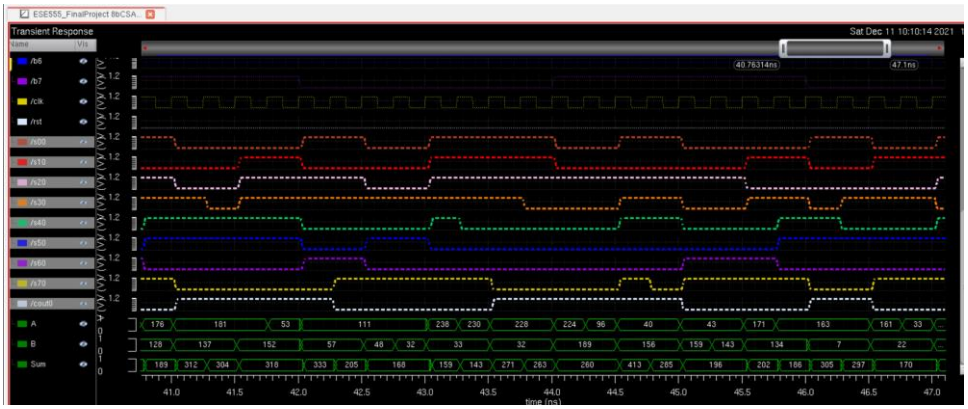
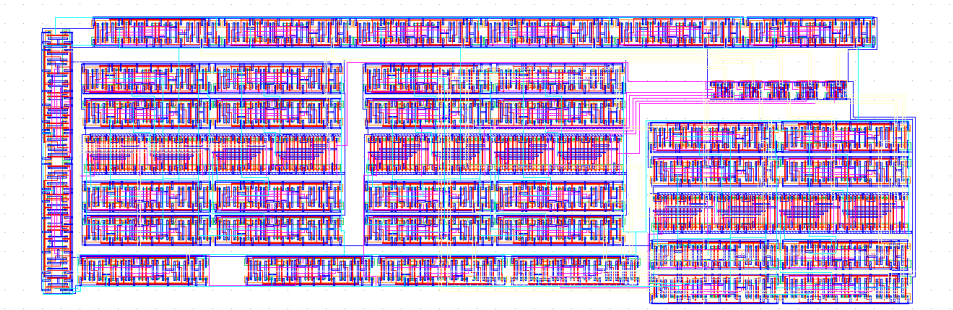
/b7
/clk
/rst
/s00
/s10
/s20
/s30
/s40
/s50
/s60
/s70
/cout0
A
B
Sum
time (ns)

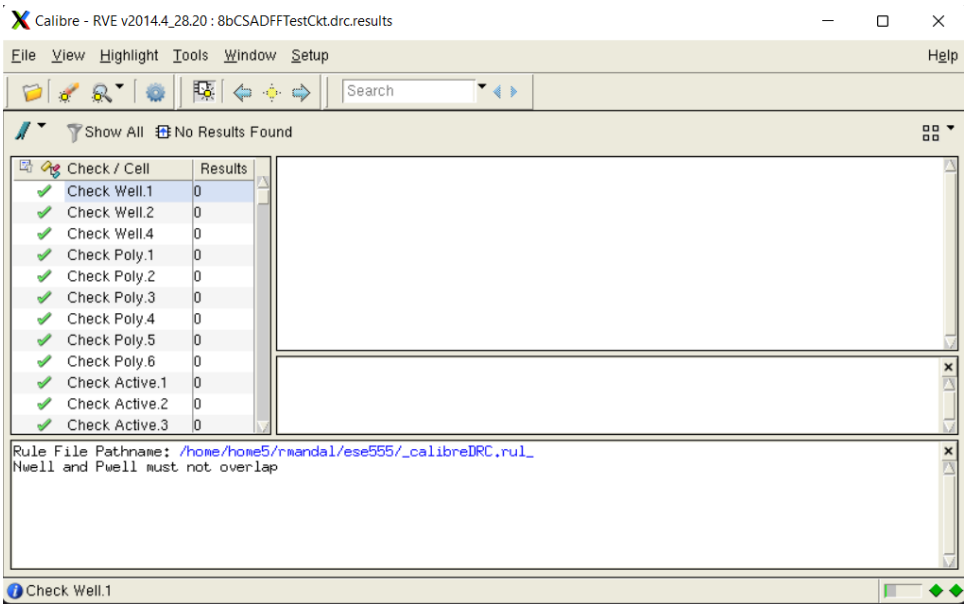


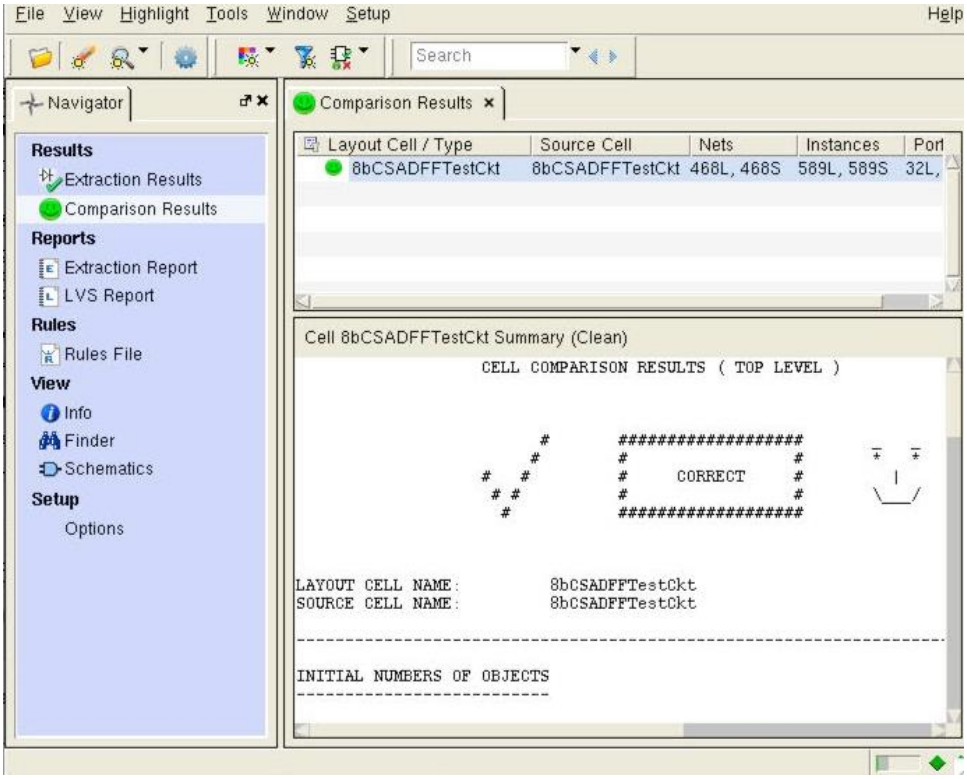
Layout Design

The 8-bit adder is built using 45nm CMOS technology. The design is optimized by keeping the distances between components minimum per the micron rules specified for this process technology.



Verification





Discussion

As demonstrated above, using D Flip Flops based pipelining increases throughput and frequency allowing the circuit to operate at 4Ghz. Furthermore, proper sizing the transistor gates helps us reduce power consumption.

Conclusion

We demonstrated the design of a pipelined 8-bit adder and its operation. We further covered optimizing the design for better power efficiency while maintaining the required performance constraints and accuracy.

References

1. N. Weste and D. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th edition, Addison Wesley
2. Design and Verification of a Pipelined 8-bit Carry Select Adder, Ashwin Venkatesh, Aishwarya Gandhi.