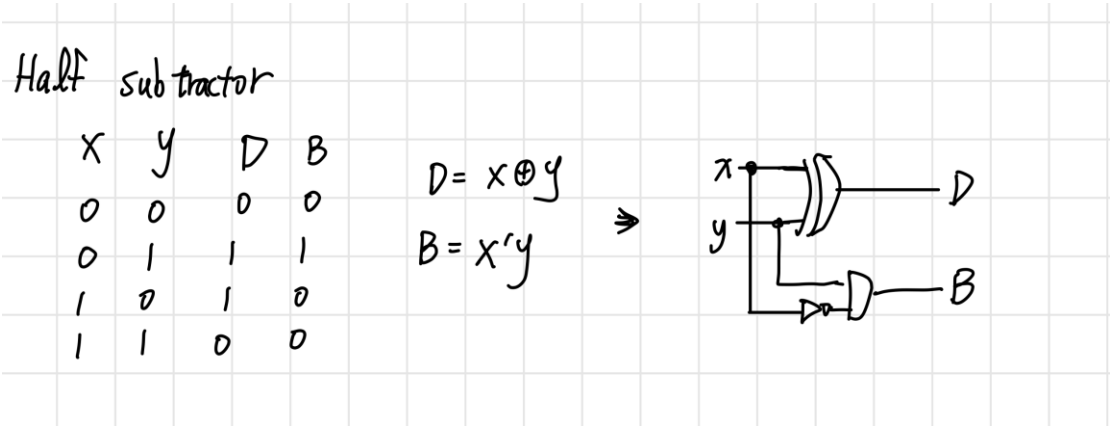
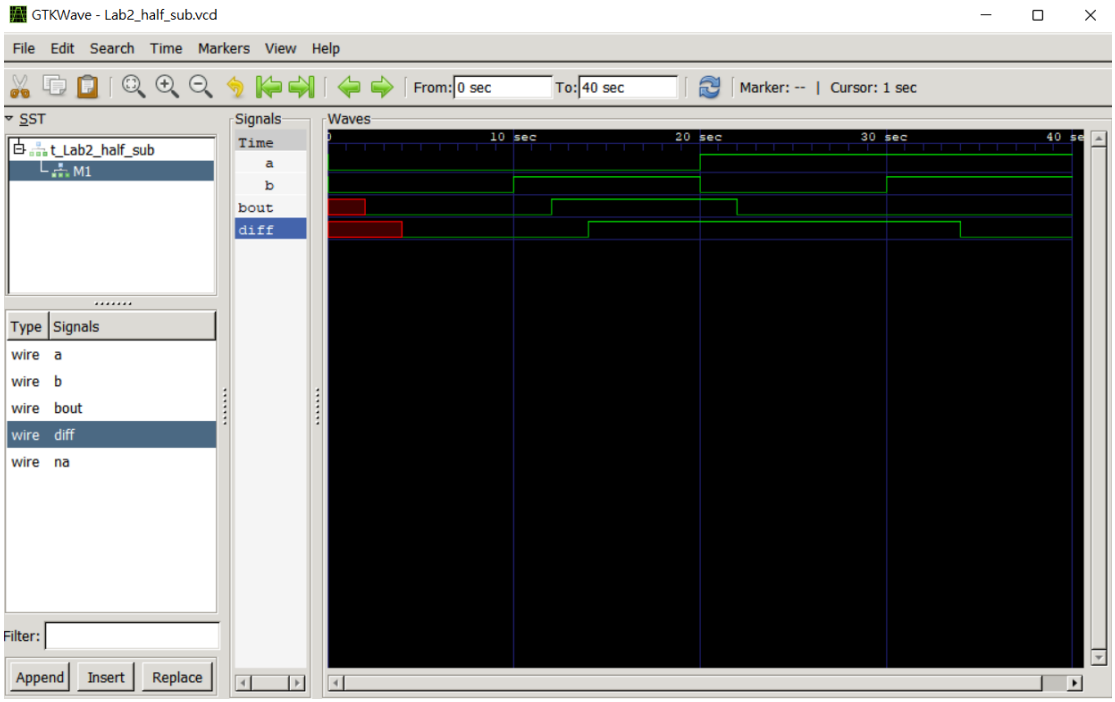
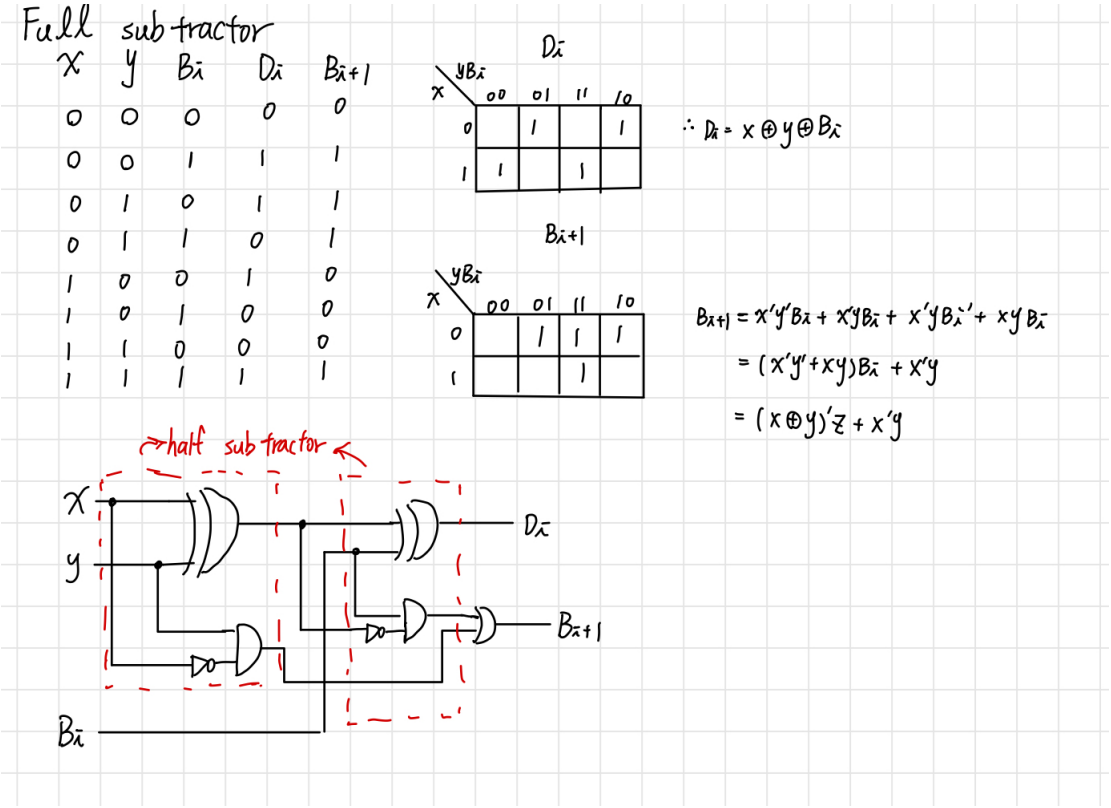
1. half subtractor

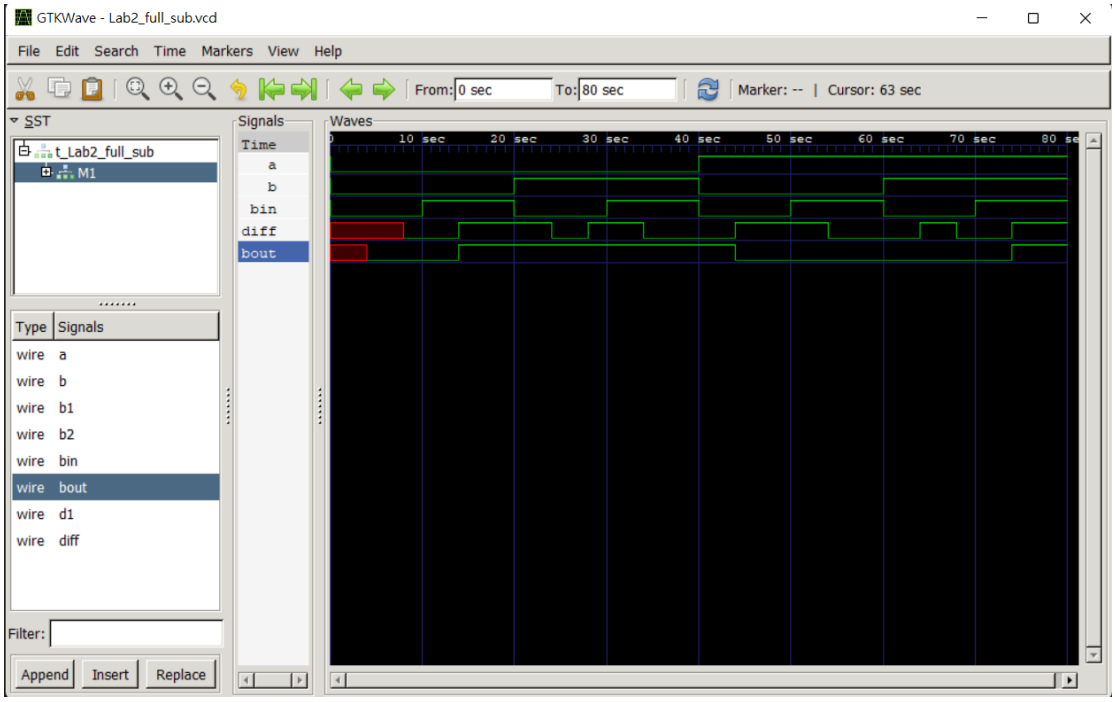




波型與 delay (bout 延遲 2 單位，diff 延遲 4 單位)皆正確

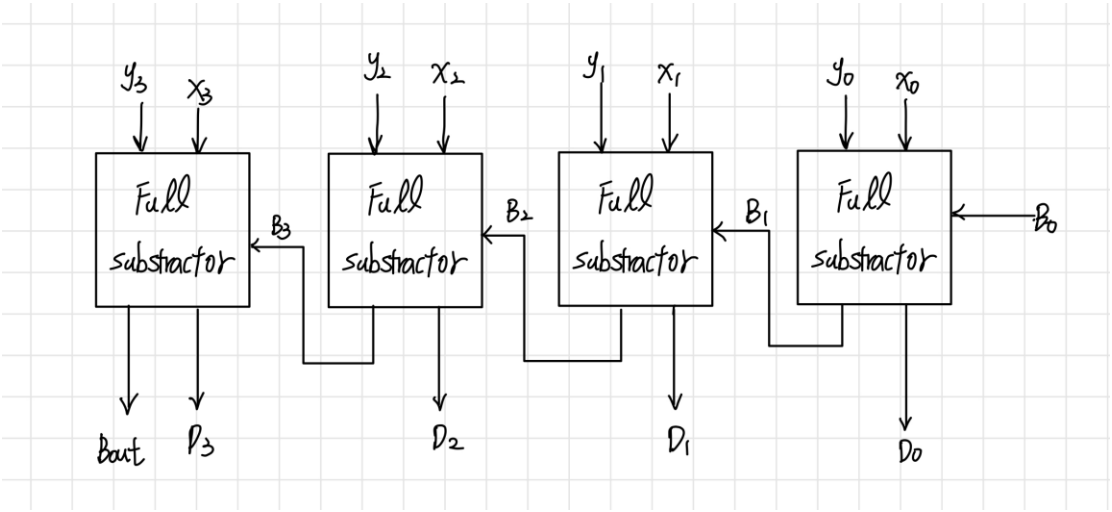
2. full subtractor

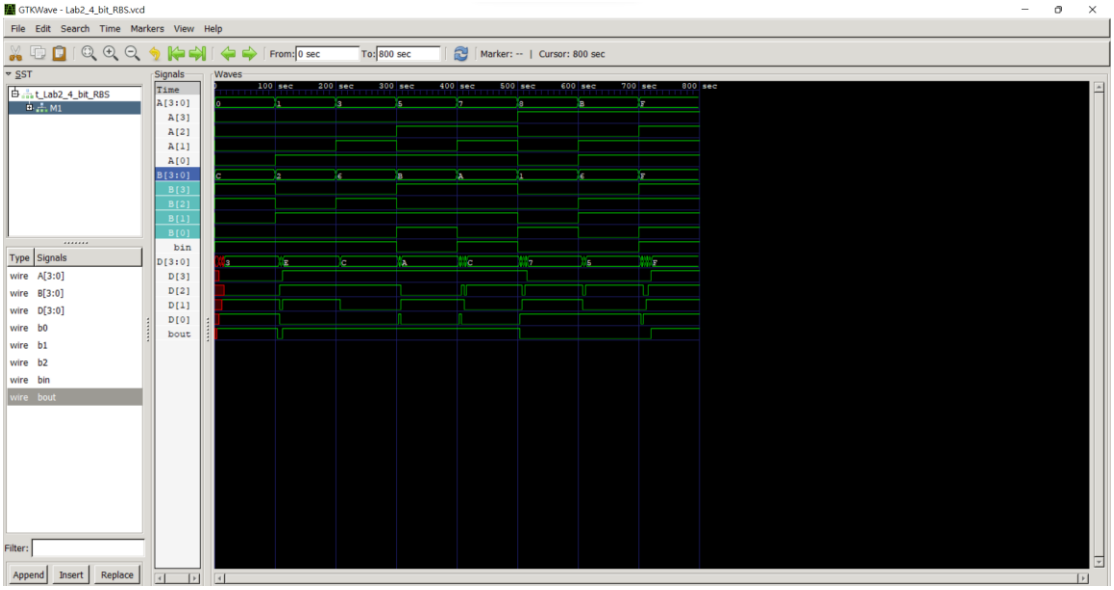




波形圖與 delay (bout 延遲 4 單位，diff 延遲 8 單位)皆正確

3. 4-bit RBS





波型正確

從波形圖上看的 delay:

D[0]=8ns,D[1]=12ns,D[2]=16ns,D[3]=8ns,bout=4ns

實際上的 delay (從電路邏輯推算):

D[0]=8ns,D[1]=12ns,D[2]=16ns,D[3]=20ns,bout=20ns

[註]Delay: 雖然在波形圖上 D[3]的未定 delay(紅色區塊)較小，然而仔細觀察波形圖，可以發現紅色區塊後的訊號從 0 變為 1。那是因為在 full subtractor 中最後有一個 or gate，因為是 or gate 所以可以在訊號未定時產生輸出，所以只看未定義的 delay 並不準確，所以觀察波形圖可以發現 D[3]的 delay 依然是最大的。

4.

由 full substractor

$$\begin{cases} D_i = x_i \oplus y_i \oplus B_i \\ B_{i+1} = (x_i \oplus y_i)' B_i + x_i' y_i \end{cases} \quad \therefore \text{令 } P_i = x_i \oplus y_i,\ G_i = x_i' y_i$$

$$\Rightarrow \begin{cases} D_i = P_i \oplus B_i \\ B_{i+1} = P_i' B_i + G_i \end{cases}$$

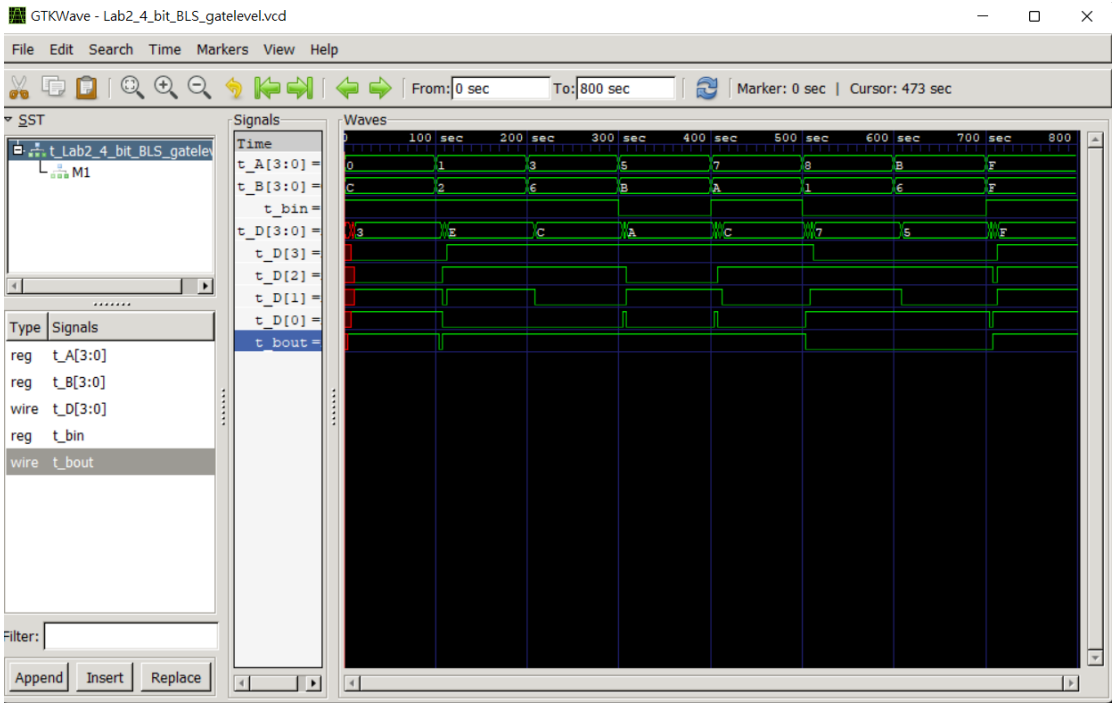
$$\therefore B_1 = P_0' B_0 + G_0$$

$$B_2 = P_1' B_1 + G_1 = P_1'(P_0' B_0 + G_0) + G_1 = P_1' P_0' B_0 + P_1' G_0 + G_1$$

$$B_3 = P_2' B_2 + G_2 = P_2' P_1' P_0' B_0 + P_2' P_1' G_0 + P_2' G_1 + G_2$$

$$B_4 = P_3' B_3 + G_3 = P_3' P_2' P_1' P_0' B_0 + P_3' P_2' P_1' G_0 + P_3' P_2' G_1 + P_3' G_2 + G_3$$

(a) gatelevel



波型正確

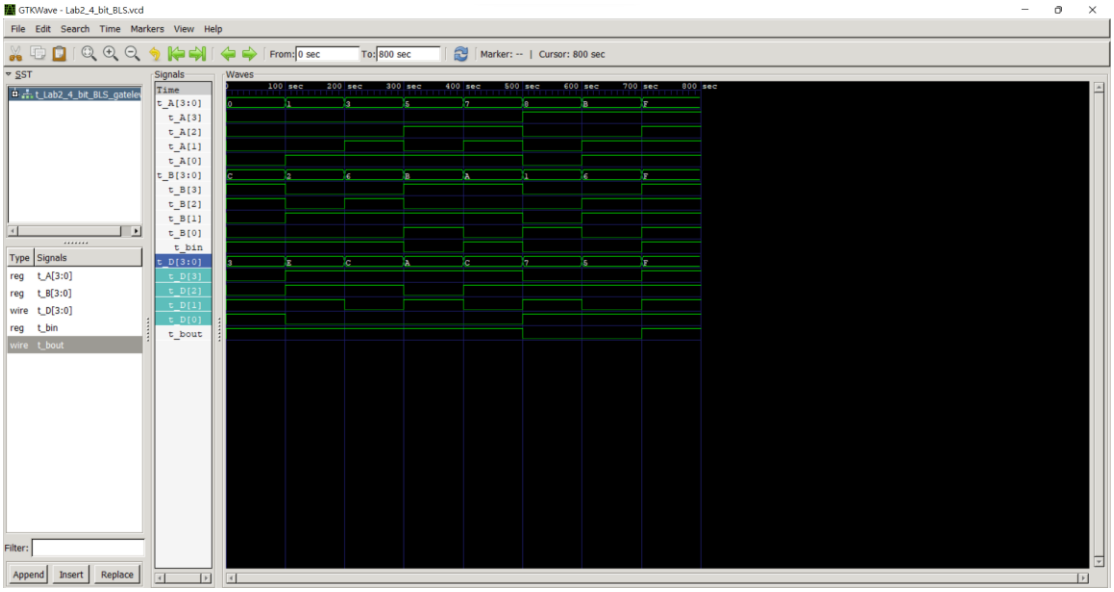
波形圖上的 Delay:

D[0]=8ns,D[1]=12ns,D[2]=12ns,D[3]=8ns,bout=4ns

實際上的 delay (從電路邏輯推算):

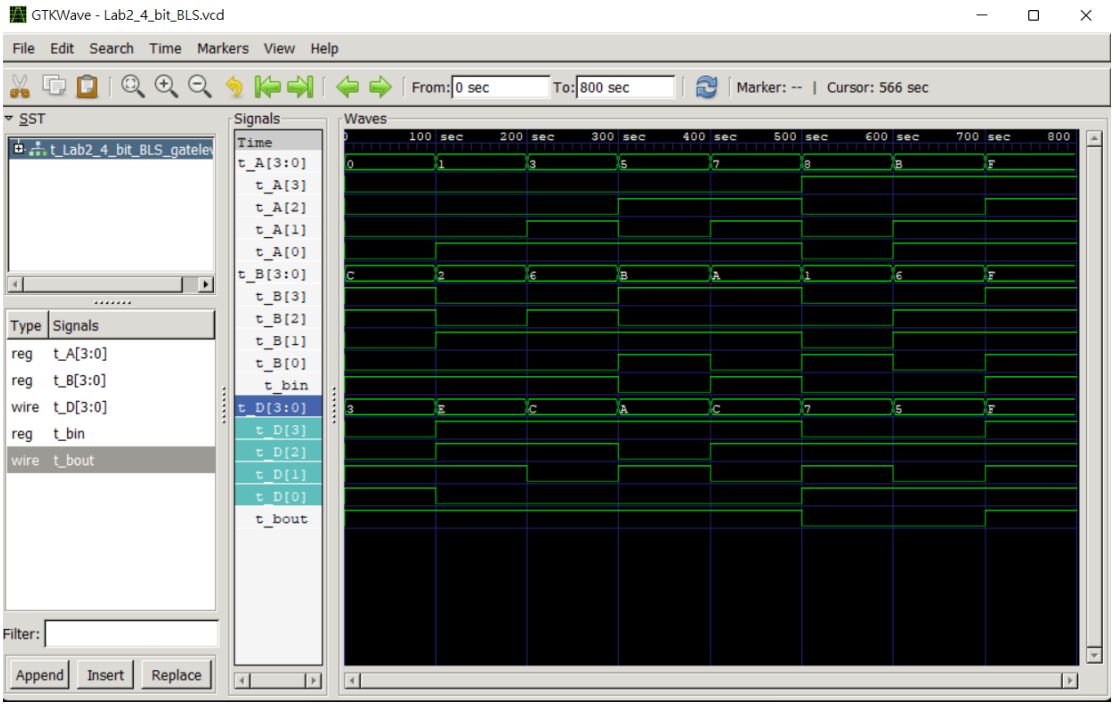
D[0]=12ns,D[1]=12ns,D[2]=12ns,D[3]=12ns,bout=8ns

(b) dataflow



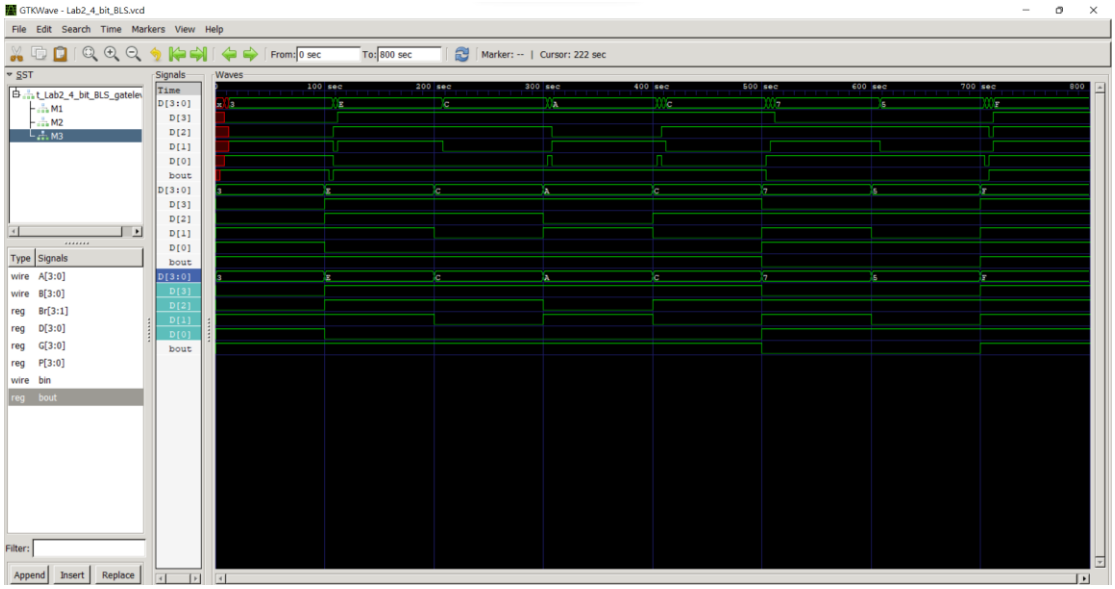
波型正確

(c) behavioral

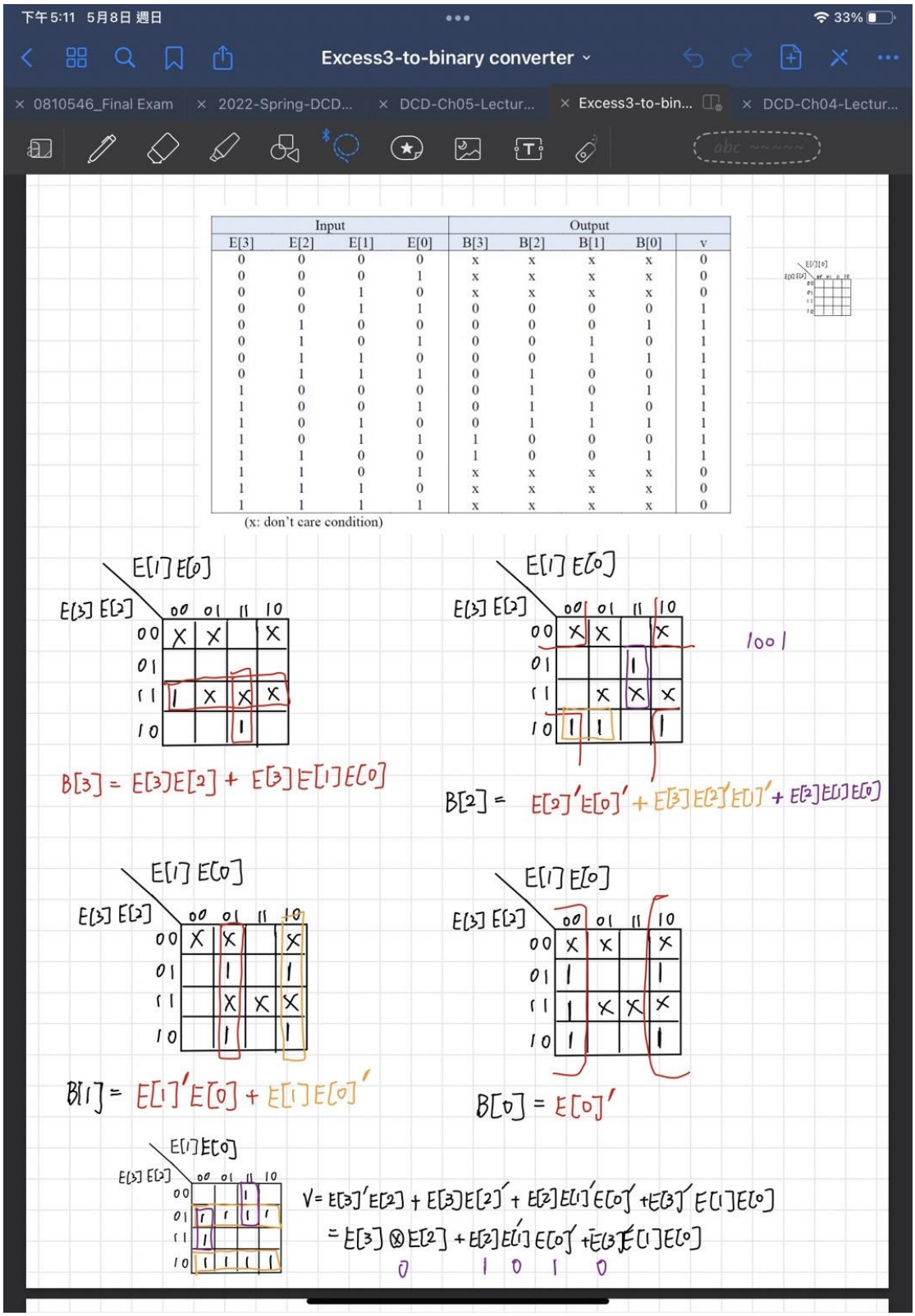


波型正確

三者合併波形圖


GTKWave - Lab2_4_bit_BLS.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 800 sec
Marker: -- | Cursor: 222 sec
SST
t_Lab2_4_bit_BLS_gatelev
M1
M2
M3
Type Signals
wire A[3:0]
wire B[3:0]
reg Br[3:1]
reg D[3:0]
reg G[3:0]
reg P[3:0]
wire bin
reg bout
Filter:
Append Insert Replace
Signals
Time
D[3:0]
D[3]
D[2]
D[1]
D[0]
bout
Waves
100 sec
200 sec
300 sec
400 sec
500 sec
600 sec
700 sec
800

5.



Input				Output				
E[3]	E[2]	E[1]	E[0]	B[3]	B[2]	B[1]	B[0]	v
0	0	0	0	x	x	x	x	0
0	0	0	1	x	x	x	x	0
0	0	1	0	x	x	x	x	0
0	0	1	1	0	0	0	0	1
0	1	0	0	0	0	0	1	1
0	1	0	1	0	0	1	0	1
0	1	1	0	0	0	1	1	1
0	1	1	1	0	1	0	0	1
1	0	0	0	0	1	0	1	1
1	0	0	1	0	1	1	0	1
1	0	1	0	0	1	1	1	1
1	0	1	1	1	0	0	0	1
1	1	0	0	1	0	0	1	1
1	1	0	1	x	x	x	x	0
1	1	1	0	x	x	x	x	0
1	1	1	1	x	x	x	x	0

$B[3] = E[3]E[2] + E[3]E[1]E[0]$

$B[2] = E[2]'E[0]' + E[3]E[2]'E[1]' + E[2]E[1]E[0]$

$B[1] = E[1]'E[0] + E[1]E[0]' = E[1] \otimes E[0]$

$B[0] = E[0]'$

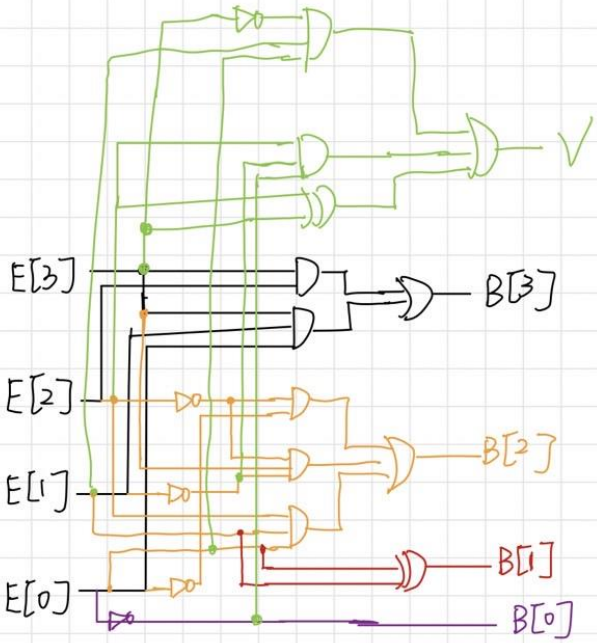
$V = = E[3] \otimes E[2] + E[2]E[1]'E[0]' + E[3]E[1]E[0]$

$AB + ACD$

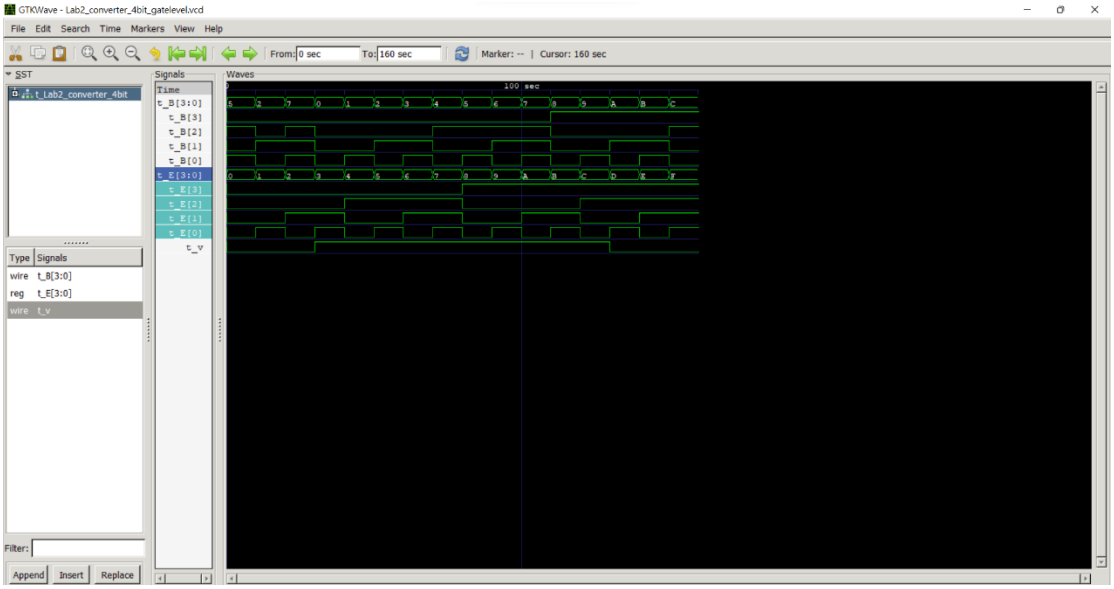
$B'D' + AB'C' + BCD$

$C'D + CD'$

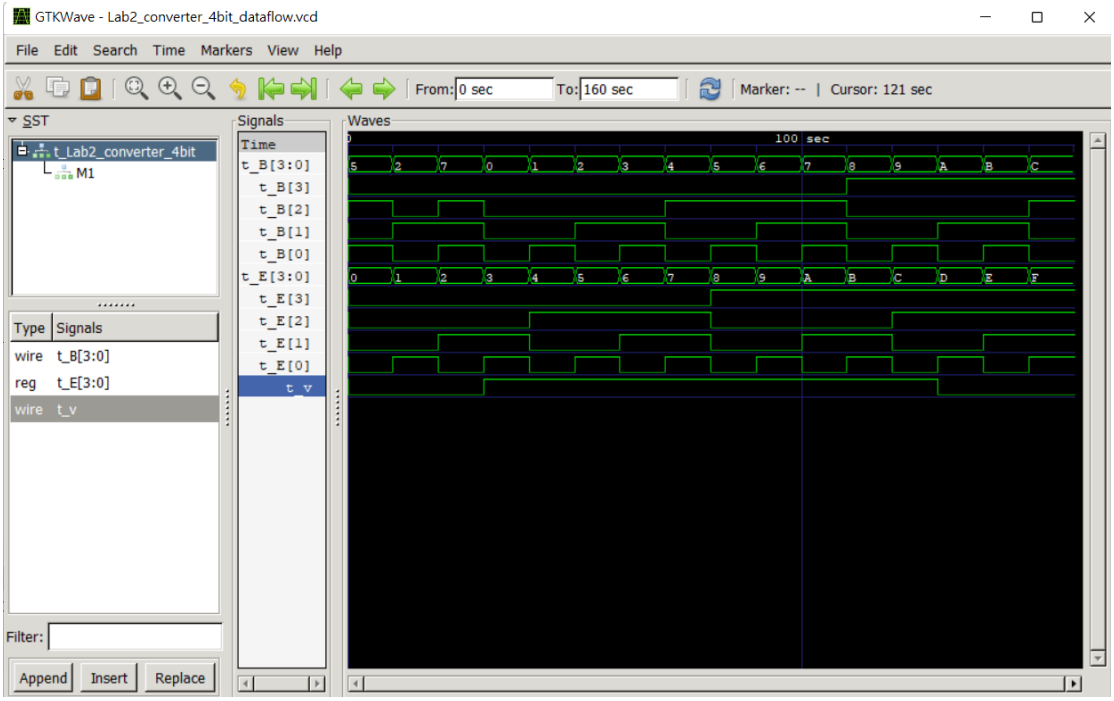
D'



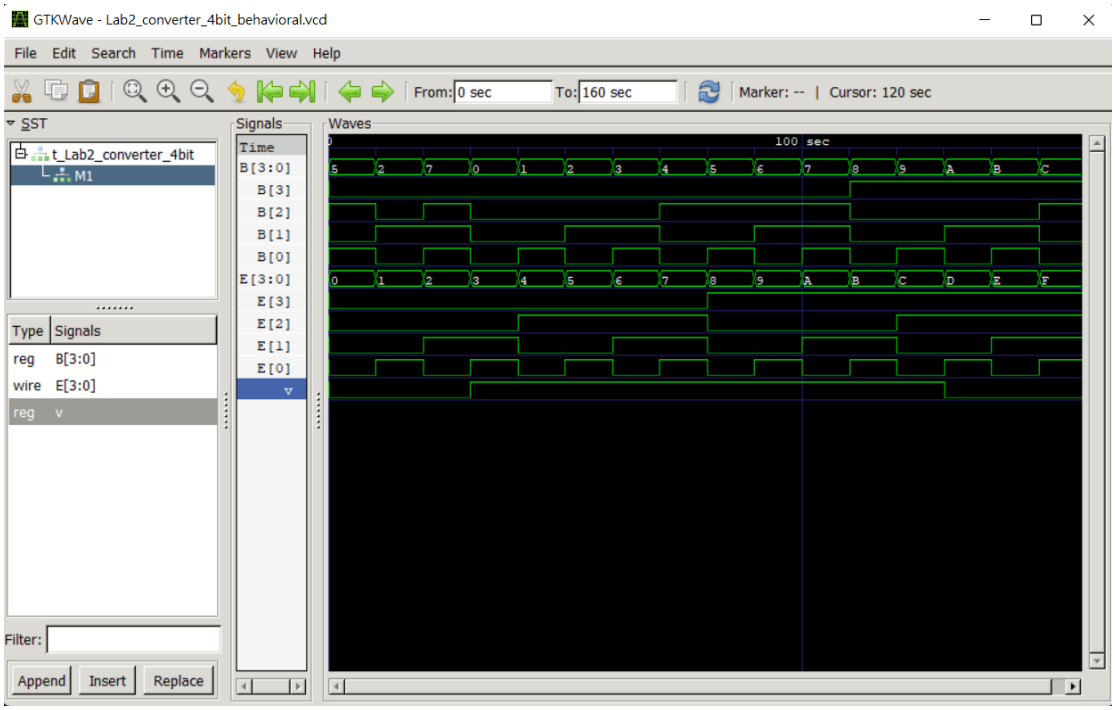
(a) gatelevel



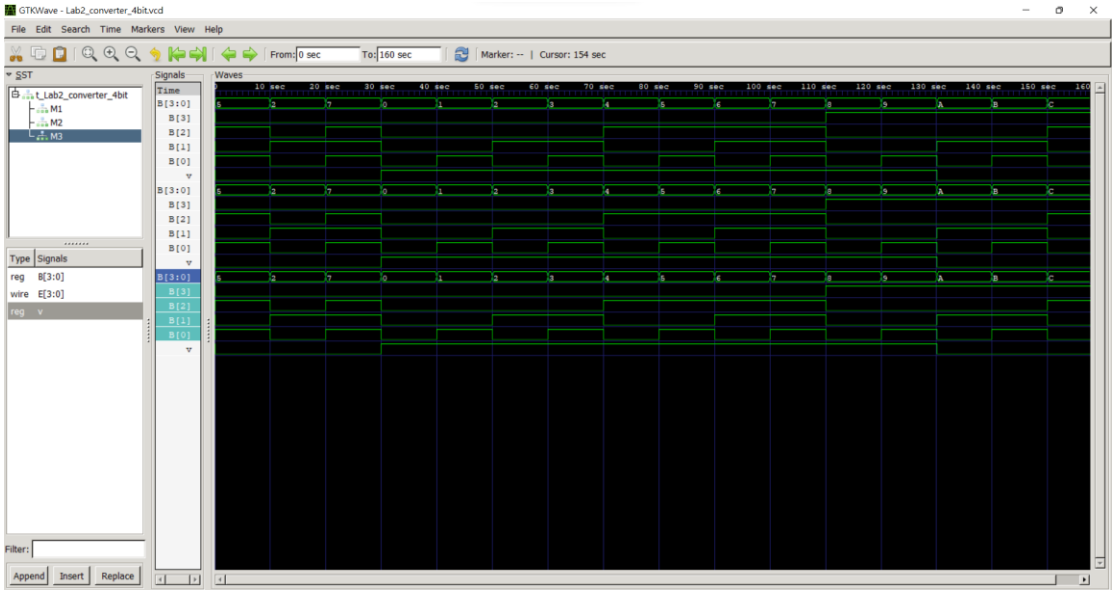
(b) dataflow



(c) behavioral



三者皆轉換正確



6. 心得

這次 Lab 比上次困難許多，但只要細心應該不會出太大的差錯，在寫 dataflow 時須注意括號的運用，小心不要將其他項也括號進來。