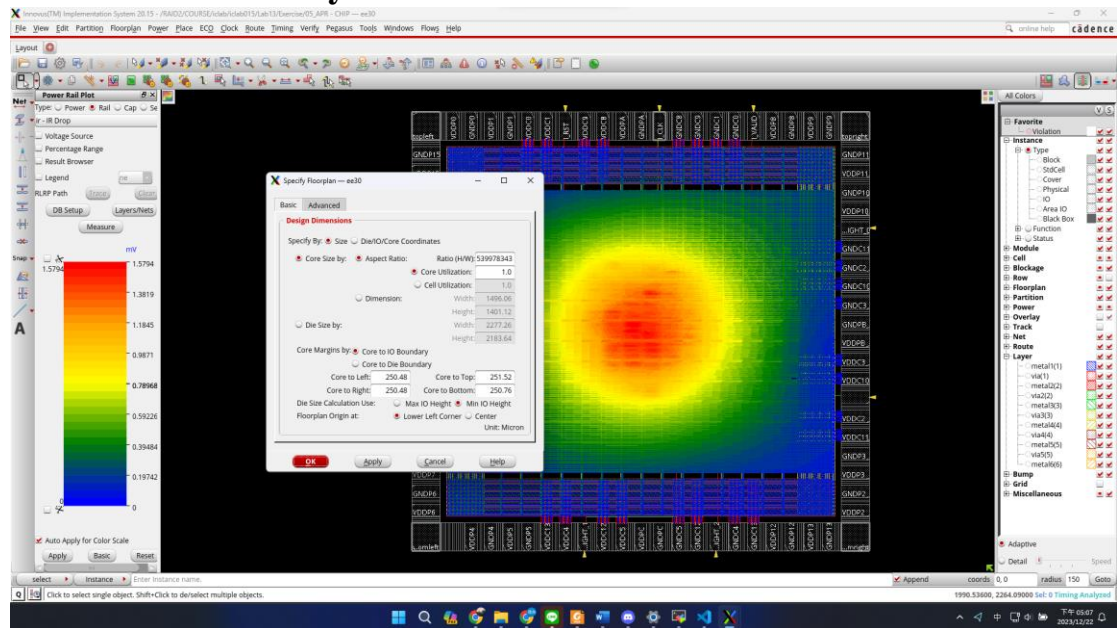
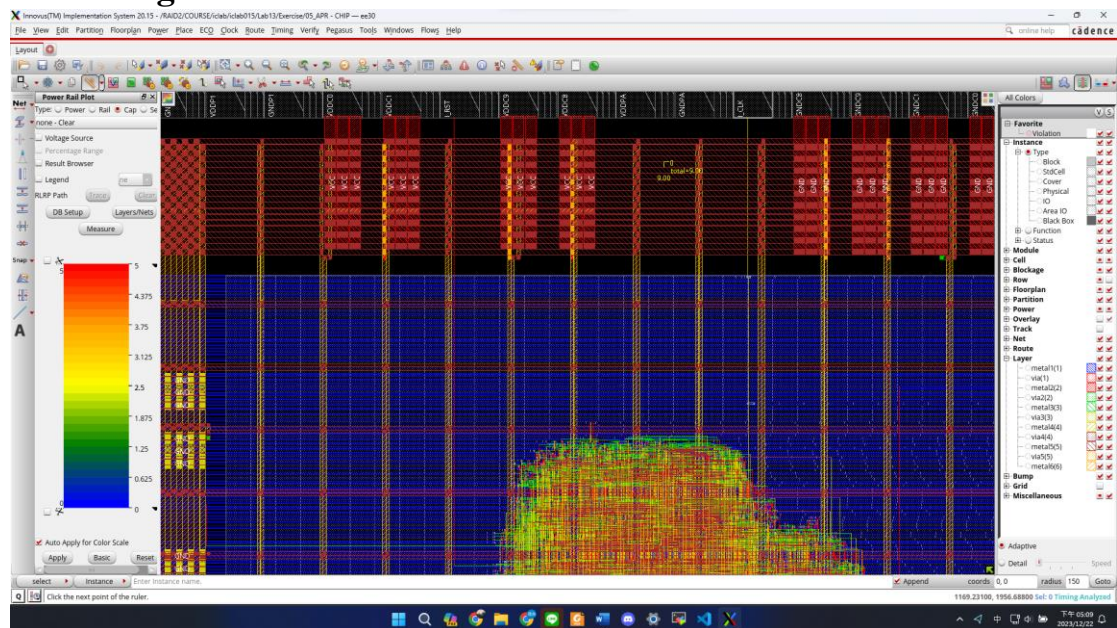


Report

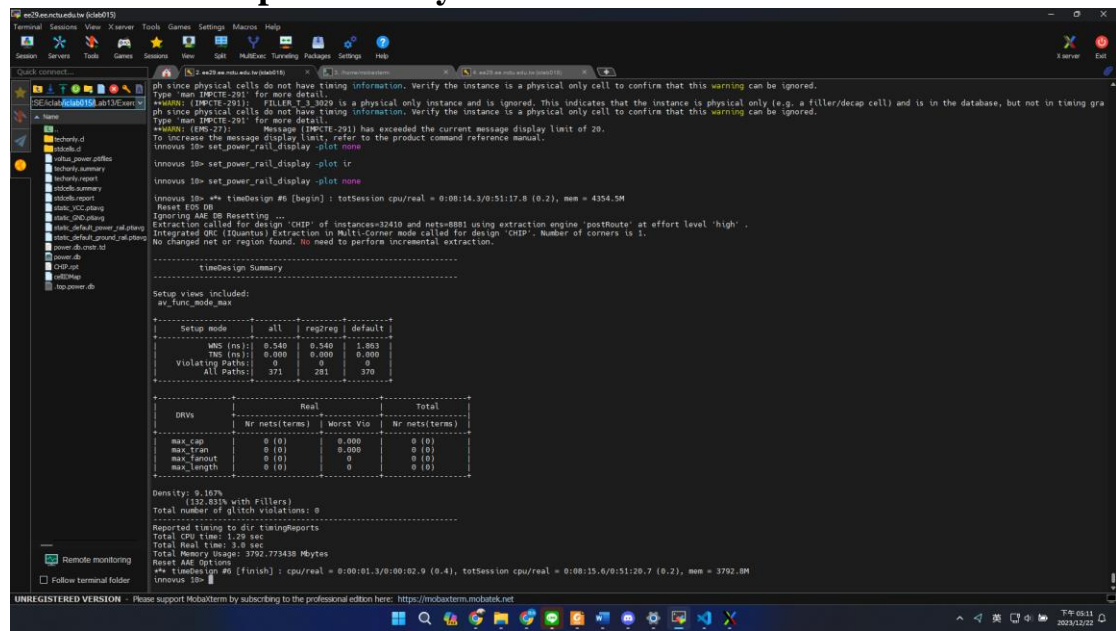
1. Core to IO boundary :



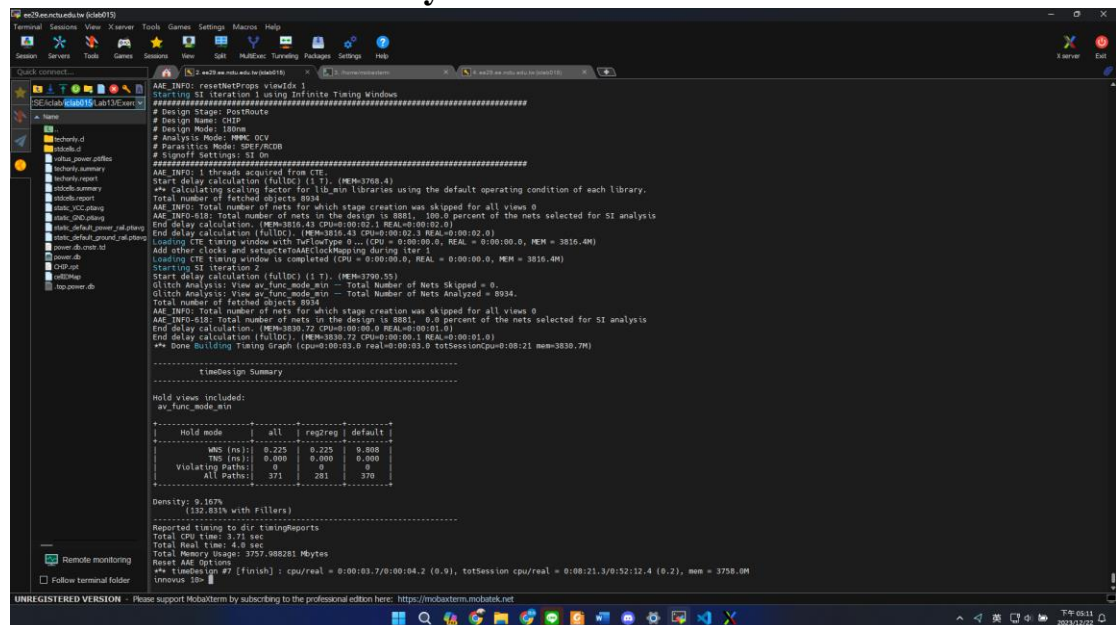
2. Core Ring :



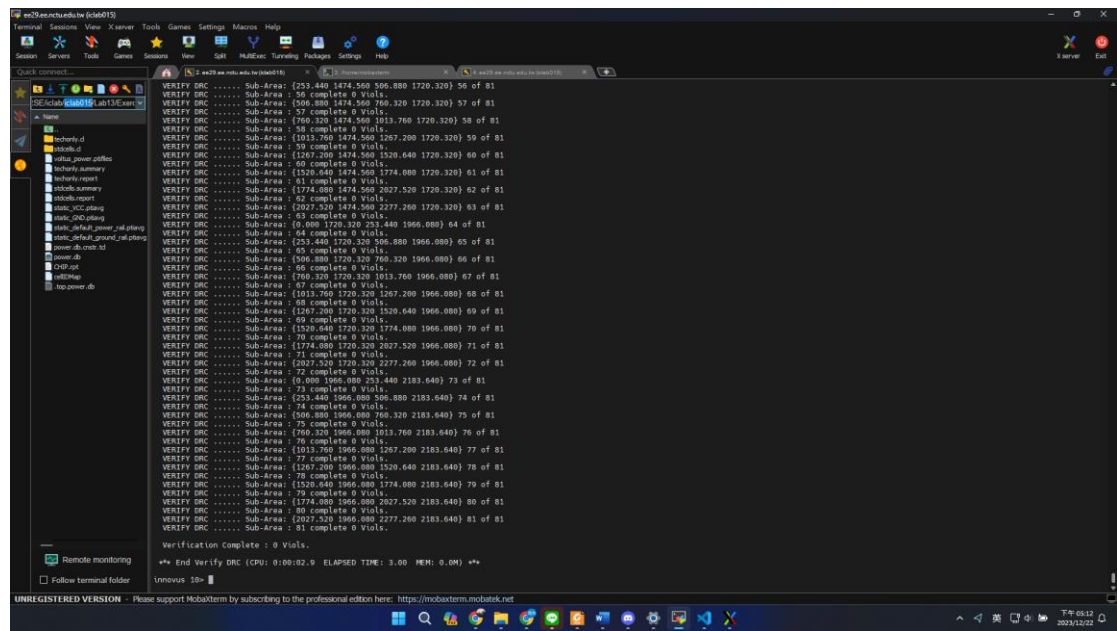
3. Post-Route setup time analysis :



4. Post-Route hold time analysis :

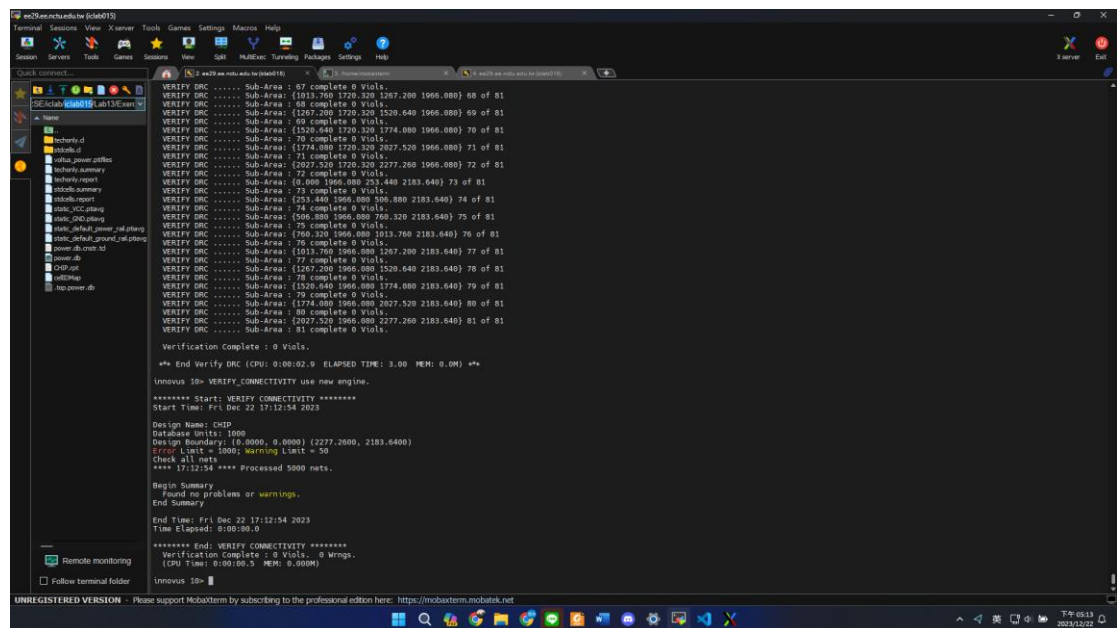


5. DRC result :



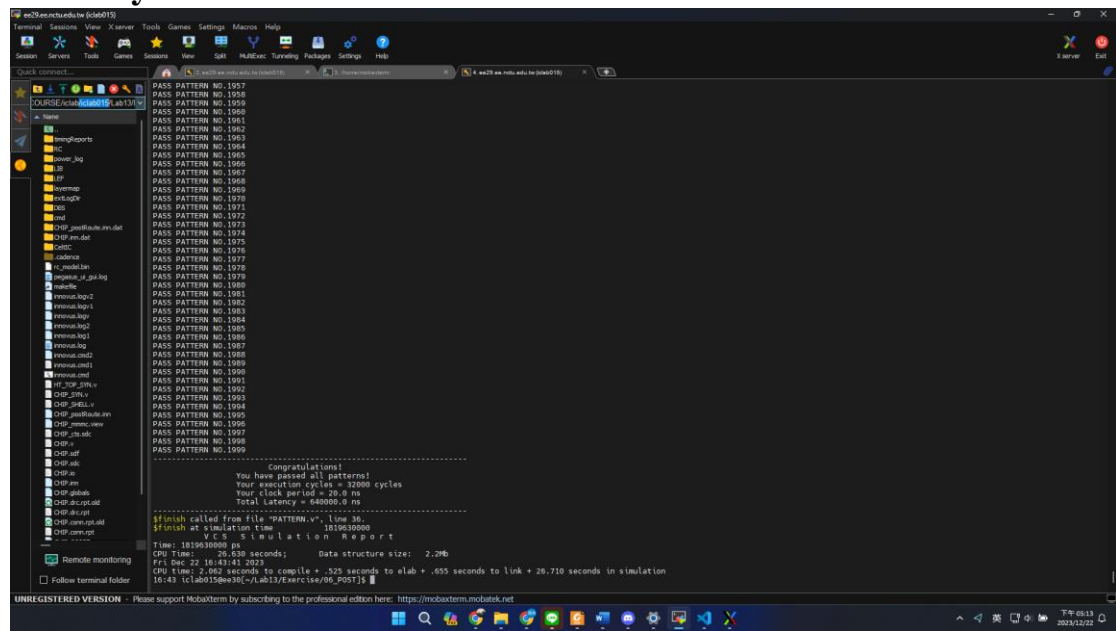
The screenshot shows the Mobaxterm interface with a terminal window displaying the results of a Design Rule Check (DRC) for a project named 'ic2024schu.edu.tw (ic2024)'. The terminal output lists 81 sub-areas, each with a 'Sub-Area' number and a status indicating the number of violations (e.g., '56 of 81', '57 of 81', etc.). The results show that all sub-areas have 0 violations, indicating a successful DRC. The terminal also displays the command 'End Verify DRC (CPU: 0:00:02.9 ELAPSED TIME: 3.00 MEM: 0.0M)' and the status 'Verification Complete : 0 Viol.'.

6. LVS result :

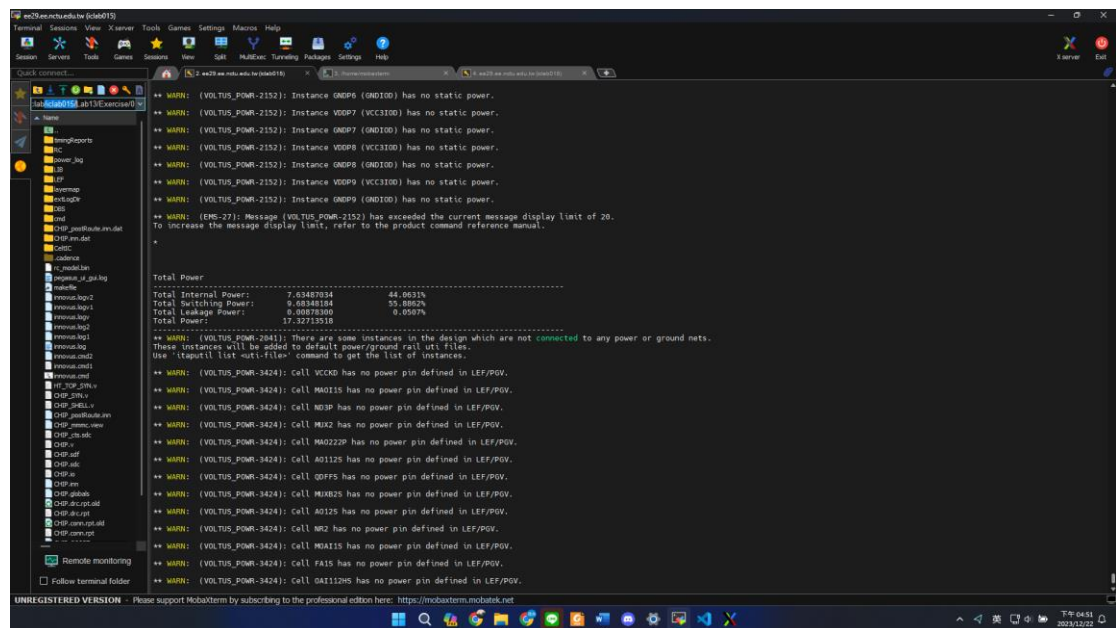


The screenshot shows the Mobaxterm interface with a terminal window displaying the results of a Layout Versus Schematic (LVS) check for a project named 'ic2024schu.edu.tw (ic2024)'. The terminal output lists 81 sub-areas, each with a 'Sub-Area' number and a status indicating the number of violations (e.g., '67 of 81', '68 of 81', etc.). The results show that all sub-areas have 0 violations, indicating a successful LVS. The terminal also displays the command 'End Verify DRC (CPU: 0:00:02.9 ELAPSED TIME: 3.00 MEM: 0.0M)' and the status 'Verification Complete : 0 Viol.'.

7. Post Layout simulation result :



8. Power result :



9. IR Drop Results :

我加了兩組power ring，跟4組stripe (metal2,3,4,5)，成功將IR drop從2.88mV 降到1.57mV。

