CSCE2301/230 – Digital Design I – FALL 2016
HW4

The objective of this assignment is to get familiar with Verilog HDL, Binary Arithmetic Circuits and CouldV. For this, you are going to model and verify several generic (parameterized) Verilog modules for binary arithmetic circuits using CloudV. The required modules are:

- *n-bit* Ripple Carry Adder (RCA) [parameter: n]
- *n-bit* Carry Look-ahead Adder (CLA); n=2, 3, 4 [parameter: n]
- *n-bit* Carry Select Adder [parameters: n (multiple of k), block size (k), and block type (CLA or RCA)]
- *nxm* unsigned array multiplier [parameters: n and m; each should be a power of 2 number]

Verilog ***generate*** and constant functions will be used to make the modules parameterized (generic). You have to verify the functionality of the modules when instantiated using different values for the parameters. Also, you have to synthesis and technology map (to OSU 180nm library) each module using different values for the parameters and note the area (gates count) and the delay for each value.

What to submit:

- CloudV repository that contains your work (more information will be passed to you on how to submit the repository).
    - The parameterized modules
    - The testbenches (including the VCD files that will be generated when you simulate them)
    - Synthesis reports and gatelevel netlist (generated automatically when you synthesize the modules).
- 2 Pages report (plus the covering page) that contains the following graphs:
    - RCA area vs. n
    - RCA delay vs. n
    - 16-bit Carry-Select Adder area vs. k (k= 2, 4 and 8) using RCA stages
    - 16-bit Carry-Select Adder delay vs. k (k= 2, 4 and 8) using RCA stages
    - nxn unsigned array multiplier area vs. n (n=4, 8, 16, and 32).
    - nxn unsigned array multiplier delay vs. n (n=4, 8, 16, and 32).

Deadline: Before Friday November 11th, 2016 - 11:59PM.