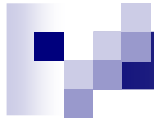# Delta-Sigma ADC Tutorial

## ECE614 Advanced Analog IC Design

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What is a Delta-Sigma ADC

- Known by various names such as Sigma-Delta ADC, Delta-Sigma ADC, over-sampling ADC, noise-shaping ADC, 1-bit ADC
- Name comes from the architecture of the modulator which integrates (Sigma) the difference (Delta) between the input and the quantized output

Sigma-Delta Modulator

Architecture

Analog input — $\Sigma\Delta$ modulator — Digital filter — Digital output
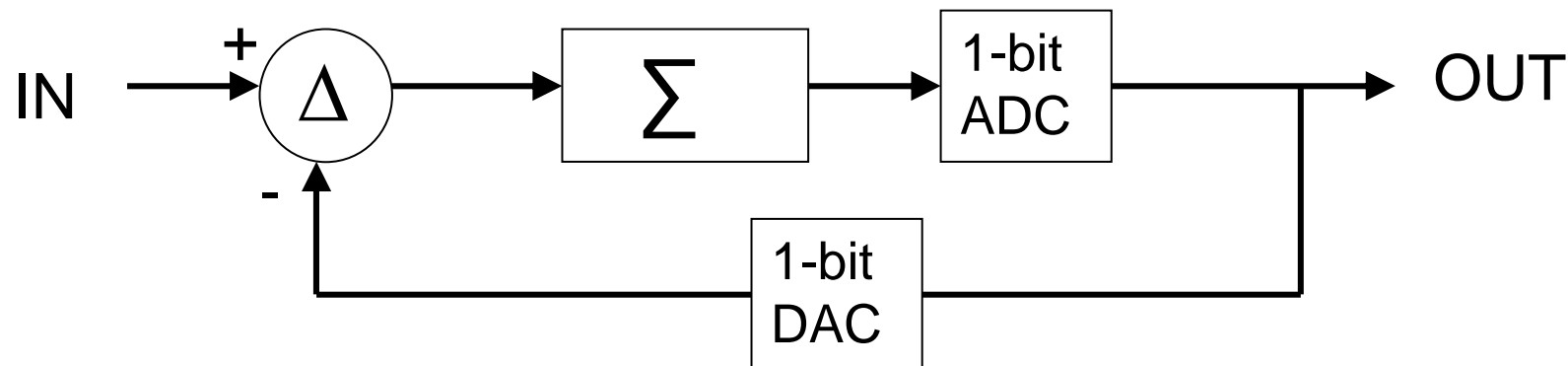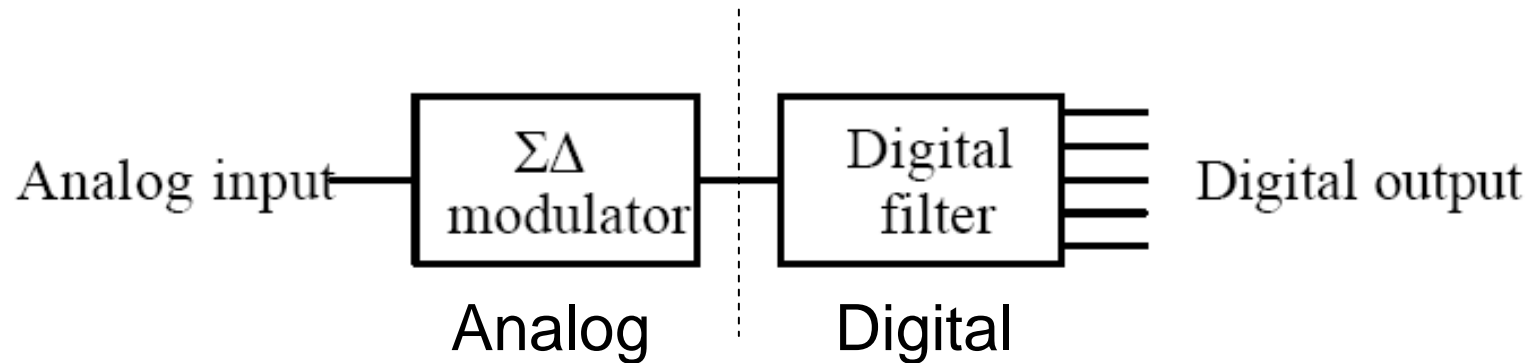
Analog   Digital

[1]

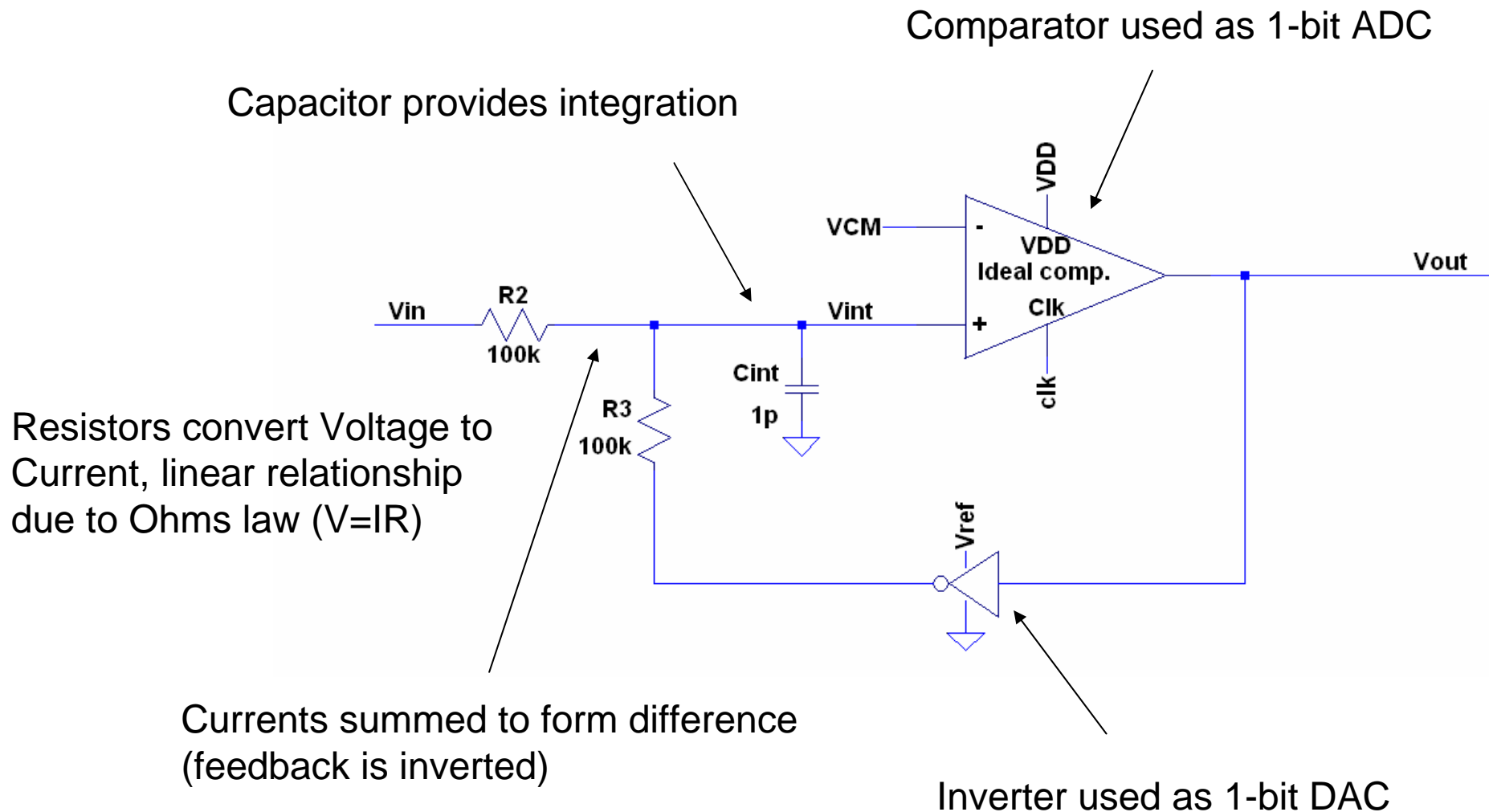- Sigma Delta ADC consists of an analog modulator followed by a digital low pass filter

Benefits

- No precision matched analog components required
- Can achieve high resolutions

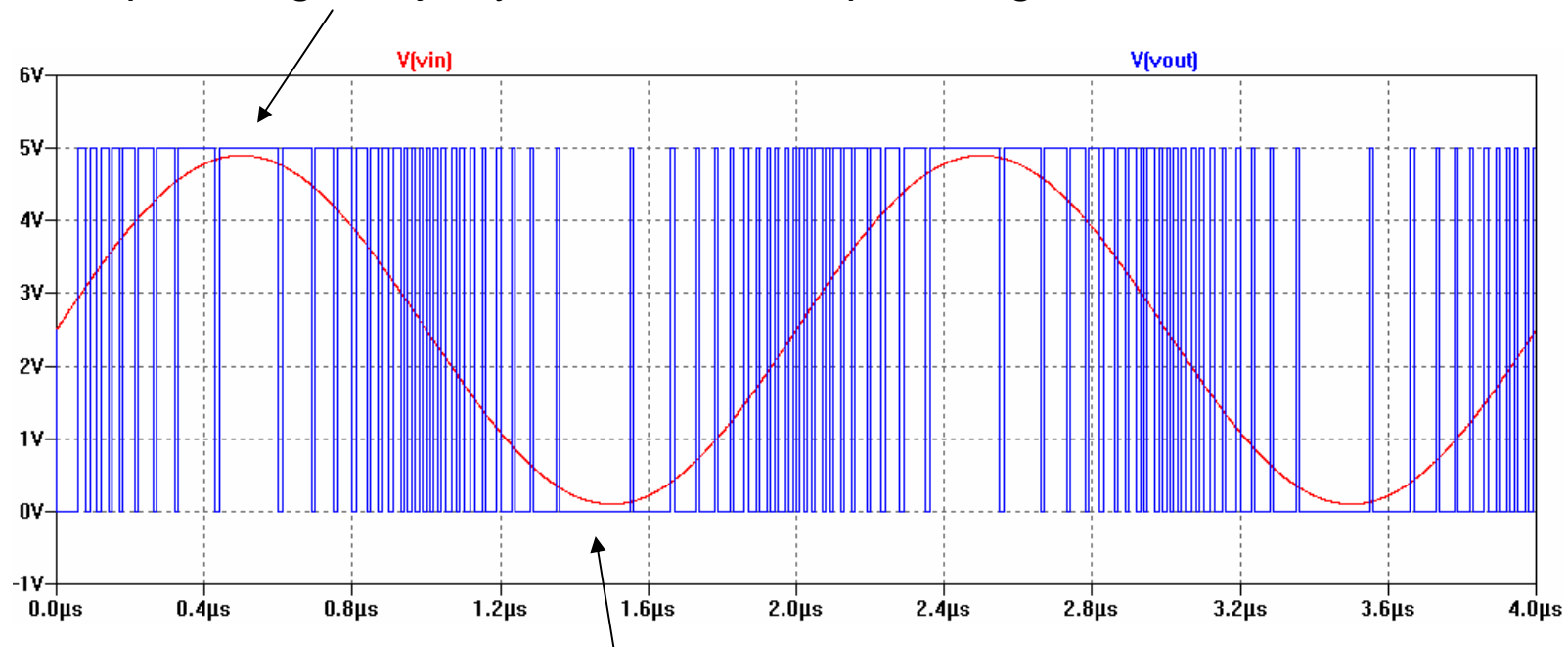# Drawbacks

- Slower conversion time

Simple Modulator

Comparator used as 1-bit ADC

Capacitor provides integration

Resistors convert Voltage to Current, linear relationship due to Ohms law (V=IR)

Currents summed to form difference (feedback is inverted)

Inverter used as 1-bit DAC
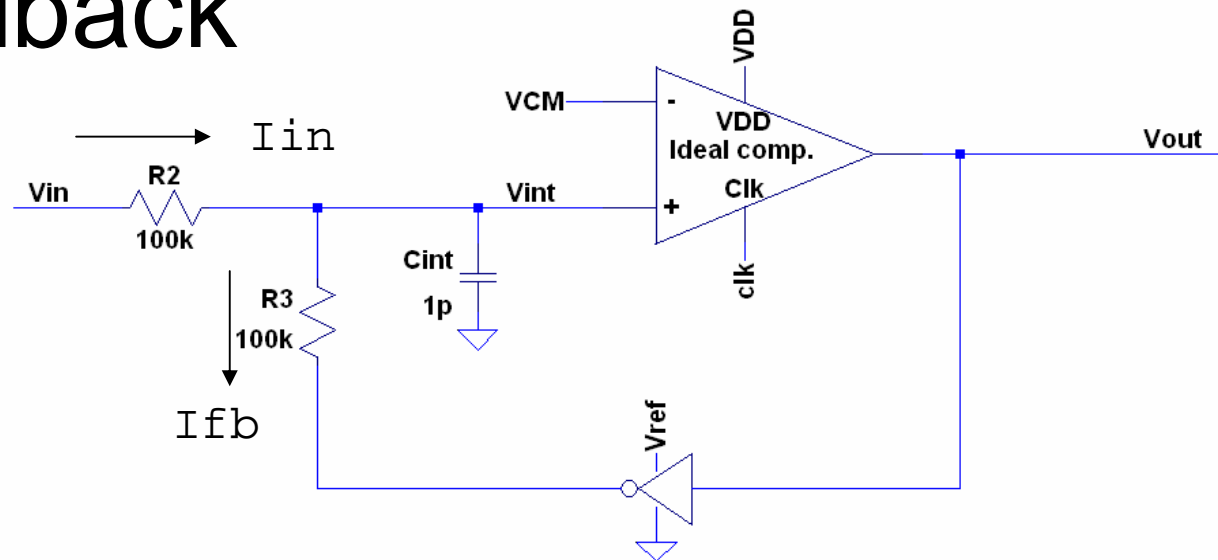
Simulation of Modulator – sim1

Output is high majority of time when input is high


Output is low majority of time when input is low

Average output of modulator is proportional to input

Feedback

- Feedback tries to hold the voltage across the capacitor at Vcm
- For the voltage across the capacitor to remain constant, there must be zero net current into the capacitor
- For there to be zero net current into the capacitor, the feedback current must be equal and opposite to the input current
- The feedback voltage (converted to a current) can only take on one of two levels, it cannot exactly match –Vin
- The duty cycle of the feedback is varied so the average voltage (current) feedback is equal and opposite to the input

Measurement
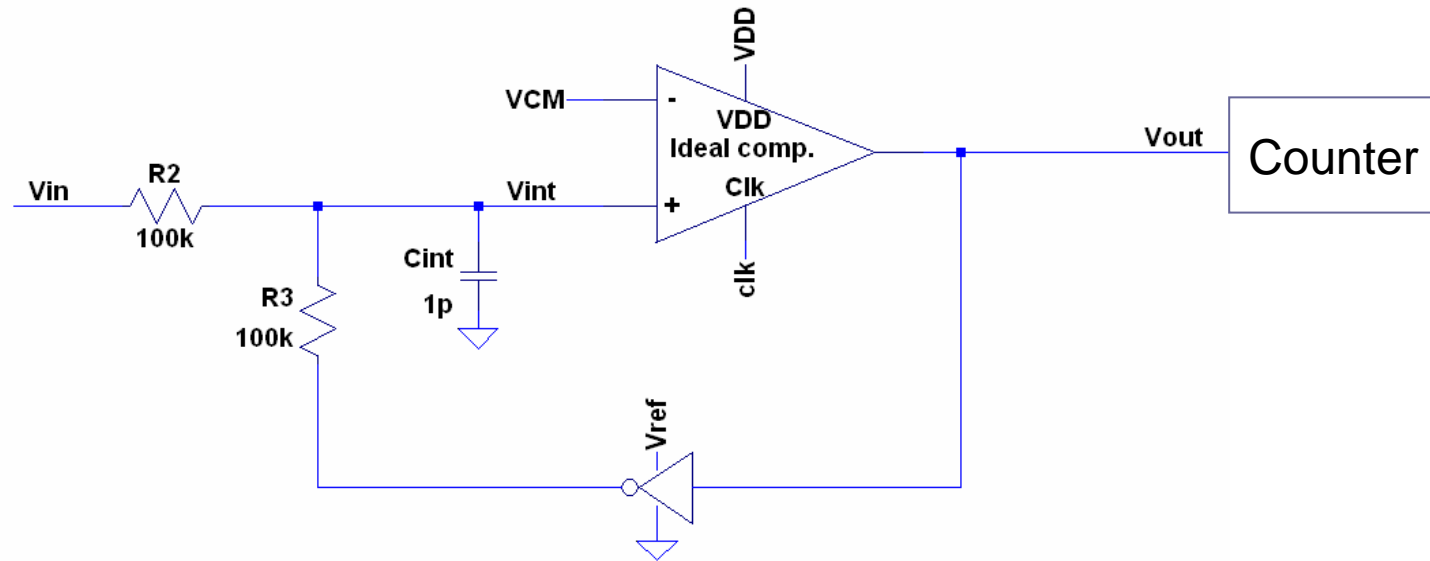
- If we use a counter on the output, we can measure the duty cycle of the feedback which is equal to the input.
- If we measure for a longer period of time, we get more accuracy.

Error caused by modulator ripple
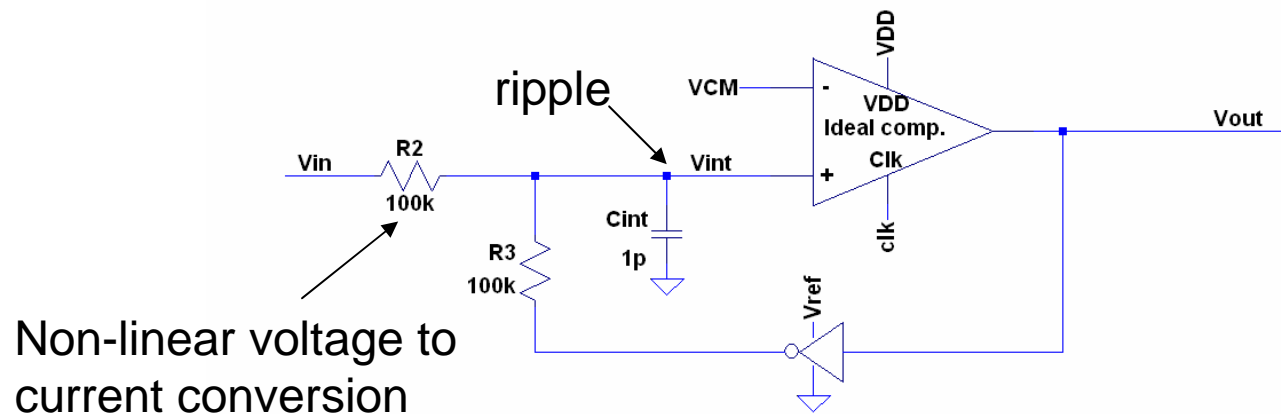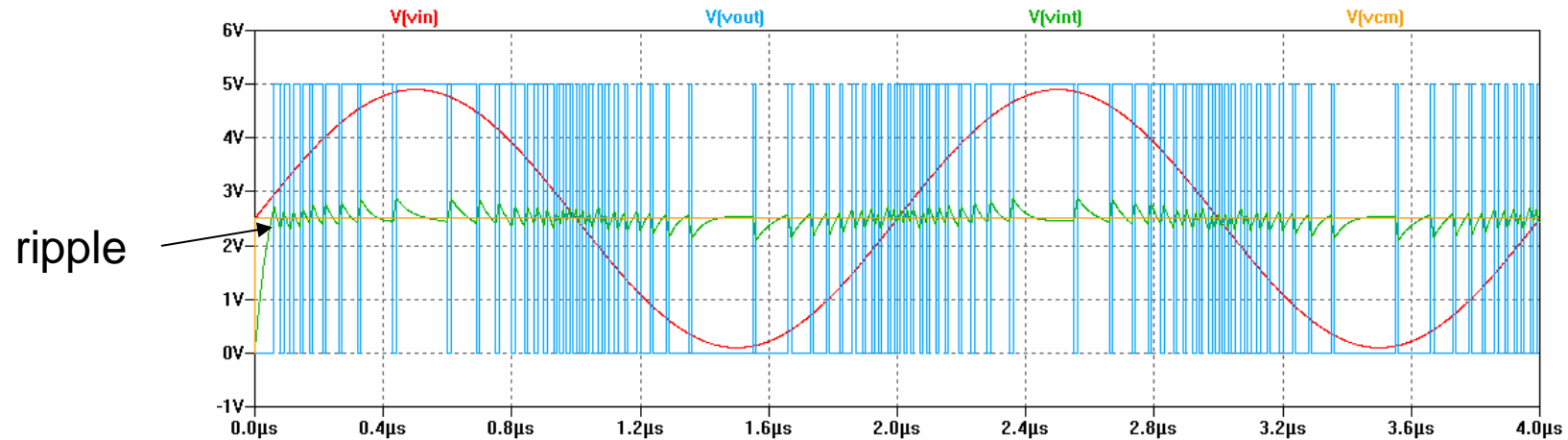
- Ripple on Vint causes non-linear voltage to current conversion resulting in distortion and limiting achievable accuracy

Eliminating ripple on simple modulator – sim2

Input voltage held
constant at Vcm

Output of integrator
swings around Vcm
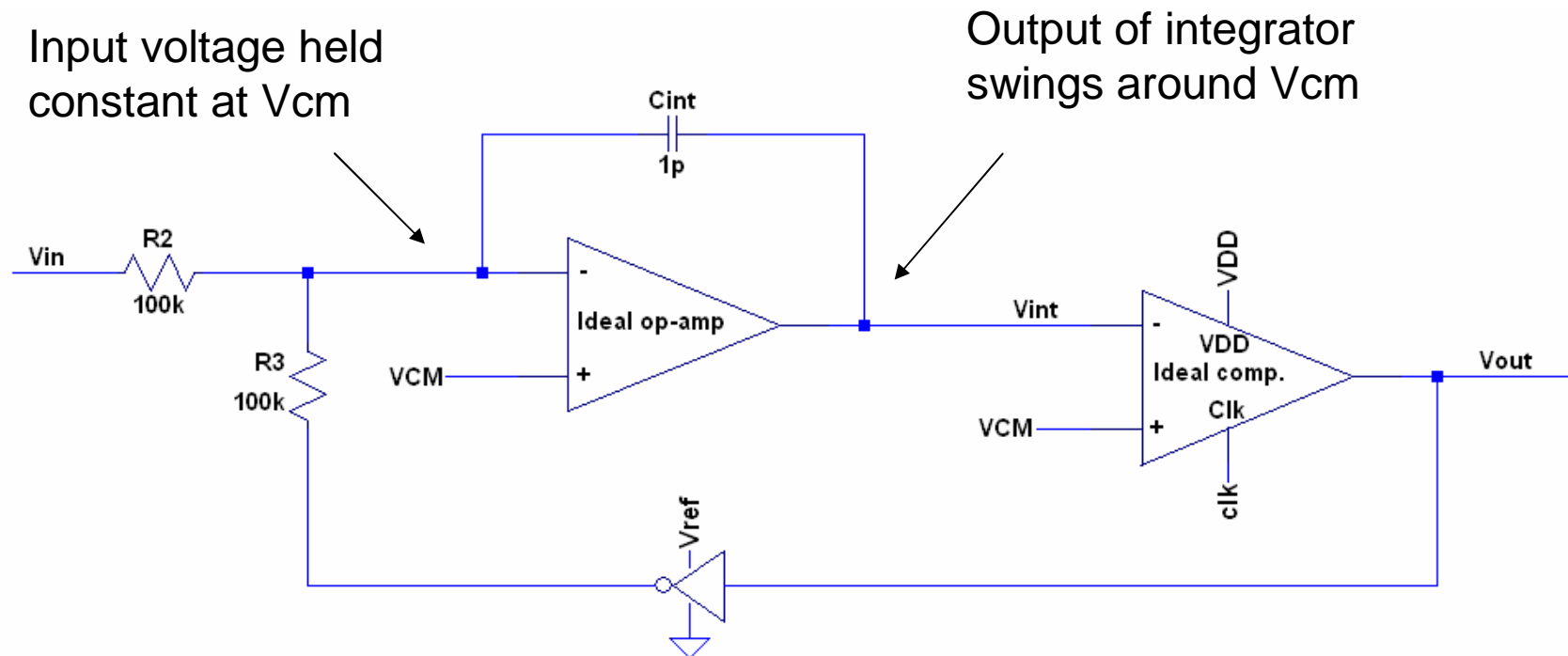
- Use an active integrator to hold input voltage constant
- Charge transferred to integration capacitor is the difference in input current minus the feedback current integrated over one clock period
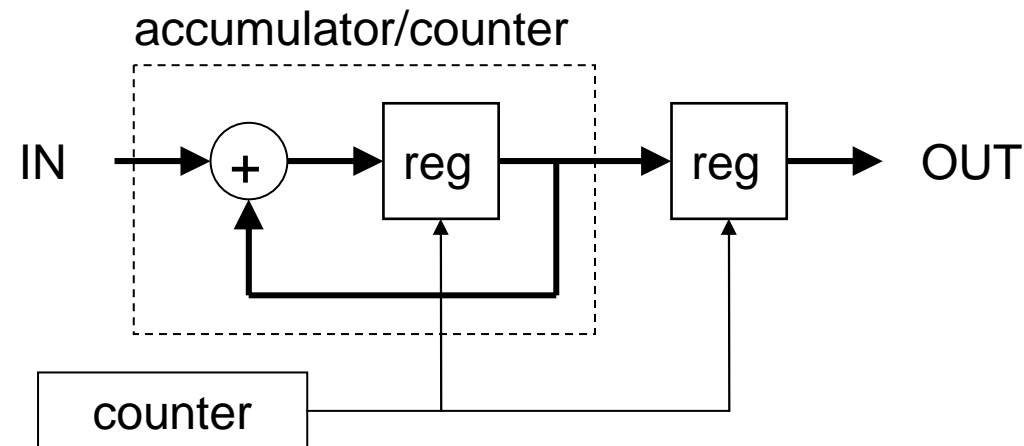
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Q = (Iin-Ifb)*t = (Vin-Vout)/R * t
```

Switched capacitor modulator – sim3
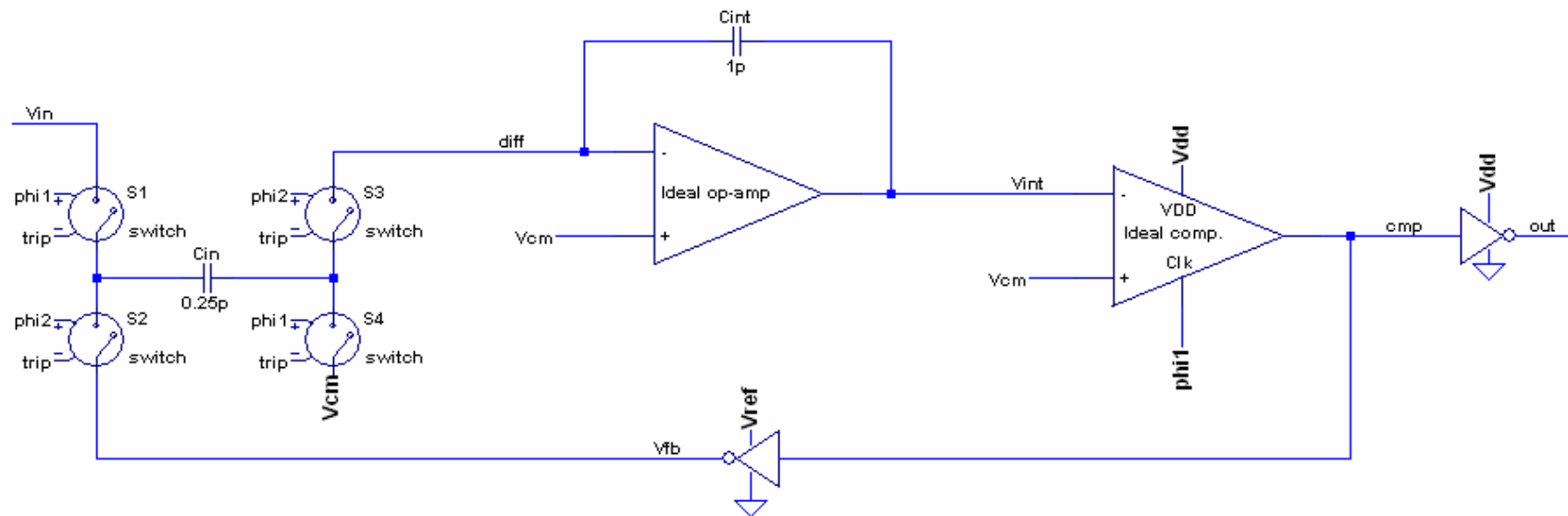
- Difference in voltages between input and feedback is converted to a charge Q=C*(Vin-Vfb), instead of a current I=(Vin-Vfb)/R that was integrated over one clock period to form a charge Q = I*t.
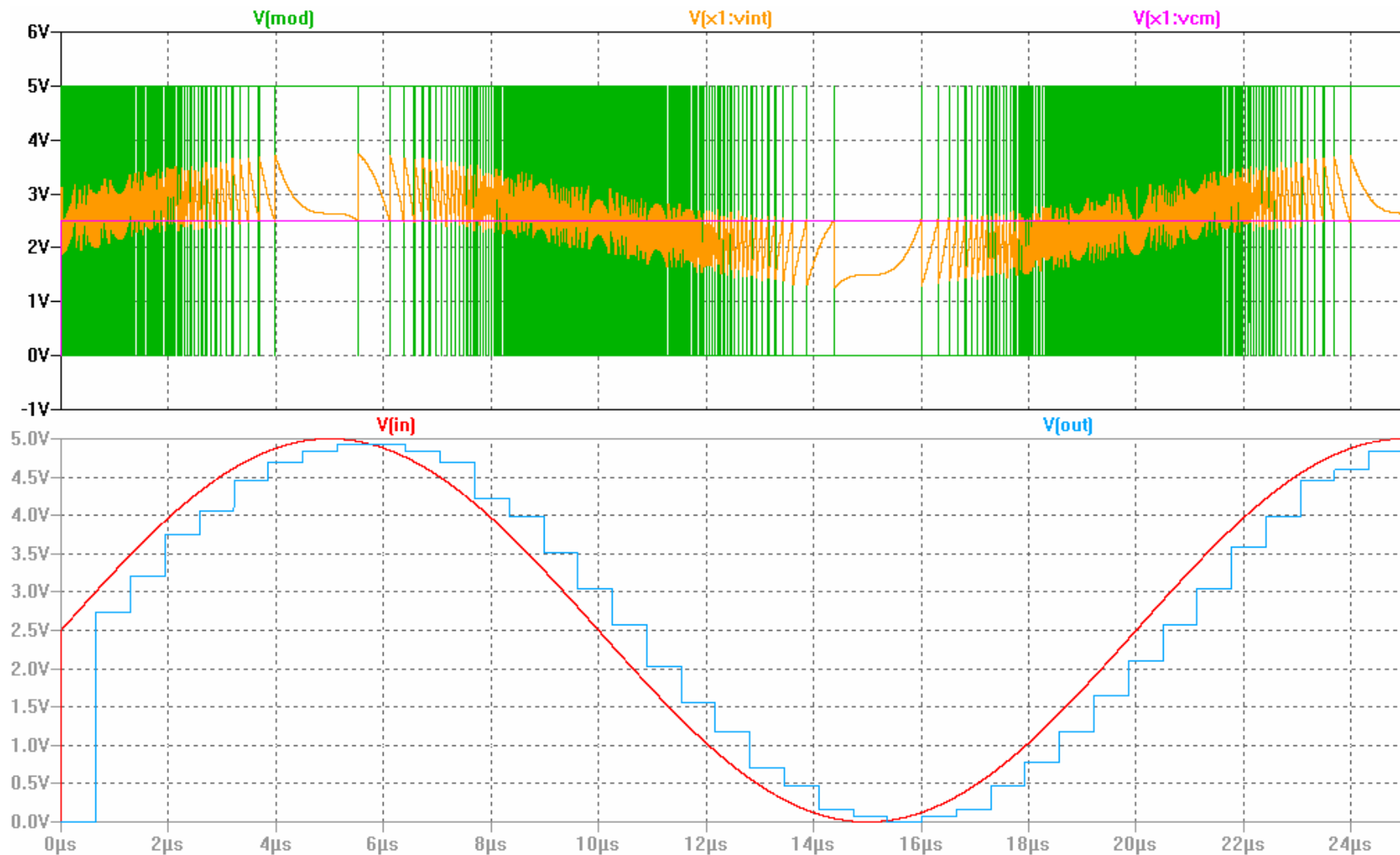
Low Pass Digital Filter

Simple Counter – used as low pass averaging filter

- Increasing length of counter increases resolution,
  but reduces output data rate

Simulation results
6-bit accumulate & dump – sim4

z-Transform

$$z = e^{j2\pi f T_s} = e^{j2\pi \frac{f}{f_s}}$$

Running average filter

$$y[n] = x[n] + x[n-1] + x[n-2] + ... + x[n-(K-1)]$$

z-Transform of running average filter

$$Y(z) = X(z) \cdot (1 + z^{-1} + z^{-2} + ... + z^{-(K-1)}) \qquad \cdot \frac{1-z^{-1}}{1-z^{-1}}$$

$$H(z) = \frac{Y(z)}{X(z)} = \frac{1-z^{-K}}{1-z^{-1}}$$

Evaluating frequency response of transfer function

$$H(z) = \frac{1 - z^{-K}}{1 - z^{-1}} \qquad z = e^{j2\pi fT_s} = e^{j2\pi \frac{f}{f_s}}$$

$$\left|H(f)\right| = \left|\frac{1 - e^{-j2\pi K \frac{f}{f_s}}}{1 - e^{-j2\pi \frac{f}{f_s}}}\right| = K\left|\frac{\operatorname{sinc}\left(\pi \frac{Kf}{f_s}\right)}{\operatorname{sinc}\left(\pi \frac{f}{f_s}\right)}\right|$$

(4.11-4.12) [3]

For large K, approximated as

$$\left|H(f)\right| \approx K\left|\operatorname{sinc}\left(\pi \frac{Kf}{f_s}\right)\right|$$

Referred to as a sinc shaped filter
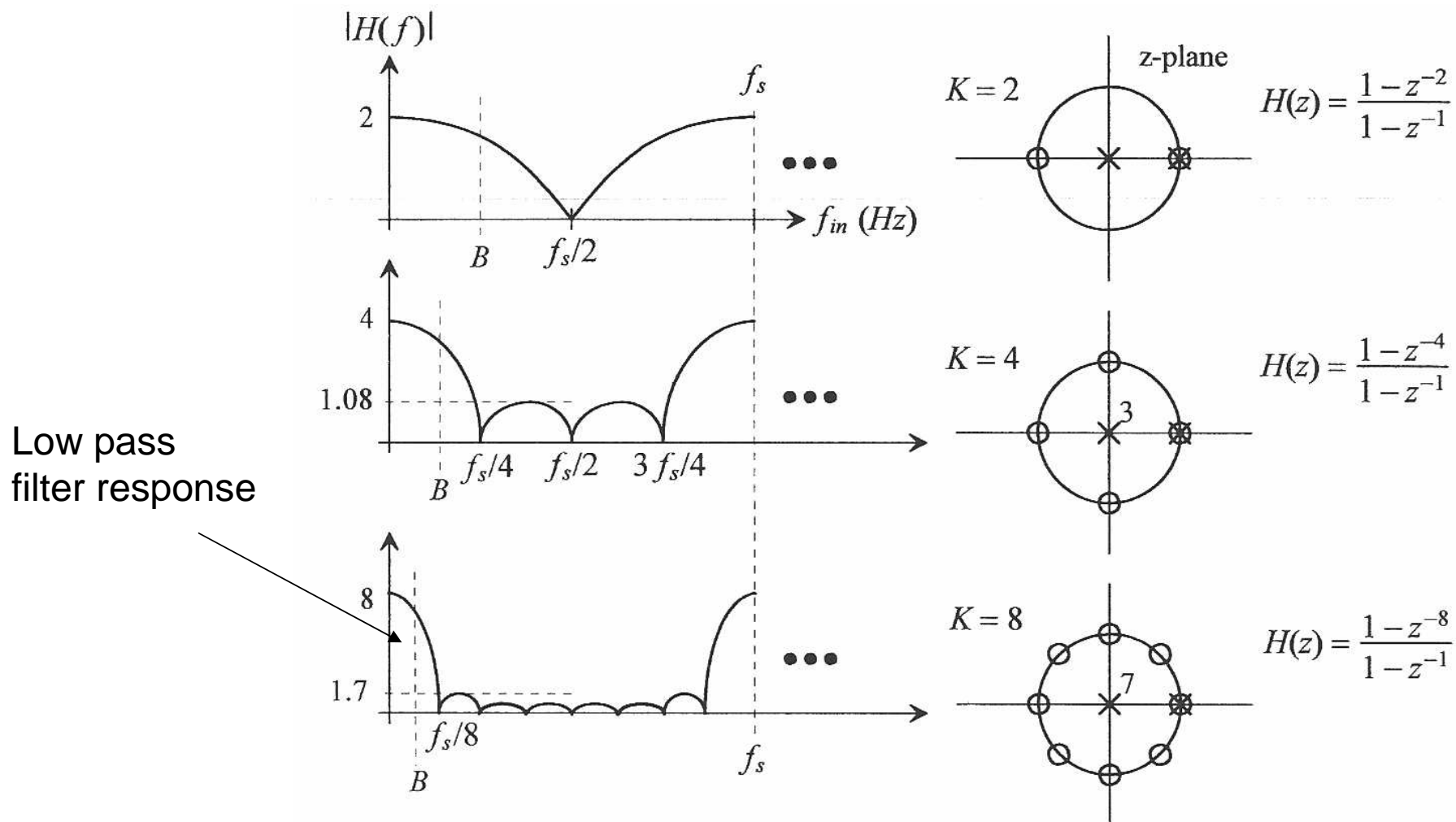
(4.13) [3]

Frequency response of sinc-shaped filters

Low pass filter response

Figure 4.13 Lowpass Sinc-response filters with varying values of K.

[3]

Attenuation of sinc-shaped filters

$$H(z) = \frac{1 - z^{-K}}{1 - z^{-1}}$$

$$|H(f)| = \frac{Sinc\left(K\pi \cdot \frac{f}{f_s}\right)}{Sinc\left(\pi \cdot \frac{f}{f_s}\right)}$$
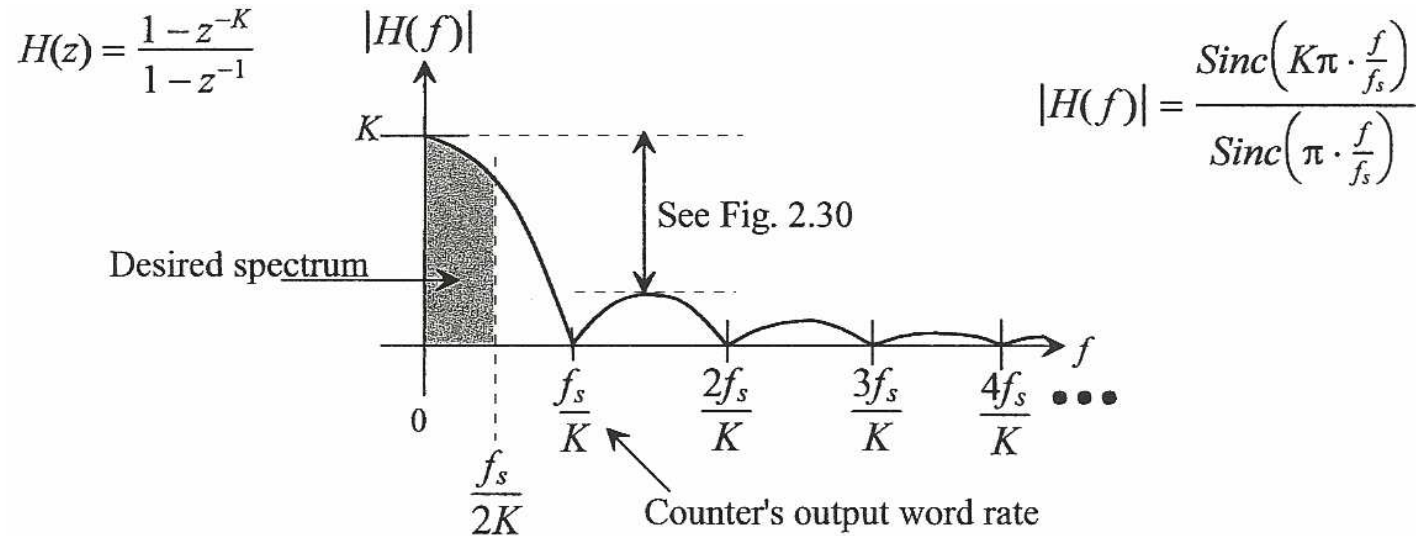
Figure 4.10 Frequency response of a Sinc-shaped digital filter.

[3]

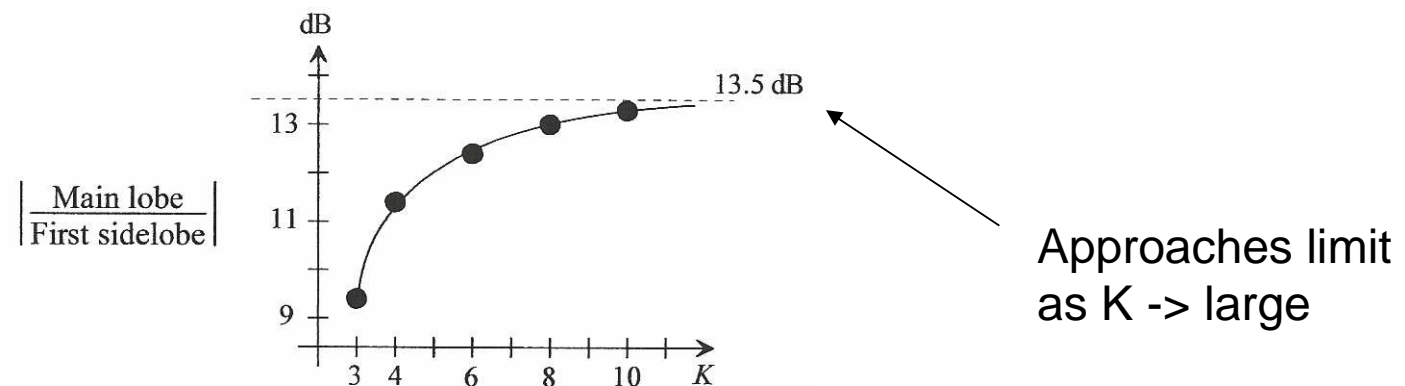Approaches limit
as K -> large

Figure 2.30 Attenuation versus K.

[3]

Cascading sinc-shaped filters

$$H(z) = \left[\frac{1 - z^{-K}}{1 - z^{-1}} \right]^{L}$$
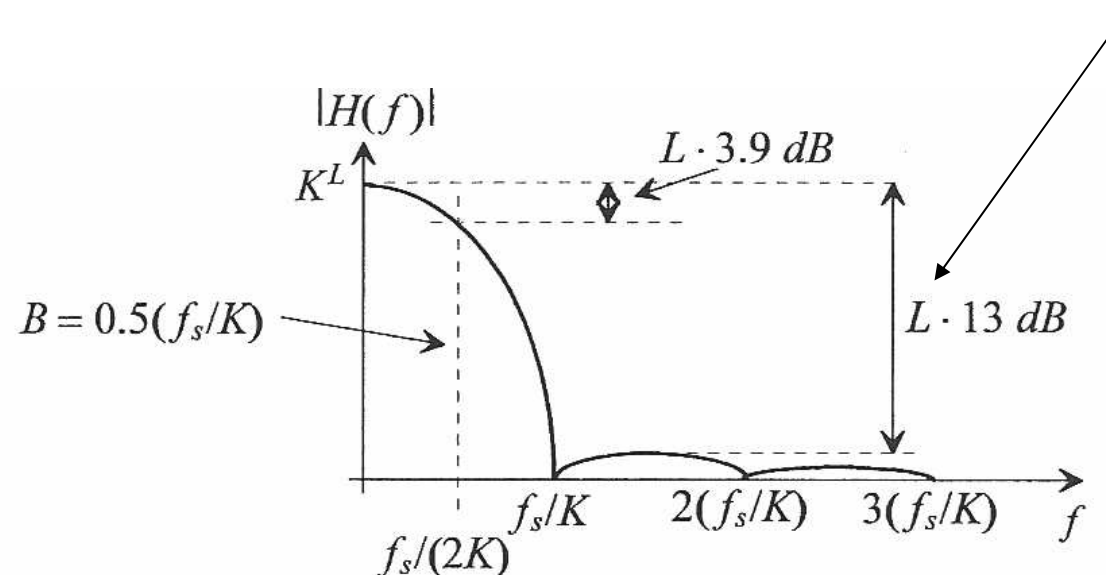
Attenuation depends on how many stages are cascaded

Figure 4.17 General frequency response of a lowpass Sinc (averaging) filter.

Implementing cascaded sinc filters with decimation

$$H(z) = \left[\frac{1 - z^{-K}}{1 - z^{-1}} \right]^{L}$$

$$= [1 + z^{-1} + z^{-2} + ... + z^{1-K}]^{L}$$

$$= [(1 + z^{-1}) \cdot (1 + z^{-2}) \cdot ... \cdot (1 + z^{-2^{\log_2 K - 1}})]^{L}$$

$$= (1 + z^{-1})^{L} \cdot (1 + z^{-2})^{L} \cdot ... \cdot (1 + z^{-2^{\log_2 K - 1}})^{L} \qquad \text{(4.34) [3]}$$

Can be implemented by cascading averagers with clock dividers
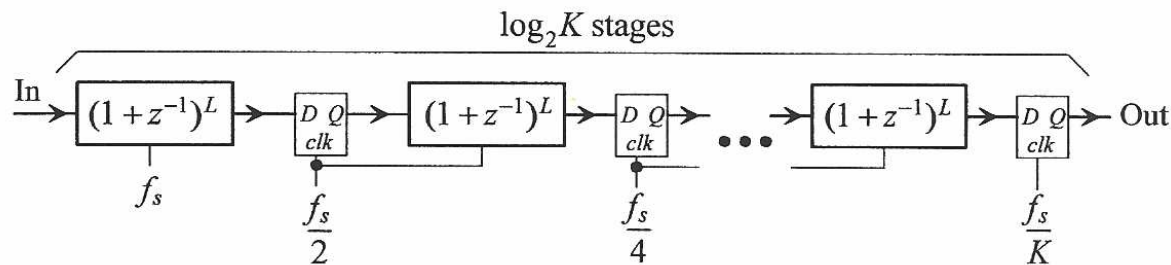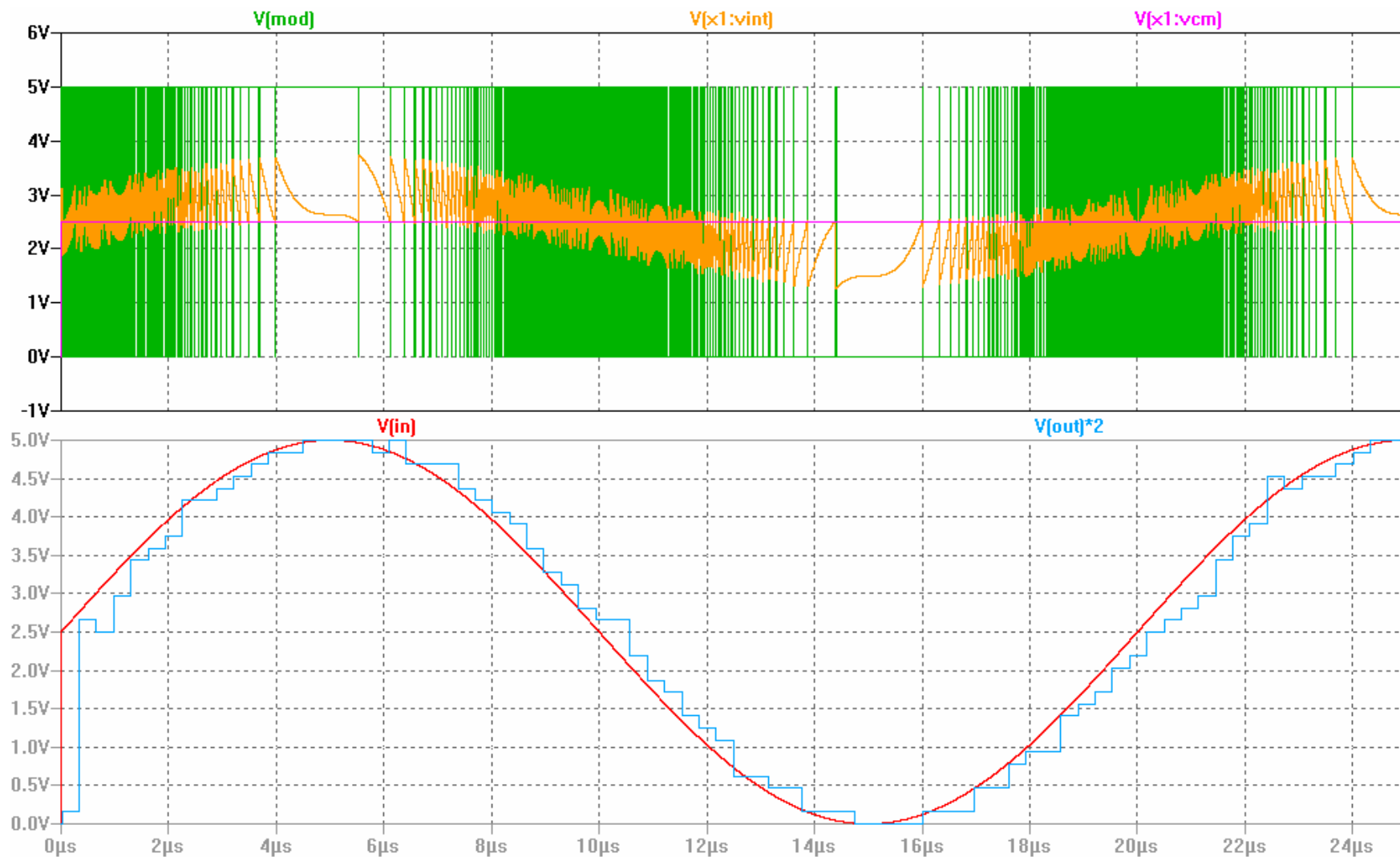

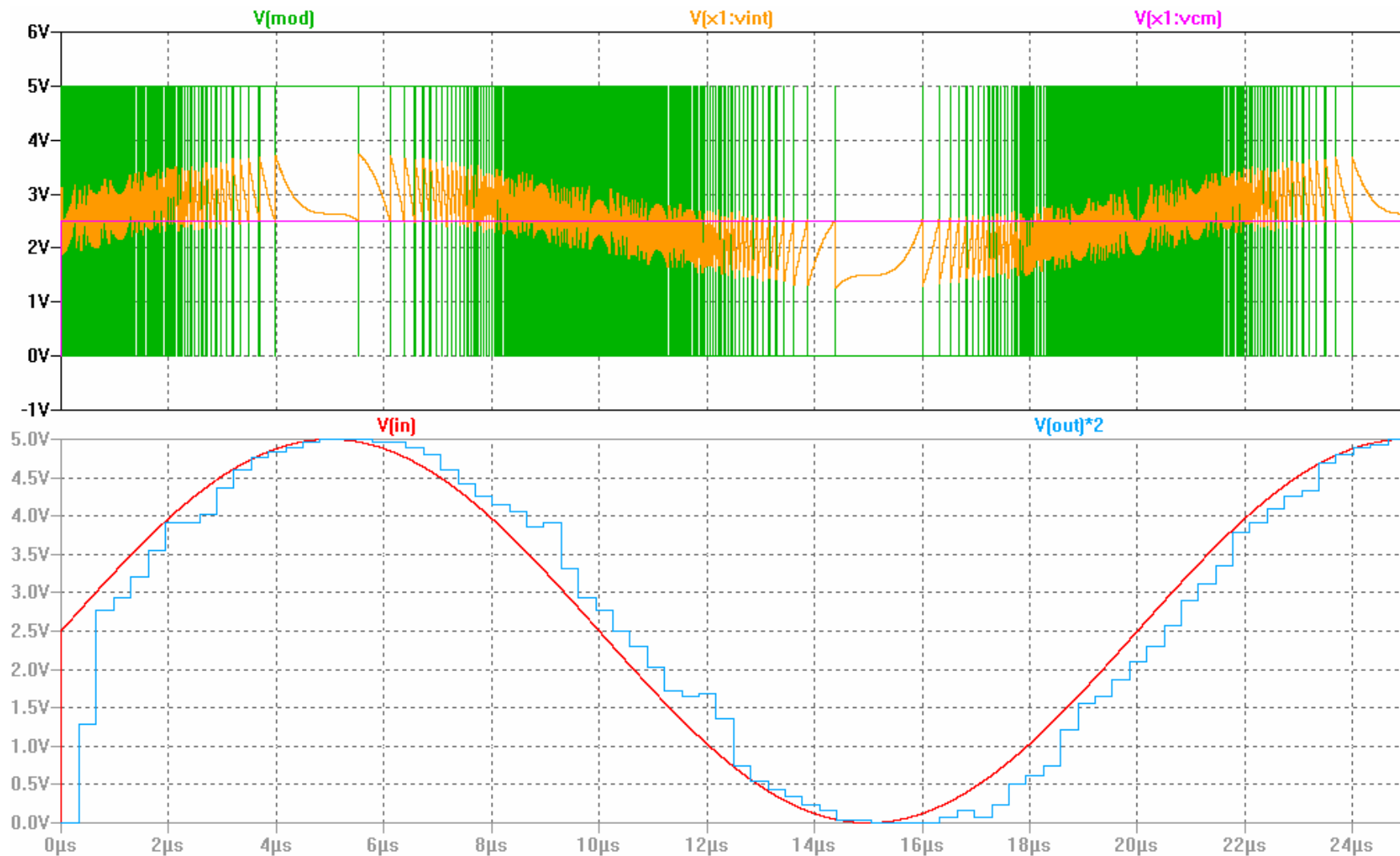Figure 4.32 Decimation using Sinc anti-aliasing filters.

[3]

Simulation results
cascade of averagers – 1st order sinc – sim5

Simulation results

cascade of averagers – 2st order sinc – sim6

References

[1] Baker, R. Jacob, CMOS: Circuit Design, Layout, and Simulation

[2] Baker, R. Jacob, CMOS: Mixed-Signal Circuit Design

[3] Baker, R. Jacob, CMOS: Mixed-Signal Circuit Design, Second Edition