THE AMERICAN UNIVERSITY IN CAIRO

الجامعة الأمريكية بالقاهرة

Digital Design II

Project 1: Designing a Standard CMOS Cell

Date: 4/18/2018

Names:

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Objectives:

1- Design (schematic and layout) and simulate few CMOS standard cells.
2- Derive the linear delay models for each cell.

Tools:

Electric VLSI software

Steps:

1- We divided the required cell between us as follows:

Refaay:
1- Inverter size 1, 2, 4, and 8.
2- The complex function: $f(x,y,z,w) = xy + wz$ (size: 1)

Lotfy:
1- NOR size 1, 2, and 4
2- The mux (size: 1)

Noor:
1- NAND size 1, 2, 4
2- The majority circuit

2- **We used the kp calculated from lab1 as follows:**

kp = (Un / Up) = (293.522312 / 120.5316596) = 2.5.

3- **We sized the transistor for each cell using the above kp.**

4- We created the schematics and layouts for all the cells.

5- We used the folded layout to do the cells with largest heights (Inverter sizes 4 & 8, NOR size 4, and NAND size 4): largest height = 82 lambda.

6- Since it's required to use (20-80%) transition time, we calculated the transition time as follows:

$$t = \frac{Transition\ x\ 100\%}{60\%}$$

7- We used the following spice codes to obtain the tpdf and tpdr :

1- For 0 ps transition time (we used transition time 0.0000001 because transition time 0 will fail to calculate tpdf and tpdr):

```
vdd vdd 0 dc 5
vin in 0 dc pulse 0 5 10n 0.00000001ps 0.00000001ps 10n
.tran 0 40n
.include E:\Spring 2018\Digital Design\scmos18.txt
.measure tpdr trig v(in) val=2.5 fall=1 TARG v(out) val=2.5 rise=1
.measure tpdf trig v(in) val=2.5 rise=1 TARG v(out) val=2.5 fall=1
```

2- For 100 ps transition time:

```
vdd vdd 0 dc 5
vin in 0 dc pulse 0 5 10n 167ps 167ps 10n
.tran 0 40n
.include E:\Spring 2018\Digital Design\scmos18.txt
.measure tpdr trig v(in) val=2.5 fall=1 TARG v(out) val=2.5 rise=1
.measure tpdf trig v(in) val=2.5 rise=1 TARG v(out) val=2.5 fall=1
```

3- For 400 ps transition time

```
vdd vdd 0 dc 5
vin in 0 dc pulse 0 5 10n 667ps 667ps 10n
.tran 0 40n
.include E:\Spring 2018\Digital Design\scmos18.txt
.measure tpdr trig v(in) val=2.5 fall=1 TARG v(out) val=2.5 rise=1
.measure tpdf trig v(in) val=2.5 rise=1 TARG v(out) val=2.5 fall=1
```

4- For 800 ps transition time

```
vdd vdd 0 dc 5
vin in 0 dc pulse 0 5 10n 1333ps 1333ps 10n
.tran 0 40n
.include E:\Spring 2018\Digital Design\scmos18.txt
.measure tpdr trig v(in) val=2.5 fall=1 TARG v(out) val=2.5 rise=1
.measure tpdf trig v(in) val=2.5 rise=1 TARG v(out) val=2.5 fall=1
```

8- Then we collected the data form simulating each cell.

9- We then derived the linear delay model for each cell.

Inverter:-

1- Sizes:-

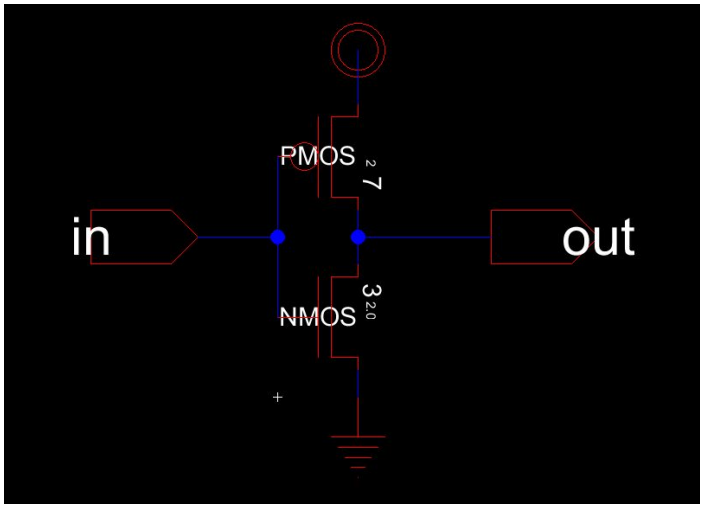
SIZE1: PMOS size is 7, NMOS size is 3

SIZE2: PMOS size is 15, NMOS size is 6

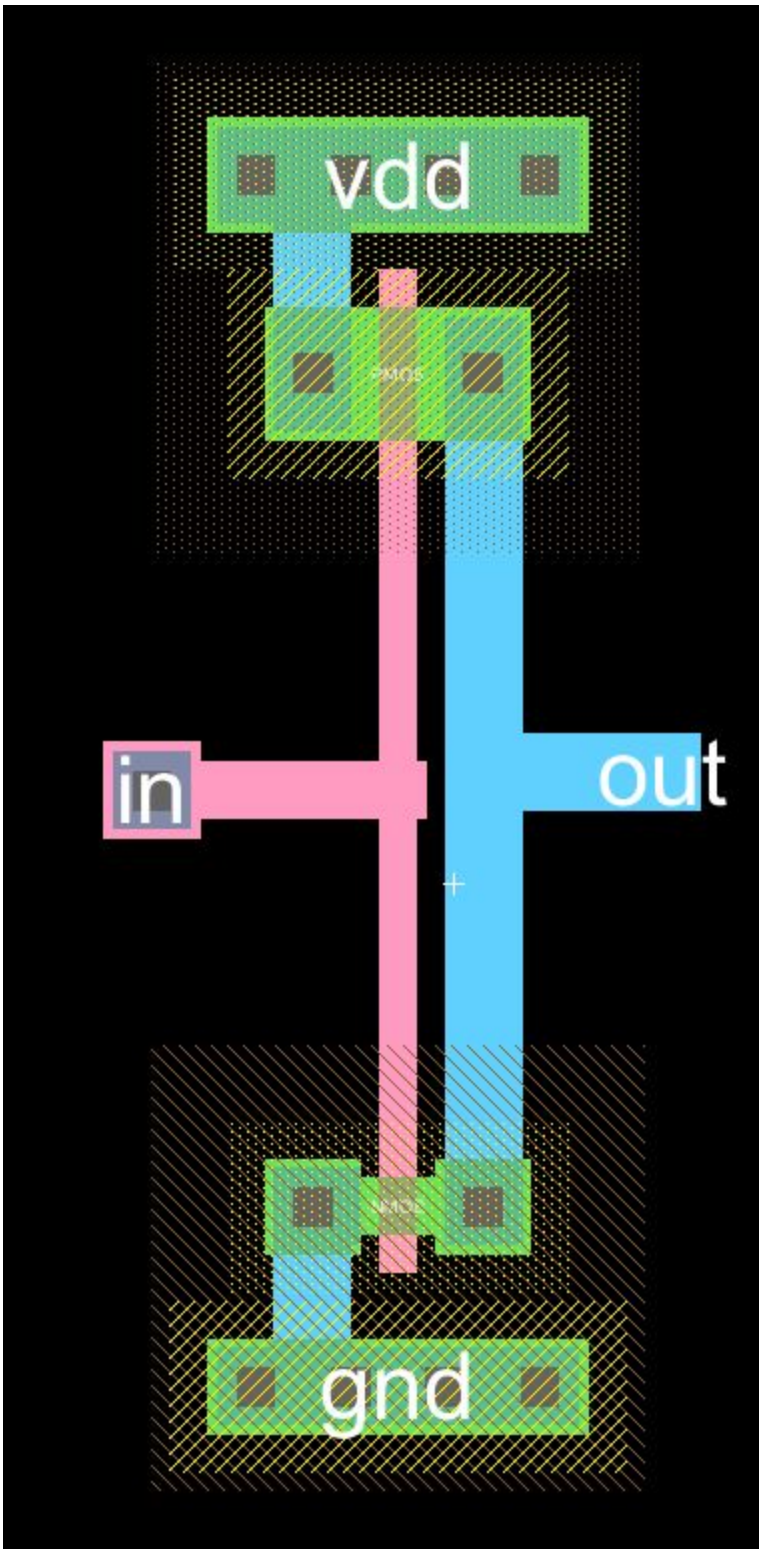
SIZE4: PMOS size is 29, NMOS size is 12

SIZE8: PMOS size is 58, NMOS size is 24

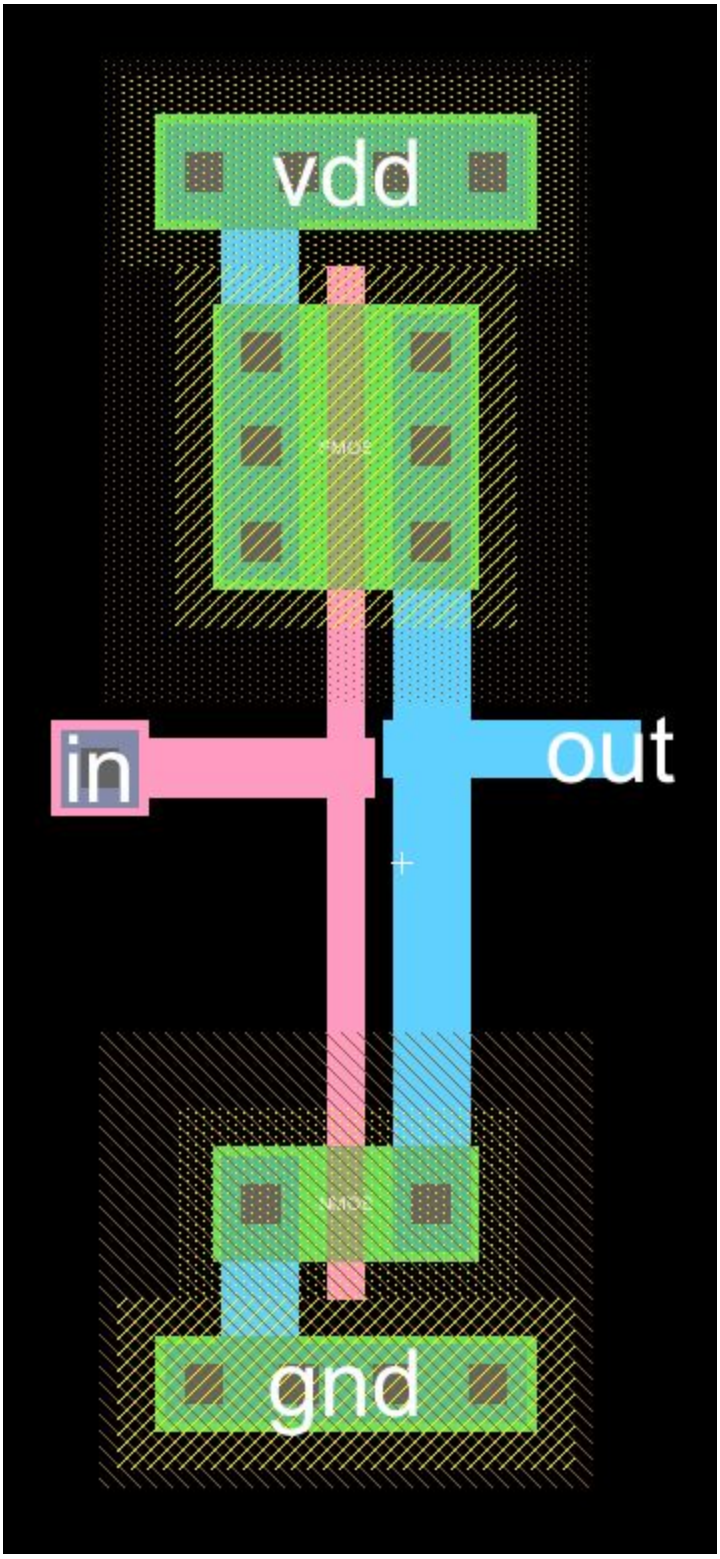
2- Schematic:-



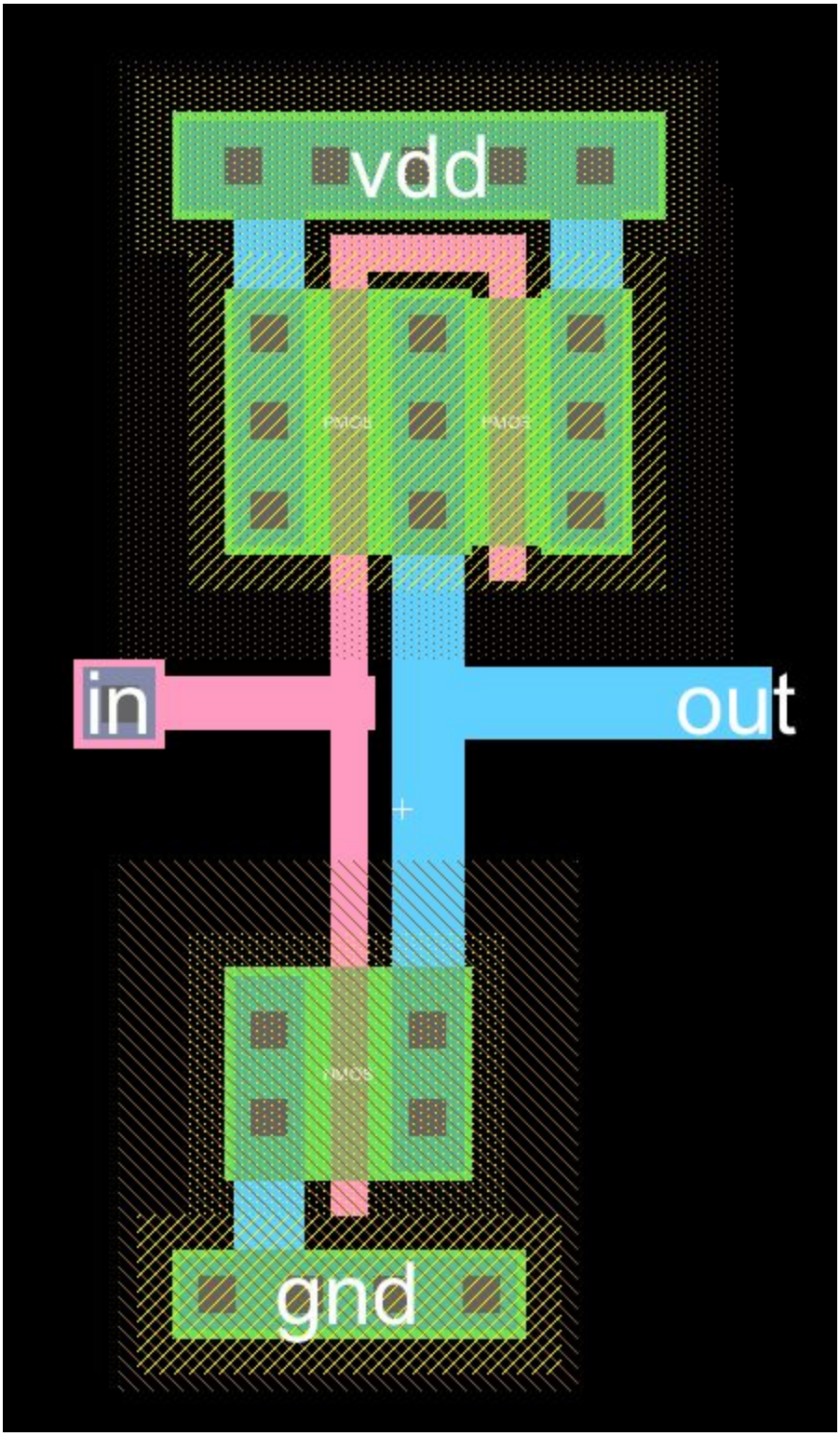
3- Layout:-



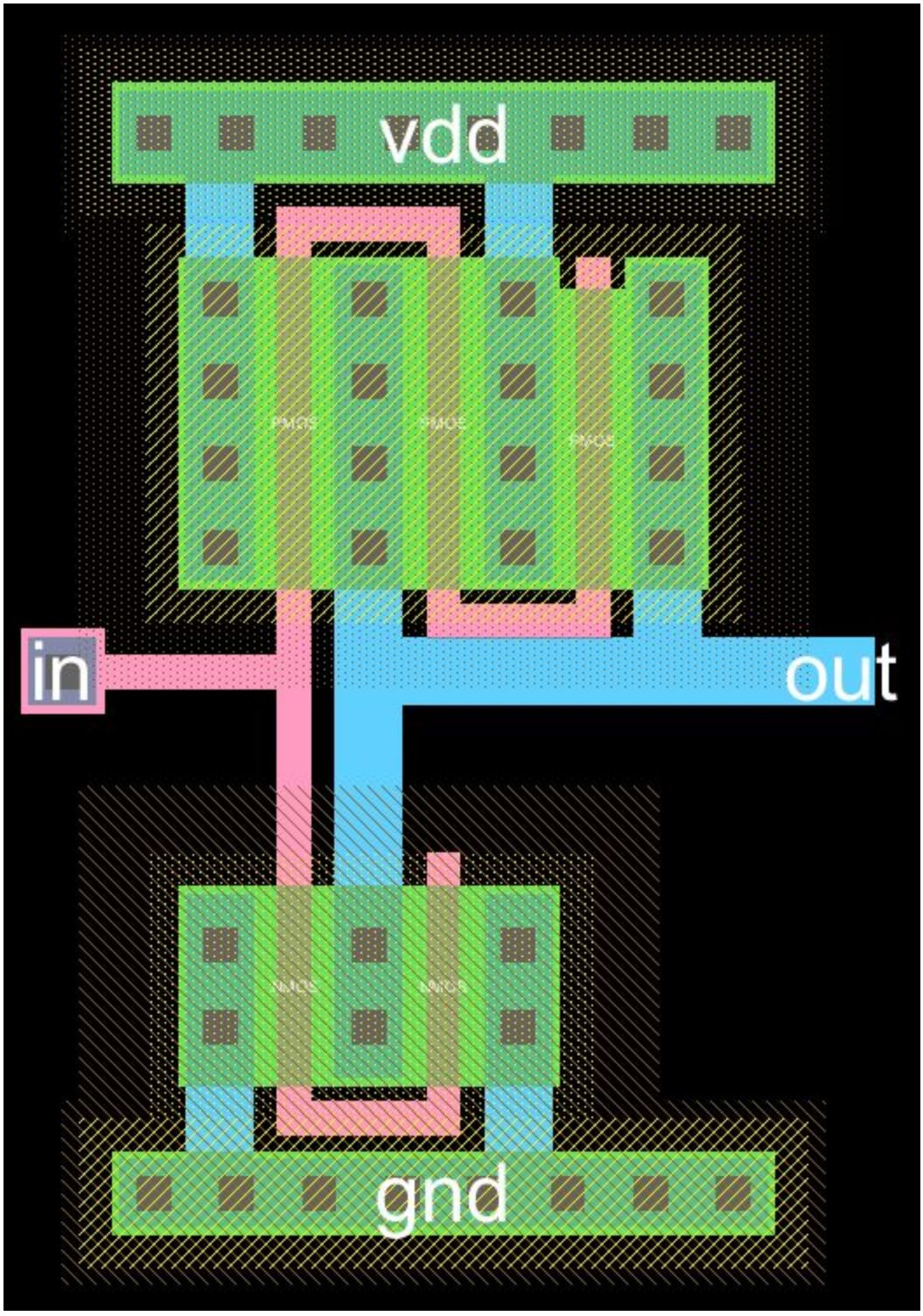
SIZE1 (32*81.5)



SIZE2 (32*81.5)



SIZE4 (40*81.5 - Folded)



SIZE8 (52*81.5 - Folded)

4- Collected Data for Delays:-

Size 1

Transition	cload	tpdf	tpdr
0	1	1.26E-11	1.90E-11
0	2	1.98E-11	3.02E-11
0	4	4.45E-11	5.01E-11
0	8	8.78E-11	8.80E-11
100	1	2.97E-11	3.54E-11
100	2	4.36E-11	4.81E-11
100	4	6.35E-11	6.70E-11
100	8	1.02E-10	1.05E-10
400	1	4.58E-11	6.38E-11
400	2	6.90E-11	9.03E-11
400	4	1.08E-10	1.29E-10
400	8	1.65E-10	1.86E-10
800	1	5.88E-11	8.80E-11
800	2	9.13E-11	1.23E-10
800	4	1.41E-10	1.76E-10
800	8	2.14E-10	2.55E-10

Size 2

Transition	cload	tpdf	tpdr
0	1	9.14E-12	1.53E-11
0	2	9.32E-12	2.16E-11
0	4	2.64E-11	2.71E-11
0	8	5.76E-11	4.85E-11
100	1	2.51E-11	2.51E-11
100	2	3.79E-11	3.39E-11
100	4	5.27E-11	4.87E-11
100	8	7.80E-11	6.90E-11
400	1	5.30E-11	3.57E-11
400	2	6.75E-11	5.31E-11
400	4	9.65E-11	7.91E-11
400	8	1.37E-10	1.20E-10
800	1	7.75E-11	3.86E-11
800	2	9.94E-11	6.45E-11
800	4	1.35E-10	1.00E-10
800	8	1.89E-10	1.57E-10

Size 4

Transition	cload	tpdf	tpdr
0	1	1.65E-13	9.44E-12
0	2	2.21E-12	1.14E-11
0	4	1.10E-11	2.13E-11
0	8	2.90E-11	2.77E-11
100	1	2.54E-11	2.01E-11
100	2	3.13E-11	2.60E-11
100	4	4.14E-11	3.52E-11
100	8	5.58E-11	5.08E-11
400	1	4.67E-11	2.49E-11
400	2	5.63E-11	3.64E-11
400	4	7.31E-11	5.53E-11
400	8	1.03E-10	8.35E-11
800	1	7.03E-11	2.29E-11
800	2	8.33E-11	4.00E-11
800	4	1.09E-10	6.59E-11
800	8	1.47E-10	1.05E-10

Size 8

Transition	cload	tpdf	tpdr
0	1	1.30E-13	1.39E-11
0	2	1.72E-13	4.49E-12
0	4	1.11E-11	1.11E-11
0	8	1.25E-11	2.18E-11
100	1	2.39E-11	1.63E-11
100	2	2.71E-11	1.96E-11
100	4	3.30E-11	2.55E-11
100	8	4.30E-11	3.51E-11
400	1	4.65E-11	1.64E-11
400	2	5.27E-11	2.36E-11
400	4	6.12E-11	3.49E-11
400	8	8.07E-11	5.30E-11
800	1	7.06E-11	8.76E-12
800	2	7.71E-11	1.82E-11
800	4	9.25E-11	3.45E-11
800	8	1.17E-10	6.08E-11

5- Linear delay model for tpdf in (ps):

k3 = -8.7345
k2 = 0.104
k1 = 14.9072

delay1 = 14.9072 C_{load} + 0.104 Transition - 8.7345

k3 = -6.8664
k2 = 0.1208
k1 = 10.538

delay2 = 10.538 C_{load} + 0.1208 Transition - 6.8664

k3 = -5.2853
k2 = 0.1077
k1 = 6.8212

delay4 = 6.8212 C_{load} + 0.1077 Transition - 5.2853

k3 = -0.056899
k2 = 0.0977
k1 = 4.036

delay8 = 4.036 C_{load} + 0.0977 Transition - 0.056899

6- Linear delay model for tpdr in (ps):

k3 = -5.5164
k2 = 0.14
k1 = 14.99

delay1 = 14.99 C_{load} + 0.14 Transition - 5.5164

k3 = -2.4842
k2 = 0.07223
k1 = 9.779

delay2 = 9.779 C_{load} + 0.07223 Transition - 2.4842

k3 = -0.6455
k2 = 0.04736
k1 = 6.6576

delay4 =6.6576 C_{load} + 0.04736 Transition - 0.6455

k3 = 2.9249
k2 = 0.01892
k1 = 4.2161

delay8 =4.2161 C_{load} + 0.01892 Transition + 2.9249

NAND2:-

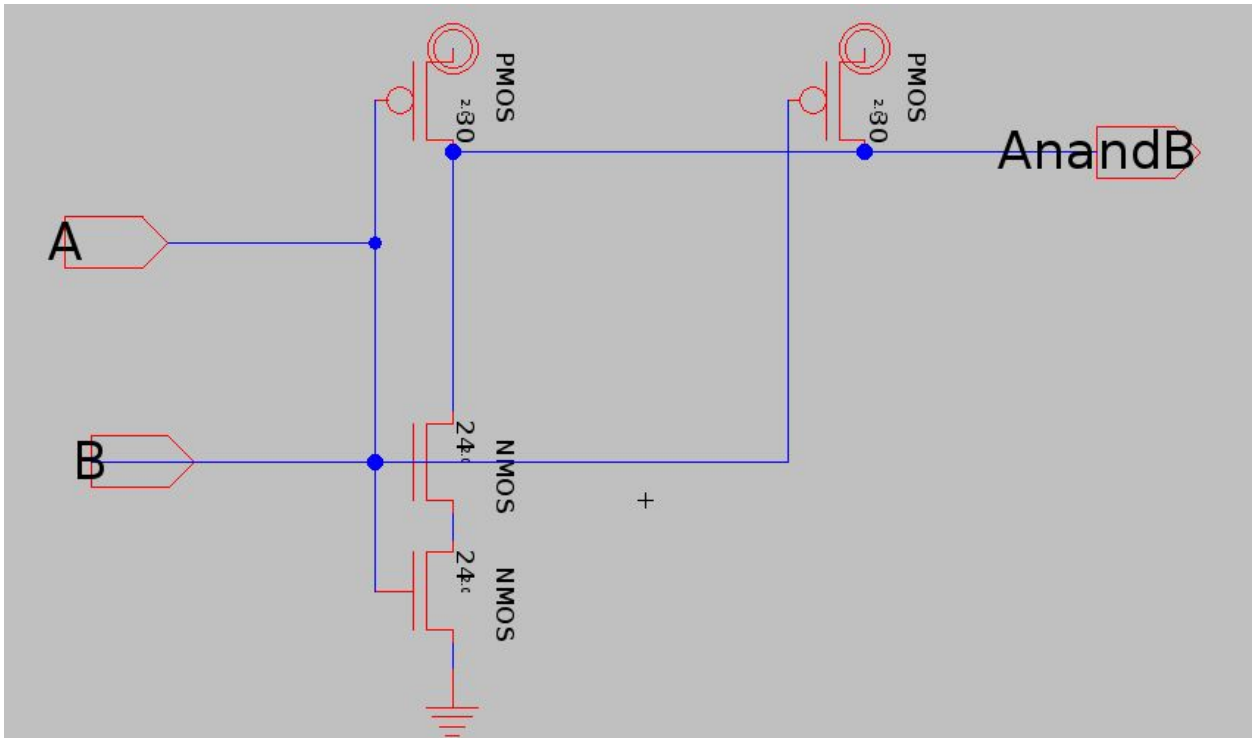
1- Sizes:-

SIZE1: PMOS size is 8, NMOS size is 6

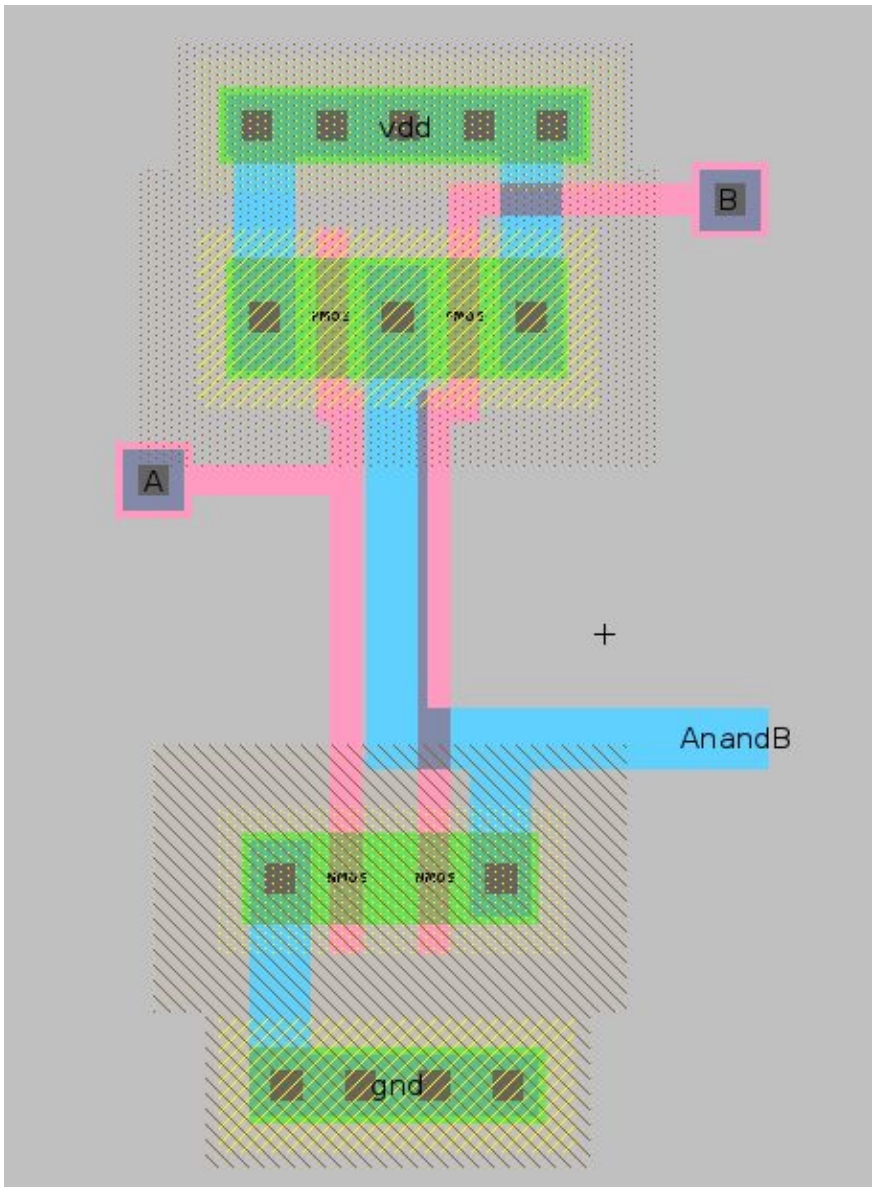
SIZE2: PMOS size is 15, NMOS size is 12

SIZE4: PMOS size is 30, NMOS size is 24

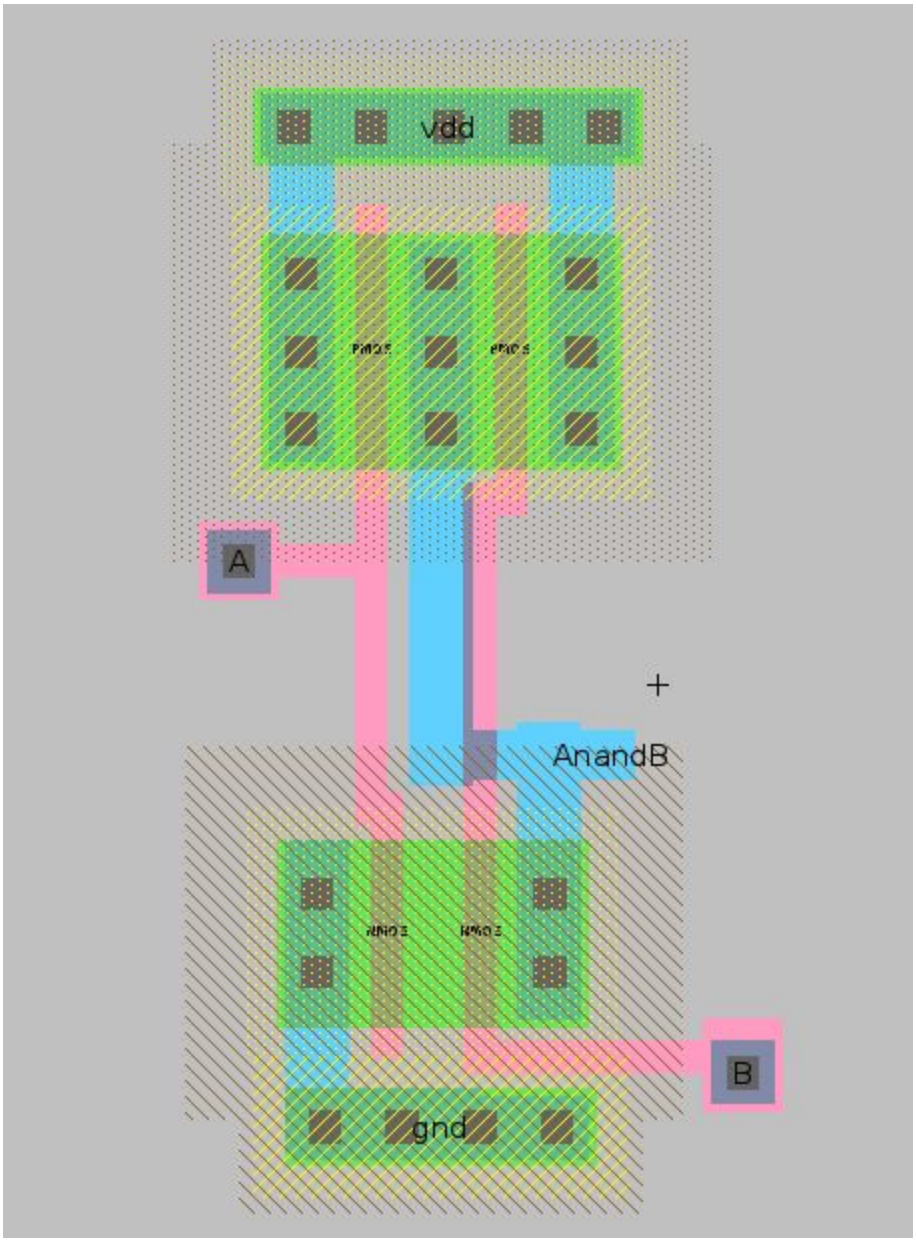
2- Schematic:-



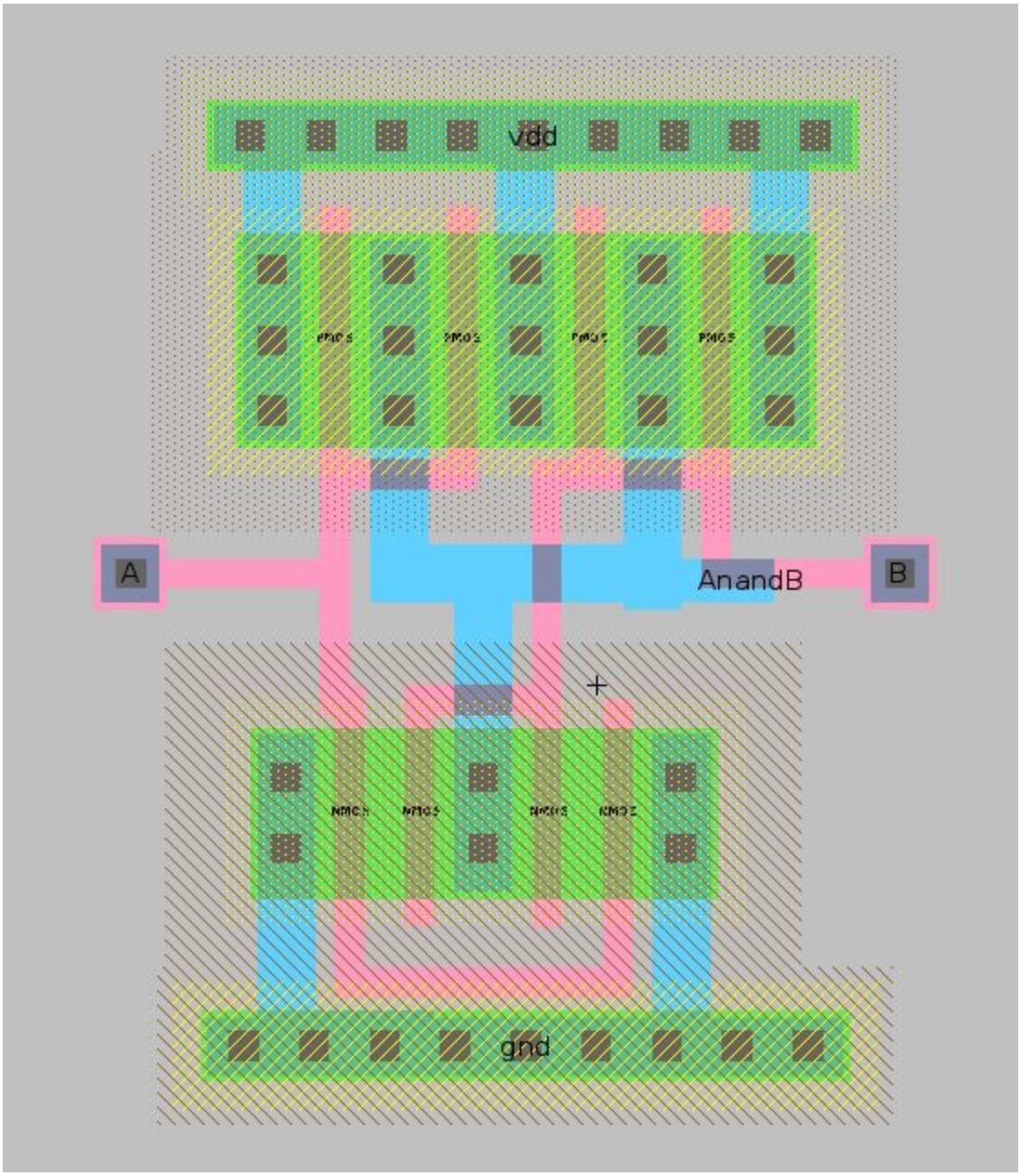
3- Layout:-



SIZE1 (40*82)



SIZE2 (40*81.5)



SIZE4 (60*81.5 - Folded)

4- Collected Data for Delays:-

Size 1				Size 2				Size 4			
Transition	cload	tpdf	tpdr	Transition	cload	tpdf	tpdr	Transition	cload	tpdf	tpdr
0	1	1.64E-11	2.13E-11	0	1	6.02E-12	2.04E-11	0	1	3.09E-12	1.63E-11
0	2	2.20E-11	3.18E-11	0	2	1.21E-11	2.21E-11	0	2	6.56E-12	1.35E-11
0	4	4.46E-11	5.02E-11	0	4	2.43E-11	3.47E-11	0	4	1.38E-11	2.46E-11
0	8	8.57E-11	8.03E-11	0	8	5.04E-11	5.22E-11	0	8	2.65E-11	3.07E-11
100	1	3.16E-11	3.86E-11	100	1	2.59E-11	3.47E-11	100	1	2.28E-11	3.11E-11
100	2	4.35E-11	5.13E-11	100	2	3.37E-11	4.27E-11	100	2	2.74E-11	3.56E-11
100	4	6.42E-11	6.85E-11	100	4	4.70E-11	5.52E-11	100	4	3.59E-11	4.32E-11
100	8	9.57E-11	1.02E-10	100	8	6.75E-11	7.36E-11	100	8	4.94E-11	5.53E-11
400	1	4.58E-11	6.95E-11	400	1	3.16E-11	6.46E-11	400	1	2.70E-11	5.59E-11
400	2	6.62E-11	9.18E-11	400	2	4.56E-11	7.82E-11	400	2	3.47E-11	6.44E-11
400	4	1.01E-10	1.26E-10	400	4	6.76E-11	1.03E-10	400	4	4.94E-11	7.95E-11
400	8	1.65E-10	1.86E-10	400	8	1.05E-10	1.41E-10	400	8	7.13E-11	1.05E-10
800	1	5.29E-11	9.73E-11	800	1	3.20E-11	9.28E-11	800	1	2.52E-11	8.10E-11
800	2	8.22E-11	1.28E-10	800	2	4.91E-11	1.15E-10	800	2	3.61E-11	9.30E-11
800	4	1.27E-10	1.75E-10	800	4	8.10E-11	1.47E-10	800	4	5.47E-11	1.16E-10
800	8	1.95E-10	2.47E-10	800	8	1.29E-10	1.98E-10	800	8	8.69E-11	1.49E-10

5- Linear delay model for tpdf in (ps):

k3 = -3.95731
k2 = 0.0890305
k1 = 13.9981

delay1 = 13.9981 C_{load} + 0.0890305 Transition + 3.95731

k3 = -1.931
k2 = 0.05665
k1 = 9.074

delay2 = 9.074 C_{load} + 0.05665 Transition + 1.931

k3 = 1.677
k2 = 0.04084
k1 = 5.525

delay4 = 5.525 C_{load} + 0.04084 Transition + 1.677

6- Linear delay model for tpdr in (ps):

k3 = -0.355247
k2 = 0.144899

k1 = 13.6139

delay1 = 13.6139C_{load} + 0.144899 Transition + 0.355247

k3 = 3.775
k2 = 0.131
k1 = 8.899

delay2 = 8.899 C_{load} + 0.131 Transition + 3.775

k3 = 6.251
k2 = 0.1074
k1 = 5.581

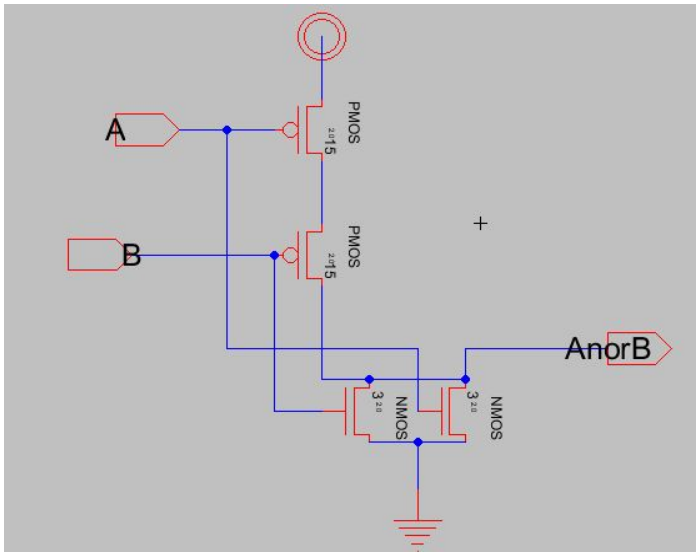
delay4 =5.581 C_{load} + 0.1074 Transition + 6.251

NOR_SIZE_1:

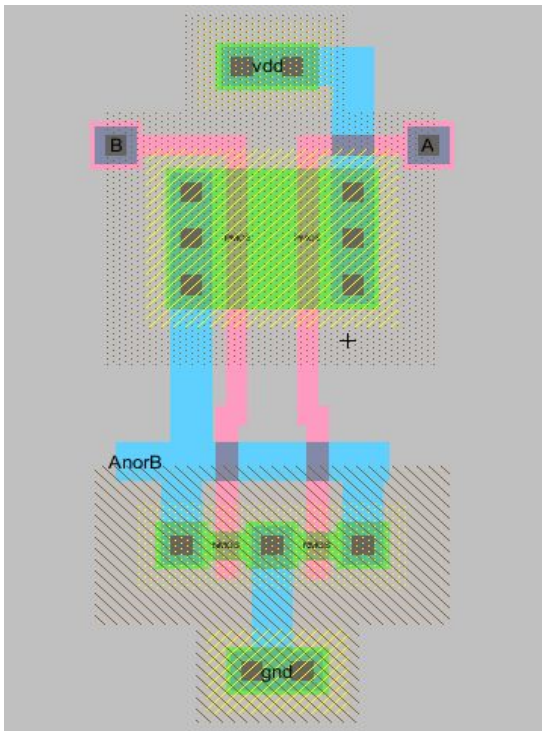
1- Sizes:

The nMOS sizes = 3 lambda & the pMOS sizes = 2*2.5*3 = 15 lambda.

2- Schematic:



3- Layout (36*82)



4- Collected data for delays:

Transition	cload	tpdf	tpdr
0	1	4.05E-11	4.49E-11
	2	7.00E-11	7.16E-11
	4	1.28E-10	1.29E-10
	8	2.44E-10	2.46E-10
100	1	7.64E-11	4.76E-11
	2	1.02E-10	7.26E-11
	4	1.59E-10	1.29E-10
	8	2.71E-10	2.44E-10
400	1	1.55E-10	4.45E-11
	2	1.91E-10	8.60E-11
	4	2.55E-10	1.55E-10
	8	3.48E-10	2.69E-10
800	1	2.42E-10	1.73E-11
	2	2.88E-10	7.32E-11
	4	3.63E-10	1.59E-10
	8	4.82E-10	2.99E-10

5- Linear delay model for tpdf in (ps):

k3 = 12.6
k2 = 0.27775
k1 = 29.5

delay = 29.5 C_{load} + 0.27775 Transition + 12.6

6- Linear delay model for tpdr in (ps):

K3= 3.68611

K2 = 0.202502

K1= 32.0695

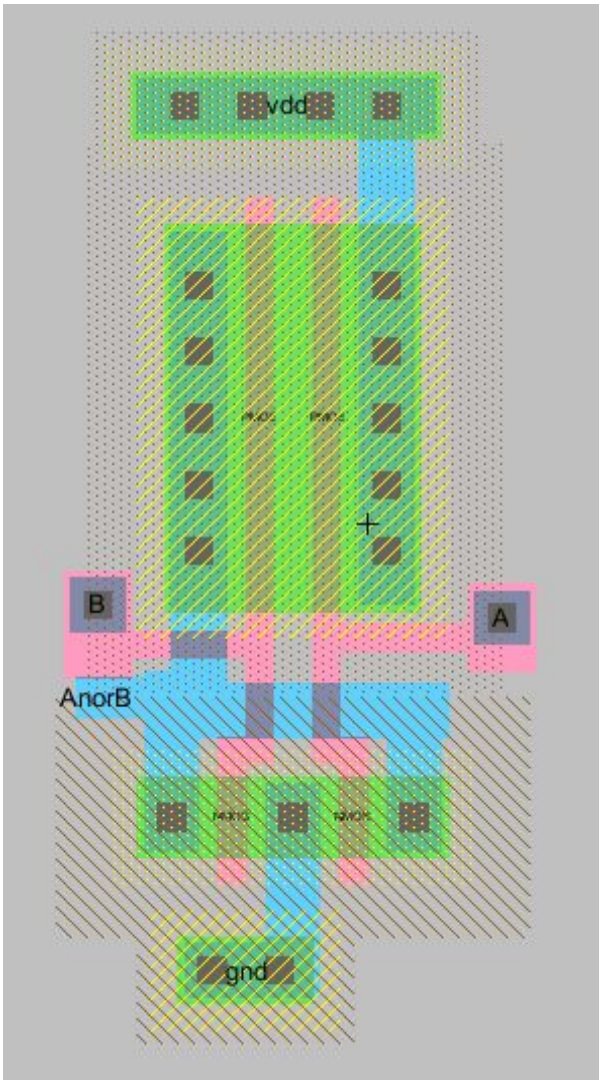
delay = 32.0695 C_{load} + 0.202502 Transition + 3.68611

NOR_SIZE_2:

1- Sizes:

The nMOS sizes = 6 lambda & the pMOS sizes = 29 lambda.

2- Layout (36*82)



3- Collected data for delays:

Transition	cload	tpdf	tpdr
0	1	3.38E-11	3.11E-11
	2	5.23E-11	4.54E-11
	4	8.89E-11	7.56E-11
	8	1.63E-10	1.40E-10
100	1	7.28E-11	3.29E-11
	2	8.84E-11	4.99E-11
	4	1.22E-10	7.86E-11
	8	1.98E-10	1.39E-10
400	1	1.55E-10	1.22E-11
	2	1.79E-10	4.11E-11
	4	2.21E-10	8.76E-11
	8	2.87E-10	1.60E-10
800	1	2.50E-10	-3.24E-11
	2	2.82E-10	4.50E-12
	4	3.32E-10	6.36E-11
	8	4.16E-10	1.57E-10

4- Linear delay model for tpdf in (ps):

k3 = 15.3585
k2 = 0.292091
k1 = 19.6064

delay = 19.6064C_{load} + = 0.292091 Transition + 15.3585

5- Linear delay model for tpdr in (ps):

K3 = 4.91
K2 = -0.312636
K1 = 19.5046

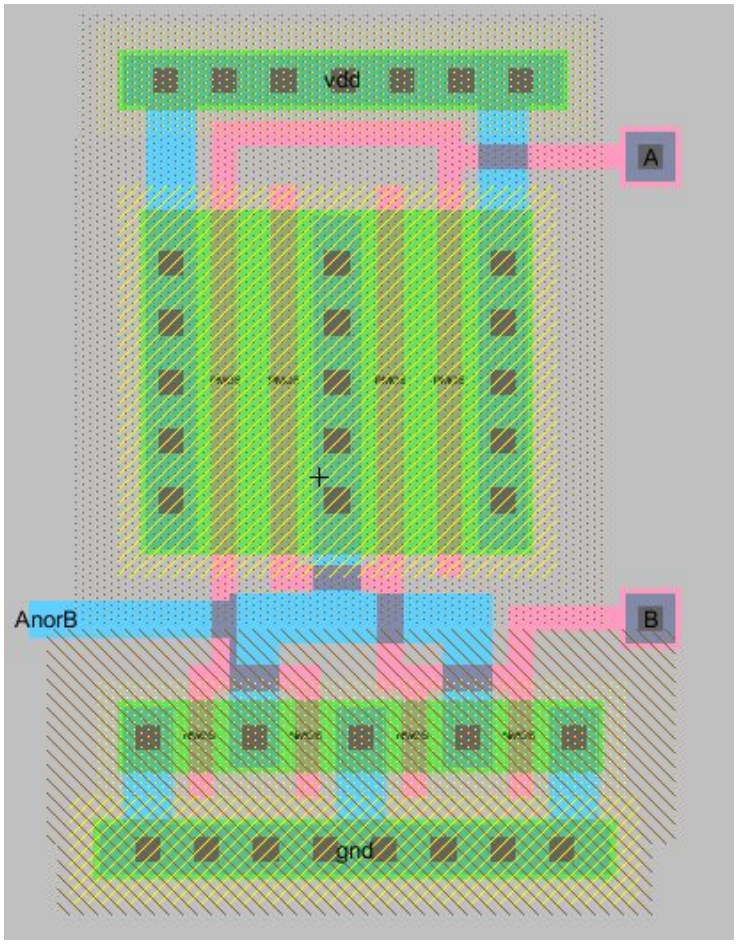
delay = 19.5046 C_{load} - 0.312636 Transition + 4.91

NOR_SIZE_4

1- **Sizes:**

The nMOS sizes = 12 lambda & the pMOS sizes = 58 lambda.

2- **Layout (56*82 - folded)**



3- **Collected data for delays:**

Transition	cload	tpdf	tpdr
0	1	2.76E-11	2.48E-11
	2	3.81E-11	3.37E-11
	4	5.88E-11	4.59E-11
	8	1.01E-10	7.98E-11
100	1	6.92E-11	2.25E-11
	2	7.84E-11	3.26E-11
	4	9.65E-11	5.00E-11
	8	1.35E-10	7.77E-11
400	1	1.54E-10	-9.47E-12
	2	1.68E-10	7.09E-12
	4	1.93E-10	3.74E-11
	8	2.36E-10	8.23E-11
800	1	2.54E-10	-6.79E-11
	2	2.73E-10	-4.45E-11
	4	3.05E-10	-6.21E-12
	8	3.61E-10	5.38E-11

4- **Linear delay model for tpdf in (ps):**

k3 = 18.2593
k2 = 0.29972
k1 = 11.6182
delay = 11.6182 C_{load} + 0.29972 Transition + 18.2593

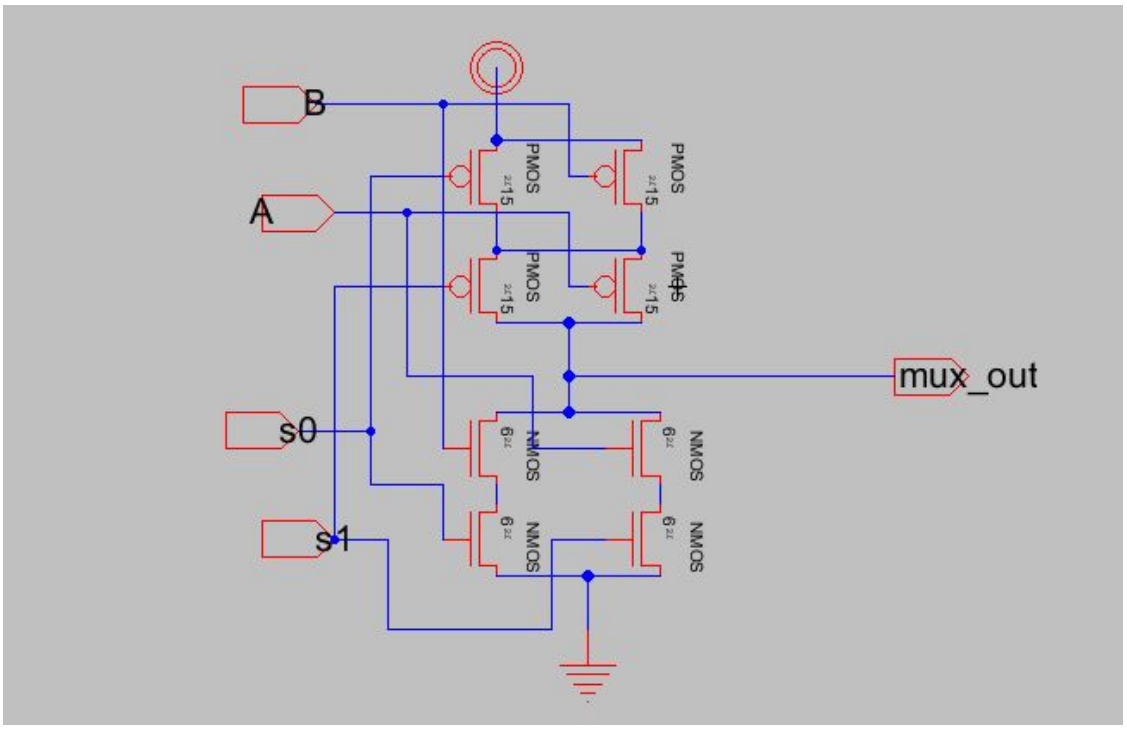
5- **Linear delay model for tpdr in (ps):**

K3 = 9.2455
K2 = -0.7.93249
K1 = 11.4007

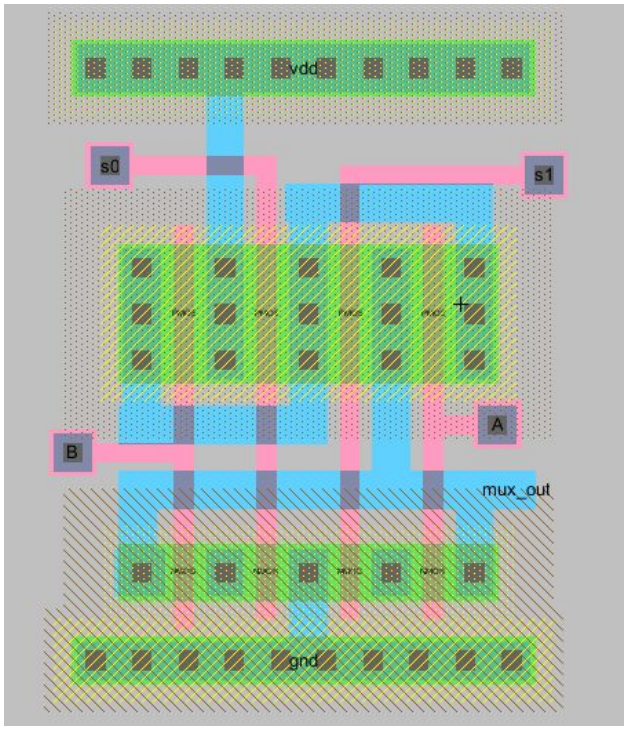
delay = 11.4007 C_{load} - 0.7.93249 Transition + 9.2455

MUX_Size_1:

1- **Sizes:**
   The nMOS sizes = 6 lambda & the pMOS sizes = 15 lambda.
2- **Schematic:**



3- **Layout (60*81.5)**



4- Collected data for delays:

Transition	cload	tpdf	tpdr
0	1	4.39E-11	4.94E-11
	2	7.22E-11	7.58E-11
	4	1.31E-10	1.39E-10
	8	2.41E-10	2.57E-10
100	1	6.78E-11	7.26E-11
	2	9.30E-11	9.92E-11
	4	1.46E-10	1.57E-10
	8	2.53E-10	2.71E-10
400	1	1.05E-10	1.31E-10
	2	1.46E-10	1.75E-10
	4	2.13E-10	2.42E-10
	8	3.16E-10	3.47E-10
800	1	1.32E-10	1.81E-10
	2	1.85E-10	2.38E-10
	4	2.70E-10	3.28E-10
	8	4.00E-10	4.66E-10

5- Linear delay model for tpdf in (ps):

k3 = 10.20967593
k2 = 0.156523226
k1 = 30.46216783

delay = 30.46216783 C_{load} + 0.156523226 Transition + 10.20967593

6- Linear delay model for tpdr in (ps):

k3 = 10.20967593
K2 = 0.218861532
K1 = 32.13621696

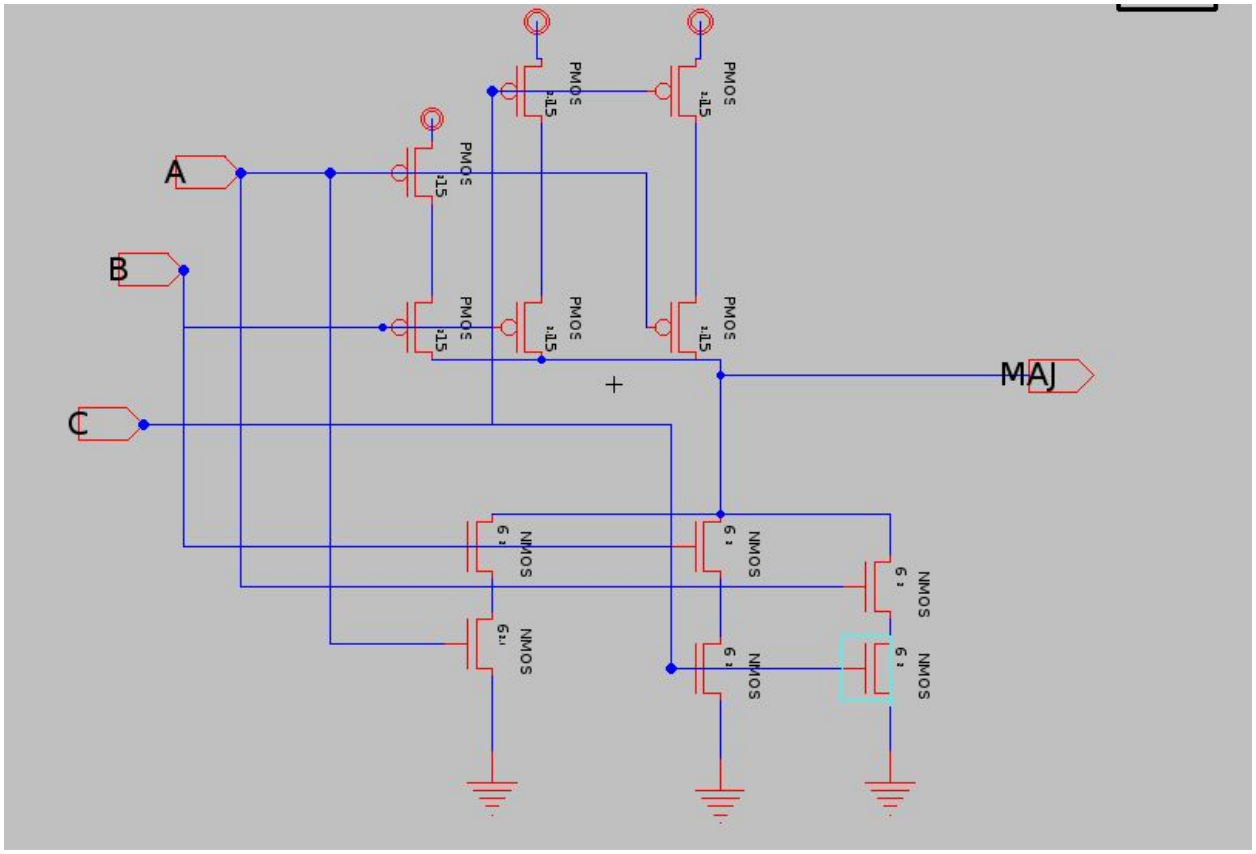
delay = 32.13621696 C_{load} + = 0.218861532 Transition + 10.20967593

MAJ_SIZE1:-

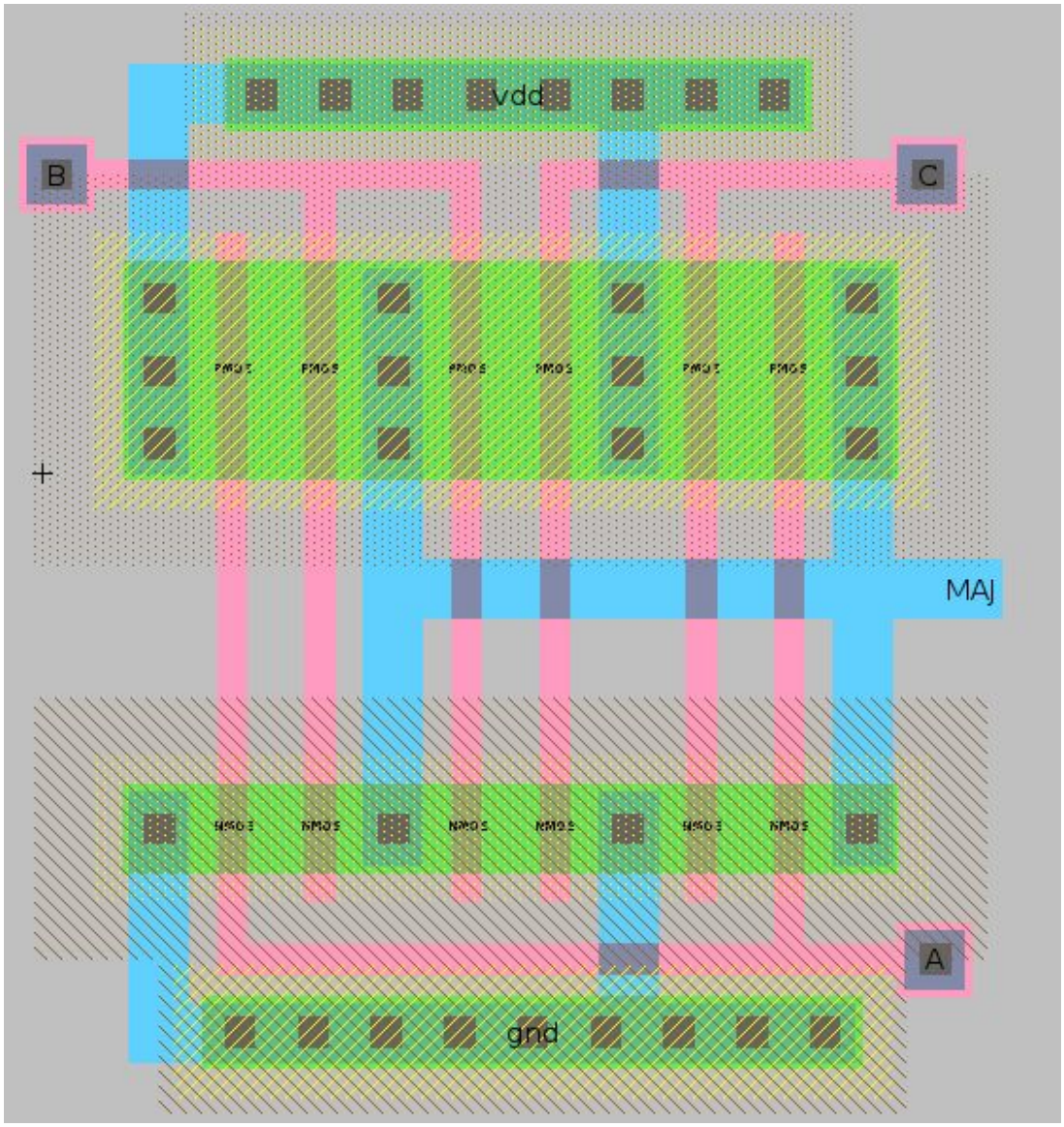
1-Sizes:-

For PMOS sizes = 15 and NMOS sizes = 6

2- Schematic:-



3- Layout (68*81.5):-



4- Collected data for Delays:-

Transition	cload	tpdf	tpdr
0	1	1.12E-11	5.97E-11
0	2	2.21E-11	6.78E-11
0	4	4.42E-11	7.26E-11
0	8	1.06E-10	1.20E-10
100	1	6.84E-11	6.72E-11
100	2	7.85E-11	7.66E-11
100	4	9.65E-11	9.67E-11
100	8	1.34E-10	1.33E-10
400	1	9.51E-11	1.12E-10
400	2	1.11E-10	1.30E-10
400	4	1.42E-10	1.61E-10
400	8	1.90E-10	2.13E-10
800	1	1.14E-10	1.52E-10
800	2	1.35E-10	1.76E-10
800	4	1.74E-10	2.16E-10
800	8	2.38E-10	2.84E-10

5- Linear delay model for tpdf in (ps):

k3 = 15.48
k2 = 0.13521
k1 = 10.3485

delay = 10.3485 C_{load} + 0.13521 Transition + 15.48

6- Linear delay model for tpdr in (ps):

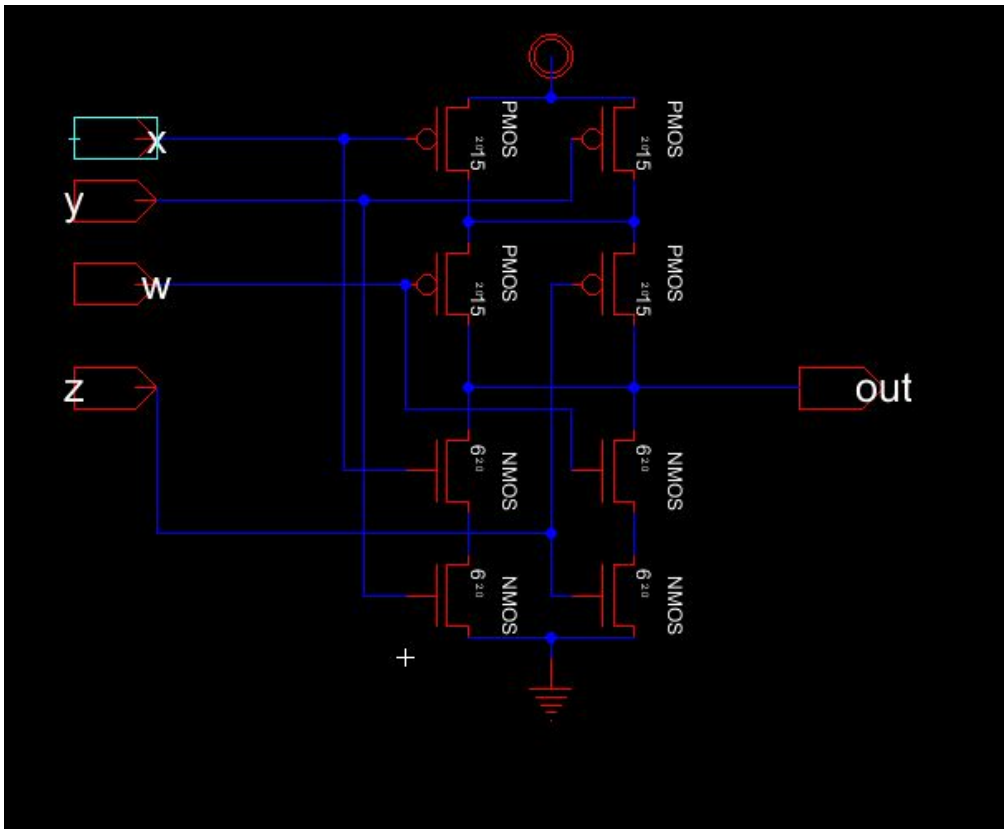
k3 = 33.262
K2 = 0.16244
K1 = 12.688

delay = 12.688 C_{load} + 0.16244 Transition + 33.262

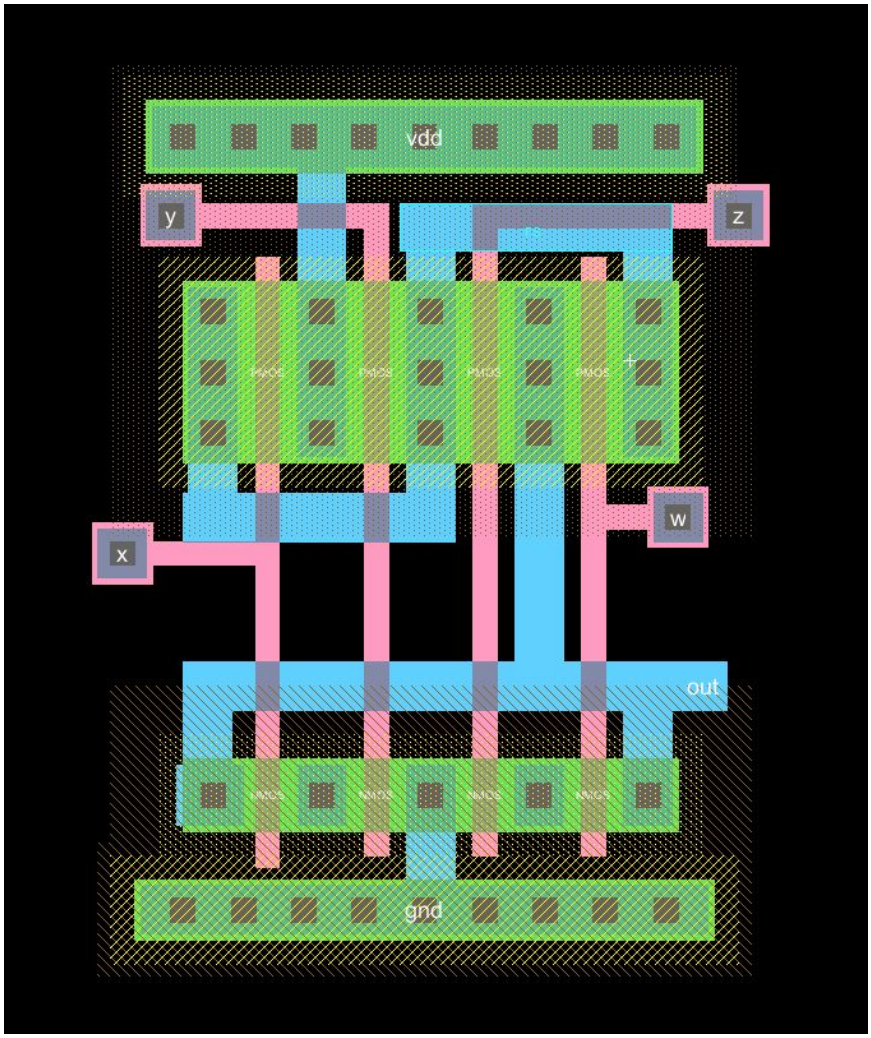
xyORwz_Size_1:

7- **Sizes:**
The nMOS sizes = 6 lambda & the pMOS sizes = 15 lambda.

8- **Schematic:**



9- Layout (60*81.5)



10- Collected data for delays:

Transition	cload	tpdf	tpdr
0	1	4.39E-11	4.94E-11
	2	7.22E-11	7.58E-11
	4	1.31E-10	1.39E-10
	8	2.41E-10	2.57E-10
100	1	6.78E-11	7.26E-11
	2	9.30E-11	9.92E-11
	4	1.46E-10	1.57E-10
	8	2.53E-10	2.71E-10
400	1	1.05E-10	1.31E-10
	2	1.46E-10	1.75E-10
	4	2.13E-10	2.42E-10
	8	3.16E-10	3.47E-10
800	1	1.32E-10	1.81E-10
	2	1.85E-10	2.38E-10
	4	2.70E-10	3.28E-10
	8	4.00E-10	4.66E-10

11- Linear delay model for tpdf in (ps):

k3 = 10.20967593
k2 = 0.156523226
k1 = 30.46216783

delay = 30.46216783 C_{load} + 0.156523226 Transition + 10.20967593

12- Linear delay model for tpdr in (ps):

k3 = 10.20967593
K2 = 0.218861532
K1 = 32.13621696

delay = 32.13621696 C_{load} + = 0.218861532 Transition + 10.20967593